



ΕΘΝΙΚΟ ΜΕΤΣΟΒΙΟ ΠΟΛΥΤΕΧΝΕΙΟ
ΣΧΟΛΗ ΗΛΕΚΤΡΟΛΟΓΩΝ ΜΗΧΑΝΙΚΩΝ
ΚΑΙ ΜΗΧΑΝΙΚΩΝ ΥΠΟΛΟΓΙΣΤΩΝ
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ΠΛΗΡΟΦΟΡΙΚΗΣ

Implementation of advanced beam abort algorithms and electronics for the ATLAS diamond beam conditions monitor (BCM)

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ανάπτυξη ηλεκτρονικών συστημάτων για τον σύστημα
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Χρήστος Σπαθαράκης

Επιβλέπων : Ιωάννης Ν. Αβαριτσιώτης
Καθηγητής Ε.Μ.Π.

Αθήνα, Ιούνιος 2010



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Καθηγητής Ε.Μ.Π.

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.....
Ι. Αβαριτσιώτης
Καθηγητής Ε.Μ.Π

.....
Β. Λούμος
Καθηγητής Ε.Μ.Π

.....
Γ. Στασινόπουλος
Καθηγητής Ε.Μ.Π

Αθήνα, Ιούνιος 2010

.....

Χρήστος Σπαθαράκης

Διπλωματούχος Ηλεκτρολόγος Μηχανικός και Μηχανικός Υπολογιστών Ε.Μ.Π.

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Απαγορεύεται η αντιγραφή, αποθήκευση και διανομή της παρούσας εργασίας, εξ ολοκλήρου ή τμήματος αυτής, για εμπορικό σκοπό. Επιτρέπεται η ανατύπωση, αποθήκευση και διανομή για σκοπό μη κερδοσκοπικό, εκπαιδευτικής ή ερευνητικής φύσης, υπό την προϋπόθεση να αναφέρεται η πηγή προέλευσης και να διατηρείται το παρόν μήνυμα. Ερωτήματα που αφορούν τη χρήση της εργασίας για κερδοσκοπικό σκοπό πρέπει να απευθύνονται προς τον συγγραφέα. Οι απόψεις και τα συμπεράσματα που περιέχονται σε αυτό το έγγραφο εκφράζουν τον συγγραφέα και δεν πρέπει να ερμηνευθεί ότι αντιπροσωπεύουν τις επίσημες θέσεις του Εθνικού Μετσόβιου Πολυτεχνείου.

Περίληψη

Κατά τη λειτουργία του μεγάλου επιταχυντή αδρονίων (LHC), του μεγαλύτερου επιταχυντή σωματιδίων στον κόσμο που βρίσκεται στο Ευρωπαϊκό Κέντρο Πυρηνικών Ερευνών (CERN) στη Γενεύη, οι εξαιρετικά υψηλές ενέργειες των συγκρουόμενων δεσμών (μέχρι και 7 TeV) προκαλούν κινδύνους στους ανιχνευτές που βρίσκονται σε λειτουργία. Η εμπειρία από παλαιότερους επιταχυντές οδήγησε κάθε ανιχνευτή στην ανάπτυξη ενός συστήματος για την έγκαιρη ανίχνευση ανωμαλών καταστάσεων στις συγκρουόμενες δέσμες. Στον ανιχνευτή ATLAS, αυτό το σύστημα είναι ο ανιχνευτής παρακολούθησης κατάστασης δέσμης (BCM), το κοντινότερο στη δέσμη σύστημα του ATLAS. Τεχνητά (pCVD) διαμάντια χρησιμοποιούνται για την ανίχνευση καθώς είναι το μόνο υλικό που μπορεί να επιβιώσει σε περιβάλλον με τόσο υψηλές δόσεις ακτινοβολίας. Ο ανιχνευτής BCM παρέχει συνεχή παρακολούθηση της δέσμης και προκαλεί απόρριψη της σε περίπτωση ασταθούς κατάστασης. Επίσης ο ανιχνευτής BCM παρέχει μετρήσεις για την φωτεινότητα (luminosity) της δέσμης καθώς και έξι σήματα trigger στους άλλους υποανιχνευτές του ATLAS όταν υπάρχει ένα γεγονός που αξίζει να καταγραφεί.

Στα πλαίσια αυτής της διπλωματικής εργασίας, δύο διαφορετικές επεκτάσεις του αλγορίθμου απόρριψης δέσμης υλοποιήθηκαν με σκοπό να βελτιώσουν την αποτελεσματικότητα στην απόφαση για απόρριψη ή μη της δέσμης. Επίσης ένα σύστημα υλοποιήθηκε σε VME πλακέτα με σκοπό να κωδικοποιήσει, να αθροίσει και να συγχρονίσει τα σήματα trigger του BCM. Τέλος, γίνεται μια μελέτη των ανιχνευτών διαμαντιού και των αναλογικών ηλεκτρονικών κυκλωμάτων που βρίσκονται κοντά στους ανιχνευτές του BCM, καθώς και μια μελέτη για την υλοποίηση ενός κυκλώματος παραγωγής παλμών στο σύστημα αναλογικών ηλεκτρονικών.

ΛΕΞΕΙΣ ΚΛΕΙΔΙΑ

BCM, ανιχνευτής, ATLAS, pCVD διαμάντια, αλγόριθμοι απόρριψης δέσμης, σύστημα άθροισης trigger, αναλογικά ηλεκτρονικά, σύστημα παραγωγής παλμών.

Abstract

During the operation of the the Large Hadron Collider (LHC), the world's largest operational particle accelerator, located at CERN, Geneva, the enormous energy levels (up to 7 TeV) of the colliding beams pose a considerable danger to the operating detectors (from the high radiation doses caused by LHC beam incidents). Experience from previous experiments led to the development of a dedicated system for every detector, capable of detecting anomalous beam incidents within strict time limits. The diamond Beam Condition Monitor (BCM) detector, innermost sub-system of the ATLAS detector was developed to meet these requirements. pCVD diamonds are used, the only sensing material capable of surviving and adequately performing under such hostile radiation environment. The BCM detector is responsible for the online monitor of the beam and triggers a beam abort signal in case of beam instability. Moreover the BCM detector provides beam luminosity measurement and six trigger signals to the other ATLAS sub-detectors in case of interesting beam events.

For the purposes of this thesis, two different abort algorithm extensions were implemented in order to enhance the efficiency of the beam abort decision. Furthermore, a VME based system was developed in order to encode, add and synchronize the outputs of the trigger signals. Finally, within this thesis, a study of the diamond detectors and the analog front-end electronics of the BCM detector, is presented and discussed, including the study for the implementation of a pulser circuit.

KEYWORDS

BCM, detector, ATLAS, pCVD diamond, beam abort algorithms, trigger adder, analog electronics, front-end, pulser circuit.

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Chapter 1:

LHC and ATLAS description

1.1 Introduction

Throughout the history of science and research it has been proven that experiments were one of the most essential tools used in order to further progress in the field. The empirical knowledge acquired from experiments was used to establish or disprove theoretical approaches and assumptions, especially in natural sciences. In the field of particle and nuclear physics, particle detectors are the utmost tool for producing useful experimental data in the search for empirical knowledge and answers. Currently the standards have been set quite high and it is essential that the particle detectors have to work up to such energy levels, capable to create and detect extremely heavy particles in a very wide range. A very important variable in particle physics is luminosity (L), which is defined as the number of particles per unit area per unit time times the opacity of the target, usually expressed in $\text{cm}^{-2} \text{s}^{-1}$. Luminosity could be explained as the “density” of the particle bunches that collide inside a detector, also related to the number of bunches that are being accelerated. High luminosity is required in order to provoke such events that will yield an adequate amount of data to be purposefully analyzed. To meet these requirements, a cooperation of more than 85 countries and 6500 researchers all around the world has been agreed upon, being driven and coordinated by the European Center for Nuclear Research (CERN). The particle accelerator built in order to achieve such a performance at CERN is the Large Hadron Collider (LHC).

1.2 The Large Hadron Collider

The Large Hadron Collider (LHC) [LHC95], the world's largest operational particle accelerator, aims to further extend the frontiers of particle physics (Figure 1-1). Located at CERN near Geneva, it expands under Swiss-French borders with a circumference of 26.7 km. This circular proton-proton collider lays from 50m to 170m underground, accelerating two counter-rotating beams in two rings up to an energy of 7 TeV, each one with a frequency of 40 MHz. Its center of mass energy of $s = 14$ TeV will be seven times higher than today's highest reached center of mass energy by the Tevatron accelerator at Fermilab. By filling each of the rings with 2808 bunches of 1.15×10^{11} protons each, LHC is designed to reach an instantaneous luminosity of $L = 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ which is two orders of magnitude above the present accelerators' luminosity levels. This results in a beam current of $I_b = 0.582 \text{ A}$ and a total stored energy in the beams of 724 MJ. This energy is sufficient to heat about 1.5 tons of copper from room temperature to its melting point. The LHC will also collide heavy ions (lead nuclei) at 5.5 TeV per nucleon pair, at a design luminosity of $10^{27} \text{ cm}^{-2} \text{ s}^{-1}$.

At the beginning of the accelerator chain, a small linear accelerator and a subsequent booster inject protons into the Proton Synchrotron (PS), which accelerates them to 26 GeV. Above this energy level and up to 450 GeV SPS (Super Proton Synchrotron) is used to accelerate the protons before inject them to the LHC. For circulating and accelerating the beams across the 26.7 km of the LHC tunnel, 1232 superconducting dipole magnets are used. They produce a magnetic field of 8.4 T in each of the beampipes able to bend, squeeze and focus the two counter-rotating beams.

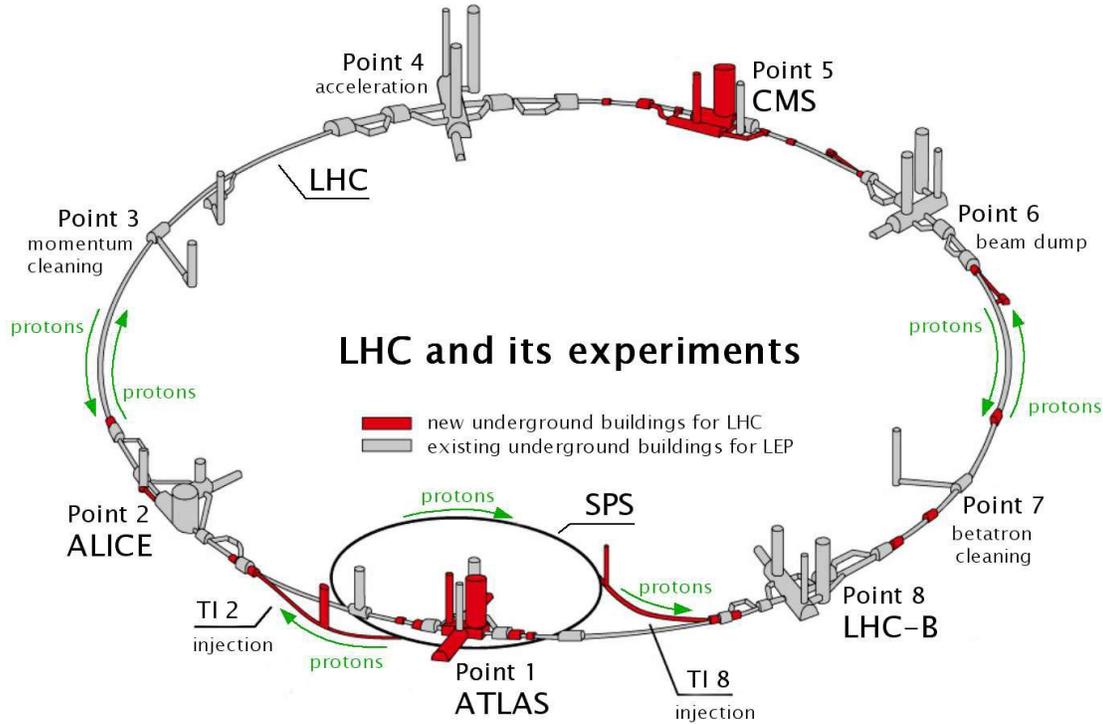


Figure 1-1: The LHC ring and the Experiments [DOB04]

The necessary cryogenic system cools down the temperature to 1.9 K using super fluid liquid helium. Around the ring, there are four experimental caverns at Points 1, 2, 5 and 8 (as seen in Figure 1-1) where detectors are installed. Two multi-purpose detectors, the ATLAS experiment as described in paragraph 2.3 and the CMS (Compact Muon Solenoid) experiment will investigate the p-p collisions and search new high energy particles. LHCb will mainly focus on b-physics and ALICE [ALI95] will elucidate the physics of the quark-gluon plasma. In each of the detectors a crossing point of the two beampipes creates the interaction point where the two counter-rotating beams collide.

1.3 ATLAS: A Toroidal Lhc ApparatuS

One of the largest particle detectors ever built, ATLAS, is placed in a cavern in point 1 of the LHC, designed to exploit the full physics potential of the proton-proton

collisions up to 14 TeV created by LHC. ATLAS aims to detect decay products of unstable standard model particles such as the Z, W, the predicted Higgs boson and other particles from theories which go beyond the standard model. The ATLAS collaboration consists of more than 2900 participants from over than 170 institutes worldwide, working continuously for the detector's successful operation. The high performance requirements of the detector were summarized in the ATLAS Technical Proposal published in 1999 based on the following criteria:

- Very good electromagnetic calorimetry for electron and photon identification and measurement, complemented by full-coverage hadronic calorimetry for accurate jet and missing transverse energy measurements
- High-precision muon momentum measurements, with the capability to guarantee accurate measurements at the highest luminosity using the external muon spectrometer alone
- Efficient tracking at high-luminosity for momentum measurement of high pT leptons, electron and photon identification, τ -lepton and heavy-flavor identification
- Large acceptance in pseudo-rapidity with almost full azimuthal angle coverage everywhere
- Triggering and measurements of particles at low-pT thresholds, providing high efficiencies for most physics processes at LHC.

The detector's dimensions are proportional to its reputation: radius of 11m, length of 46 m and a paramount weight of 7000 tons. For better understanding the size of ATLAS, one could imagine that it is about half as big as the Notre Dame Cathedral in Paris and weighs the same as the Eiffel Tower. The overall detector layout is shown in Figure (find figure), showing the subdetectors and magnet systems. Concerning the coordinate system, beam direction defines the positive z-axis, the positive x-axis points from the interaction

point to the center of the LHC and the positive y -axis points upwards. The azimuthal angle φ is measured around the beam axis and the polar angle θ is the angle with respect to the beam axis. The major components of the detector are briefly described below in figure 1-2:

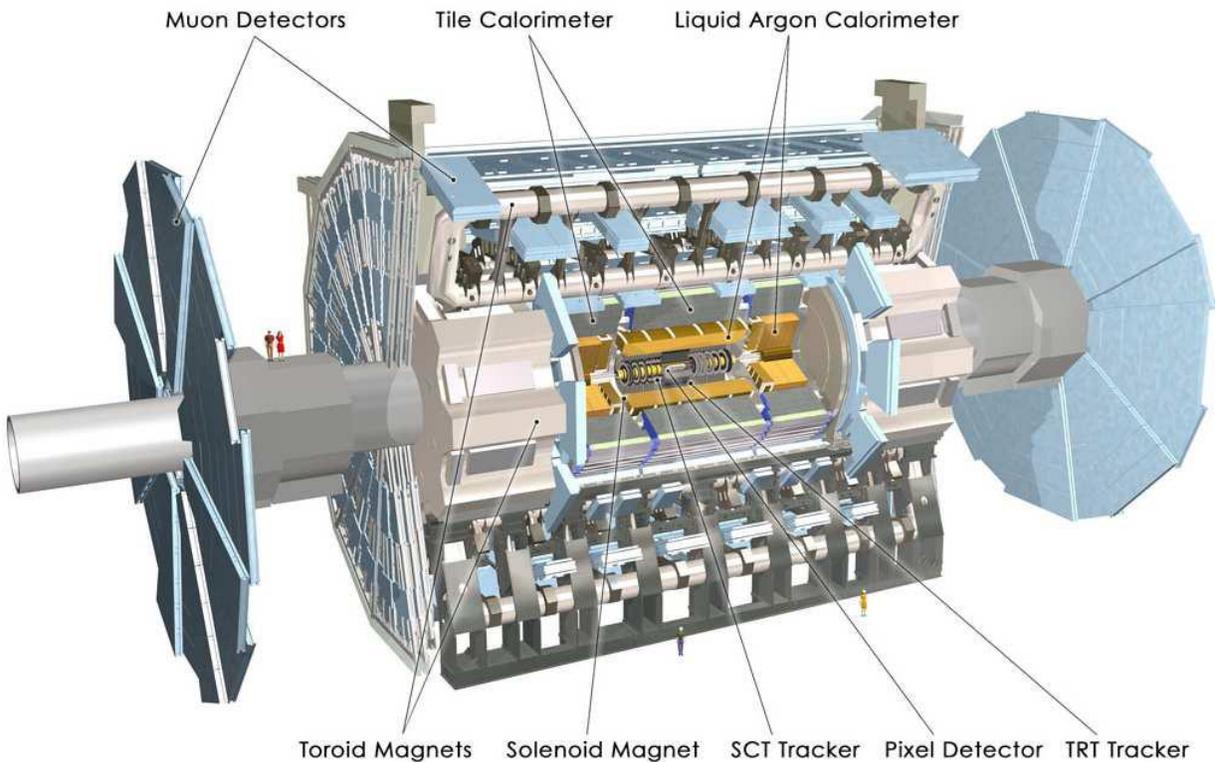


Figure 1-2: The ATLAS Detector Overview [ATL08]

1.3.1 Magnet System

Two different superconducting magnet systems are used in ATLAS [ATL97a], a central solenoid that surrounds the inner detector and an outer toroid system responsible for the momentum measurement in the muon spectrometer. This system of superconducting magnets has been one of ATLAS most challenging engineering accomplishments due to its size, weight of 1300 tons and the energy of 1600 MJ being stored when fully operational. The magnet coils are made from aluminum stabilized NbTi

superconductor, which will be cooled down to 4 K by a cryogenic liquid helium system.

The solenoid magnet is located in the barrel cryostat between the electromagnetic calorimeter and the inner detector. Designed to be as thin as possible (only 45 mm) in order to minimize the radiation length as the particles are on their way to the calorimeter, it has a length of 5.3m with a diameter of 2.4m and the total assembly weight reaches 5.7 tons. The solenoid magnet provides a 2 T axial field for inner detector tracking, powered by an approximately 8 kA power supply.

The toroid magnet consists of the barrel toroid and two end-cap toroids, designed to provide the magnetic field for the muon spectrometer. Each toroid has eight superconducting coils powered by a 20,5 kA power supply. The barrel toroid coils provide a peak toroidal magnetic field at their superconductors of 3.9 T and are housed in eight individual cryostats.

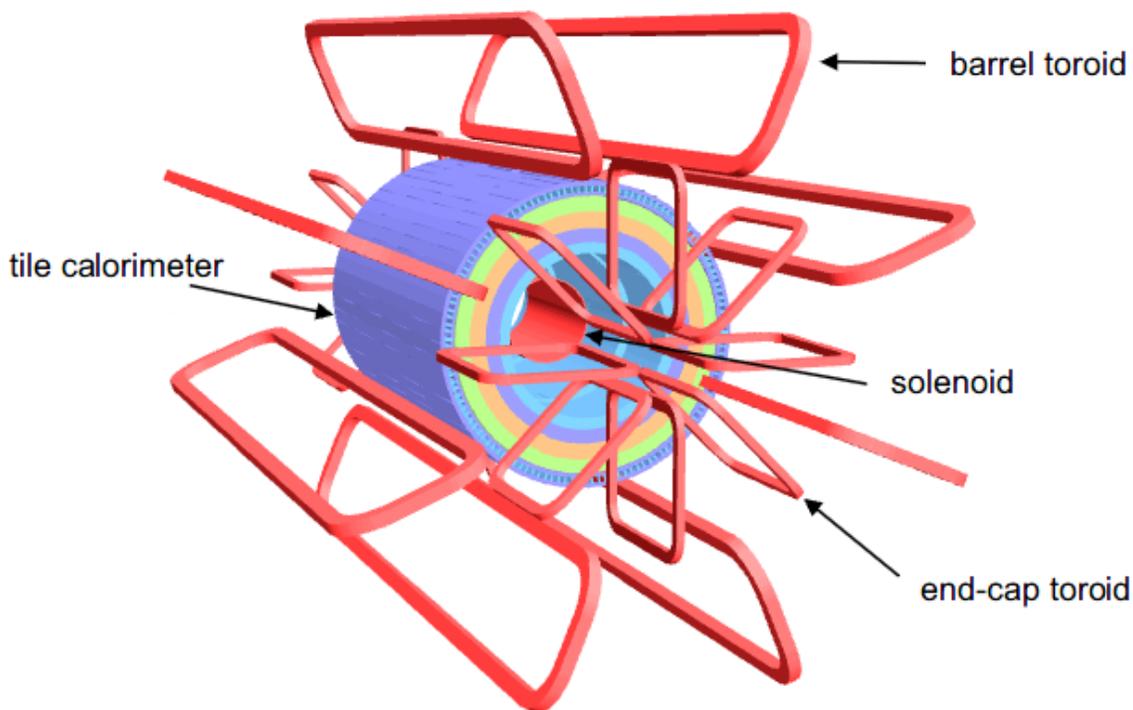


Figure 1-1: The ATLAS Magnet system [ATL04]

With an outer diameter of 20m and 26m length in the barrel area, they were the first components to be installed in the pit, as the rest of ATLAS fits within them. The end-cap coils are smaller and were installed last to “close off” the detector, housed in one large cryostat per side. Each coil has an axial length of 5m and extends radially from 1.65m to 10.7m, providing a magnetic field at their superconductors of 4.1 T. They are rotated by 22.5° with respect to the Barrel Toroids in order to provide radial overlap and to optimize the bending power in the interface regions of both coil systems.

1.3.2 Muon System

The muon spectrometer [ATL97e] (figure 1-4) is the outermost subdetector of ATLAS thus defining the size of the whole detector. It is designed to measure precisely the momentum of charged muons, the only detectable particles that traverse all the calorimeter absorbers without being stopped. The calculation of the muon’s momentum is achieved by measuring the bending of their tracks in the toroidal magnetic field instrumented with separate trigger and high-precision tracking chambers. In the muon system, the average magnetic field is 0.6 T, allowing for a measurement of muon momentum up to 6 TeV.

The alignment of the muon system is critical since its dimensions are so large and prone to displacement and deformations. An optical alignment system monitors the chambers and misalignments can be detected and corrected to a design precision of $30\ \mu\text{m}$ via offline analysis. Depending on the pseudorapidity η (add reference) and the aim to be achieved different technologies are used in the muon system.

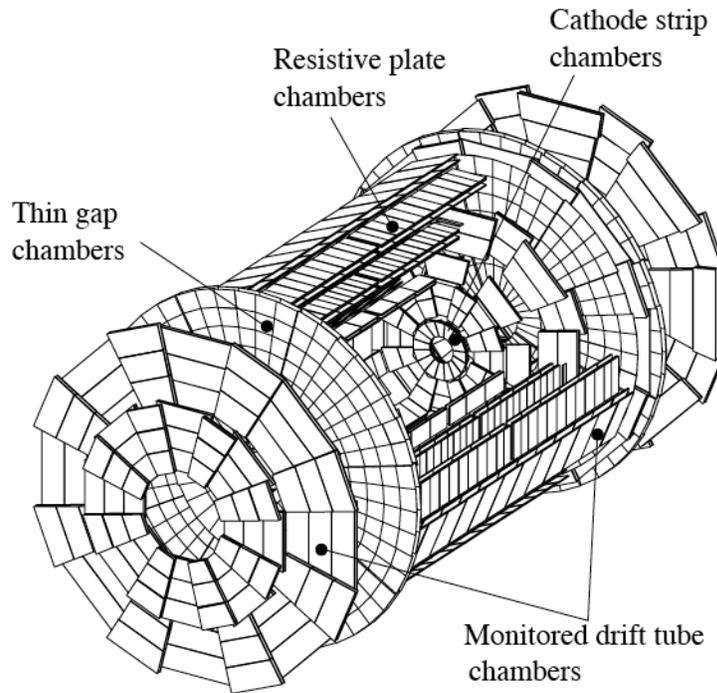


Figure 1- 2: The ATLAS Muon System [BIL07]

The Monitored Drift Tubes (MDTs) chambers consist of aluminum tubes of 30 mm diameter and a central wire. When a muon crosses a tube, electrons are being released by ionization and then drift to the wire. The distance between the muon track and the wire is determined by measuring the drift time of the first cluster that reaches the wire. The resolution on the drift distance is around 80 μm . MDT chambers are used both in the barrel and end-caps of the muon system in the region of $\eta < 1.05$ in the barrel and up to $\eta < 2.7$ in the end-caps.

The Cathode Strip Chambers (CSCs) are multi-wire proportional chambers with a cathode strip readout. The precision coordinate is determined from the charge distribution measured on the cathode strips while the second coordinate is obtained using strips which are vertical to the anodes. The CSCs are used in the inner-most end-cap ring, closest to the beam-pipe, in the region $2 < \eta < 2.7$. They have high spatial resolution of 60 μm , very small electron drift time of less than 30 ns and low neutron sensitivity.

The muon trigger is provided by Resistive Plate Chambers (RPCs) in the barrel region and by Thin Gap Chambers (TGCs) in the end-cap region. The RPCs are much simpler to make due to the fact that no wires are used. They are constructed from two parallel resistive Bakelite plates separated by insulating spacers, creating a narrow 2 mm gas gap. A uniform electric field of 4.5 kV/mm is used to multiply the primary ionizations. Metal strips, coupled to both sides of the detector read the signals with the excellent time resolution of 1.5 ns. The TGCs are similar to the CSCs but with the anode wire pitch larger than the cathode-anode distance. The chambers are operated using a highly flammable gas mixture (55% CO₂ and 45% n-pentane). The gas gap has a length of 2.8 mm and an expected operating high voltage of 2.9 kV resulting in a short drift time and good time resolution.

1.3.3 Calorimeter system

The goal of the ATLAS calorimeter system is the identification and precise measurement of the energy of particles as well as the process of distinguishing them. An electromagnetic calorimeter [ATL96c] is used to measure and identify electrons and photons and a hadronic calorimeter [ATL96b] to measure the energy of both charged and neutral hadrons. Showers of lighter particles such as the γ and e^\pm are totally contained in the electromagnetic calorimeter. The hadronic showers consist of hadrons and muons and overpass the EM calorimeter. Most of them will be absorbed in the hadronic calorimeter as only neutrinos and muons with enough energy can escape through the calorimeter system.

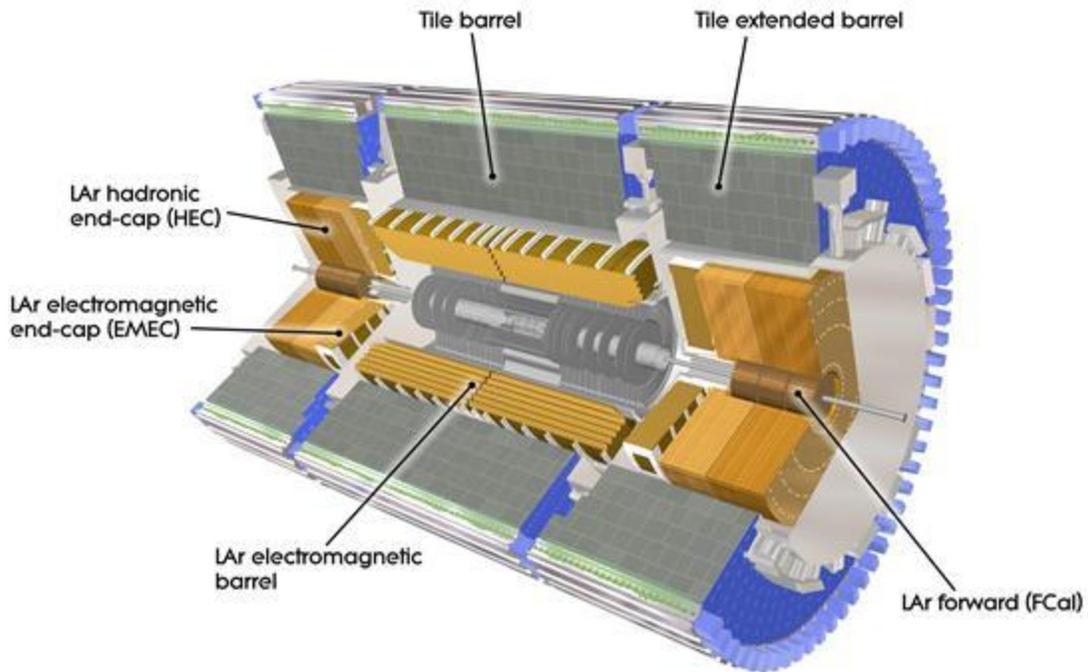


Figure 1- 5: The ATLAS Calorimeter System [EIF09]

The electromagnetic calorimeter is a lead and liquid-argon sampling calorimeter that consists of a barrel sector and two end-caps. The Kapton[®] cathodes have an innovative geometry similar to accordion which ensures hermetic coverage by minimizing the gaps between different detector modules. Lead plates are used as absorbers and the liquid argon (LAr) gap sampling material. The electromagnetic showers in the argon liberate electrons that are collected and recorded. Inside the barrel the LAr gap has a constant thickness of 2.1 mm but in the end-caps the amplitude of the accordion waves increases with radius so the gap thickness varies. As electromagnetic showers start from the inner-detector region a pre-sampler of an active layer of liquid-argon with a thickness of 1.1 cm is placed in the barrel region of $\eta < 1.8$ to correct the energy measurements.

In the hadronic calorimeters three different techniques are used depending in the pseudorapidity of the different regions. In the barrel ($\eta < 1.0$) and the two extended barrel regions ($0.8 < \eta < 1.7$) scintillating tiles of plastic 3mm thick are used as active material and

iron plates 14 mm thick as absorbers. The hadronic showers cause the plastic scintillating tiles to emit light which is detected and recorded. As a result of the active material the barrels and the two extended barrels are called Tile Calorimeter. The two end-caps receive much higher radiation dose ($1.5 < \eta < 3.2$) and therefore liquid argon (LAr) is used as sampler due to its radiation hardness add copper plates as absorber material. Accordingly, the forward calorimeter covers the pseudorapidity region $3.9 < \eta < 4.9$ where the radiation dose is extremely high. For this reason a new technology of copper and tungsten as absorbers is used combined with liquid argon as sampling material. To prevent neutrons from being scattered back into the inner detector the forward calorimeter is placed 1.2 meter further away from the interaction point compared to the electromagnetic calorimeter end-caps.

1.3.4 Inner Detector

The ATLAS Inner Detector (ID) [ATL97f] is designed to provide among others: exact momentum resolution and pattern recognition for charged particles as well as the primary and secondary vertex measurements. This means that ID has the possibility to reconstruct the tracks of particles that are products of the interaction in the collision point (primary vertex) or decays (secondary vertex) of the outgoing particles. Placed inside the solenoid magnet, Inner Detector uses the creating magnet field of 2T for accurate measurements in the region of pseudorapidity $\eta < 2.5$. The outer radius of the Inner Detector is 1.15 m and the total length 7 m. In the barrel region the high-precision detectors are arranged in concentric cylinders around the beam axis, while the end-cap detectors are mounted on disks vertical in respect to the beam axis. It consists of a Pixel detector, a Semi-Conductor Tracker (SCT) and a Transition Radiation Tracker (TRT) that will be briefly described below. The innermost subdetector is diamond Beam Condition Monitor (BCM) detector which will be explicitly described in the next chapter.

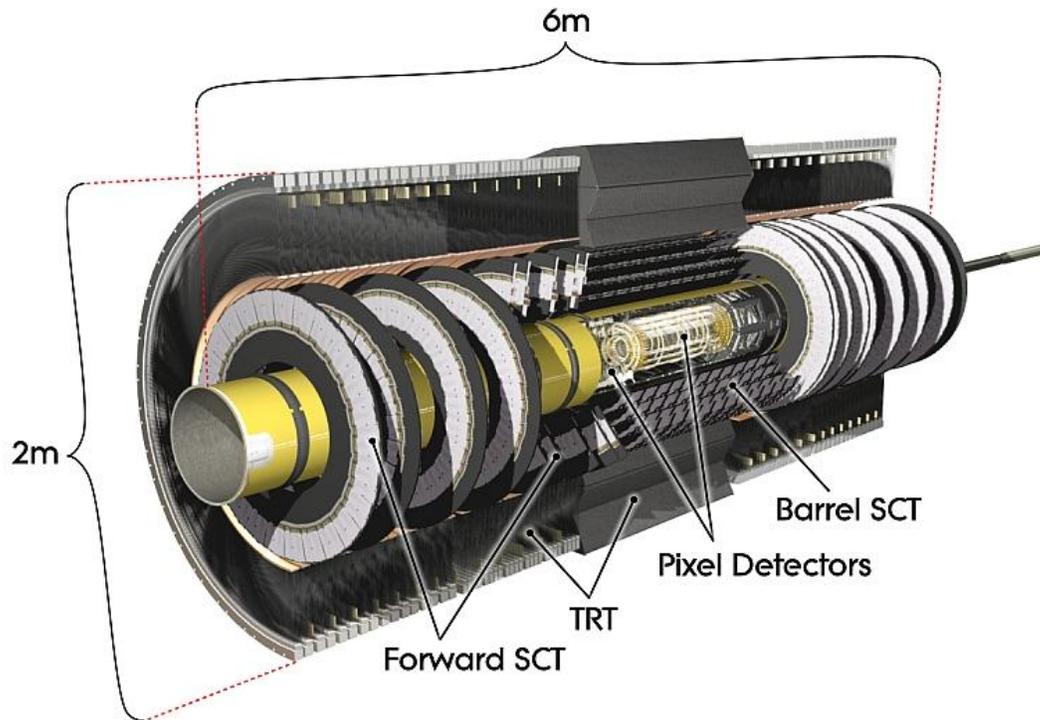


Figure 1- 6: The Inner Detector and the subsystems [ATL04]

Pixel Detector

Located very close to the interaction point, pixel detector [ATL98a] is involved in precise measurements for short lived particles and pattern recognition as well as for providing important tracking information for B-physics. It consists of three concentric barrels with radii of 5 cm, 9 cm, and 12 cm and three end-cap disks on each side with radii between 9cm and 15cm. As far as the detector modules are concerned, 1456 are located in the barrels and 288 in the disks. Each module is 6.2cm long and 2.1cm wide, hosting 46080 pixel elements i.e. silicon sensors that are read out by 16 chips. The modules are placed on an overlapping architecture, thus providing a hermetic coverage. More than 80 million pixels totally measure the charge deposition caused by the ionization of charged particles driven through them.

A process of recording the time over-threshold of the signal gives a measure of the amount of charge deposited in a single pixel while charge distribution over adjacent pixels determines the hit position. The pixel modules have a resolution of 12 μm in the R-coordinate, and 110 μm in the Z-coordinate. For each pixel channel, the electrical signal is amplified, shaped and compared to a threshold in order to provide a binary output for the readout system. The pixel tracker is situated so close to the beam pipe that has to cope with high particle flux density and a severe radiation environment. The readout chips must withstand more than 300 kGy of ionizing radiation and $5 \cdot 10^{14}$ neutrons per cm^2 over ten years of operation. Although pixel modules have been designed and tested thoroughly to meet the necessary requirements the replacement of the chips is necessary every few years.

Semi-Conductor Tracker (SCT)

The SCT system [ATL97g] is a tracker designed to provide precise measurements per track using strips of silicon sensors. Totally eight accurate measurements give important information about momentum, impact parameter (put reference) and vertex position for particles originating from the interaction point, up to a pseudorapidity coverage of $\eta \leq 5$. Additionally, SCT provides pattern recognition using the very good granularity of the system. It consists of a barrel region with 4 barrel layers and one end-cap in each side with 9 end-cap disks.

The barrel area has 4 different concentric barrels with radii of 30, 37.1, 44.3 and 51.4 cm. In the 4 barrels, silicon p-i-n detectors with dimensions of 6.36 x 6.40 cm^2 are composed by 768 readout microstrips of 80 μm pitch each. In each side of an SCT barrel module, two of these silicon detectors are wire-bonded together to give an active strip length of 12.3 cm. The two sides of a module are glued together with a small stereo angle of 40 mrad in order to provide positional information along the z-direction, separated by a heat transport plate. On each barrel, the modules are placed in rows with a slight angle of 11° between them, thus providing coverage in $R\phi$ -z coordinates and reducing the effects of

the ionization electrons. The front-end electronics are included on the detector itself, consisting of a front-end amplifier, a discriminator and a binary pipeline to store the hits.

The end-caps consist of nine disks and a cylinder for supporting in each side, placed from 27.5cm to 56cm from the interaction point. Depending on this distance, the disks are equipped with three rings of modules: inner (52 modules), middle (40 modules) and outer (40 modules). To provide overlap in $R\phi$ direction, inner and outer modules are placed on one side of each end-cap disk, the middle modules are placed on the other side. There are totally 988 modules in each end-cap partited to four different types. The modules have trapezoidal shape and are similar to the barrel ones using the same front end electronics and readout system. The basic difference is that the end-cap modules use tapered strips with one set aligned radially. In total SCT uses 6.2 million channels to reach a spatial resolution of 16 μm in $R\phi$ direction and 580 μm in z direction. So, it is possible to distinguish tracks which are separated more than 200 μm .

The detector design is constrained by the expected levels of irradiation during the 10 years LHC will run. The modules are operated cold (sensors at -7 C°) in order to prevent overheating from the front-end electronics heat emission as well as to keep the consequences of radiation damage within limits.

Transition Radiation Tracker (TRT)

The Transition Radiation Tracker (TRT) [ATL97g] consists of small straw detectors placed in the barrel and the two end-caps, designed to provide information related to tracking measurements as well as particle identification. In the barrel region, 73 layers of 144 cm long straws are placed in parallel with the beam while in the end-cap region the 37 cm long straws are arranged radially in wheels. Due to the geometry of the TRT straws, the 420.000 electronic channels provide typical 36 space points per track. The straws in the barrel part are divided in two pairs and read out at each end to give a more accurate measurement whereas the readout for the end-cap straws is positioned at their outer end.

The barrel section contains individual modules between 329 and 793 straws each, covering the radial range from 56 to 107 cm. The first six layers are inactive over the central 80 cm of their length to reduce their occupancy. Each end-cap consists of 18 wheels. The innermost 14 cover the radial range from 64 to 103 cm, while the last four extend to an inner radius of 48 cm. Wheels 7 to 14 have half as many straws per cm in z as the others, to avoid an unnecessary increase of crossed straws and material at medium rapidity.

The straw detectors have a diameter of 4mm enclosing a gold plated wire in the center and are filled with a gas mixture containing Xenon. The 30 μm diameter gold-plated W-Re wire has fast response, good mechanical and electrical properties and is radiation hard. The transition radiation measurement works on the principle that a charged particle emits X-rays when crossing the boundary between two materials with different dielectric constants such as the straw detectors. The drift-time measurement is based on the fact that the gas is becoming ionized by the passage of a charged particle causing the electrons' drift towards the wire and forming an avalanche close to the wire where the electric field is high. The time that is needed for the electrons to drift to the wire is measured every 3.125 ns or in 24 time bins in total of 75 ns.

Each channel can carry out a drift-time measurement with two different thresholds. The lower threshold detects the usual energy loss resulting from hitting the gas, and the higher threshold detects the energy loss plus the energy deposition from the X-ray. For each channel, this provides an accurate spatial resolution of 170 μm per straw.

1.3.5 Trigger and data-acquisition system

The bunch crossing (BC) rate in LHC is 40 MHz which means that every 25ns a collision is taking place in the detector when in operation. As ATLAS has approximately 200 million channels, the amount of the collected data is far too much to be fully

recorded. Hence, an advanced trigger system is designed to filter effectively the meaningful physics events from the needless information. The ATLAS trigger and data-acquisition (DAQ) system [ATL98b] is organized in three levels of online event selection, and each of these trigger levels refines the decision of the previous level by using a larger fraction of the data and more advanced algorithms. With an interaction rate of $\sim 10^9$ Hz and a goal of permanent storage rate of about 100 Hz, a rejection factor of 10^7 is required. Nevertheless excellent efficiency is needed for the rare new physics processes, e.g. Higgs boson decays. The trigger and DAQ system is schematically shown in Figure 1-453534.

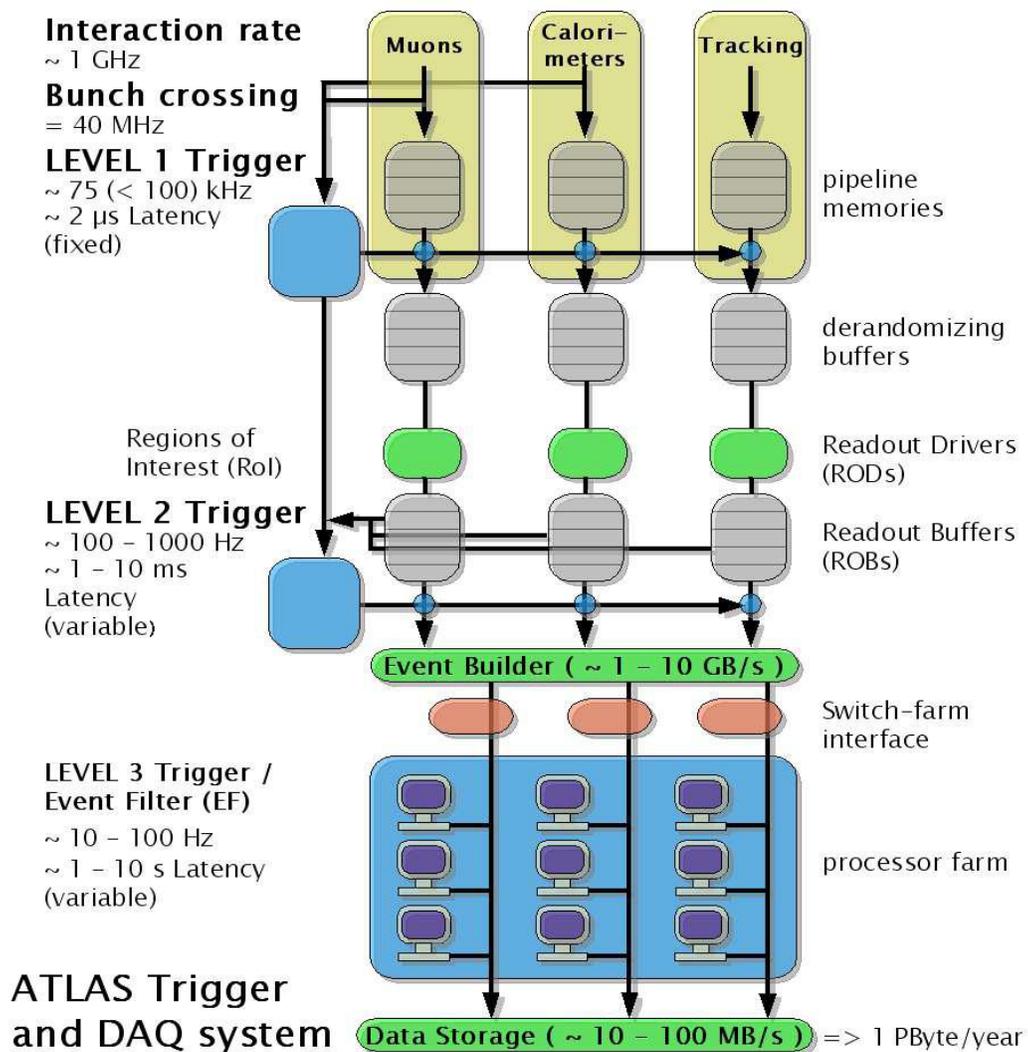


Figure 1-7: The ATLAS Trigger and Data-Acquisition System [DOB04]

The Level-1 trigger is a highly complex hardware system built from a calorimeter trigger, a muon trigger and a central trigger processor (CTP). The muon spectrometer identifies high transverse momentum muons using the RPC (barrel) and TGC (end-caps) trigger chambers. The remaining objects are identified using reduced-granularity information from all the calorimeters. The Level-1 decision is made by the CTP and distributed to all detectors in ATLAS at a maximum rate of 75 kHz by the TTC (Timing, Trigger and Command) system. The distribution of the signal to all the sub-detectors needs to be done quickly, as all detector front-ends have to pipeline and store information until the Level-1 decision arrives. The total Level-1 trigger latency is defined to be $\approx 2.5 \mu\text{s}$ for ATLAS which leaves about $1 \mu\text{s}$ for the CTP to make the Level-1 decision. Given the Level-1 trigger decision, all information from the front-ends of all sub-detectors is read out through the RODs (Read-Out Drivers) into the ROBs (Read-Out Buffers) by the ROS (Read-Out Sub-system). This data can be accessed selectively by the LVL2 trigger which uses regions of interest defined by the LVL1 trigger.

The Level-2 trigger [ATL98c] is an advanced software system that refines the selection of the events compared to Level-1, using full-granularity information from all detectors. The inner detector tracking information is also available for the Level-2 decision. The Level-2 trigger uses the Region of Interest (ROI) information provided by the Level-1 trigger to access information from every sub-detector but only for those sectors which triggered Level-1 and are temporarily stored in the ROBs. This allows an efficient event selection process since only a small percentage ($\approx 2\%$) of the full event data is needed for the event reconstruction. Triggers signals are generated at an average rate of 1 kHz with a maximum of 3 kHz while the event dependent latency varies from 1ms up to 10 ms for events with high track multiplicity.

The Level-3 trigger system, also known as the Event Filter (EF), is responsible for the final event selection. After the entire event building, which is performed using a data switch, the event information is passed on to the Event Filter Linux PC Farm. Advanced

off-line selection algorithms use the fully reconstructed event information, including up to date calibration and alignment software. Data is written to disk at a rate of 100 Hz (100 MB/s) with an average latency of 4 seconds. Every event stored contains ≈ 1.5 MB of information and is available for further analysis with the ATLAS offline software.

The trigger and data-acquisition system (TDAQ) provides also configuration, control, and monitoring of the ATLAS detector during data-taking. Supervision of the detector hardware (gas systems, power supply voltages, etc.) is provided separately by the detector control system (DCS).

Chapter 2

The ATLAS Beam Conditions Monitor (BCM)

2.1 Introduction

During the operation of the LHC the enormous energy levels (up to 7 TeV) of the colliding beams pose a considerable danger to the Inner Detector silicon trackers from the high radiation doses caused by LHC beam incidents. Experience from previous experiments shows that beam instabilities can cause serious damages to the inner parts of the detector. The most probable anomalous beam event is the pilot bunch¹ (450 GeV protons) scraping the Target Absorber Secondaries (TAS)² collimators. Other potential anomalous beam events that one should take notice of, are the beam-gas interactions, where beam protons interact with gas that has remained in the beam pipe and beam halo protons interacting with a TAS collimator close to the entrance of ATLAS cavern. All these unwanted events result in showers of particles, dangerous for the Inner parts of the ATLAS detector, thus, a dedicated system capable to detect such events and protect the other sub-detectors is necessary.

The system developed in ATLAS to serve these needs is the Beam Conditions Monitor (BCM) [BCM08]. Located very close to the beam pipe ($r \approx 55\text{mm}$), BCM is designed to detect anomalous beam events or instabilities and to protect the experiment

¹ To avoid beam failures at injection, the injection in an empty LHC ring always starts with a single bunch of low intensity, the so called pilot bunch, in order to probe the machine settings.

² TAS collimators are 1.8m long copper blocks located at $z = \pm 18\text{m}$ away from the interaction point. Their basic use is to protect the inner triplet of cryogenic quadrupoles (Q1) around the interaction point P1 and the Inner Detector from a variety of excessive heat loads and beam failures respectively.

against damaging beam losses by initiating a beam abort. It is also responsible for providing real-time monitoring of instantaneous particle rate close to the interaction point in order to distinguish between normal collisions and background events. At last, BCM provides a coarse luminosity measurement as a complementary information to LUCID, the main ATLAS luminosity monitor.

2.2 Principles of operation and requirements

The BCM detector consists of two stations, each with 4 diamond detector modules integrated in the Beam Pipe Support Structure (BPSS) at a radius of about 55 mm from the beam axis. Both stations (A and C sides) are placed symmetrically around the interaction point at $z = 184\text{cm}$, thus making possible to have a Time of Flight (TOF) measurement. Between two detector stations located at positions $\pm z$ along the beam-pipe, the TOF is measured in order to distinguish background from collision events. A collision event in the middle of the two stations results in $\Delta t^3 = 0$, whereas a background event outside of the two stations results in Δt measurements of $\pm 2z/c$. More specifically, collisions taking place in the interaction point (IP) reach both stations after 6.25 ns with $\Delta t = 0$ ns (in-time hits). Events taking place in a $z > 1.83\text{m}$ (outside the BCM stations) such as the TAS scraping, have $\Delta t = 12.5$ ns (out-of-time hits). Shower particles induced by background events generate signals in the nearest station 6.25 ns before the proton-proton collision at interaction point (out-of-time hits). The basic principle of the BCM operation is to use out-of-time hits to identify the background events and in-time hits to monitor the luminosity on a bunch-by-bunch basis [DOL08].

³ Δt is the time difference between the two stations of BCM detecting the same event

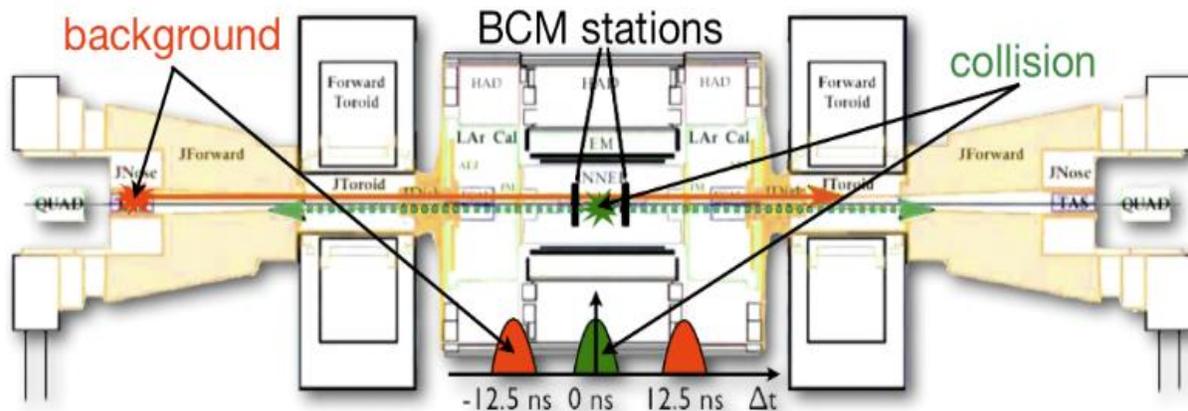


Figure 2-1: Schematic view of the TOF distinction between collisions [BCM09]

The design requirements for ATLAS BCM sensors and electronics are determined by the radiation environment and the necessary speed. Due to extremely hostile radiation conditions ($10^{15}/\text{cm}^2$ particles per 10 years of operation), it is mandatory to use a sensor that is completely radiation hard. Moreover, the rate of interactions in LHC (multiple interactions each every 25 ns) induce severe limitations on the requirements for the timing properties of the BCM detectors. More specifically, the timing characteristics should be: fast rise time ($\approx 1\text{ns}$), narrow width ($\approx 3\text{ns}$) and fast baseline restoration ($\approx 10\text{ns}$).

As far as the efficiency of event detection is concerned, a lot of simulations took place. One lost proton hitting the TAS collimator results in 0.06 out-of-time hits in the BCM system. One lost proton hitting the beam pipe at $z=3\text{m}$ simulation results in 0.14 hits in the BCM system. The case of one 7 TeV proton hitting the TAS was also studied resulting in 1.15 of hits in the BCM system. Accordingly, a simulation of proton-proton collision in ATLAS gives around 0.40 hits per collision. The need for distinguishing normal collisions from background events requires the BCM to be sensitive enough to detect single minimum ionizing particles (MIPs). This sensitivity is also required for the luminosity measurements. Poly-crystalline chemical vapor deposition diamonds (pCVD) were chosen as the more appropriate sensor material able to meet these strict requirements.

2.3 Diamond detectors

Due to its basic characteristics and properties, diamond is considered to be a very suitable sensor material for particle detectors. The large energy gap of 5.5 eV has as a result a very low leakage current ($\leq 1\text{nA}$) which is a very desirable and important property. The high thermal conductivity of diamond renders the cooling of the detector unnecessary. Moreover, due to its low dielectric constant ($\epsilon = 5.7$), diamond exhibits very low noise and detector capacitance. Finally, the high displacement energy makes diamond radiation tolerant while at the same time the high saturation drift velocity and high breakdown electric field strength allow very fast signal response. However, the natural diamonds have a lot of disadvantages such as the high cost, the small size and the variability of some of its properties according to different diamond stones. These disadvantages were overcome with the development of the polycrystalline chemical vapour deposition (pCVD) diamonds. These are artificial diamonds which maintain the advantages of the diamond while eliminating the disadvantages of the natural diamonds as they were mentioned above.

The basic principle of the diamond operating as a particle detector is illustrated in figure 2-2. Two electrodes are placed across the material and a voltage difference V is applied to create an electric field inside the diamond. Due to diamond's high resistivity, no significant currents are developed inside the material. The bias voltage V_{bias} applied between the electrodes generates an electric drift field equal to that of an ideal plate capacitor with strength:

$$\mathcal{E} = \frac{V_{\text{bias}}}{D} \quad [\text{DOL08}]$$

where D is the thickness of the diamond [DOL08]. When an ionizing particle passes through the diamond, it leaves a trail of electron-hole pairs. The drift of electrons and holes as a result of the applied electric field induces a current pulse on the electrodes.

According to the Shockley-Ramo's theorem [BCM08], the current induced by a charge q drifting in a uniform electric field is calculated as:

$$I = \frac{Q_{gen}v}{D} \quad [BCM08]$$

where v denotes drift velocity and Q_{gen} the total generated ionization charge. The total charge measured Q_{meas} or integrated current (integration over time of the equation above) is then measured from the read-out electronics.

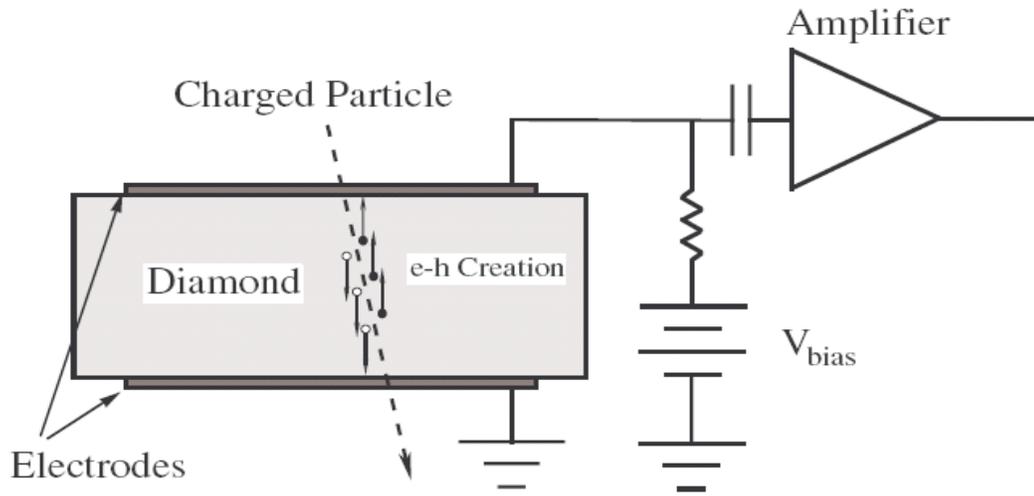


Figure 2-2: Schematic layout of a diamond particle detector [BCM08]

However, the induced ionization charge is reduced by charge trapping during its drift [BCM08]. For the characterization of CVD diamonds it is commonly used to measure the mean distance that electrons and holes drift apart before being trapped, called charge collection distance (CCD).

$$CCD = \frac{dQ_{meas}}{Q_{gen}} \quad [BCM08]$$

As diamond sensors are usually operated at high field strength, a normal value for the charge collection distance is set where the CCD saturates at $1 \text{ V}/\mu\text{m}$. For BCM

diamonds, an initial charge collection distance beyond 200 μm is required to achieve reliable single MIP signals. It should be noticed that the timing properties of the ionization current signal are excellent due to the high velocity of carriers ($> 10^7$ cm/s), at the BCM operating field of 2 V/ m, and short trapping times even before irradiation, as explained below. A characteristic of the pCVD diamonds is the increase of the charge collection efficiency caused by the exposure to ionizing radiation. This feature is called pumping and can be exploited by irradiating pCVD diamonds prior to its use as detectors to create an amount of free charge carriers, thus improving the charge collection efficiency. As mentioned before, the large displacement energy of diamond makes it radiation tolerant. High radiation doses could cause a decrease in the signal due to the trapping of drifting charge and an increase in leakage current which is not harmful and usually decreases after irradiation.

2.4 BCM detectors and front-end (FE) electronics

As mentioned earlier in this chapter, pCVD diamond was chosen as the sensor material for BCM to meet the requirements of the hostile radiation environment and the fast signals. A total of 8 diamond detector modules are fixed in the two BCM stations at $z=183$ cm from the interaction point as it is illustrated in figure 2-3. Each station contains 4 modules fixed in the beam pipe support structure (BPSS) at a radius of $r=55$ mm. Placed symmetrically around the beam axis at $\varphi=0^\circ, 90^\circ, 180^\circ$ and 270° , they are mounted at 45° in respect to the beam pipe, thus covering a pseudorapidity of $\eta \leq 4.2$ (figure 2-4) and increasing the signal by a factor of $\sqrt{2}$.

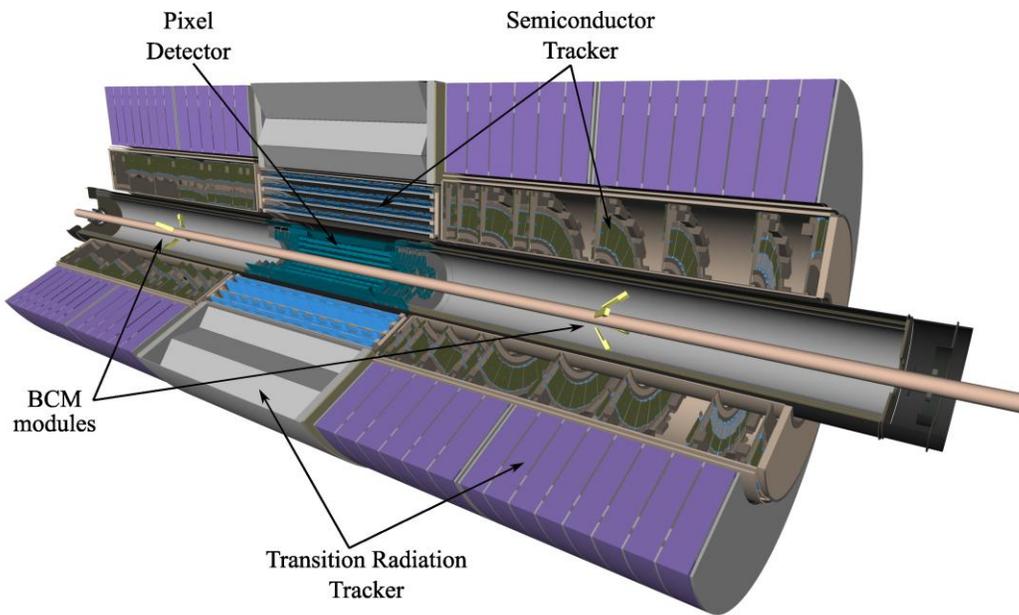


Figure 2-3: Position of the 8 BCM modules inside the Pixel volume [DOL08]

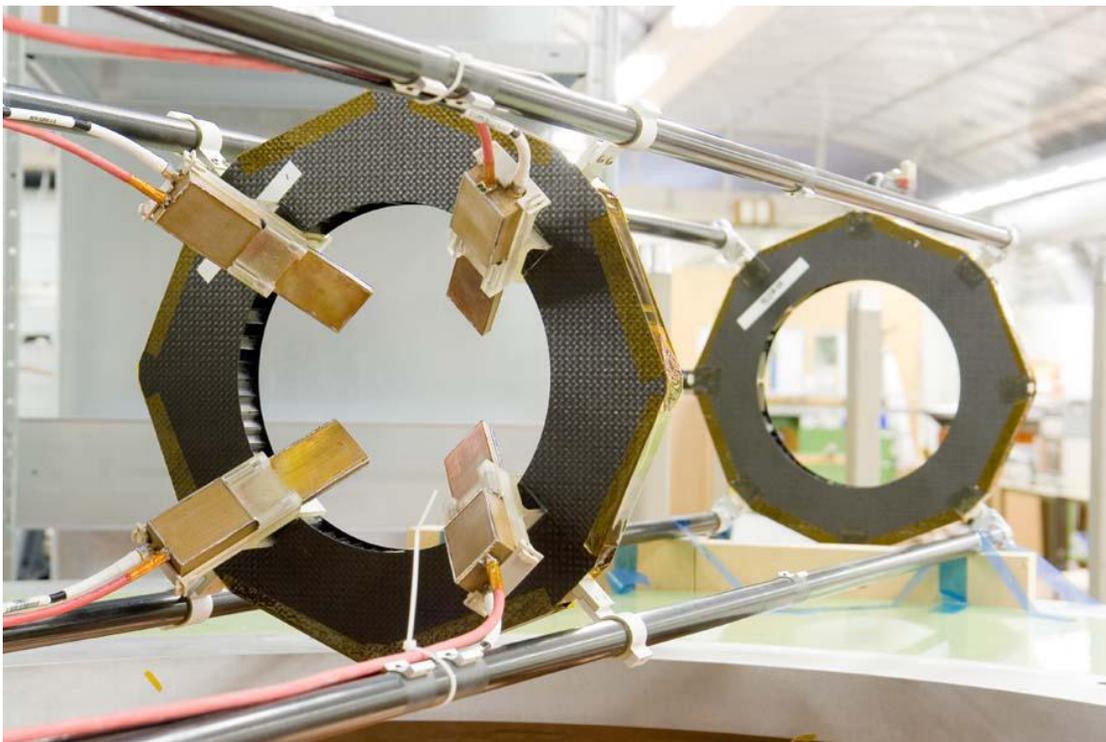


Figure 2-4: BCM modules mounted with an angle of 45° on the BPSS [NIE07]

Each module contains a pair of diamonds that are glued back to back to an alumina ceramic base board and the front-end electronics. The diamonds were developed by the CERN RD42 Collaboration [RD42] and produced by Element Six Ltd [ELS]. The dimensions of the diamond sensors are 1cm by 1cm with Ti-Pt-Au metal electrodes covering 8 mm by 8 mm (figure 2-5), and the thickness D is around $500\mu\text{m}$. The bias voltage V_{bias} is 1000 V which means that the uniform electric field is $2\text{V}/\mu\text{m}$. After measurements the leakage current is less than 100pA and the charge collection distance (CCD) is around $250\mu\text{m}$. The two sensors are assembled in a back-to-back or 'double-decker' configuration, thus doubling the charge signal while the noise is increased only up to 30%. Due to the ceramic base, the presence of leakage current is minimized at 1000 V which is the operating point of the diamond sensor system. The signals from the two diamonds sensors are transmitted via wire bonds to the printed circuit board and then to the read-out amplifiers.

The signal is sent to the front-end amplifier via a 5cm long 50 Ohm cable in order to reduce the radiation field by 30%. The front-end amplifier was designed by FOTEC [FOT] and consists of two separate amplifiers. The first stage of amplification is achieved by a 500 MHz Agilent MGA-62563 Gas MMIC low noise amplifier while the second stage uses a Mini Circuits Gali 52 In-Ga-P HBT broadband microwave amplifier. The first stage provides an excellent noise factor of only 0.9 db, with both stages providing an amplification of 20 dB each. The whole front-end system including the diamond sensors are shielded by a copper module box, in order to prevent RF intermodulations and each amplification stage is also isolated in a separate compartment (figure2-5).

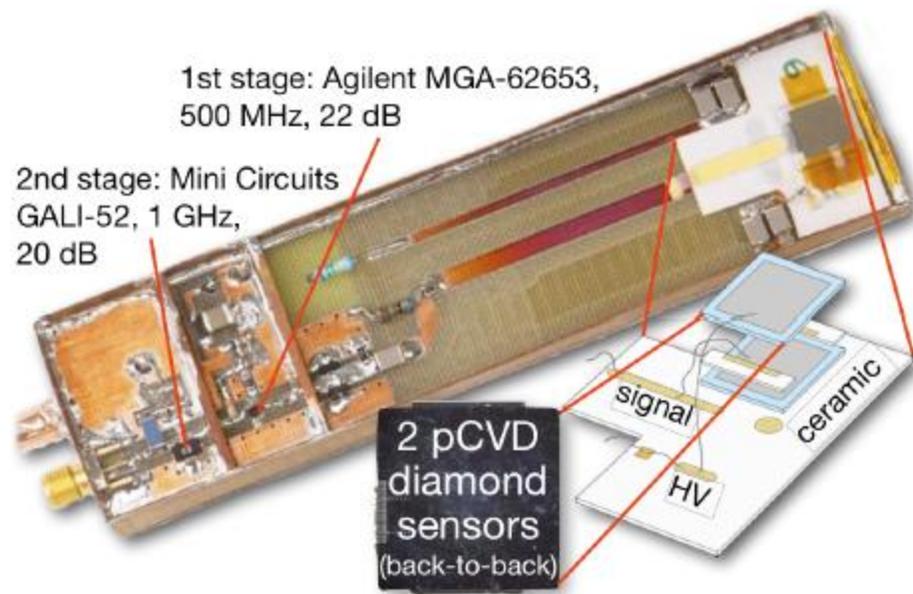


Figure 2-5 A BCM module with the 2 diamond sensors back-to-back and the read-out amplifiers [BCM09]

The feature of radiation tolerance was necessary during the selection of the readout amplifiers. Both stages were tested by irradiating them with protons and neutrons in fluencies up to $10^{14}/\text{cm}^2$. The results show an amplification loss of 4 dB in the first stage without any noise increase while the second stage exhibited an amplification loss of 0.5 dB. These results were more than adequate for the purpose of these experiments, performed under such a hostile radiation environment. Supplying the high voltage needed to the detectors, ISEG EHQ-8210 [ISE] units are used, also capable of providing monitoring of the current with 1nA resolution. The low voltage supply for the amplifiers is provided by a modified version of custom made power supplies for the ATLAS SCT detector. The circuit and features of the front-end electronics will be examined further in the 5th chapter where a simulation of the circuit will also be presented and discussed. The signals are routed via 14 m long 50 Ohm coaxial cables to readout electronics outside the ATLAS Hadronic Tile

Calorimeter, where less radiation tolerant readout electronics, with an expected ionization dose of 10 Gy⁴ in 10 years, can be used.

2.5 Off-detector electronics and readout

The back-end of the BCM readout system receives the signals from the front-end electronics and is responsible for the readout and the necessary online analysis. A digitization of the signals is initially performed inducing a marginal noise increase. Following the digitization a temporary storage of data is performed and a basic online analysis. The description of the off-detector electronics and the readout scheme follows, illustrated in figure 2-6.

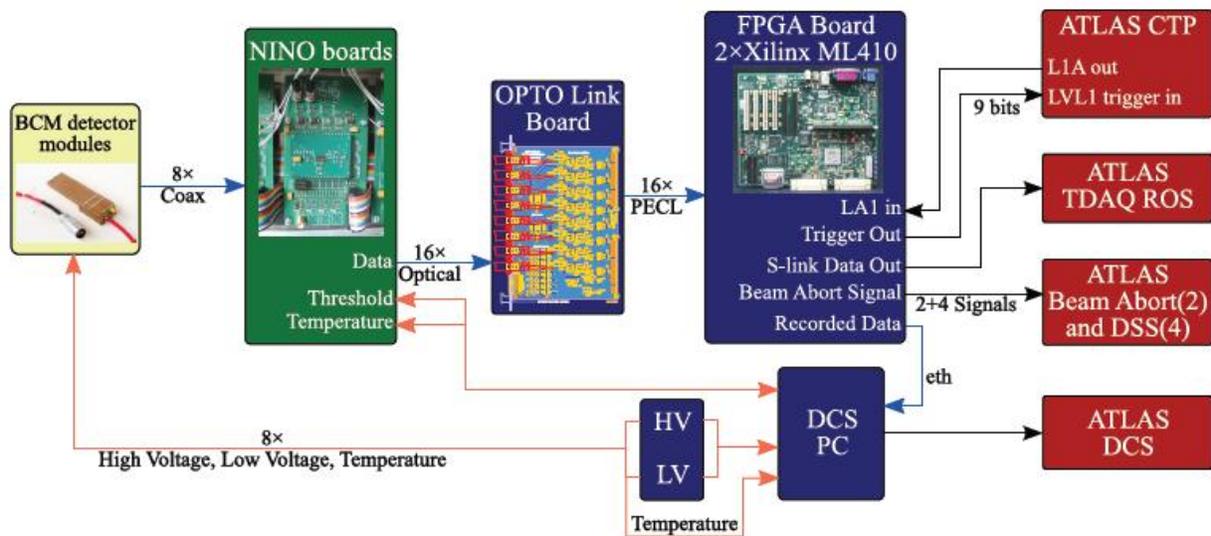


Figure 2-6: BCM read-out scheme [DOL08]

⁴ The **gray** (Gy) is the SI unit of absorbed radiation dose of ionizing radiation (for example, X-rays), and is defined as the absorption of one joule of ionizing radiation by one kilogram of matter

2.5.1 The Nino Digitizers

The output signals from the read-out amplifiers are sent outside the Tile Calorimeter where a 200 MHz fourth order Butterworth low-pass filter is used to eliminate reflections at the end of the 14 m coaxial cable and optimize the signal-to-noise ratio. After the filter, the signals are split with a ratio of 1:11, thus achieving a considerable increase of the dynamic range of the measurements as it will be explained below and the 16 in total signals are fed into the 2 NINO boards [A+04] for further signal processing. The NINO boards were initially designed for TOF measurements in the ALICE experiment at CERN.

In the Nino boards, the analogue signals of varying amplitude are amplified and digitized to give an output digital signal after a fixed time. The discriminators use to digitize the analog signals have adjustable thresholds in order to encode the charge seen at the front-end in terms of a Time-over-Threshold (TOT) measurement. Hence, the length of the digital output signal is correlated to the amplitude of the analog input signal.

The splitting of input signals with ratio 1:11 is necessary as the dynamic range of the NINO is small and the TOT response of NINO as a function of NINO threshold saturates quickly [DOL08]. The thresholds of NINO are set in a way that the larger signal is used for truly minimum ionizing signals (up to about 10 MIPs) while the smaller signal more than 10 MIPs, fact that means serious beam loss situations. The larger signals of each detector are called high gain channels (low threshold) due to the high gain of amplification and the smaller are respectively called low gain (high threshold), giving in total the 16 output channels of BCM. The output signals of NINO boards are LVDS⁵ compliant with rise time of 1 ns and jitter of only 25 ps.

These signals are then converted to optical via a set of radiation tolerant Mitsubishi FU-427SLD-FV1 laser diodes, and transmitted through 70 m optical fibers to the ATLAS USA15 counting room. There, an OPTO link board receives the signals and the inversed

⁵ Positive emitter-coupled logic (PECL) is a family of high speed digital integrated circuits.

procedure of converting the optical signals to PECL⁶ differential signals is followed, using a set of Lightron LP 104-SNC photo diodes as receivers. The complete optical system has a 3 dB bandwidth of 1.5 GHz, rise and fall times of about 300 ps and is radiation hard up to 10^{14} neutrons/cm² in the side of transmission.

2.5.2 The FPGA based Read Out Drivers (RODS)

The PECL differential signals coming out from the OPTO link receiver, are fed into the main part of the BCM readout system, the two FPGA based Read Out Drivers (RODs). These Xilinx ML410 development boards [XILa] are mounted in 19", 1U housings created also by Xilinx. [XILb] The heart of each ROD is a Xilinx Virtex-4 FX60 FPGA that performs all the necessary operations and analysis for BCM. It features 8 Rocket-IO Serial Multi-Gigabit Transceivers, two PowerPC cores and 56kB logic blocks. The mapping of which input is fed to each ROD is organized in a way that every ROD receives inputs from all BCM detectors. Thus, even if one of the RODs loses connection, the other ROD has the necessary information to perform the data analysis. For operating synchronously with the LHC bunch structure, the FPGA has to run at a multiple of the bunch clock (BC). This LHC CLK as well as other synchronization signals like the ORBIT⁷ signal are obtained from the Local Trigger Processor (LTP).

The selection of the specific FPGA model was based on its sampling capabilities of the Rocket-IO channels (up to 6.5 Gbps). The sampling of the incoming data is performed synchronously with the LHC bunch clock (40 MHz) at a rate of 2.56 Gbps. By using 2 Phase Locked Loops (PLLs), every LHC BC is divided into 64 slices of 390 ps each, a time

⁶ Low-voltage differential signaling (LVDS) is an electrical signaling system that can run at very high speeds over inexpensive twisted-pair copper cables.

⁷ The LHC Orbit corresponds to 3564 bunch crossings (BCs) and is sent to all detectors for data and operation issues synchronization.

resolution that is extremely accurate. To achieve such high sampling rates, the Rocket-IO channels require transitions in the incoming data stream so a fixed pattern is necessary to be generated and XOR-ed with the incoming signals. Internally, the complementary XOR operation is performed, restoring the original waveform.

After the sampling, the Raw data is stored in a DDR2 RAM which is a buffer that keeps data for the 3×10^6 last LHC bunch crossings (3 LHC orbits). In parallel, an advanced algorithm determines the leading edges of pulses and a time-to-digital conversion is performed, while the pulse widths are encoded to digitize the TOT information coming from the NINO. The data analysis for the hits of each detector is performed by an algorithm that uses a pipelined binary search tree and look-up tables. This way, the algorithm exploits the extremely fast processes of the FPGA to send the signals to the ATLAS CTP for the Level one decision. The signals should be sent within $2.5 \mu\text{s}$ and the time needed for the FPGA to implement this pipelining calculation is 5 BCs or 125 ns, time that is fast enough taking into account the delays of the cabling as well.

Additional analysis is performed by the FPGA including the calculation of in-time and out-of-time coincidences of signals between detectors in the two BCM stations. The determination of in-time and out-off time hits as well as the rates of each module or coincidences is done by using time windows. The BCM provides a lot of different information through the FPGA analysis to the several ATLAS and LHC systems:

LHC Beam Abort

In case of hazardous beam condition, BCM sends 2 signals through the ATLAS CIBU (Controls Interlocks Beam User) system to the LHC beam interlock system (BIS). These signals have to be fully redundant, able to trigger an immediate beam abort within 3 LHC turns. In the same way, abort and alarm signals are provided to the Detector Safety System (DSS) that is responsible for the safety of the various ATLAS sub-detectors. The

algorithms for deciding to abort the beam in case of beam instability will be discussed in chapter 4.

ATLAS Trigger and Data Acquisition (TDAQ)

Every time that BCM receives a L1A (Level 1 Accept) signal from the CTP, the raw event data is sent from the FPGA to the ATLAS TDAQ system using the standard ATLAS optical link (S-link). Digitized information about signal arrival times and their widths are stored as part of the ATLAS DAQ data stream. Moreover, an Ethernet connection to the ROD Crate DAQ (RCD) controller and a Single- Board-Computer (SBC) in a VME⁸-Rack are used.

ATLAS Level 1 Trigger

BCM is sending 6 trigger bits to the CTP for the Level 1 decision. These trigger bits are calculated in each ROD and then combined externally on a trigger adder board before send to the CTP. This board will be discussed in chapter 3.

ATLAS Detector Control System (DCS)

DCS takes care of controlling and monitoring voltages, temperatures and other important parameters of the detectors. The FPGA is connected to via Ethernet to a specific ATLAS DCS PC in order to monitor the temperature of detector modules and NINO electronics boards as well as to control and adjust parameters such as the high and low voltages. Moreover, useful information about average rates and histograms of the processed signals is made available to ATLAS DCS. If BCM or any other detector requests a beam abort, BCM freezes its circular buffers in both RODs and send all the recent data via Ethernet to the SBC for post-mortem analysis. This analysis gives information about the

⁸ VMEbus is a computer bus standard used for many applications and standardized by the IEC as ANSI/IEEE.

last 1000 orbits and when it is finished is then sent again to the DCS for further investigation.

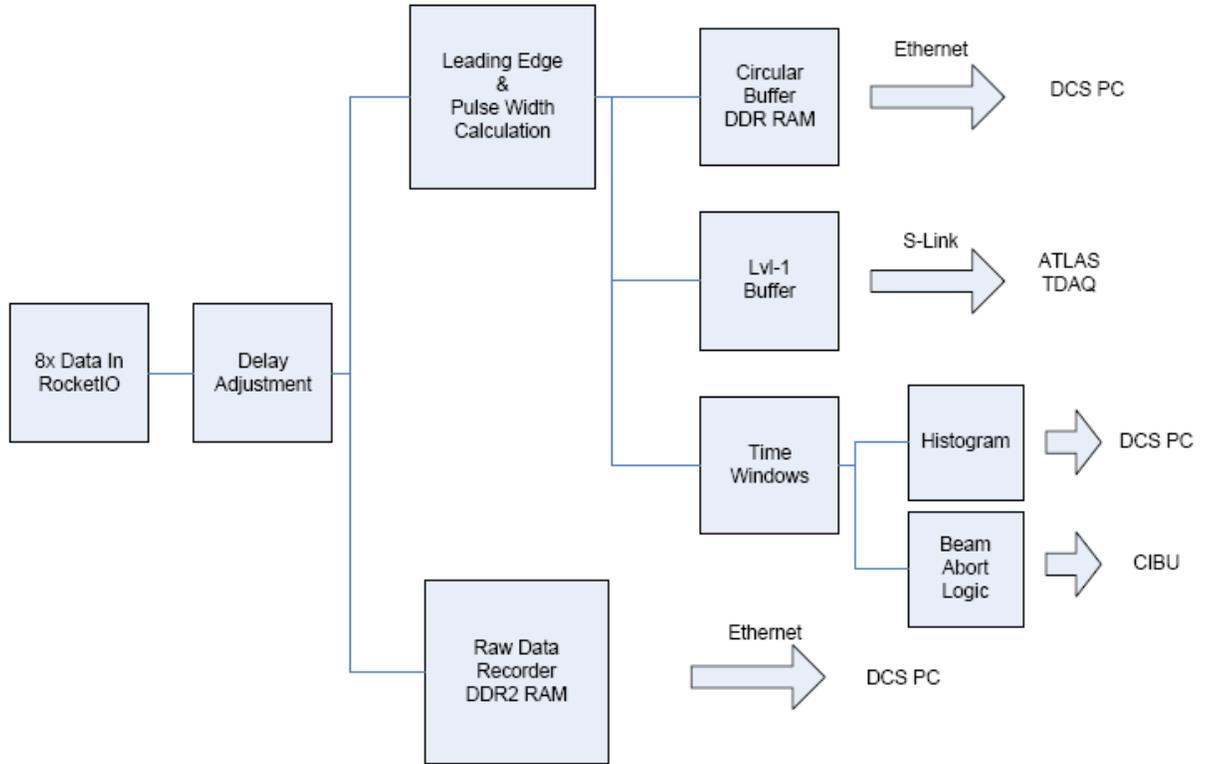


Figure 2-7: Block diagram of the basic FPGA operations [NIE07]

Chapter 3

BCM Trigger Adder board

3.1 Introduction

During the operation of ATLAS detector each subdetector provides several trigger signals to the CTP (Central Trigger Processor) which in turn feeds them to the other subdetectors. Apart from its crucial role in regards to the safety of ATLAS and providing important monitoring data, the BCM provides ATLAS with 6 trigger signals. Initially, the readout and real time analysis system was designed to provide 9 triggers but later on it was the consensus to reduce them down to 6. In order, though, to retain the same functionality with the reduced number of trigger signals an encoding of those signals, provided by the BCM, was necessary.

Two independent RODs are used for data analysis, receiving signals from the front-end electronics and the diamond detectors (as they were presented in Chapter 2). Each ROD outputs 6 triggers that are independently processed in the FPGA which also constitutes the basic building block for the analysis of the readout chain. The communication between the two RODs is not yet performed, although this is a feature which is being researched and due to be implemented in the near future, thus making it necessary to combine, synchronize and calculate the total number of combined triggers provided by the BCM.

In order to better handle the trigger signals from both RODs, a trigger adder for handling and encoding was used. The basic characteristics and behavior of the system developed are outlined within this chapter.

3.2 Trigger signals description

Each ROD accepts input from 8 channels (4 high and 4 low threshold channels) and calculates and outputs 6 trigger signals. The first three triggers are:

- A to C side : out-of-time hit on A side and in-time hit on C side on the same ROD
- C to A side : out-of-time hit on A side and in-time hit on C side on the same ROD
- Wide: in-time hit on A side and in-time hit on C side in wider time windows on the same ROD

Three OR gates receive the same trigger signals from the two different RODs, combining signal output from both RODs outputs to one signal. These gates were initially implemented with a NIM module which was placed in the pit (ATLAS USA 15) and are now included in the trigger adder system. The other three trigger signals are:

- One signal declares if any high threshold (low gain) channel has a hit
- Two signals are multiplicity triggers and encode how many channels of each ROD have a hit using a binary encoding.

Specifically, the multiplicity triggers from each ROD are used as binary bits of a two bit binary number. The following table is describing the possible states.

Table 1: Encoding of multiplicity triggers

Trigger bit 1	Trigger bit 0	State encoded
0	0	no channel has a hit in this ROD
0	1	1 channel has a hit in this ROD
1	0	2 channels have a hit in this ROD
1	1	3 or more channels have a hit in this ROD

3.3 Board description

The basic component of the trigger adder system is a V1495 CAEN [CAE] board (figure 3-1). It is a general purpose VME board that uses two FPGAs for user and VME interface and communication respectively. The FPGA that controls the VME interface, also called “Bridge”, is responsible for handling the board registers and make it possibly to reprogram the board on the fly. Within the scope of the aforementioned application it is used only for uploading the necessary firmware on the flash memory permanently. The USER FPGA is programmable by the user for implementing the desired operations. The software used and uploaded to the USER FPGA is the demo edition that CAEN provides, modified to include the necessary changes for the trigger adder function implementation.

There are 3 standard PECL/LVDS/ECL ports and three additional connectors that support different types of mezzanine boards. For the aforementioned application 3 additional NIM/TTL mezzanine boards are used as inputs and outputs. There are also 2 NIM/TTL inputs on the board, one of which is used as the LHC CLK input. The maximum frequency the board can handle is 405 MHz while the NIM/TTL mezzanine boards support up to 250 MHz frequency. The A395D mezzanine boards that are used have 8 lemo I/O channels and were mounted to the additional connectors. Two of the boards are defined as NIM inputs for the triggers coming from the RODs and the third as

an NIM output for the encoded trigger signals. This input-output operation is controlled entirely by the firmware uploaded in the USER FPGA.

Although the standard CLK that the board provides to the FPGA is 40 MHz, the additional NIM/TTL channel G0 is used as an input for the LHC CLK. This way, the trigger signals that are outputted from the board are synchronized to the LHC CLK (a time delay that was measured and is taken into account is discussed in this Chapter).

3.4 System description

The trigger adder has two mezzanines used for inputs. One combines the two multiplicity triggers and the high threshold trigger from each ROD and encodes them to three output signals. The encoding of the signals is binary, assuming that each of the three output signals is a single bit that makes up a three-bit binary number.

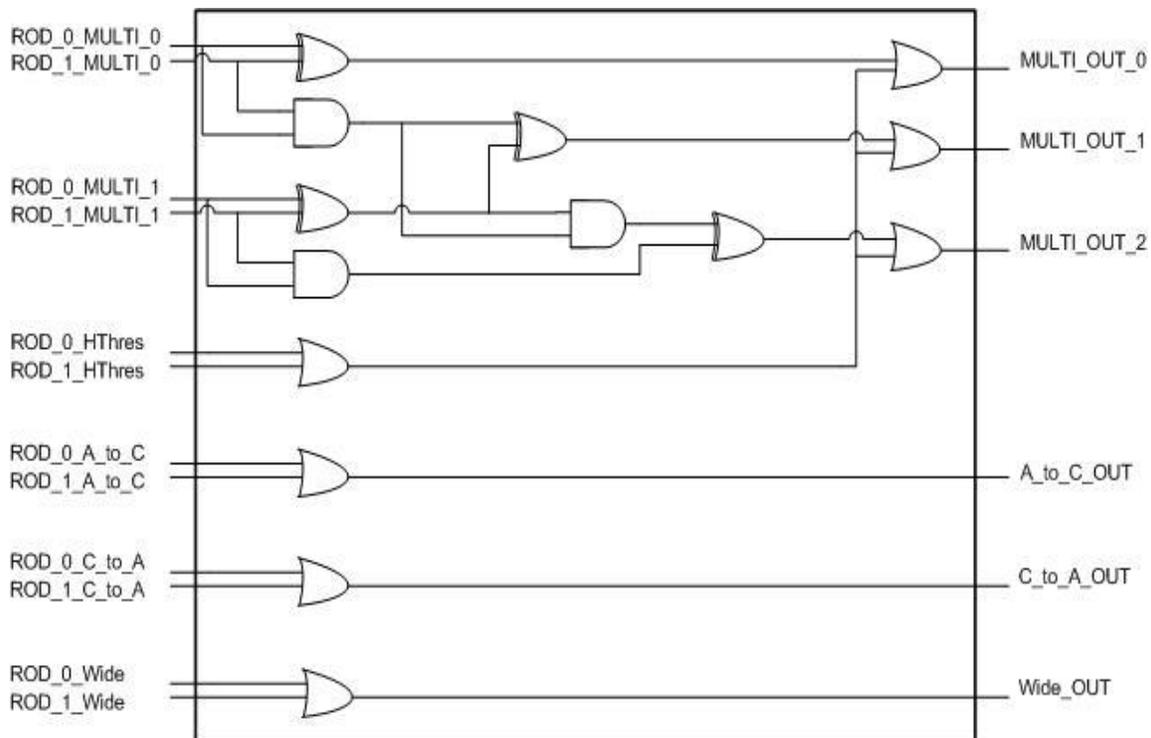


Figure 3-1: Gate logic of trigger adder

The two multiplicity signals from each ROD are added while the two high threshold signals from each RODs are fed into an OR gate. The outputs of the adder and the OR gate are fed into another OR gate in order to obtain the final outputs. The outputs are 3 “bits” that encode 8 different states. These states are described in Table 2 according to the inputs of the multiplicity and the high threshold trigger inputs.

Table 2: State description for multiplicity and the high threshold trigger

Outputs			Inputs
If ROD_0_HThres AND ROD_1_HThres =0			
MULTI OUT 2	MULTI OUT 1	MULTI OUT 0	ROD_0_MULTI + ROD_1_MULTI
0	0	0	00+00
0	0	1	01+00 or 00+01
0	1	0	10+00 or 00+10 or 01+01
0	1	1	11+00 or 00+11 or 10+01 or 01+10
1	0	0	11+01 or 01+11 or 10+10
1	0	1	11+10 or 10+11
1	1	0	11+11
If ROD_0_HThres OR ROD_1_HThres =1			
1	1	1	Independently of the Multi Inputs

The 2-bit multiplicity signals from both RODs are added to encode the output states from 0 (000) to 6 (110) giving the total number of channels hit. This means that 0 encodes the state where no channel is hit in any of the two RODs while 6 is the state where at least 3 channels from each ROD have a hit registered. If a high threshold trigger is recorded in either or both RODs then the output of the adder is 7 (111) which is the 8th state.

The second mezzanine is input for A to C, C to A and Wide triggers from each ROD. This means that totally 6 inputs are gated to three OR gates in order to give three more output signals. This gating procedure is described in Table 3. Totally the trigger adder system receives 12 inputs (4 multiplicity, 2 high threshold and 6 for A to C, C to A and Wide) and yields 6 outputs. These are the 6 trigger signals that the BCM sends to the CTP.

Table 3: Encoding for A to C, C to A and Wide triggers

Outputs	Inputs
A to C	A to C ROD 0 + A to C ROD 1
0	0+0
1	1+0 or 0+1 or 1+1
C to A	C to A ROD 0 + C to A ROD 1
0	0+0
1	1+0 or 0+1 or 1+1
Wide	Wide ROD 0 + Wide ROD 1
0	0+0
1	1+0 or 0+1 or 1+1

3.5 Implementation overview

Before the decision to use the V1495 board for the trigger adder implementation was made a different approach was tested, as described below. The adding of the multiplicity triggers was initially designed to logic gates level. Le Croy 428F and 622 NIM boards were used to implement the logic gates and the necessary splitting of a signal into two new signals. The main disadvantage of this system was the instability caused by the sensitivity of the NIM modules to the time difference of the incoming signals. These

problems led to the rejection of the NIM based system and the V1495 board was chosen due to its stability even with time delays between the inputs that had to be dealt with. In order to achieve this a BC is spent in order to buffer the inputs and add them in the next BC. This allows the input signals to have a relative time delay half a BC or 12.5 ns when the LHC CLK is used. The user FPGA in this system is working with two different CLKs.

The trigger adder script uses LHC CLK in order to be completely synchronized with the input signals, i.e. to avoid a shift in time of the outputs in respect to the other trigger signals in the CTP. All the other scripts inside the FPGA as well as the VME interface actions use the 40 MHz CLK of the board in order to ensure stable operation and communication with the VME crate when necessary. The trigger adder code works as shown in figure 2. In the first BC the input signals are buffered in order to achieve stability and in the next BC cycle the results are calculated in order to yield the output signals.

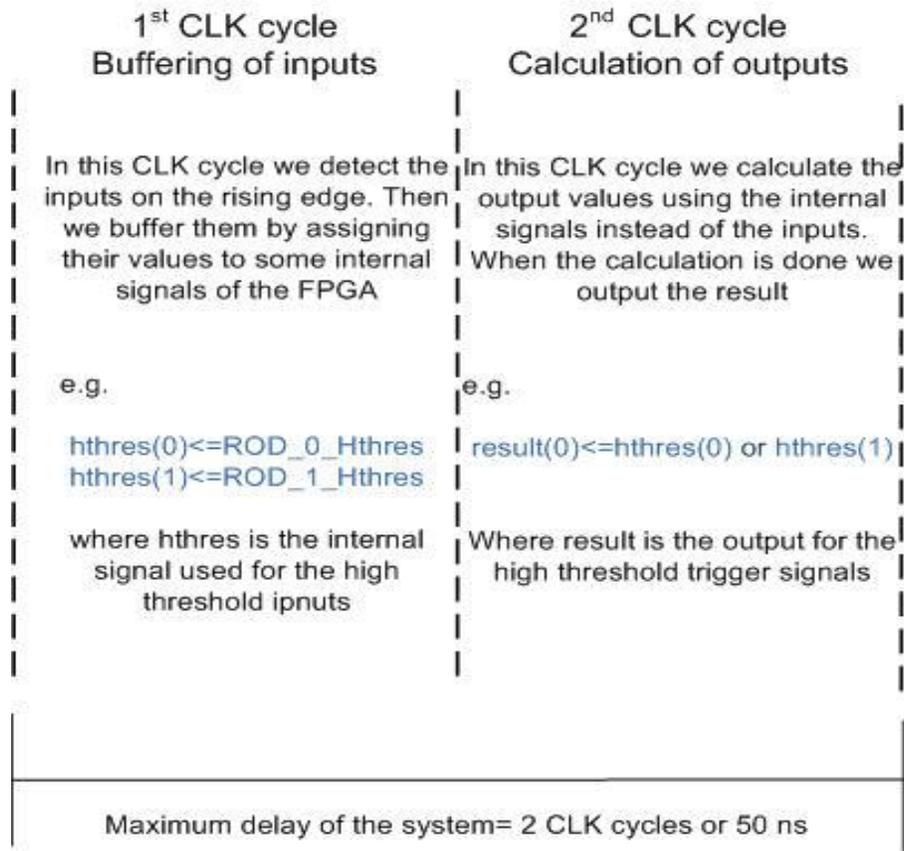


Figure 3-2: Description of code operation

3.6 Testing and measurements

Three different setups were used to test the performance of the system. The main goal of the testing was to measure the synchronization of the CLK and the triggers signals generated through the testing procedure. A brief explanation of the plots and the representation of each channel is presented below. In all three setups we the Tektronix TDS5104B digital oscilloscope was used. Furthermore, if not stated otherwise, the first 3 channels display the output signals, where channel 1 stands for MULTI_OUT 0, channel 2 for MULTI_OUT 1 and channel 3 for MULTI_OUT 2. Specifically, channels 1-3 encode the 8 different states, as discussed in Table 2, and channel 4 is the CLK coming out from the board, which is always synchronous to the outputs.

3.7 Test with asynchronous LHC CLK

In the first setup we used LHC CLK from an ATLAS Pixel TPLL board which was asynchronous in respect to the trigger pulses. The pulse generator which was used is a Wavetek 395, able to provide test pulses used as inputs in frequencies up to 40 MHz. The output of the pulse generator was split to 4 identical signals with NIM voltage levels (0 V stands for active low or logic 0 while -0.8 V stands for active high or logic 1). These signals were used to simulate the input trigger signals. The main disadvantage of this setup is that the CLK arrives at different times in respect to the pulses. The board checks for inputs every rising edge of the CLK (≈ 2 ns) and even slight time delays between the inputs results in two input pulses not being detected within the same BC. Figure 3 shows schematically this synchronization problem. The active high inputs are: a) one high threshold trigger, and

b) 11+01 in the multiplicity trigger inputs. The multiplicity triggers added give a result of 4 which means that if no high threshold trigger had a hit (pulse), only channel 3 should have a pulse as an output.

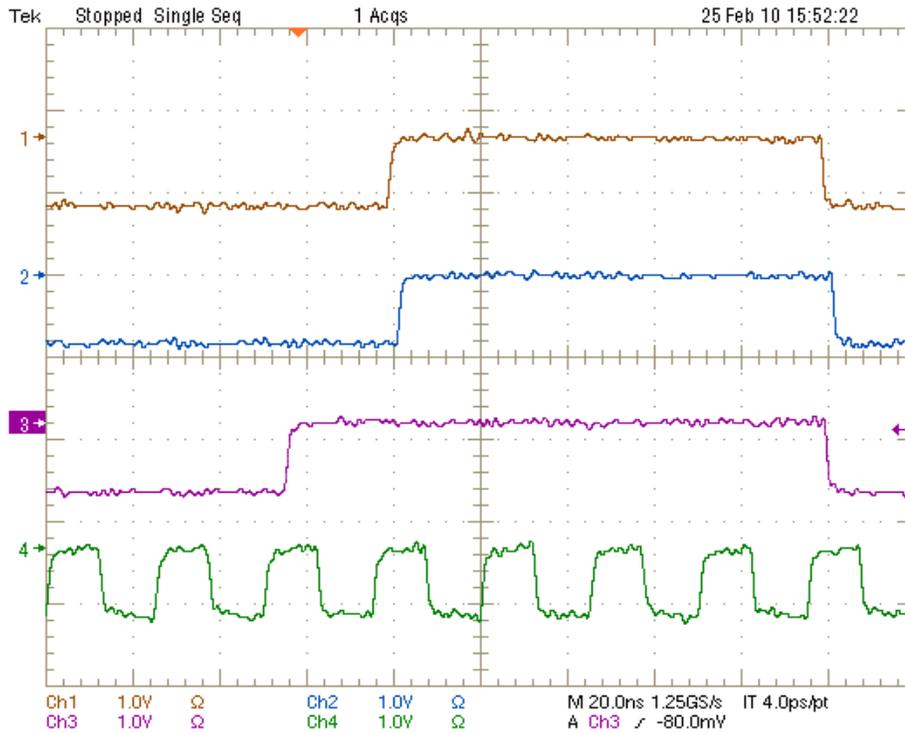


Figure 3-3: Wrong result due to synchronization failure between the inputs and the CLK

In the first BC the multiplicity inputs are detected by the board but the high threshold signal has a delay and is not taken into account. As a result in the first BC we see channel 3 going high which stands for the multiplicity 3+1 result. In the second BC and until the end of the input pulses high threshold inputs is detected and we have channels 1-3 high which stands for state 7 or high threshold trigger. This is the case when the phase between the clock and the incoming pulse is wrong.

In figures 4-5 this synchronization problem is evident. In channel 3 we have an input pulse and in channel 4 the LHC CLK that is input for the board. As it can be seen

the pulse and the CLK have no standard phase between them. In the first plot the delay of the pulse is 8.4 ns in respect to the CLK and in the second plots 25.2 ns.

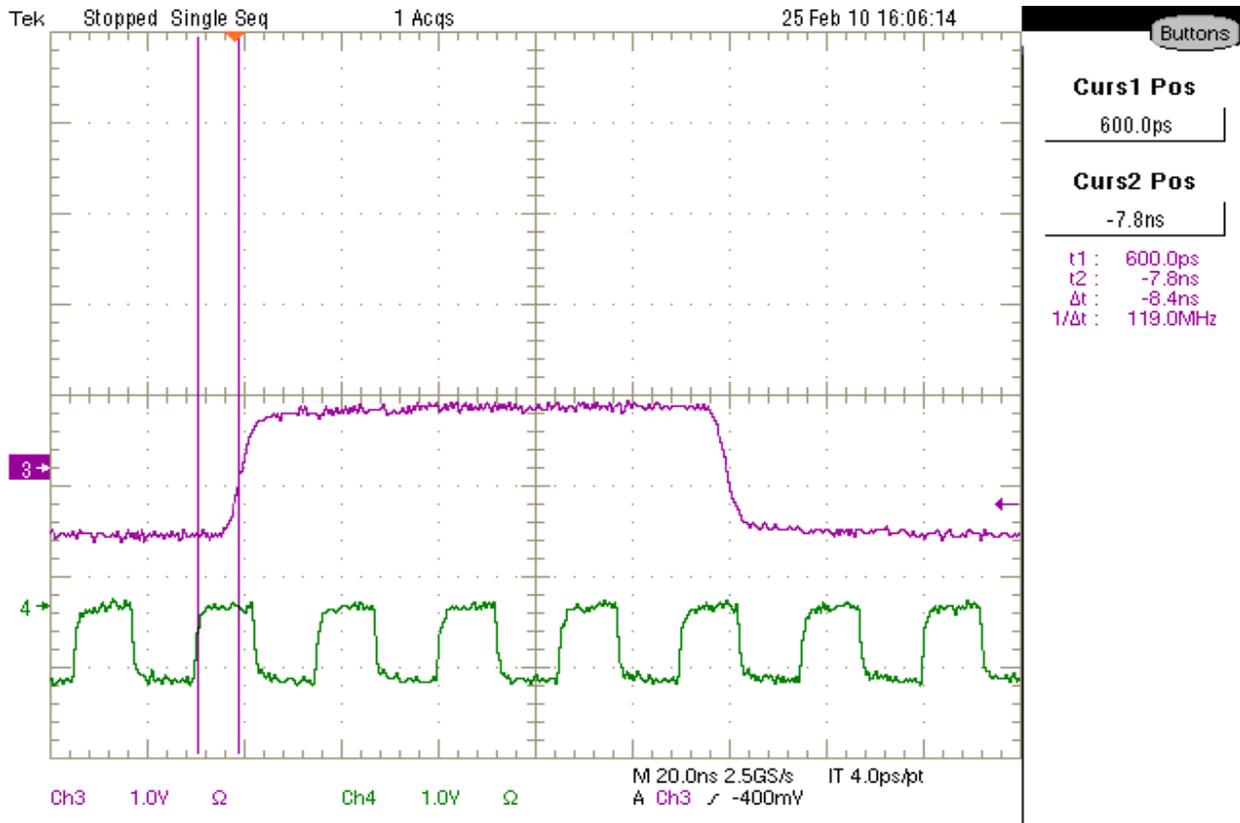


Figure 3-4 Input pulse- CLK time difference of 8.4 ns

At the beginning and end of the pulses there was a flickering as in the previous example. This unstable condition was a problem of the setup and not of the board as the real trigger signals are fully synchronized to the LHC CLK. As last comment for this setup, the input pulses were not inverted as the NIM signals usually are. This means that the 0 V stands for active high and -0.8 V for active low.

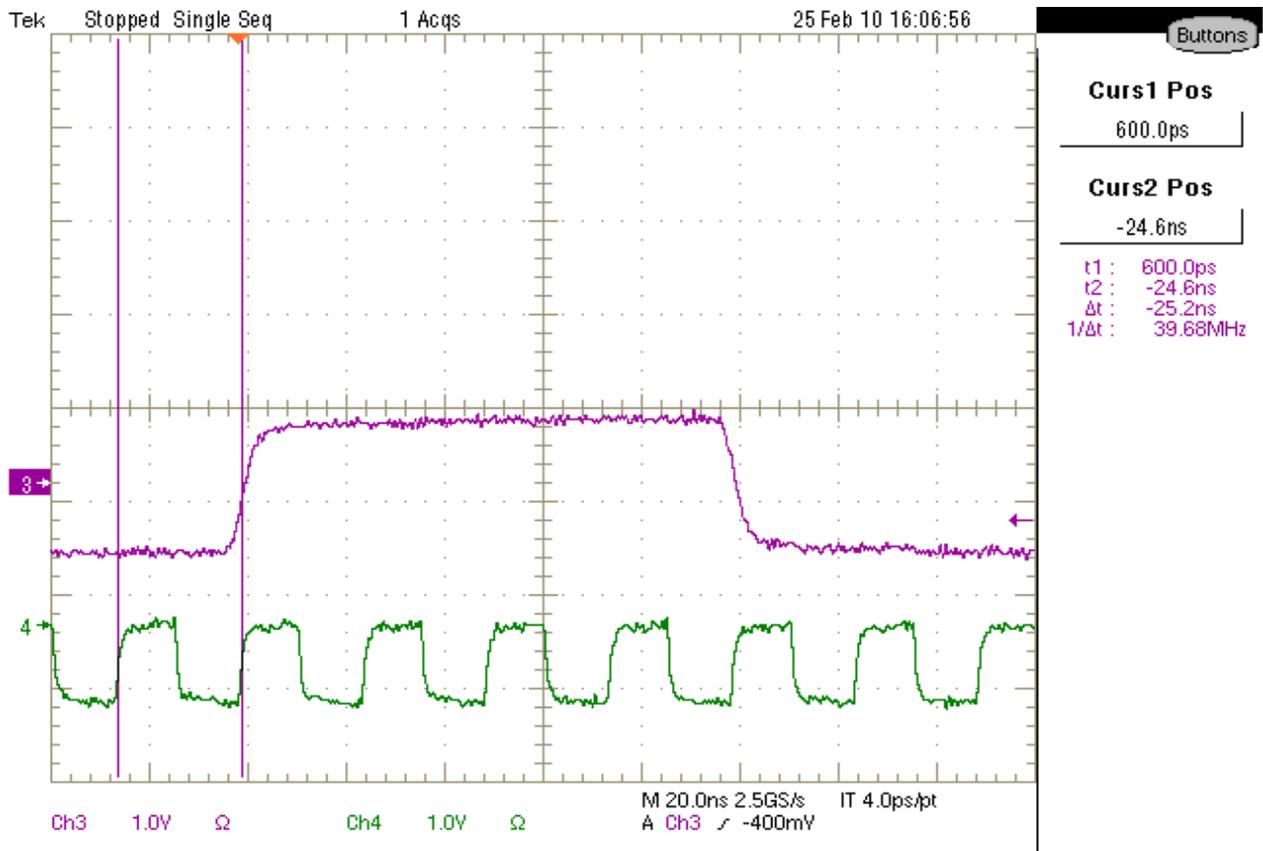


Figure 3-5: Input pulse- CLK time difference of 25.2 ns

3.8 Test with synchronous CLK of 10 MHz

In this setup we used the same pulser and a reference CLK of 10MHz (Figure 7) provided by the pulser. The CLK was at TTL voltage levels and a LeCroy 688AL NIM/TTL Converter was used to transform it to NIM signal. In this test setup the CLK synchronization problem was partially solved. When the input pulses have the same frequency with the CLK (i.e. 10 MHz) and the right phase, the results are calculated correctly. This proves that when the CLK has rising edge and the input signals are active high, the results are calculated without flickering in the edges of the pulses. However, this test was not enough as the frequency of 10 MHz is not high enough to ensure the stable

operation of the board and the trigger signals are not periodic. When the frequency of the inputs was not 10 MHz they were sliding in time according to the CLK due to the different frequency.

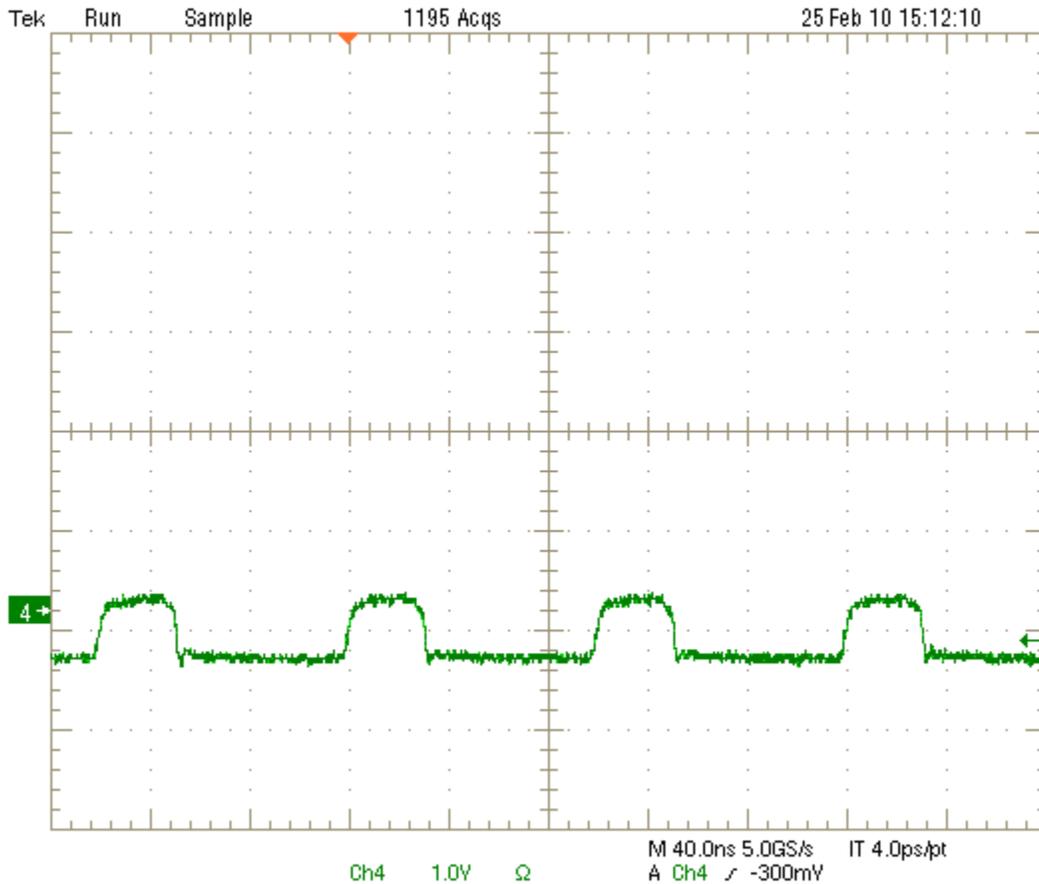


Figure 3-6: pulser's REF CLK with frequency of 10 MHz after TTL/NIM conversion

Despite the CLK problems which were explained above during the first two test setups, the calculation of the results was otherwise accurate and no other instability issues were noticed. The delay of the system was calculated but it was not fixed due to the fact that it was not possible to have a fixed phase CLK with respect to the inputs.. Even in the event the input pulses' frequency is 10 MHz, the phase was not the same when the pulse

generator was switched off and on, resulting in a change in the delay related to the phase difference.

3.9 Test with synchronous 40 MHz CLK

The setup that will be discussed in this chapter solves the CLK synchronization issues encountered in the previous two setups. The pulser, a PM 5786 PHILIPS pulse generator, provided a feature which allowed the REF CLK to be synchronized to the pulses and frequencies higher than 40 MHz (frequency of LHC CLK). Moreover, the phase of the CLK in respect to the input pulse is adjustable, thus making it possible to measure the total delay of the system. In the chapter only the measurements and tests performed with this setup that are necessary to prove the validity of the test are presented (Appendix A contains the complete set of measurements and tests obtained from this setup). Initially it was tested that no flickering occurred at the outputs of the board in order to ascertain the accuracy and validity of the calculations. Pulses with NIM logic voltage levels (0 V active low, -0.8 V active high) and different pulse-widths were used. Figure 7 shows a result $2+1$ of the multiplicity triggers.

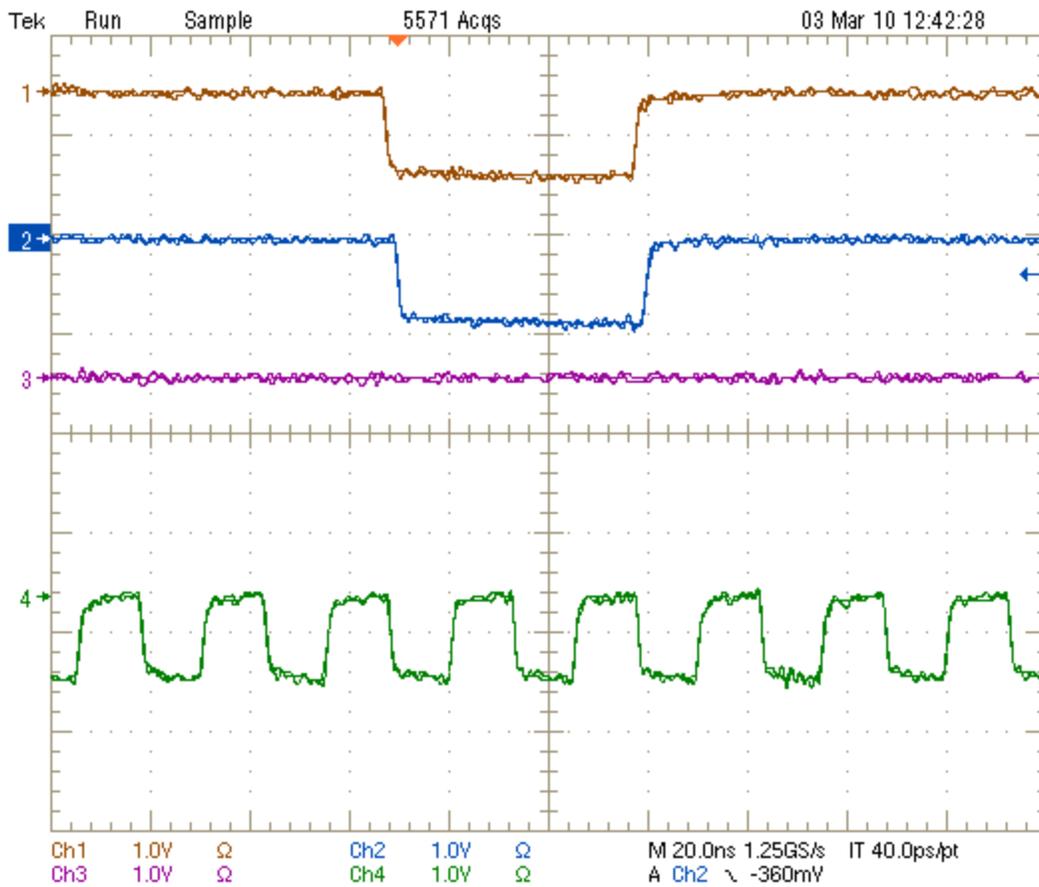


Figure 3-7: 2+1 output result for the multiplicity signals

The slight time difference between the output pulses observed was measured in Figure 8. If MULTI_OUT_0 (channel 1) is reference, MULTI_OUT_1 (channel 2) has a delay of 2.48 ns and MULTI_OUT_2 (channel 3) 880 ps. This time delays are not significant and can be compensated by using output cables of different delays (lengths). A measurement that was possible with the new pulse generator was to adjust the phase between the input CLK and the input pulses, thus measuring the total delay of the system, which yielded interesting results, as will be discussed below. As mentioned previously, the board is sampling the input signals during the rising edge of the CLK and requires two BCs for the internal buffering and calculation.

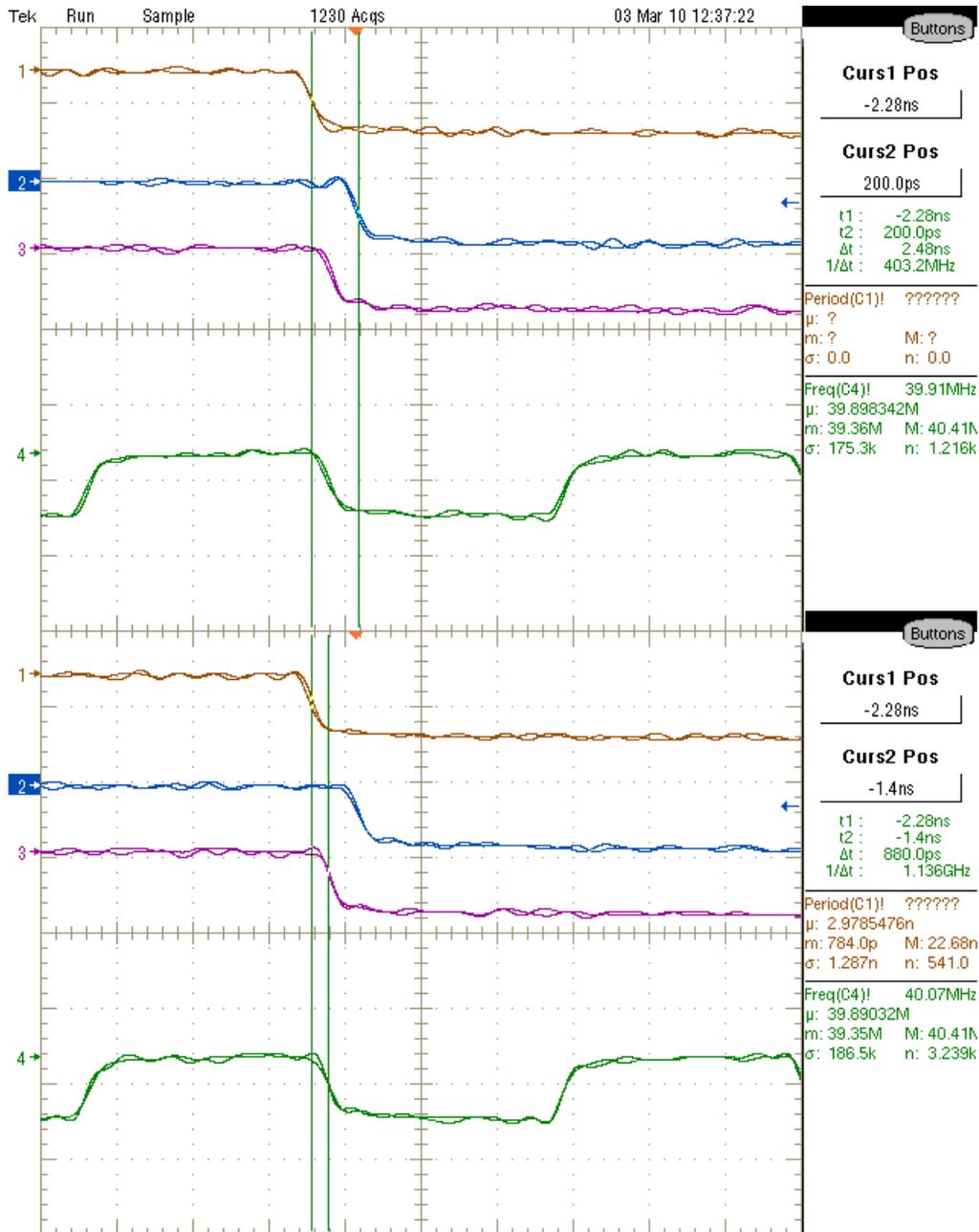


Figure 3-8: Delays of MULTI_OUT_1 and MULTI_OUT_2 in respect to MULTI_OUT_0

If the input pulses arrive exactly at the CLK rising edge then:

$$\text{Total delay of the system} = 50 \text{ ns (2 BCs needed for internal process)} + dt$$

If the input pulse arrives earlier in respect to the CLK, it will be detected in the current BC but the delay will be bigger than 50 ns and an additional dt will be added to

the delay (where dt is the time delay of the current CLK rising edge in respect to the leading input pulse). If the input pulse arrives after the rising edge of the CLK it will be detected in the next BC. Then the delay will be different again, and dt will be the time delay of the next CLK rising edge in respect to the earlier input pulse. As a result, the minimum and maximum delays will be:

Min delay of the system ≈ 50 ns

CLK rising edge is in phase with the rising edge of the pulse, $dt = 0$ ns

Max delay of the system ≈ 74 ns

CLK rising edge and pulse rising edge have time difference of $dt = 24$ ns

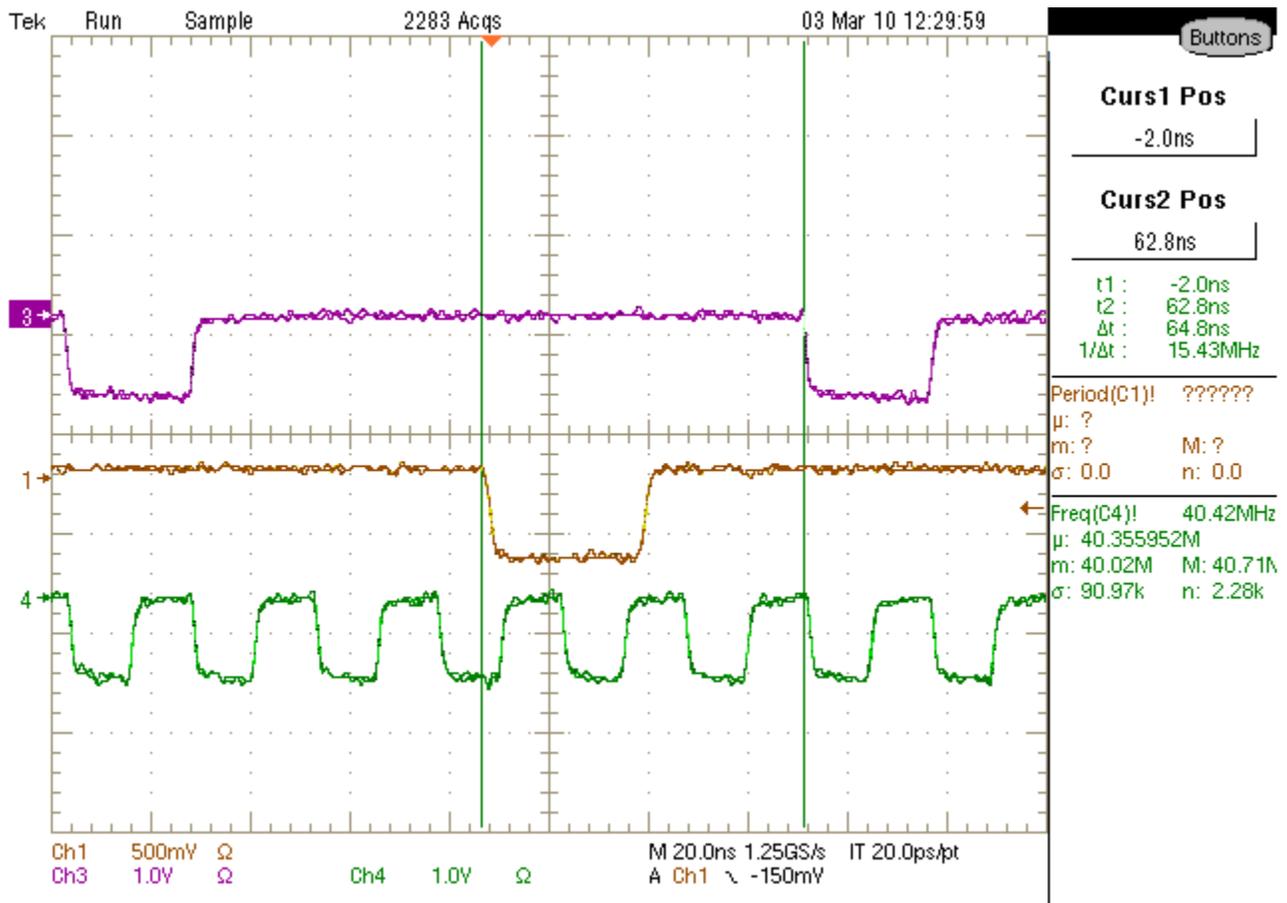


Figure 3-9: Minimum total delay of the system= 48.8 ns

The maximum delay is less than 74 ns, due to the fact that if dt is approximately 25 ns then the input pulse is detected by the previous BC rising edge. In Figures 9 and 10 the minimum and maximum delays are displayed respectively. The time delays in the aforementioned plots are 16 ns bigger due to the 16 ns delay cables used between the board and the scope.

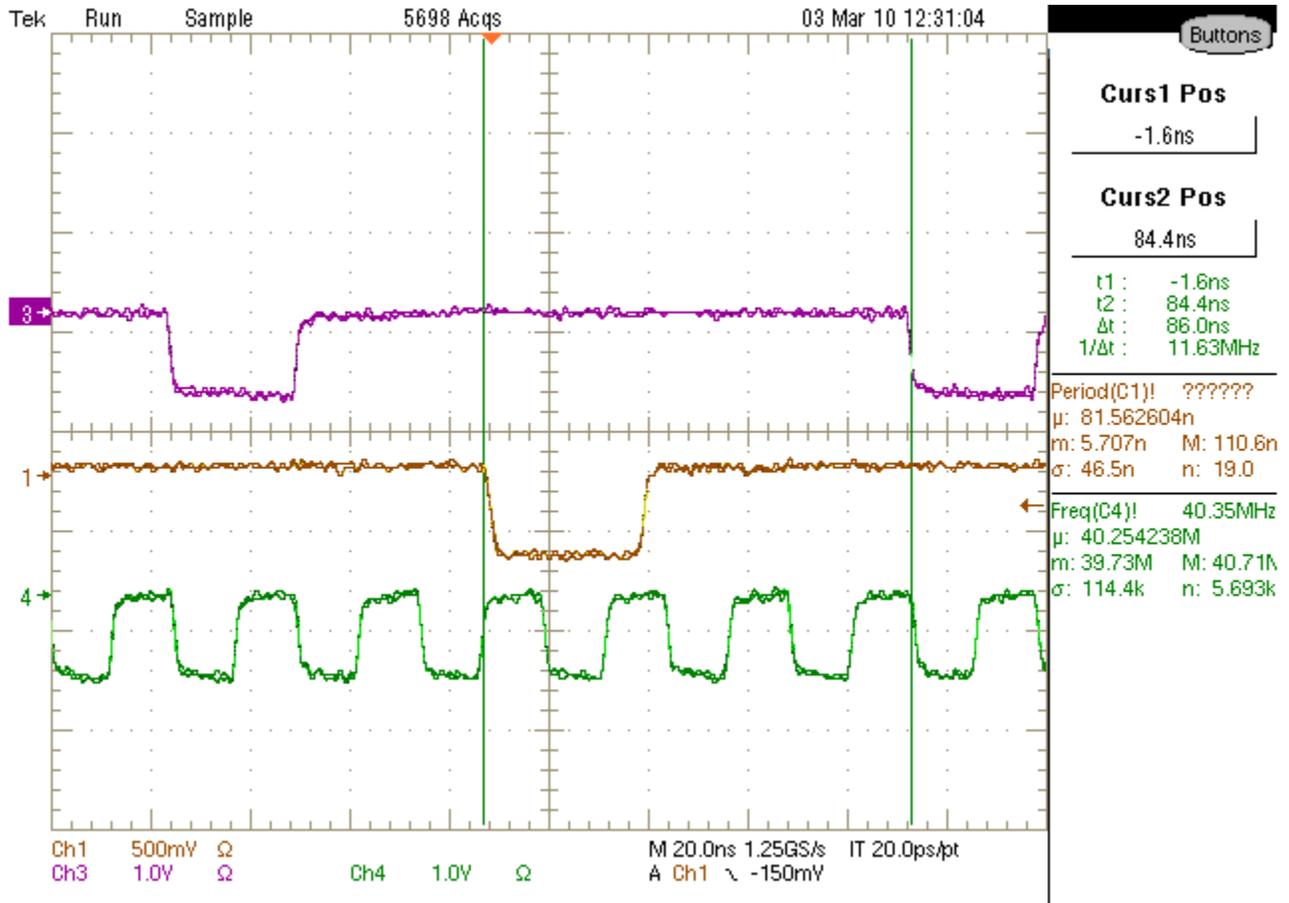


Figure 3-10: Maximum total delay of the system= 70 ns

The last measurement to be discussed in this chapter is the jittering of the CLK that the board produces on the output dedicated to the CLK.. In the pit (USA 15) where the board is installed the TTCVi provides to BCM 2 CLK outputs for the CTP CLK, which were used adequately for the 2 RODs operation. Apart from those two signals the board

installed in the pit required a different CLK signal. The additional CLK could be provided by either splitting an existing clock signal (using a NIM fan-in fan out) or by using the output of the board CLK as input for one of the RODs. The fact that the CLK that the board produces is very stable led us to the implementation of the latter solution. The jitter of the CLK signal used is discussed below.. In Figure 3-11 we measured the jitter of the TPLL pixel LHC CLK as that is established in the lab.

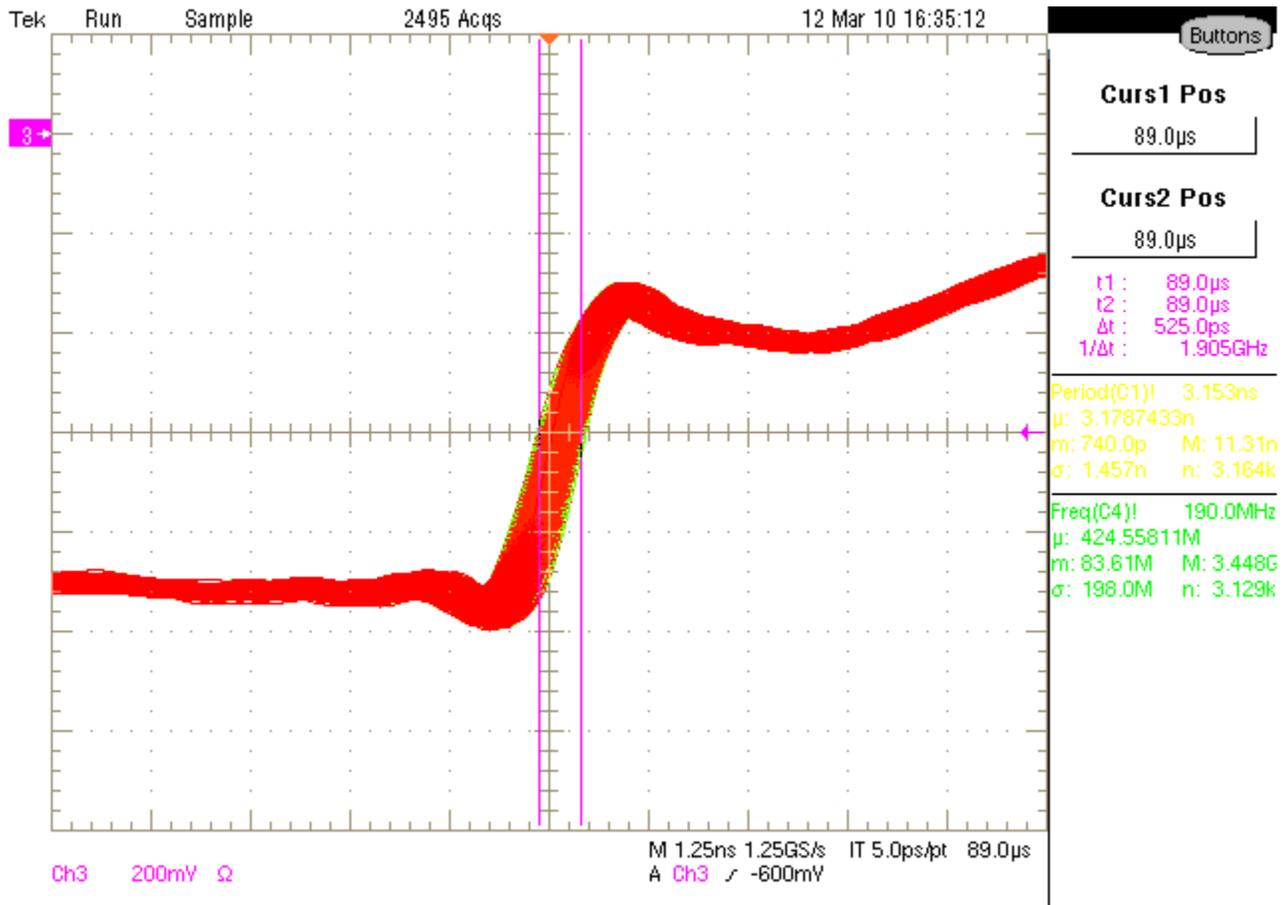


Figure 3-11: Jitter of the TPLL pixel LHC CLK = 525 ps

The jitter of the scope (measured to be 325 ps) has to be taken into account, hence the true jitter of the TPLL pixel LHC CLK is not 525 ps. Figure 12 displays the jitter of the CLK as it is outputted from the board. It is noteworthy that the rising timing of the board's CLK is smaller than the pixel's LHC CLK and that the curve is smoother, as it can be seen

from the two plots. Figures 13, 14, 15 display the board's CLK frequency, the output pulse's pulse-width and a description of the connection on input and output ports respectively. To summarize, the trigger adder board was tested thoroughly and the results indicate a stable behavior, suitable for the purposes of this experiment. The outputs are synchronized and sent to the CTP. The only functional issue remaining to address is the more accurate alignment of different phases of incoming pulses and the CLK in order to optimize the overall performance of the setup. The board was placed in the ATLAS USA 15, is fully operational and the triggers signals can be observed in the BCM FSM panel.

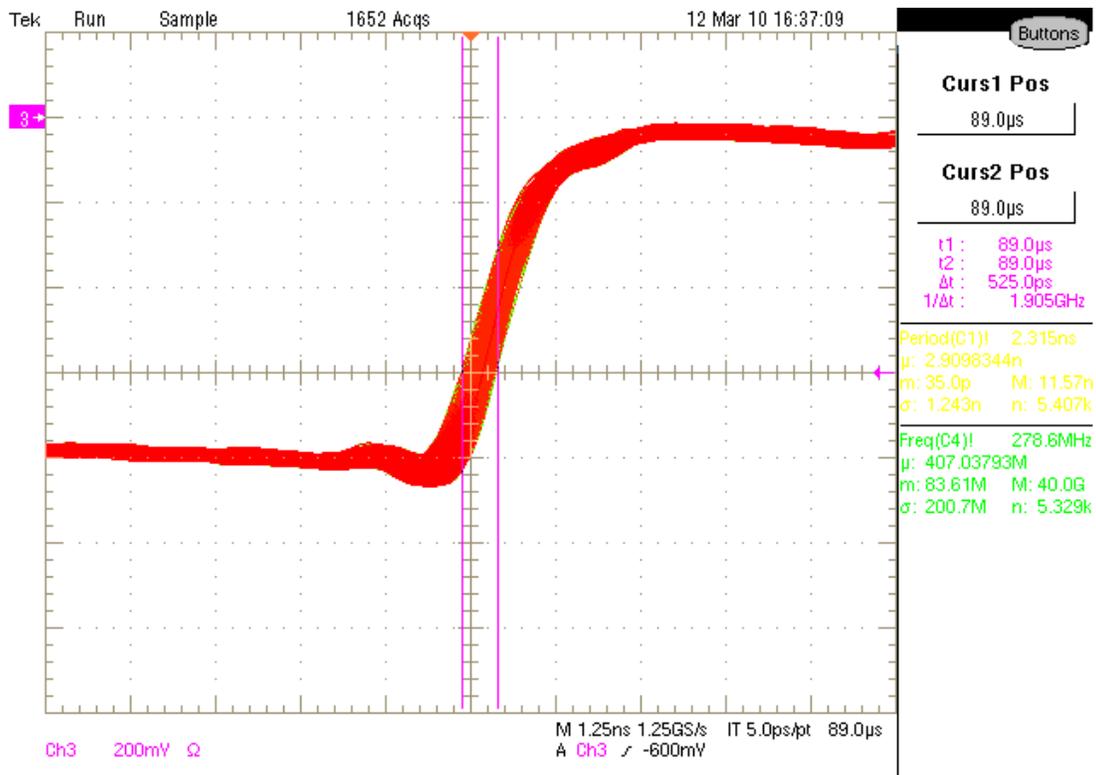


Figure 3-12: Jitter of the board's CLK_OUT < 525 ns

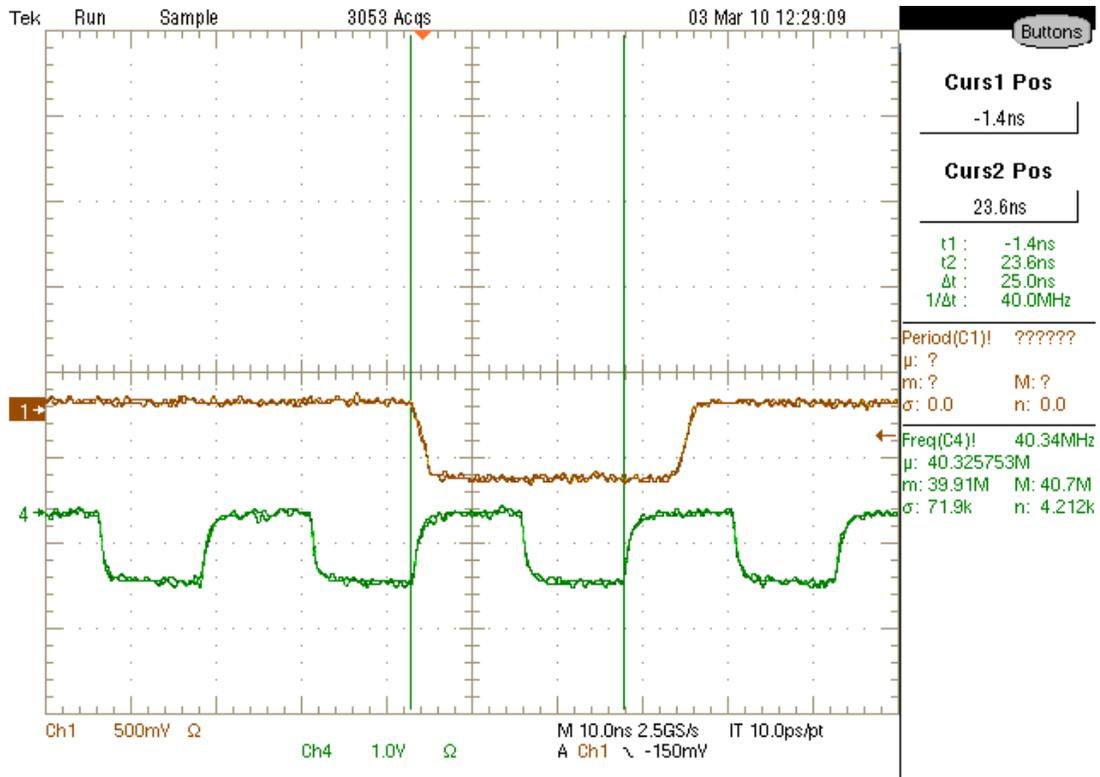


Figure 3-13: Frequency and pulsewidth of the board's CLK_OUT= 40.34 MHz, 25 ns

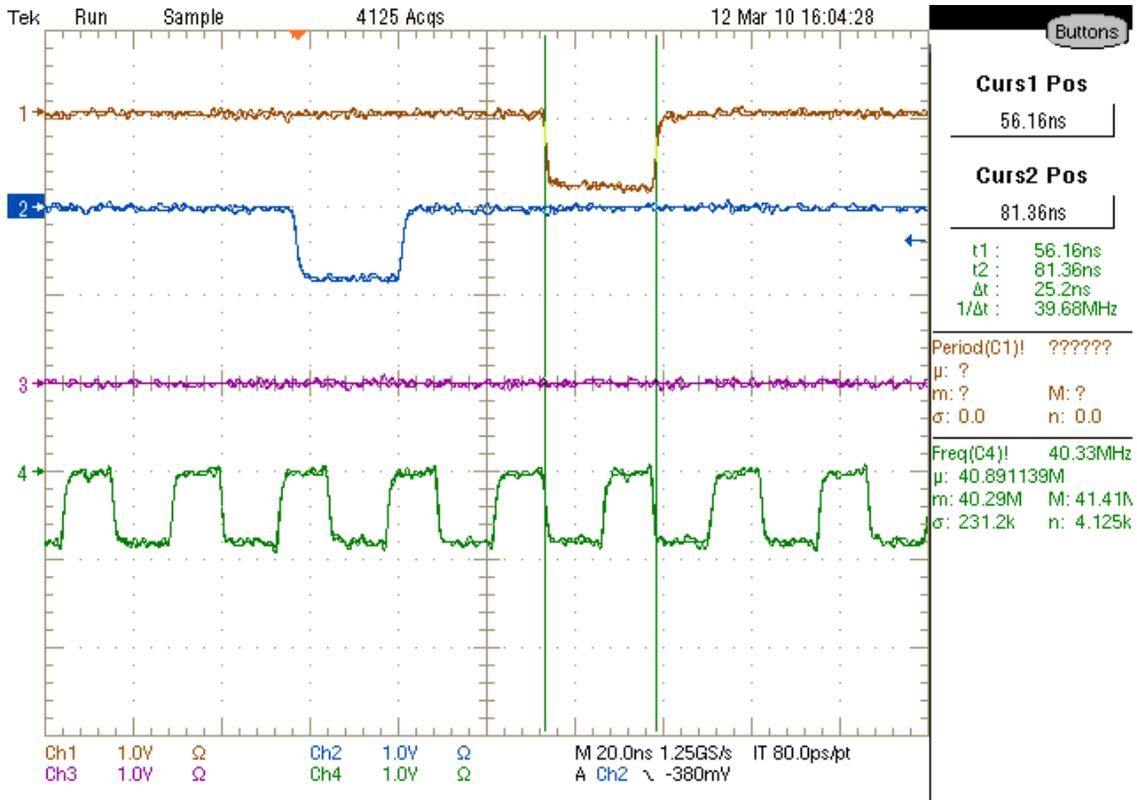


Figure 3-14: Pulsewidth of the board's output pulses (channel 1) = 25.2 ns

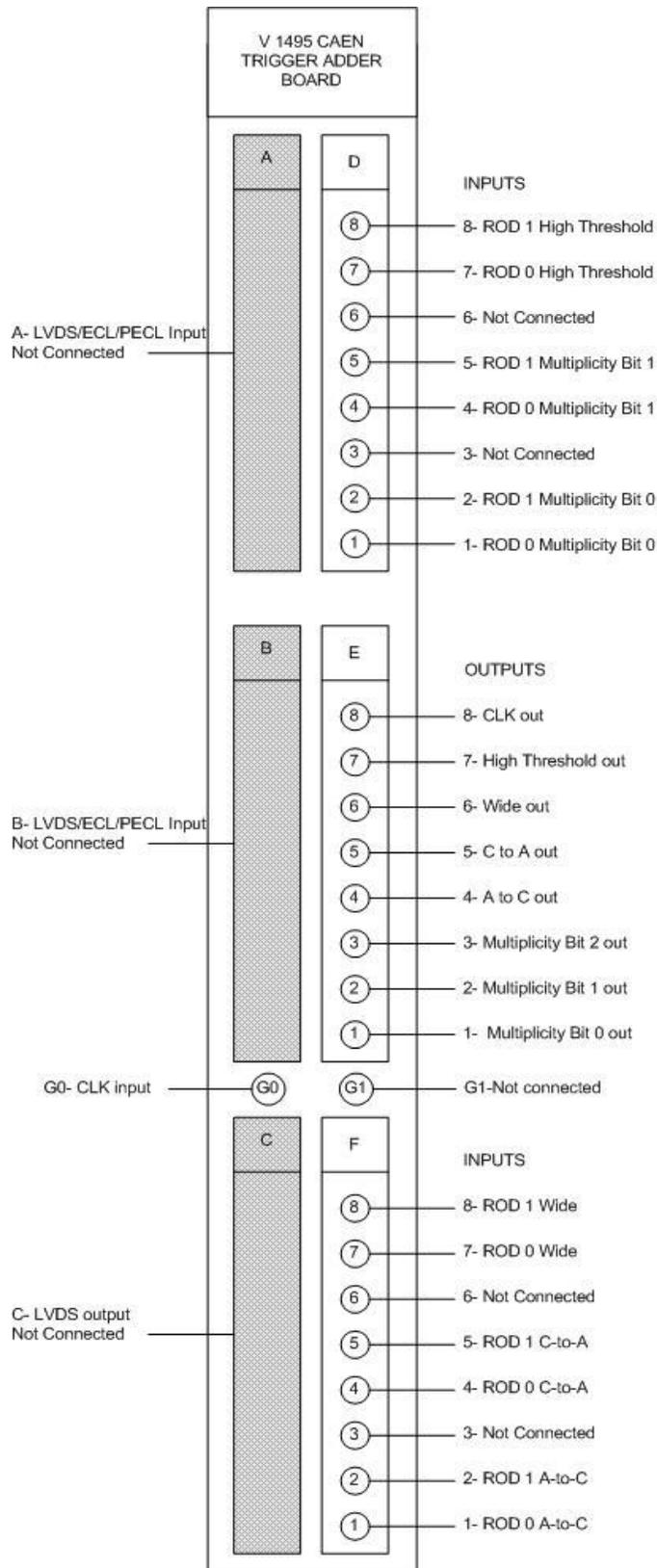


Figure 3-15: Ports connection description

Chapter 4

Beam abort extension algorithms

4.1 Introduction

As discussed in previous Chapters, the main operation of the BCM is to monitor the beam condition and fire a beam abort signal in case of beam instabilities. It is crucial to note that the requirements of such a system are extremely high as the decision of aborting or not the beam affects all the systems not only in ATLAS but in all LHC experiments. In the case of not aborting the beam when it is necessary could prove to be extremely dangerous for other ATLAS sub-detectors, especially the other Inner Detector parts. On the other hand, firing a spurious beam abort stops the operation of ATLAS if not of the entire LHC ring, a fact that is unwanted and should be avoided as much as possible. A beam dump (beam abort) is an operation that has adverse effects in terms of cost and prolonging the experiments while the accelerator is not in operation. Therefore a beam dump request from any sub-system in LHC has to be justified with sufficient data, showing at least a potentially dangerous situation.

These harsh requirements pose the necessity of a very fast, stable and effective system. To meet these needs, BCM uses two independent RODs using FPGA as the main processor, thus achieving stability and very fast response. The decision of the beam abort condition is made by an algorithm inside the FPGA of each ROD. Two extensions of this algorithm were implemented to increase the effectiveness of the system and will be discussed in this chapter.

4.2 Basic algorithm and edge detection

The signals coming from the detectors and the front-end electronics are fed into the NINO system for digitization and amplification. Prior to NINO each channel is split to two signals at a ratio of 10:1 in order to increase the NINO dynamic range. As a result, the initial 8 signals are doubled and split to 8 high gain and 8 low gain channels. The NINO system has a threshold for all the channels. If a channel surpasses the threshold then the NINO will send a digital pulse to the FPGA for that channel. It is more likely for a high gain channel to surpass the threshold as it contains the 90% of the initial signal amplitude. If the initial pulse's amplitude is large enough even the low gain channel that contains the 10% of the initial amplitude will surpass the threshold. It is obvious that if the low gain channel has a hit (surpasses the threshold), the high gain will also have a hit. The channels are distributed in both RODs in a way that if a high gain channel of a detector module is fed to the one ROD, the corresponding low gain will be fed to the other ROD. This ensures that information is received from all the detectors in each ROD. Hence, the condition of all the detectors is monitored in each ROD and in the case of loss of connection with one ROD the online data analysis is still possible. The connection scheme of the channels to the NINOs and then the RODs is illustrated in figure 4-1.

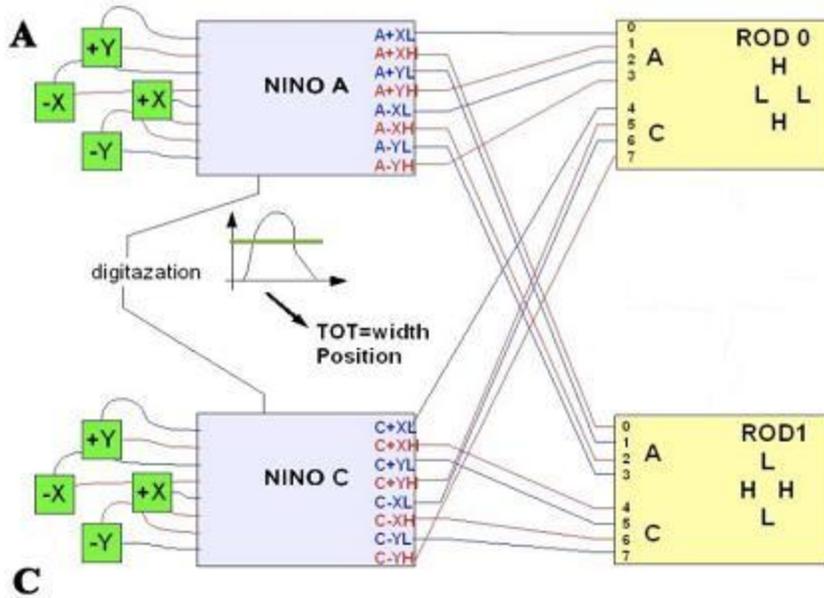


Figure 4-1: Connection scheme of the channels to the NINOs and the RODs

In each FPGA a dedicated algorithm performs a detection of rising and falling edges in every channel. Simulation results show that one BCM detector module is unlikely to have more than 2 proton hits in a single BC. Therefore, the edge detection algorithm is designed to detect up to 2 rising and 2 falling edges, resulting to a maximum detection of 2 hits per BC per channel. The current condition for injecting a beam abort signal is often called “3+3”. It requires at least 3 high gain and 3 low gain channels in one ROD to have a hit in one BC. It is possible to fire a beam abort based on results only from one ROD.. This is possible due to the high and low gain channels connection to the 2 RODs as it illustrated in Figure 4-1. In this case the BCM will inject immediately a beam abort signal and distribute it to CIBU and to the ATLAS DSS system. As a result, the beam will be dumped within 3 LHC turns while the beam permit flag of ATLAS and injection permit flag of LHC will go red.

The “3+3” condition satisfies almost all the requirements of the beam abort operation but it cannot prevent all spurious beam aborts due to its heightened sensitivity. The main reason for this heightened sensitivity is that the “3+3” is taking into account

information only from one BC. As a result, instant noise increase or beam instability occurring during one BC could potentially cause a beam abort without it being necessary. The decision of aborting the beam should be taken early enough in order to prevent an accident but should also take into account information from previous BCs. The need to surpass this static moment in time characteristic of “3+3” condition led to the development of 2 extensions of the beam abort algorithm. Both extensions take into account information from previous BCs resulting in a more dynamic behaviour of the already used beam abort algorithm. These extensions were implemented inside the FPGA of each ROD and use as input the results of the “3+3” condition.

4.2 The X out of Y extension algorithm

The basic concept of the X out of Y algorithm is similar to the moving average algorithm. It is mainly used to analyze a set of data points by creating a series of averages of different subsets of the full data set [WIK]. The average of the last N measurements is given by the equation:

$$SMA = \frac{P_M + P_{M-1} + P_{M-2} + \dots + P_{M-(N-1)}}{N}$$

When a new value is inserted drops in the average the oldest one has to be discarded. The same equations above can be used but it is more practical to use the following equation:

$$SMA_{new} = SMA_{previous} - \frac{P_{M-N}}{N} + \frac{P_M}{N}$$

In the above equation the algorithm takes into account the last N measurements and calculates their mean average. In X out of Y the same concept of the moving frame in time is being used. The frame Y corresponds to the number of the previous measurements

that we observe, or more accurately to the number of the last Y BCs that we take into account. The parameter X is the minimum number of BCs that must satisfy the “3+3” condition. If at least X past results out of Y satisfy the “3+3” criterion the algorithm fires a beam abort. Figure 4-2 gives a schematic of the operation of the algorithm.

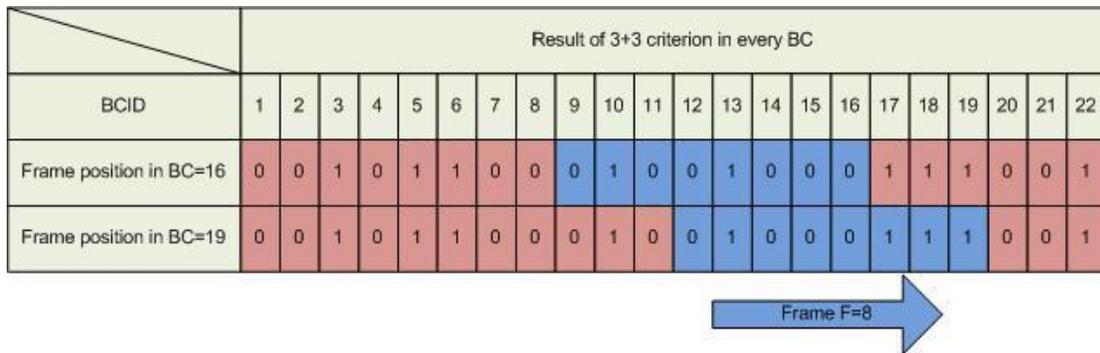


Figure 4-2: A frame Y=8 running over time

In this example (as depicted in Figure 4-2) the frame Y is set to 8, thus the last 8 BCs are taken into account. If the threshold X is set to 3, we demand at least 3 (X) of the 8 (Y) past results to satisfy the “3+3” condition in order to fire a beam abort signal. In figure 4-2 the criterion “3+3” can be satisfied or not and the results can be “1” or “0” respectively... It is also important to note that the frame position varies and corresponds to the current BC, i.e. the frame position in BC=16 means that the current BC has BCID⁹=16.

If the current BCID is 16 the frame Y contains only 2 out of 8 past results with value 1. Therefore, even though in two of these BCs the “3+3” condition would demand to fire an abort beam signal, the X out of Y algorithm does not allow that signal to be fired. In the case of current BCID 19, in the frame there are 4 out of 8 past results with value “1”.

⁹ BCID is the BC identification number and is used as tag to all the data derived from the detectors during this BC.

Hence, the X out of Y algorithm does fire an abort beam signal since the threshold of $X=3$ is surpassed. Using the X out of Y algorithm can lead to the following case where even if the result of the current BC is not “1” (the “3+3” condition is not satisfied), if the X threshold is surpassed an abort beam signal will be fired. The actual condition for surpassing the X threshold is for the number of “1”s to be bigger or equal (\geq) than the chosen threshold value.

The algorithm takes into account information from the past Y BCs resulting in a less instantaneous decision for dumping the beam. A basic feature of this algorithm is that it minimizes the possibility of a spurious abort caused by an instant noise increase or a beam instability that takes place during only one BC. The two parameters frame Y and threshold X can be set via DCS whenever it is necessary. The freedom to have parameters of varied values adds a dynamic behaviour to the algorithm, since different sets of parameters may be more appropriate to deal with different situations. For instance, if the thresholds of the BCM are low for whatever reason a set of high X in respect to Y will save the BCM from unwanted spurious aborts. On the other hand if a more tolerant behaviour towards instantaneous deceitful information is preferred, a low value of X may be used in order to achieve this.

4.2.1 Implementation of the X out of Y algorithm

The X out of Y algorithm was implemented as a VHDL module in the main BCM code which runs in each FPGA. The inputs of the algorithm are the parameters frame Y and threshold X, the result of the “3+3” algorithm for the current BC and the 40 MHz LHC CLK used for the majority of the processes inside the FPGA. Two more inputs are dedicated to the RESET and ENABLE signals that are used in the VHDL code of the FPGA for reset and normal operation respectively. The output of the algorithm is a signal called TRIGGER that contains the result of the algorithm which in turn triggers or not a

beam abort signal. The past BC results are stored in an independent ram module, called Bitram. Two counters are used, increasing by one for each BC and are connected to 2 address pointers. These pointers indicate the addresses within the RAM that correspond to the beginning and the end of the frame Y. After each BC the address pointer which shows the end of the frame Y is increased by one, kicking out of the frame the oldest result. Similarly after each BC the address pointer which shows the beginning of the frame saves the current BC result in the current address within the RAM and then is increased by one. The 2 address pointers are shown as arrows in figure 4-3, where the operation of the algorithm for two consecutive BCs is illustrated.

The number of results with value 1 is stored in a counter which refreshes every BC... For every BC the counter “looks” at the current result that just came in to the frame and at the result of the BC that just dropped out of the frame. If both incoming and outgoing results have the same value (both “0” or both “1”) the counter keeps the same value. In the case where the incoming result is “1” and the outgoing is “0” the counter is increased by 1. In the case where the incoming result is “0” and the outgoing is “1” the counter is decreased by 1 (figure 4-3).

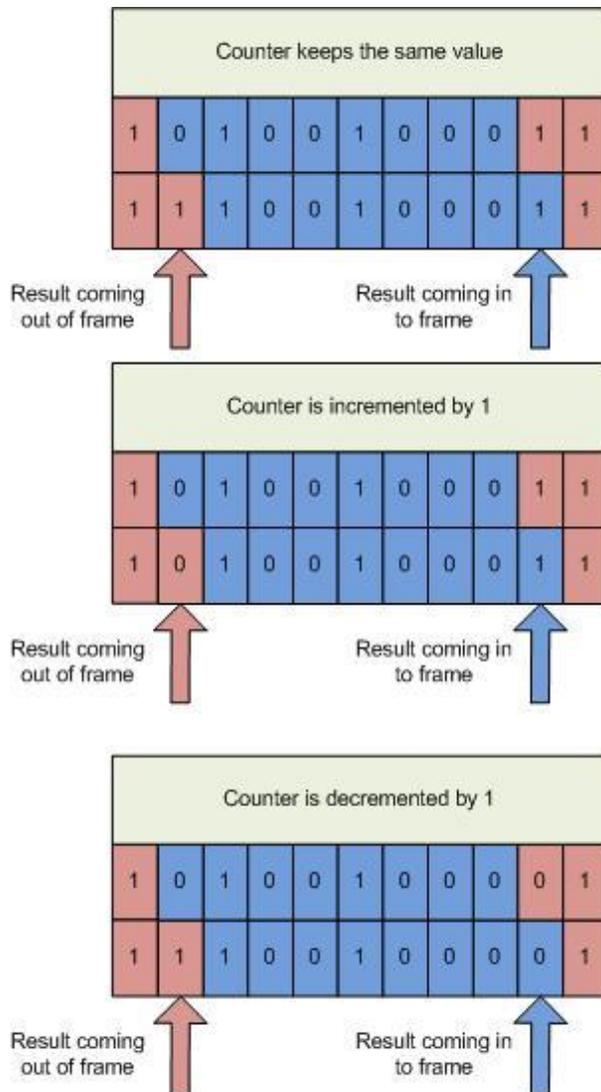


Figure 4:3 Value of the counter changing in one BC related to the incoming and outgoing results

In the current implementation the parameters of frame and threshold (Y and X respectively) have a binary length of 15 bits i.e. the possible value of both parameters varies from 0 to 65535. Another restriction applied is that the threshold X cannot be larger than the frame Y. It is also important to note that the output of the VHDL module is synchronized so that all the data refer to the current BC. The values of the parameters X, Y as well as the results of the TREGGER output of the algorithm can be monitored through the control panel of the BCM.

4.2.2 Simulation and probabilistic analysis

The algorithm was first simulated with CHIPSCOPE [CHI], the simulation and debugging tool of XILINX ISE NAVIGATOR 10 [XILb]. This is the environment in which the VHDL code for the FPGA was written, simulated and compiled. The results have shown that the algorithm works perfectly with different values for both parameters and that the output of the TRIGGER signal is synchronized to all the other data as they come out for each BC. Dominique Tardif and Ernest Jankowski, both BCM collaborators created 2 sets of simulations for the beam abort algorithms. They simulated some scenarios of beam instabilities and the results were related to the result of dumping the beam for each algorithm. Figures 4-4 and 4-5 show 2 of the plots constructed from the aforementioned simulation results.

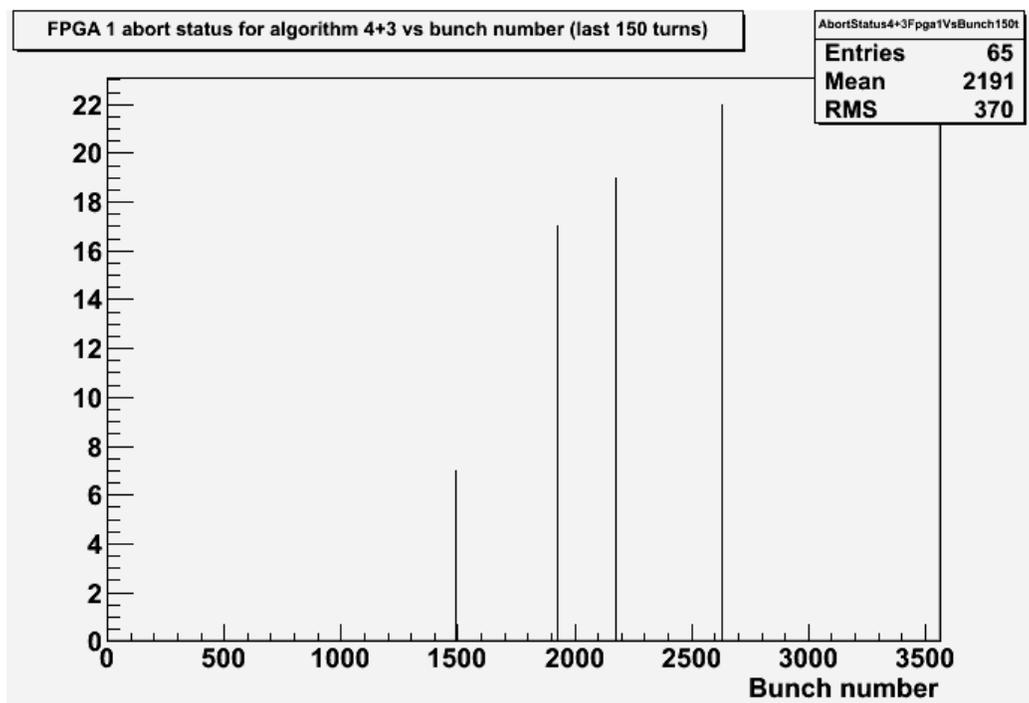


Figure 4-4: The simulation result for the 4+3 algorithm for 4 different scenarios

In figure 4-4 the result of the simulation for the $4+3^{10}$ algorithm is illustrated. The 4 different scenarios are 1, 10, 20 and 100 lost protons scraping the TAS collimator with an energy of 7TeV. The simulation time window was 1 orbit (3564 BCs- X axis) and it was repeated for 1178 times (Y axis). The results in figure 4-4 show how many times out of the total 1178 each scenario would fire an abort. For instance the lowest spike corresponds to 1 lost proton and it would the algorithm would inject a beam abort signal 7 of the 1178 times the simulation was repeated. In figure 4-5 the same result is illustrated for the X out of Y algorithm.

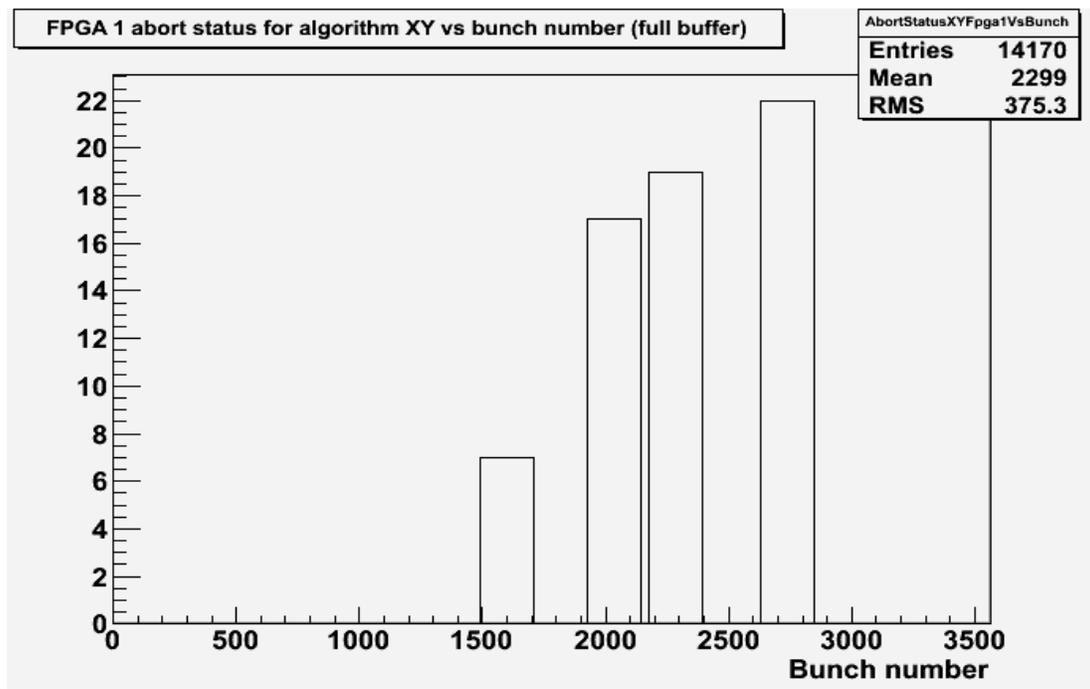


Figure 4-5: The same result for the X out of Y algorithm. It is clear that the frame F extends the time that the beam abort signal is fired

The parameters $X=1$ and $Y=200$ were chosen in order to provide a high possibility of aborting the beam. As a result of the parameter's values, the algorithm aborts for 200

¹⁰ Initially the $3+3$ condition was $4+3$ demanding 4 low gain and 3 high gain channels to fire in order to inject a beam abort signal.

BCs as the condition 1(X) out of 200(Y) is satisfied for 200 BCs until the BC in which the 4+3 algorithm fired an abort (BC=1500) is kicked out of the frame. From the previous plots is more clear that the X out of Y algorithm can be set to operate as very sensitive or not, depending on the parameters. Assuming that X was set to 2 the algorithm would not abort at any case as the condition 2 out of 200 would not be satisfied at any moment during this simulation.

The second simulation was performed only for the 4+3 algorithm for the same energy scenarios while the cases of lost protons were chosen to be 1, 10, 100 and 1000 protons. One plots of this simulation is illustrated in figure 4-6 and refers again to the 4+3 criterion.

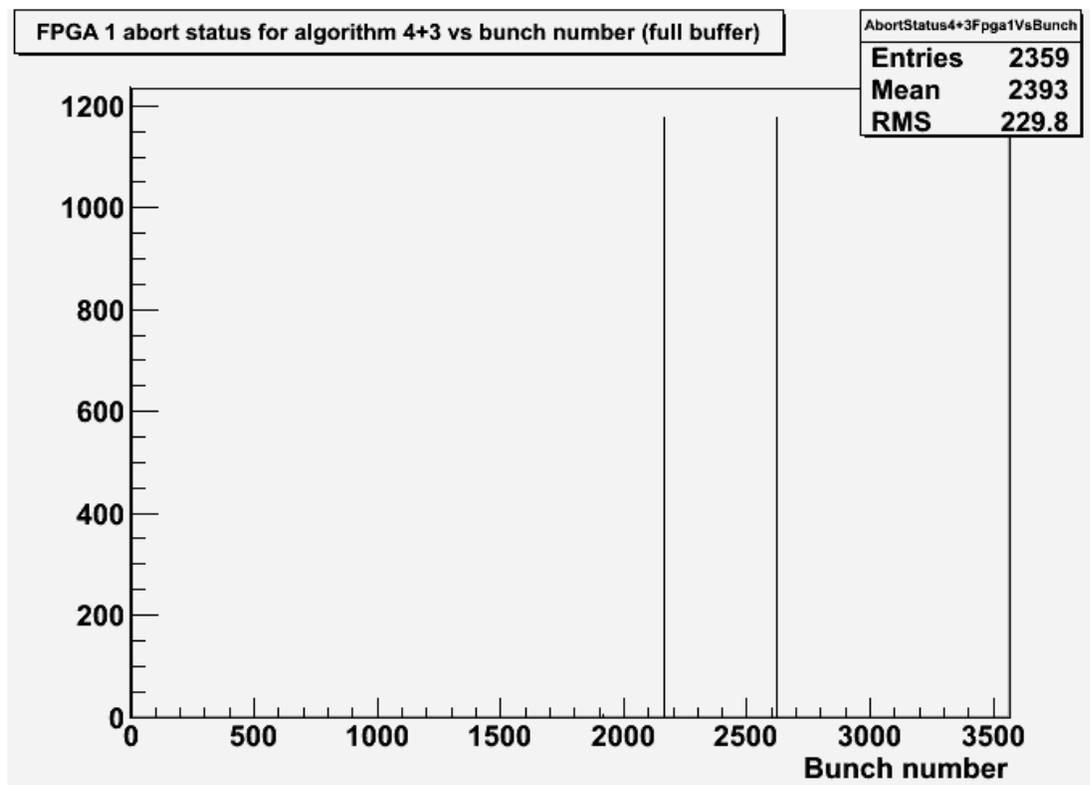


Figure 4-6: A plot for the 4+3 algorithm simulating the scenario of 1, 10, 100 and 1000 lost protons scraping the TAS collimator with energy 7 TeV

The 2 highest spikes refer to the scenarios of 100 and 1000 lost protons while the scenario of 1 proton had result 0 and the scenario of 10 protons results is 5 (a barely visible short spike in Figure 4-6). This simulation was performed for both FPGAs and the results for the 4+3 algorithm were used for a probabilistic analysis. From the 1178 repeats of the simulation the probability of each scenario to abort the beam during a BC can be calculated. These probabilities are shown in table 4-1 and were used for defining the probability to abort with the X out of Y algorithm for different values of the parameters. For each combination of energy and lost protons scenario the probability of satisfying the 4+3 condition in one BC was calculated by dividing the number of aborting out of the 1178 times repeated. For instance, in the plot 4-4 1 lost proton with energy 7 TeV would abort 7 out of 1178 times in total thus giving a probability of $P= 0,00594$. The simulation was done for both FPGAs and the biggest number of aborts was selected in each case.

Table 4-1: Number of aborts and probabilities P for each beam event scenario

Energy cases	Number of aborts/ probability P			
Lost proton cases	1 pr.	10 pr.	100 pr.	1000 pr.
7TeV on TAS	0/0	21/0,0178	1177/1	1177/1
450GeV on TAS	0/0	0/0	0/0	1111/0,943
450GeV on beampipe	0/0	0/0	3/0,0025	1171/0,994

It is important to note that there are 2 scenarios that the probability P is 1, when 100 or 1000 lost protons hit the TAS collimator. In these scenarios it is certain ($P=1$) that 4+3 algorithm will fire a beam abort in each BC and as a result also X out of Y algorithm will do so as well.

The second step in the probabilistic analysis procedure is to define the probability function $\Pi=f(x,y)$ related to the values of X and Y. This function has 2 independent variables and should cover the whole domain of both variables. The probability P is calculated as shown in table 4-1 for the different scenarios. If we define as P the probability of a random scenario then the function can be constructed step by step. If $x^{11}=2$ and $y=2$ then we need 2 out of 2 results with value 1. If the probability of each result to occur is $P=0,2$ the total probability to have 2 out of 2 is:

$$K=P \cdot P=(0,2) \cdot (0,2)=(0,2)^2 \quad (4.1)$$

If we assume that $x=2$ and $y=3$ then we need 2 out of 3 and the probability of result with value 0 (not abort) is $P'=1-P=0.8$. The probability of having a result of 2 out of 3 is:

$$K=P \cdot P \cdot (1-P)=(0,2) \cdot (0,2) \cdot (1-0,2)=(0,2)^2 \cdot (0,8) \quad (4.2)$$

However, there are 3 possible arrangements of the results (110, 101, 011) so the total probability of having 2 out of 3 is:

$$K_{total}=3 \cdot P \cdot P \cdot (1-P)=3 \cdot (0,2) \cdot (0,2) \cdot (1-0,2)=3 \cdot (0,2)^2 \cdot (0,8) \quad (4.3)$$

The total probability K of having x out of y results with value 1 (abort), if we take into account all the possible arrangements is:

$$K_x = \binom{y}{x} \cdot (P)^x \cdot (1-P)^{y-x} \quad (4.4)$$

In (4.4) the factor $\binom{y}{x}$ gives the number of all the possible arrangements of x results with value 1 (abort) out of the total number of y. The factor $(P)^x$ corresponds to the number of the x results with probability P (abort) and the factor $(1-P)^{y-x}$ to the number of the rest y-x results with value 0 (not abort) and probability $P'=1-P$. The final step to derive the function is to add K_x from x up to y, as we need at least x out of y and we have to consider the possibilities of having more than X results with value 1. The final equation for Π s:

¹¹ The parameters X and Y are defined in uppercase while when they are used as variables within the function they are designated as lowercase x and y.

$$\Pi = \sum_{k=x}^y \binom{y}{k} \cdot (P)^k \cdot (1-P)^{y-k} \quad (4.5)$$

The equation (4.5) gives the result of the probability that the X out of Y algorithm will fire an abort for each value of x,y and for every scenario (P). The probability function 4.5 is the cumulative binomial distribution.

The scenario of protons at 7 TeV hitting the TAS collimator will be studied because it is the most catastrophic and should always be detected and the beam should always be dumped in time. The scenario of lost protons scraping the beampipe with energy 450 GeV will be commented upon as it gives a good overview of how the probability value is distributed depending on the variables x and y.

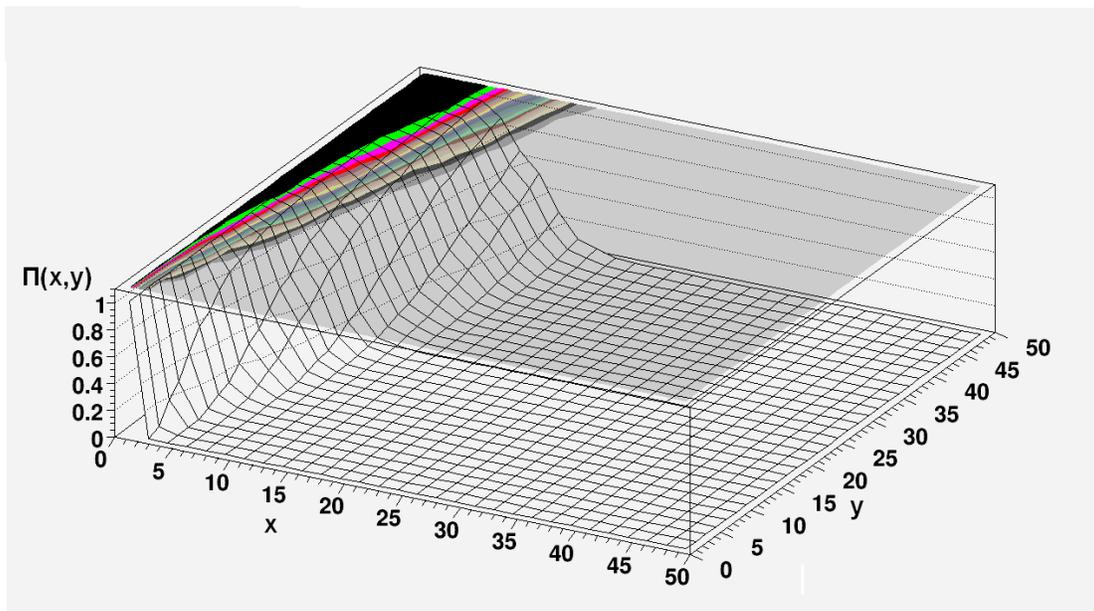


Figure 4-7: The probability function $\Pi(x,y,p)$ for $y=(0,50)$, $x=(0,y)$ and $p=0,0178$

In figure 4-7 the probability function $\Pi(x,y,p)$ is presented for different values of x and y for the scenario where $P=0,0178$ i.e. 10 lost protons with energy 7 TeV hitting the TAS collimator. In the figure it can be seen that for y constant, as the x is decreasing the probability of injecting an abort signal is increasing. Similarly for a constant x as y increases

the probability of injecting an abort signal is increasing as well. Finally, on Figure 4-7, it can be seen that x is taking values from 0 up to y (since we want the $x \geq y$ restriction to apply).

In figure 4-8, frame Y was set to value 500 and the scenario of lost protons hitting the TAS with energy 7 TeV was simulated. For 1 lost proton the probability P is 0 and as a result it is not shown in figure 4-8. For 10 lost protons the probability $P=0,017842$, while the blue curve illustrates the probability for different values of x . It is important to note that for very small values of x the probability is very high and decreases rapidly as x is increasing. For 100 and 1000 lost protons the probability P was calculated to be 1, both of which correspond to the green curve shown in Figure 4-8. In this case, for all the values of x the algorithm will trigger a beam abort signal, as it should for such a dangerous scenario.

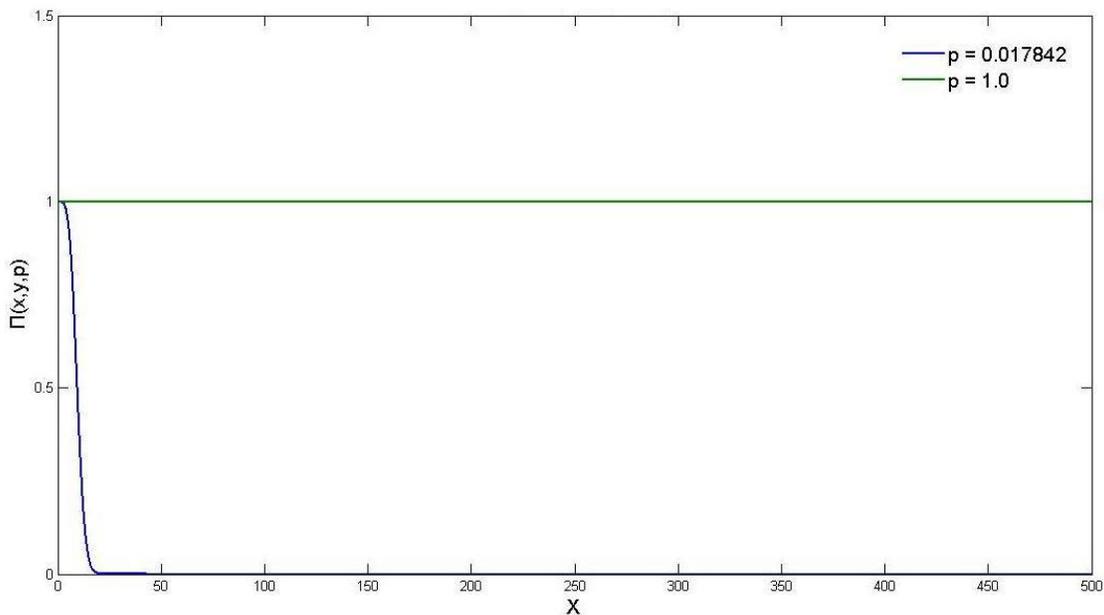


Figure 4-8: The probability function $\Pi(x,p)$ of lost protons hitting the TAS with energy 7 TeV when $y=500$

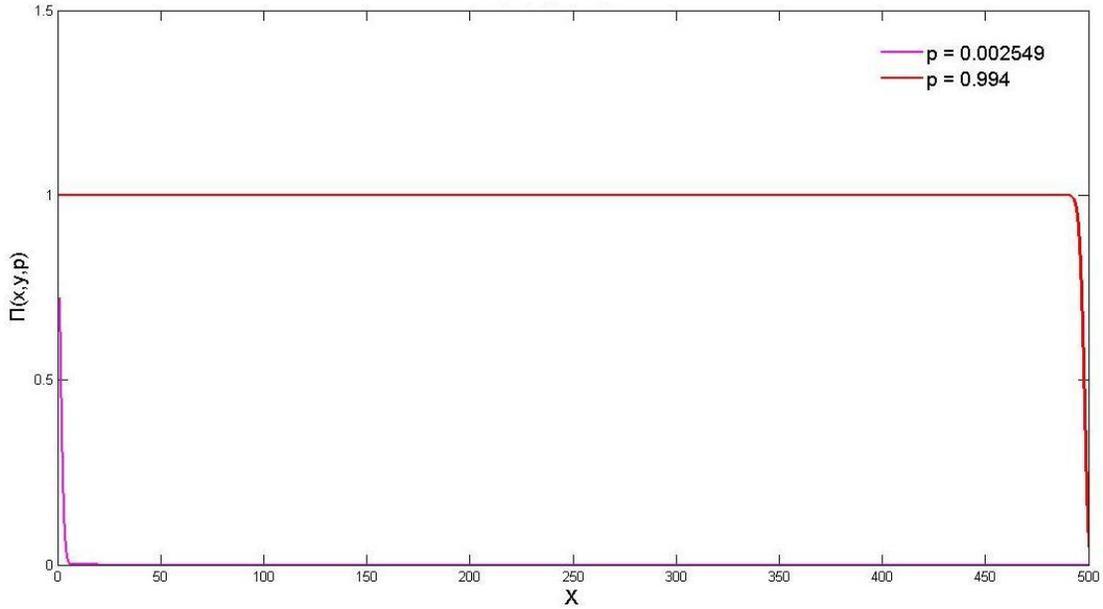


Figure 4-9: The probability function $\Pi(\mathbf{k},p)$ of lost protons scraping the beampipe with energy 450 GeV when $y=500$

Finally in figure 4-9, the scenario of lost protons with energy 450 GeV scraping the beampipe is presented. In this Figure it is interesting to point out that the 2 curves are almost complementary. For 100 lost protons where $P=0,002549$, the pink curve shows that the probability of injecting a beam abort signal is considerably high only when x is very small related to $y=500$. On the contrary, for 1000 lost protons with $P=0.994$ the red curve shows that the probability of injecting a beam abort signal is almost 1 for the most of x values except those values very close to $y=500$, where the probability is reduced.

4.3 The forgetting factor algorithm

The second beam abort algorithm developed to achieve a more dynamic behavior is called forgetting factor (FF) algorithm. The concept of the algorithm is similar to two others: the exponentially weighted moving average and the leaky bucket algorithm [WIK].

The exponentially weighted moving average (EWMA) algorithm is a more sophisticated version of the simple moving average related to the X out of Y algorithm as discussed earlier in this chapter. Weighting factors that are exponentially decreased are applied to older observations. Hence, much more importance is given to recent observations while not discarding altogether the older observations. The observation at a point n is designated Y_n and the value of the average S_n and is calculated as:

$$S_n = a \cdot Y_{n-1} + (1-a) \cdot S_{n-1} \quad (4.6)$$

where a is the decreasing factor of the older measurements. It can take values between 0 and 1 and the higher the value the faster is the degradation of the past observations. The FF algorithm works in a similar way. Y_n is defined as the current value of a counter at point n. The counter is related to the value of the previous point (n-1) decreased by a factor of f, and to the current result of the “3+3” condition.

$$Y_n = f \cdot Y_{n-1} + I_n \quad (4.7)$$

The factor f can take values between 0 and 1, similarly to factor a in the EWMA algorithm. I_n , which represents the current result of the “3+3” condition, is introduced into equation 4.7 Unlike the X out of Y algorithm, the value of I_n is not 1 if the “3+3” result is 1. In order to increase the dynamic behavior of the algorithm and compensate for some unavoidable implementation difficulties (presented below), it is assumed that when the “3+3” result is 1, I_n will be assigned the value of I (influence).

$$I_n = (\text{3+3 result}) \cdot I \quad (4.8)$$

The condition for the FF algorithm to trigger a beam abort signal is the counter Y_n to be equal or bigger to a threshold T. This threshold is a parameter that has to be set to a value that is considerably higher than the influence to prevent firing an abort each time 3+3 result is 1. All the parameters f, I and T are monitored via DCS and can be changed at anytime to new desired values.

The FF algorithm bears also resemblance to the leaky bucket algorithm. This algorithm is used often for network traffic shaping or rate limiting. To understand the

concept of the algorithm let's assume a bucket with a hole in the bottom as the one in figure 4-7. Packets are sent into the bucket at a constant rate, same as the rate of the outgoing packets from the hole. If the bucket is full the packets inside the bucket are discarded. In the case where the rate of outgoing packets is lower than the incoming rate, the algorithm behaves similarly to the FF algorithm.

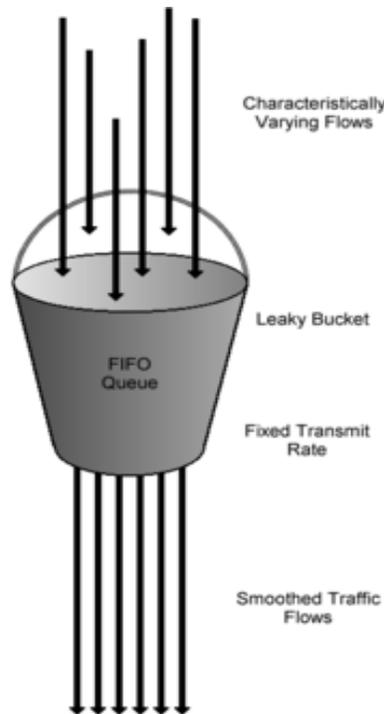


Figure 4-10: A leaky bucket showing the leaky bucket algorithm concept

Factor f corresponds to the hole at the bottom of the bucket that is pouring out (forgetting) the packets in situated at the bottom (older results). The threshold corresponds to the case where the bucket is full and all packets are discarded. Similarly, in the FF algorithm if the counter is higher or equal to the threshold the abort signal is triggered. The bucket is using FIFO queue, thus reducing the influence of the older measurements in respect to the new ones.

The development of the final “homebrew” algorithm that was used was influenced from the abovementioned two algorithms using different characteristics from each one.

One of those characteristics was a very dynamic behavior that can handle a variety of possible scenarios. Another characteristic was the choice to decrease the weight of the past results as the time goes by but not to discard their influence to the overall decision. The final algorithm's equation can be written in a way that gives the result related only to I_n and the factor f . By replacing each counter value with its equivalent from equation 4.7 then the counter after n number of BCs becomes:

$$Y_n = f \cdot Y_{n-1} + I_n = (f \cdot Y_{n-2} + I_{n-1}) \cdot f + I_n = Y_{n-2} \cdot f^2 + I_{n-1} \cdot f + I_n \quad (4.9)$$

Performing the recursive calculation we arrive at:

$$Y_n = Y_0 \cdot f^n + I_1 \cdot f^{n-1} + I_2 \cdot f^{n-2} + \dots + I_{n-1} \cdot f^1 + I_n \cdot f^0 \quad (4.10)$$

As Y_0 we define the initial value of the counter:

$$Y_0 = I_0 \quad (4.11)$$

If we replace Y_0 with I_0 then equation 4.9 can be expressed as the following sum:

$$Y_n = \sum_{k=0}^n f^k I_{n-k} \quad (4.12)$$

Equation 4.12 is a very convenient expression for our purposes as it contains only the factor f and the results of all the previous BCs. According to equation 4.12, in the case of $f \leq 1$, the older a result is the less it contributes to the current value of the Y_n counter. However, equations 4.12 and 4.7 do not correspond to a known probability distribution. As a result it is very difficult to define the probability function where according to the FF algorithm a beam abort is fired (i.e. the value of Y_n is higher or equal to threshold T). Hence, instead of probabilistic analysis, various scenarios with preset values for the parameters will be studied.

The FF algorithm is the most complex of the algorithms mentioned and as a result the desired definition of the parameter's values is not straightforward. On the other hand the structure of the algorithm allows considerable changes to be made in its behavior, based on different set of parameters. For example a low factor with high influence in respect to the value of the threshold, would lead to an algorithm that would trigger a beam

abort only when a set number of consecutive “3+3” results (value of “1”) occurs. Another example would be if the factor is set very high (close to 0.99) and the threshold is set to double the influence. In this case the algorithm will “remember” the older results and would trigger an abort with just few “3+3”(value of “1”). Different scenarios like the ones presented here will be discussed later within this Chapter.

4.3.1 Implementation of the FF algorithm

The FF algorithm was implemented in the FPGA as a VHDL module. The input of the “3+3” algorithm result, the CLK RESET signal and ENABLE signal have already been described in the case of the X out of Y algorithm and are being used in the case of FF algorithm as well. Additional inputs are: parameter T (THRESHOLD), parameter I (INFLUENCE) and an input called CODE (which encodes the value of the factor parameter). The input CODE has 8 binary bits and its encoding is based on the idea that every bit, except for the MSB, corresponds to a factor division. The factor is allowed to take values from 0.0078125 to 0,9921875, which are formatted by the sum of the all the necessary divisions to its actual values ranging from 0,5 down to 0,0078125. If for example the desire value of factor is 0,75 then the factor will be constructed as:

$$F=0,75=0,5+0,25$$

The input CODE uses one bit for every factor division. If the bit is 1 then the corresponding division is added in order to construct the desired value of the factor F. If the bit is 0 then the division is ignored. For instance if the desired value of factor is F= 0,71875 then this will be constructed as:

$$F=0,71875=0,5+0,125+0,0625+0,03125$$

The CODE signal that encodes the value F= 0,71875 would be 0101110. The Code bits that have value 1 show that the related factor division will be used in the construction

of the factor. In table 4-2 the encoding of factor in the CODE bits is presented. If all CODE bits are 1 then the factor is 1 while if all CODE bits are 0 the factor is set to 0.

Table 4-2: CODE bits and corresponding factor divisions encoding for constructing the final value of the factor

	CODE bits							
Factor Division	7	6	5	4	3	2	1	0
+0,5		1						
+0,25			1					
+0,125				1				
+0,0625					1			
+0,03125						1		
+0.015625							1	
+0.0078125								1
Factor=1	1	1	1	1	1	1	1	1
Factor=0	0	0	0	0	0	0	0	0

As far as the outputs are concerned, the FF algorithm has an output called TRIGGER (similarly to the X out of Y algorithm) that provides the result of the algorithm for firing or not a beam abort signal.

An internal variable is used as a counter to represent the value of Y_n . During each BC the value of this counter is compared to the threshold T. The use of floating point variables is prohibited by the restricted memory within the FPGA. As a result the division

of the previous value of the counter by the factor cannot be mathematically perfect. For instance the division by a factor 0,5 is implemented by cutting off the least significant bit (LSB) of the counter while for factor 0,25 two LSBs are discarded etc. This technique for performing the division is basically the use of the operator “div” that keeps only the integer part of the division with $1/f$. For instance if the previous value counter is 5 and factor is 0,5 the new value of the counter will be:

$$Y_n = Y_{n-1} \left(\text{div} \frac{1}{f}\right) + I_n = 5 \left(\text{div} 2\right) + I_n = 2 + I_n$$

This characteristic is in no way reducing the efficiency or functionality of the algorithm but it is increasing the complexity of determining the appropriate values for the parameters. Implementing this division technique changes equation 4.7 into:

$$Y_n = \left(Y_{n-1} \text{div} \frac{1}{f}\right) + I_n \quad (4.13)$$

By calculating Y_{n-1} :

$$Y_{n-1} = \left(Y_{n-2} \text{div} \frac{1}{f}\right) + I_{n-1} \quad (4.14)$$

In order to give the same format as equation 4.7 to equation 4.13, we performing the recursive procedure down to Y_0 while Y_n is a function only of factor f and I_k . Hence equation 4.13 becomes:

$$Y_n = \{[\dots((((I_0 \text{div} \frac{1}{f}) + I_1) \text{div} \frac{1}{f}) + I_2) \text{div} \frac{1}{f}) + \dots + I_{n-1}] \text{div} \frac{1}{f}\} + I_n \quad (4.15)$$

From the equation 4.15 it is can be deduced that any probabilistic analysis is impossible. The infinite sequence of results $I_k \left(\text{div} \frac{1}{f}\right)$ cannot be expressed in a sum, as it has been done for equation 4.7, hence it is impossible to calculate the probability of $Y_n \geq T$ for any given T . For the FF algorithm the simulation will be replaced by the discussion and analysis of certain scenarios with given “3+3” inputs and fixed values for the parameters.

The FF algorithm implementation uses just one counter instead of the two used for the RAM addresses, in the case of the X out of Y algorithm. The counter has 8 binary bits

as well as the THRESHOLD T and INFLUENCE I. As a result, the value range of this counter ranges from 0 to 255. Such a range for the value of the parameters is considered large enough that the algorithm can maintain its very desirable dynamic behavior.

4.3.2 Tests with the XILINX CHIPSCOPE

For testing the operation of the FF algorithm two different procedures were employed. The first was to use the CHIPSCOPE [XILc] tool, which is usually used to debug and test XILINX VHDL modules. In every scenario tested, the parameters were set to their specific values and the result was observed. Hence it was possible to test different sets of values for the parameters and obtain specific sets of values that would optimize the algorithm's behavior. These tests are similar to a simulation and they do not prove the normal operation of the FF algorithm, but can be used as very good guideline for setting the values of the parameters' by using a reliable XILINX tool.

One scenario of those examined is shown in figure 4-11. In the presented screenshot of the CHIPSCOPE panel all the inputs, the outputs and the some of the internal signals can be seen.

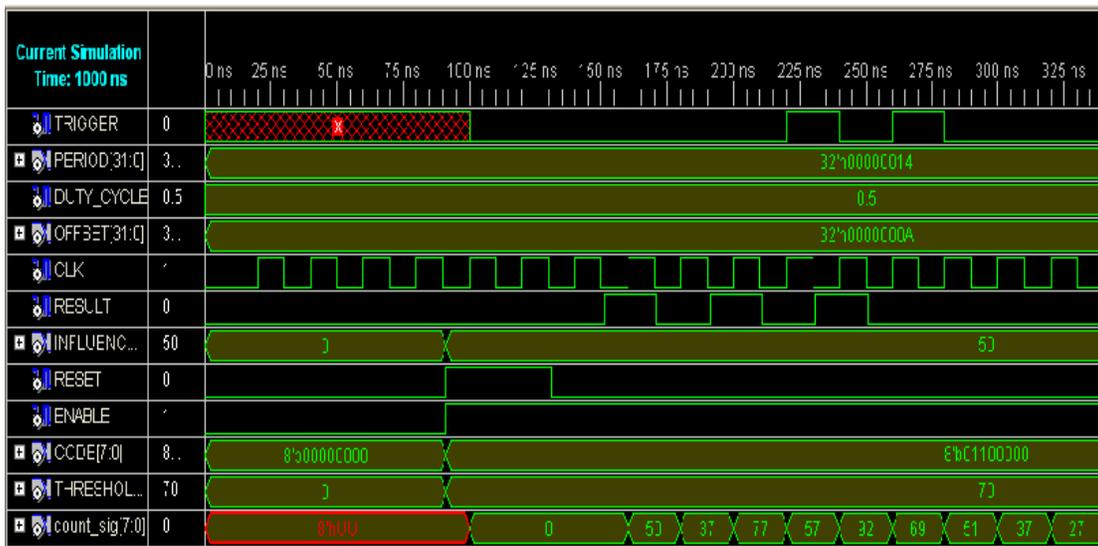


Figure 4-11: Test in CHIPSCOPE of a scenario for the FF algorithm

The pattern of the “3+3” results input is represented in Figure 4-11 by the RESULT pulse. The counter of the algorithm is shown at the bottom along with the changing value for every BC. In the scenario shown in figure 4-11, the CODE input is 01100000 and as a result the factor is calculated to be $f=0,75$. INFLUENCE is set to $I=50$ and Threshold to $T=70$. In this scenario the algorithm will trigger a beam abort signal as it can be seen from the two pulses in the TRIGGER signal. Every BC the counter is refreshing and at the end of each BC it is compared to the threshold. At the end of the 3rd BC the counter value is 77 i.e. higher than the threshold value $T=70$. As a result, at the end of the 3rd BC the TRIGGER output will trigger a beam abort. In the 4th BC the input RESULT is 0 and the counter is reduced to 57 which is lower than T . This can be seen as in the end of the BC the TRIGGER output has value 0 which means that the abort is not triggered any more. Similarly during the next BC the counter will be higher than T and the TRIGGER output will fire a beam abort signal again. This example shows that in the 4th BC that the RESULT is 0 the counter is reduced in a level lower than T and the algorithm stops triggering a beam abort. This doesn't mean that the beam will continue circulating as it has already started the dumping procedure in the previous BC and will be aborted nonetheless.

However, using the dynamic behavior of the algorithm, for this scenario, if we would like not to abort the beam when only 3 results of “3+3” are high we could use a different set of parameter values, as shown in figure 4-12.

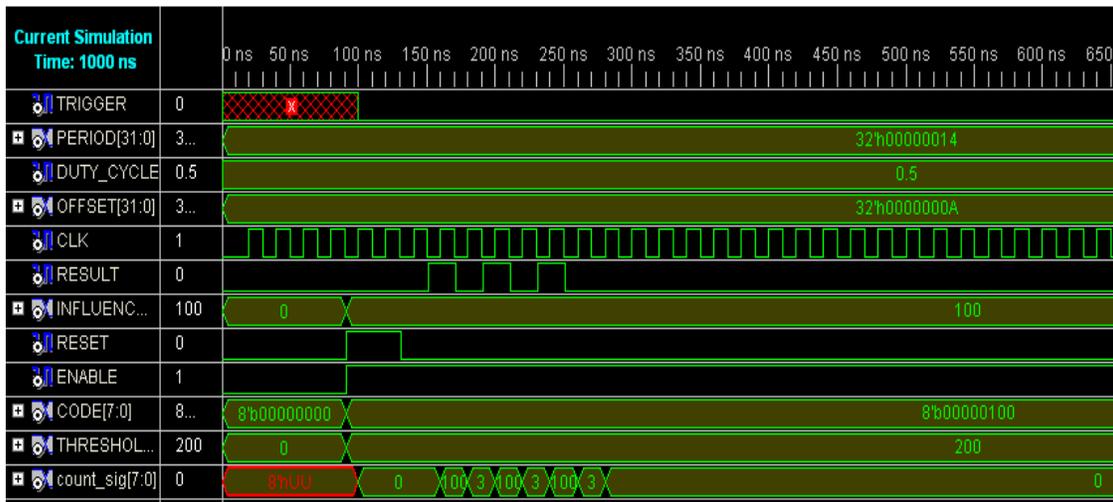


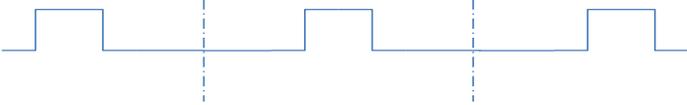
Figure 4-12: The same input pattern with different set of parameters does not trigger an abort

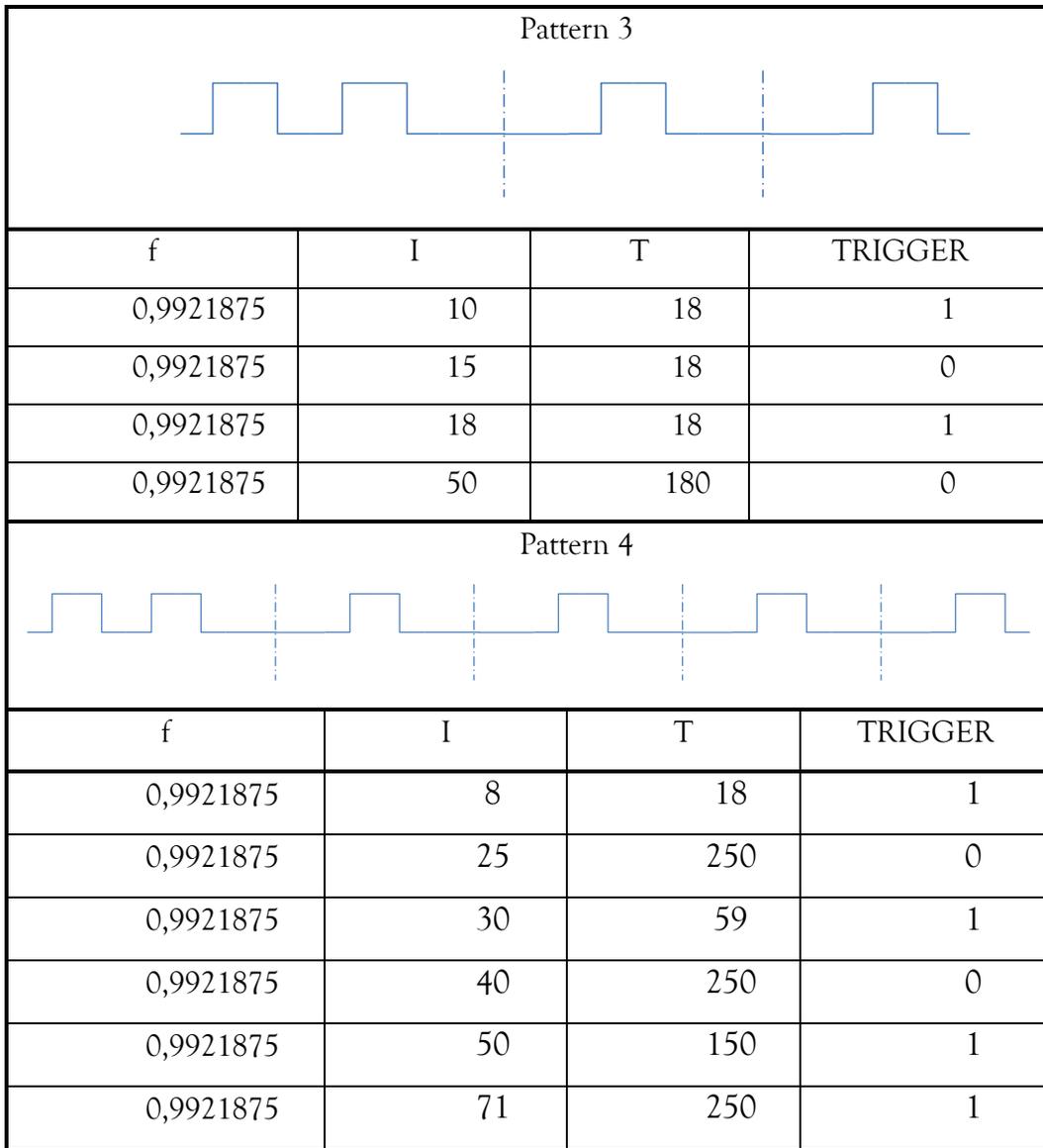
In the case presented in figure 4-12, the parameters are set now as: $f=0,03125$, $I=100$ and $T=200$. In this case, using the same input pattern will not fire a beam abort signal, since it would need consecutive “3+3” high results for a large number of BCs to fire an abort. This example illustrates the versatility and dynamic behavior of the FF algorithm, allowing to deal with many different requirements.

Tables 4-3 contain all the patterns that were tested, the different sets of parameters’ values and the TRIGGER result. Factor was set from very low to very high values to test how it influences the result of the FF algorithm. In the same way influence I and threshold T were set to values from very low to very high. The difference between influence and threshold was based on the value of factor (when a factor was close to 1, the threshold should be big enough in respect to influence to prevent the triggering of the abort signal to occur very often). The patterns vary from consecutive “3+3” high results (pattern 1) to more rare high “3+3” results (pattern 4). These tests give different sets of parameter values that yield the wanted Trigger result for each case (pattern). Other scenarios with longer patterns were also tested for in order to simulate scenarios with very rare “3+3” high results. All these tests, including the ones presented in this chapter, prove that the FF algorithm module performs effectively and works very efficiently. The CHIPSCOPE

simulation gives the initial indication that the algorithm is performing as desired but further tests under real conditions, while the BCM is in operation, had to be performed. These tests with real pulses coming into the FPGAs, simulating real beam events will be discussed in the next chapter. Some of the patterns described here were also used in the real pulses tests and results from both tests were compared and were found to be identical.

Table 4-3: Simulation of FF algorithm TRIGGER result for different patterns and parameter values

Pattern 1			
			
f	I	T	TRIGGER
0,03125	100	200	0
0,03125	200	201	1
0,03125	200	204	0
0,75	40	60	1
0,75	40	70	1
0,75	50	70	1
Pattern 2			
			
f	I	T	TRIGGER
0,75	40	60	1
0,75	40	70	1
0,75	50	70	0



4.3.3 Pulser run tests and online monitoring results

Even when there is no beam, ATLAS might be in operation in order for example to check that DCS, other control and monitoring systems are working, as well as using various tests and equipment for calibration purposes. The BCM has a “pulser” integrated before each ROD that can produce pulses similar to the real ones coming from the front-end electronics and the detector modules. The pulse sent by the pulser during each BC in

every channel, which in turn is detected by the FPGAs, it can be considered as a real pulse. Hence, a lot of tests can be performed with no real danger for the detectors as well as allowing the calibration of various parameters.. Several pulser runs were used for testing of the FF algorithm in order to ensure that it will behave during live operation as it was expected to, considering the results from the simulations. In figure 4.13 is shown that a pulse (sent from the pulser) can be detected in every channel, as monitored by the OHP monitoring tool of ATLAS.

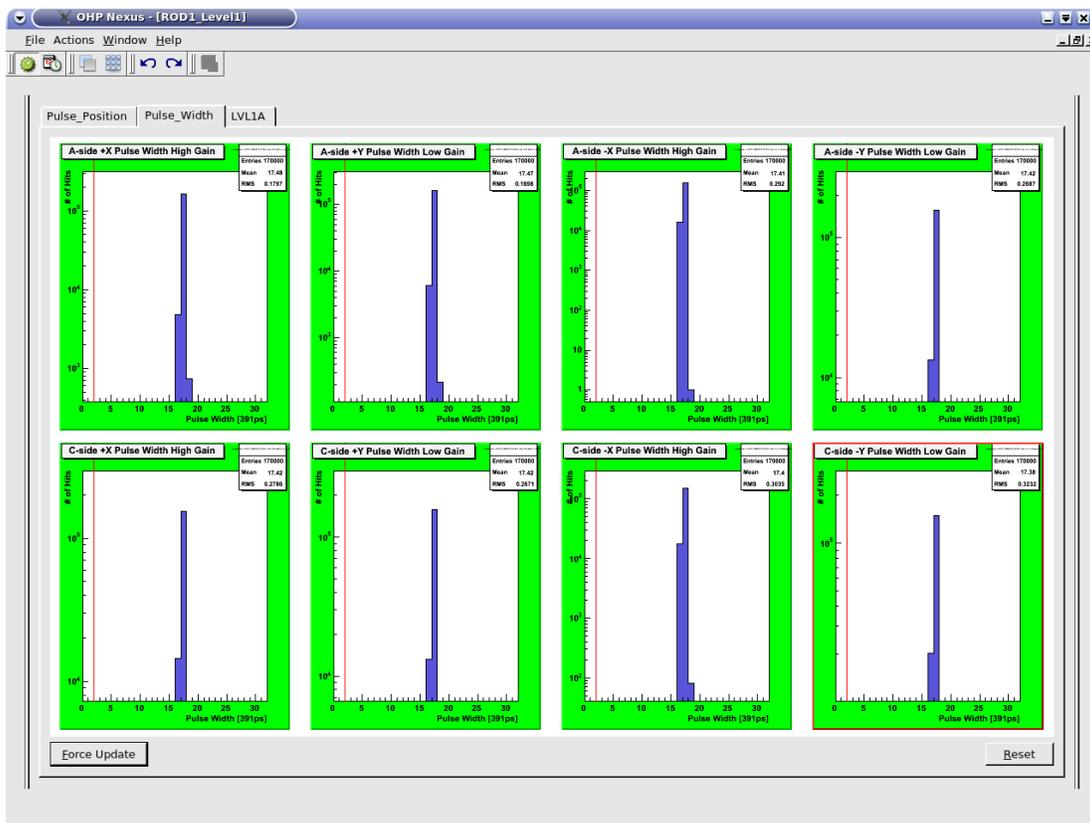


Figure 4-13: Pulses from pulser run monitoring the pulses' width in every channel of ROD1

These pulses were used to create the necessary patterns used in the pulser run tests. The first pattern to be discussed, Pattern 1, has been used before in the CHIPSCOPE simulation (as discussed in the previous Chapter) and consist of 3 high “3+3” results with a

gap of one BC low “3+3” result in between them. The parameters were set at: factor $f= 0,5$ in a low value and influence I close to threshold T ($I=4$ and $T=5$ respectively).

In figure 4-14 the result show as LV1A is triggered two times. The horizontal axis presents the total of 32 bins (i.e. 32 consecutive BCs) and the vertical axis presents each channel, color coded according to the number of hits. The results presented include signals from both RODs and all the 16 BCM channels are monitored simultaneously.

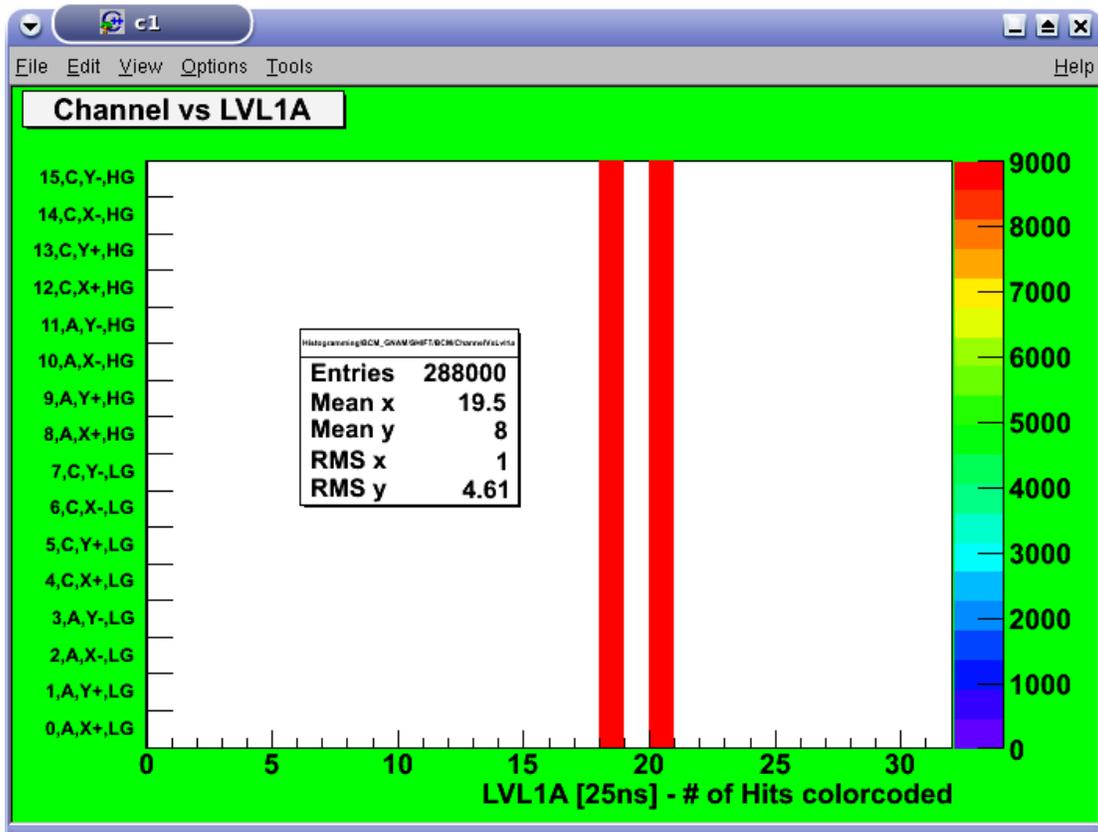


Figure 4-14: Number of hits for all BCM channels with input from a pulser run constructing pattern 1

The number of hits shown is higher than the actual expected hits produced by the BCM under normal operation. This discrepancy is produced due to the fact that the pulser produces a high number of hits (as an indication, the number of monitored hits in figure 4-13 is higher than 10^5). The FF algorithm triggers an abort signal two times, after the second and third pulse of the pattern respectively. The counter has a value of 5 during

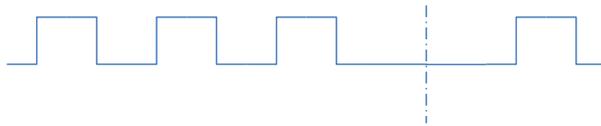
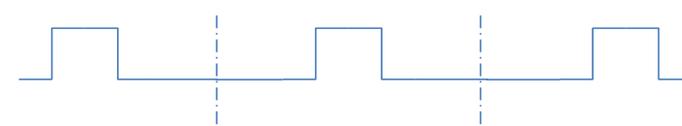
both times, which is equal to the threshold. After the third pulse the counter goes rapidly down to 0 and the algorithm does not trigger any other abort signal. In this example it is shown that the FF algorithm triggers with counter is also equal to the threshold.

During the pulser runs, four different patterns were used along with different sets of parameters. The first pattern is the identical to Pattern 1 and one of the scenarios tested is presented in figure 4-14. Using the pulser all the desired patterns could be constructed, excluding patterns with consecutive high “3+3” results. The result of each scenario and all the hits per channel were monitored with OHP. The pulses provided by the pulser were also recorded as a reference (see Appendix B). The parameters of the algorithm were changed and monitored via the DCS control panel called DCS FSM Panel.

Some values of the parameters were set to the same values to those used in the simulation tests and the results were compared. Table 4-4 lists most of them in respect to the pattern used as an input. Different patterns, similar to those presented in table 4-4, were also tested, yielding almost identical results (presented in Appendix B).

Table 4-4: FF algorithm TRIGGER result of pulser runs for different patterns and parameter values

Pattern 1			
			
f	I	T	TRIGGER
0,25	15	17	0
0,25	16	17	1
0,5	4	5	1
0,5	4	6	0
0,9531215	20	50	1
0,9531215	20	60	0

Pattern 2			
			
f	I	T	TRIGGER
0,9531215	20	55	1
0,9531215	20	56	1
0,9531215	20	80	0
Pattern 3			
			
f	I	T	TRIGGER
0,5	15	17	1
0,5	15	18	0
0,75	40	58	1
0,75	40	62	1
0,75	40	63	0
Pattern 4			
			
f	I	T	TRIGGER
0,5	4	5	1
0,5	4	6	0
0,9921875	3	10	0
0,9921875	5	10	1

All the results of table 4-4 were as expected compared to the simulation tests, thus the final test, under normal operation conditions, of the FF algorithm was deemed

successful. Finally in figure 4-15, where the output of the pulser run using Pattern 4 as an input is presented, it can be seen that a total of 15 pulses are monitored and some of them have a higher number of hits than the others. This is due to the fact that the ATLAS trigger system is using a gap of at least 7 bins before it triggers again. Hence the pattern can be seen three times in total, at the beginning, moved by 8 and finally moved by 15 bins. This effect can be monitored and it can be seen as a double number of hits when two patterns coincide in time and a tripled number of hits when three patterns coincide, as measured in the OHP.

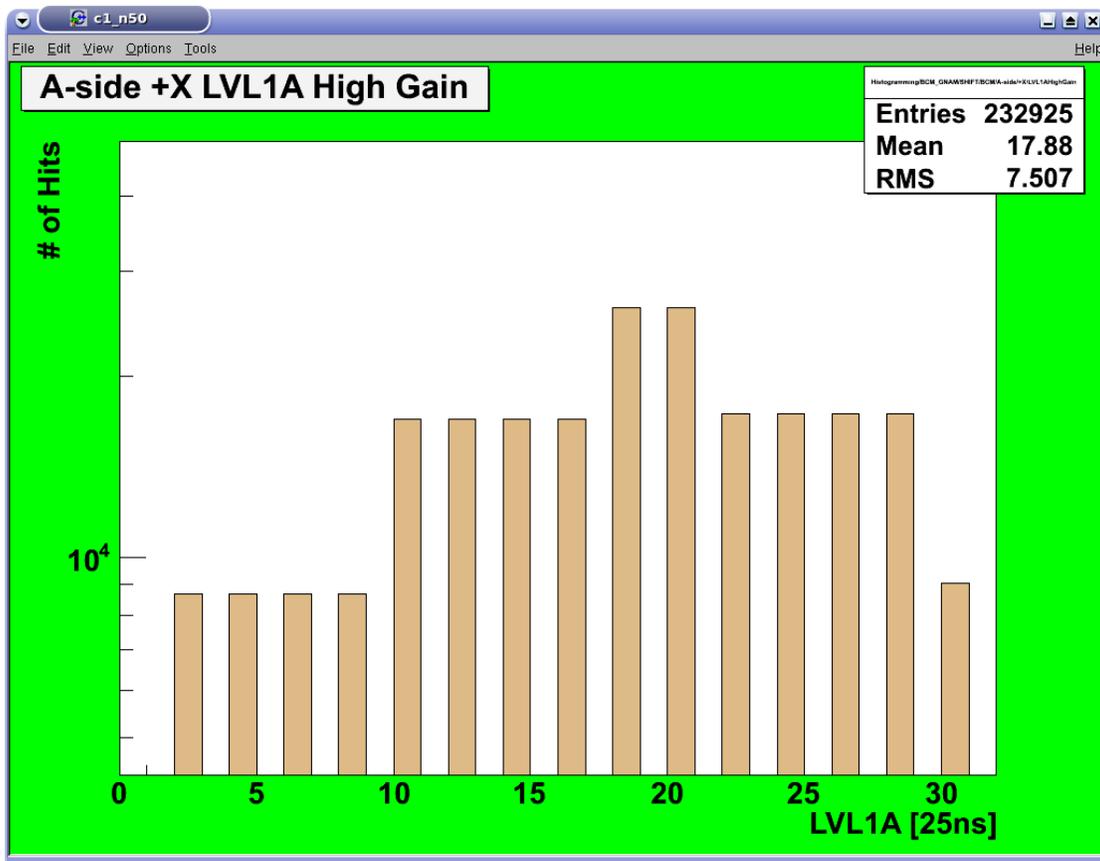


Figure 4-15: Multiple trigger of the same pulses in pattern 4

4.4 Conclusion and improvements

Both extension algorithms mentioned in this chapter were simulated and tested separately. All the results, from both extensions show a stable operation as was expected. Currently both algorithms are running simultaneously and the results are monitored and can be recorded via the DCS. Since the appropriate values for each set of parameters need to be verified during normal operation, the abort trigger signals produced by those algorithm are closely monitored and evaluated but are not yet in use for the abort beam procedures.

A possible further extension for the BCM abort algorithms would be to have as an input the actual state of each channel as that is detected by the RODs and not the “3+3” condition result. This could potentially detect any beam instability that would constantly affect a lesser number of the six channels (which are currently needed for the “3+3” condition) and further increase the certainty with which a beam abort signal is fired. Finally, in figure 4-16, a beam event occurring in ATLAS that led to the BCM firing a beam abort signal is presented, as recorded by the OHP on 3/12/2009

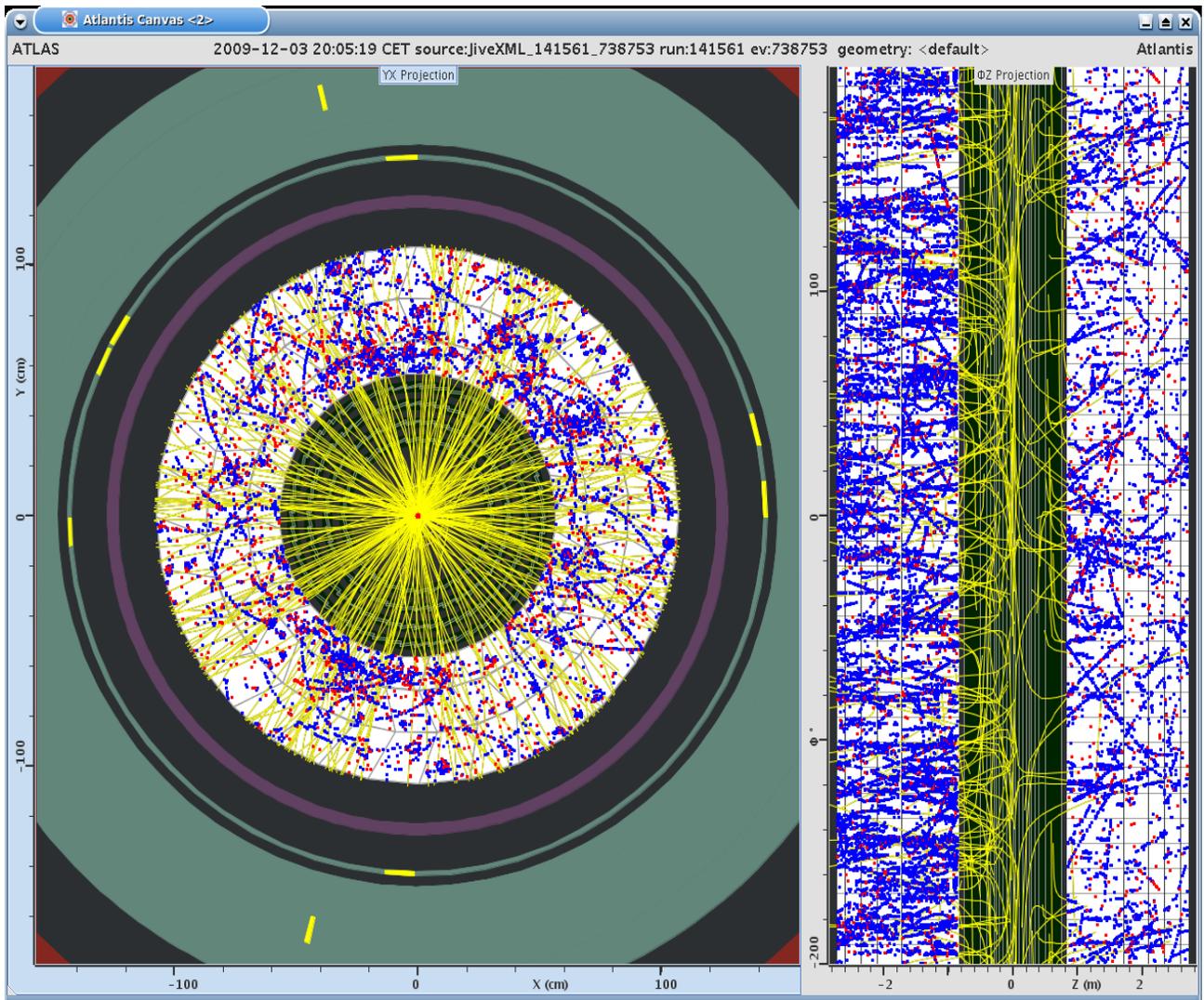


Figure 4-16: Event taking place in ATLAS right before BCM fires a beam abort on 3/12/2009

Chapter 5

Analog front-end electronics

5.1 Introduction

The analog front-end electronics constitute a very important part of the BCM detector. Strict requirements for the analog electronics must be fulfilled and the system should overcome the hostility of the radiation environment and fulfill the needs of very fast response time. Other, less strict requirements that the analog front-end electronics should meet are: a) a high signal to noise ratio (SNR), since the incoming signal has low amplitude and b) a very low signal distortion. The front-end system was designed and developed by FOTEC as described in chapter 2. It meets all the requirements, as discussed above, and it has exhibited excellent performance during the operation of ATLAS.

In this chapter the performance of the front-end electronics will be discussed in more detail, using a set of measurements related to the performance of the amplifiers. A brief analysis of the BCM spice model is also presented in this chapter. Finally, a study including a proposal for a pulser circuitry is presented, which in theory can replace the real pulses incoming from the detectors and could be used for calibration and testing purposes.

5.2 BCM amplifiers and measurements

Both amplifiers used in the front-end part are monolithic microwave integrated circuits (MMIC) used for high frequency signal amplification. The first stage is a 500 MHz Agilent MGA-62563 GaAs MMIC low noise amplifier and was chosen for its excellent linearity and low noise performance exhibited within the range of the operating

frequencies of the BCM system (the range of the amplifier is from 0,1 up to 3 GHz). The amplification gain of the first stage is 20dB while the noise factor is close to 0.9dB. The connection of the amplifier to the detector inputs is filtered by a 1nF capacitor, a 3.3pF capacitor connected to ground and a 15nH inductor.

The second stage of amplification is implemented by a Mini Circuits Gali 52 InGaP HBT broadband microwave amplifier used as the main amplifier. The high dynamic range of this amplifier is an important feature for the linear amplification of the input signal. The amplification gain of the InGaP amplifier is 20dB.

Both amplifiers were tested in order to ensure that the radiation does not affect noticeably the amplification gain. These tests mostly included the irradiation of the amplifiers with photons, neutrons and protons, exhibiting a degradation of only 0.5 db in the GALI amplifier gain. As far as the Agilent amplifier is concerned, it was also tested by replacing one amplifier module, with an irradiated one. The irradiation applied was up to a mixed fluence of $5 \cdot 10^{14}$ protons/cm² and $5 \cdot 10^{14}$ neutrons/cm². The results observed were an amplification degradation of 20% and no noise increase for the Agilent amplifier. The total SNR of the front-end electronics was measured close to 6 which is a very good performance under this environment, taking into account the high frequencies and low amplitudes of the input signals.

Apart from the abovementioned tests, which were performed previously to the measurements presented in this thesis, another test was setup in order to measure the amplification and the performance of the amplifiers in more detail. The input pulse used in these tests was produced by a Wavetek 395 pulse generator that was able to produce a square pulse. The main reason to select the aforementioned pulse generator was the need for a very short rise time (the requirement was a rise time of the order of 1ns). The pulse produced and used was measured to have a 2.12 ns rise time at amplitude of 1V. The pulse was then fed into a circuitry, transforming the square pulse into a spike inducing a degradation of 65% on the signal's amplitude. The signal was then fed into an attenuator in order to decrease it by 20dB and then it was split into two signals. One of the split

signals was sent to the amplifiers and the other was sent to a TEKTRONIX DP04034 analog oscilloscope, in order to provide an accurate measurement for the input signal fed into the amplifiers. A restriction of 2,5V on the maximum output from all amplifiers, during these tests, was imposed, and in order to achieve these two attenuators (10dB and 20dB) were used before the amplification was performed.

During the first test a GALI 52 1-2000MHz (S.N. 00048A4_AKG) with 20 dB gain was used. The input spikes had voltage from 1mV to 200mV so as not to exceed the output limit, as discussed above. The amplification was measured to be at least 20dB and the results are illustrated in figure 5-1.

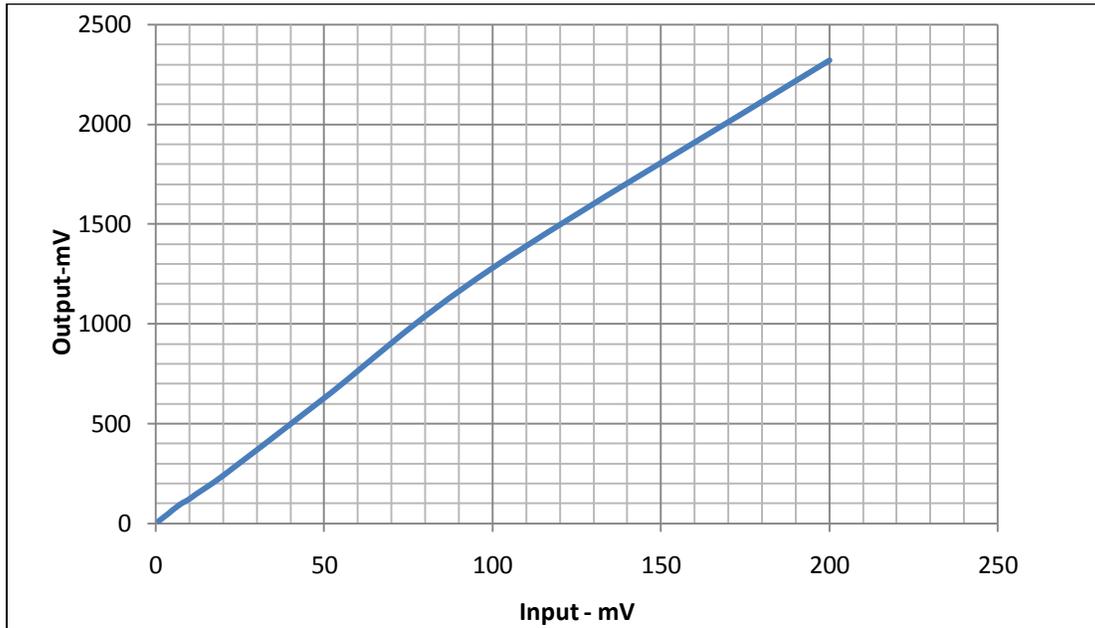


Figure 5-1: Plot of the amplified output of a GALI 52 20dB

As it can be seen from figure 5-1 the amplification is almost linear for the whole range of input values. The test described above was also performed for the GALI 52 40dB (S.N. 00063GALI_AKG), where the range of the input signal was limited to 12 mV in order to limit the maximum output from the amplifier to under 1,5V. The results from these measurements are shown in figure 5-2.

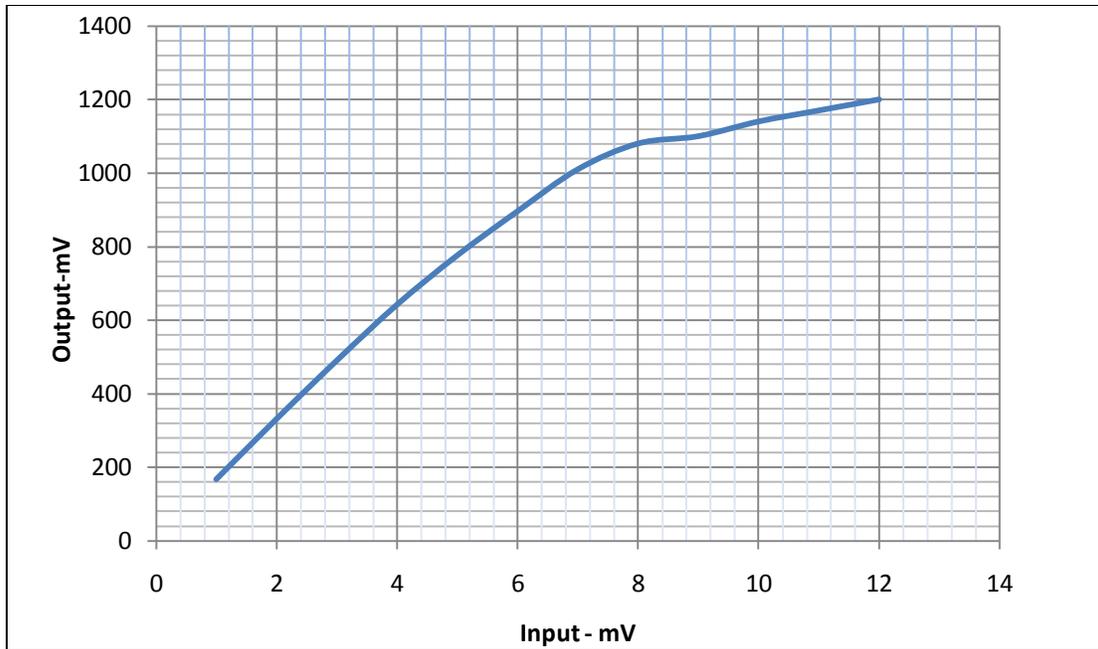


Figure 5-2: Plot of the amplified output of a GALI52 40dB

By comparing figure 5-1 and figure 5-2 it can be deduced that the behavior of the 40dB gain GALI amplifier is not as linear as the 20dB one, for the accepted values of the input signal. In the case of the 40db Gain amplifier, when the output was increased above 1V the amplifier, as expected, was entering its saturation range. The rise time of the input pulses was varying from 2,52ns to 2,92ns, providing a very good input signal for performing the amplification tests. Finally the BCM front-end amplification scheme was tested and measured as the MGA AGILENT 20dB was connected to a GALI52 20dB in order to give a total amplification of 40dB. The rise time was measured to be 1.90 ± 0.02 ns and a plot of the measurements obtained is depicted in figure 5-3.

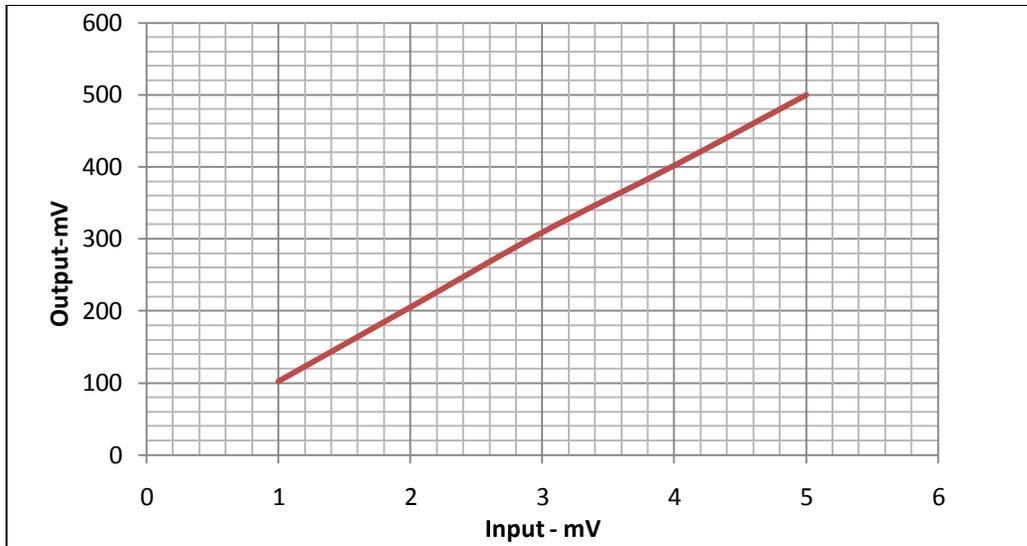


Figure 5-3: plot of the amplified output of the BCM set of amplifiers, in total 40 dB gain

As it can be seen from figure 5-3 the amplification of the signal, considering both amplifiers, is very linear within the entire range of values, proving the excellent performance of the amplifiers currently used in the BCM front-end electronics.

5.3 Front-end schematic and SPICE model

In addition to the tests and measurements mentioned in the previous chapter and the irradiation tests performed, a SPICE circuit simulation was deemed necessary and was performed. The SPICE model was created by the collaborators working on the BCM in order to simulate the input of the amplifiers incoming from the detector modules. This was necessary before ATLAS was in operation but is still important to study the BCM analog electronics and search for implementation improvements. In figure 5-4 the schematic of the BCM front-end system, including the models used for the diamond detectors and the amplification stage, is presented.

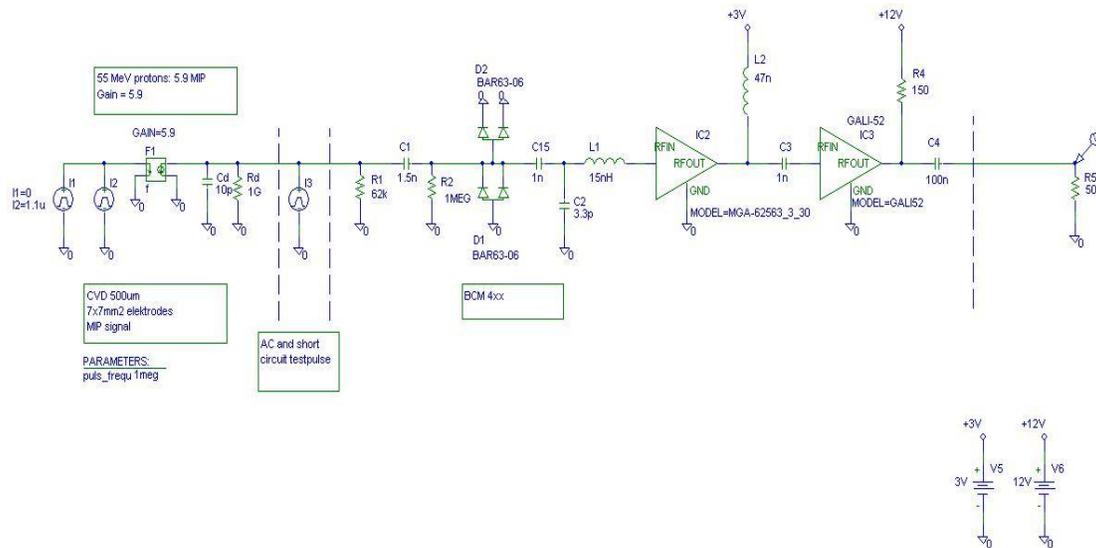


Figure 5-4: Schematic of the BCM front-end electronics designed in SPICE

In the schematic presented in figure 5-4, the left part represents the diamond detectors, simulating the creation of spike pulses similar to the real pulses coming out from the diamond detectors. On the right part, the amplification stage is simulated using custom made models, created specifically for simulating the behavior of the two amplifiers mentioned above. The input pulse fed into the first amplification stage is shown in figure 5-5. The pulse, although not identical to the real one, it does exhibit same main features observed in real pulses.. The rise time of the pulse is very short, the base line restoration is relatively fast and the amplitude is within the same levels. The fact that the output from the amplification stage is similar in SPICE and in reality proves that in the input pulse used in SPICE is adequate to use in further simulation runs.

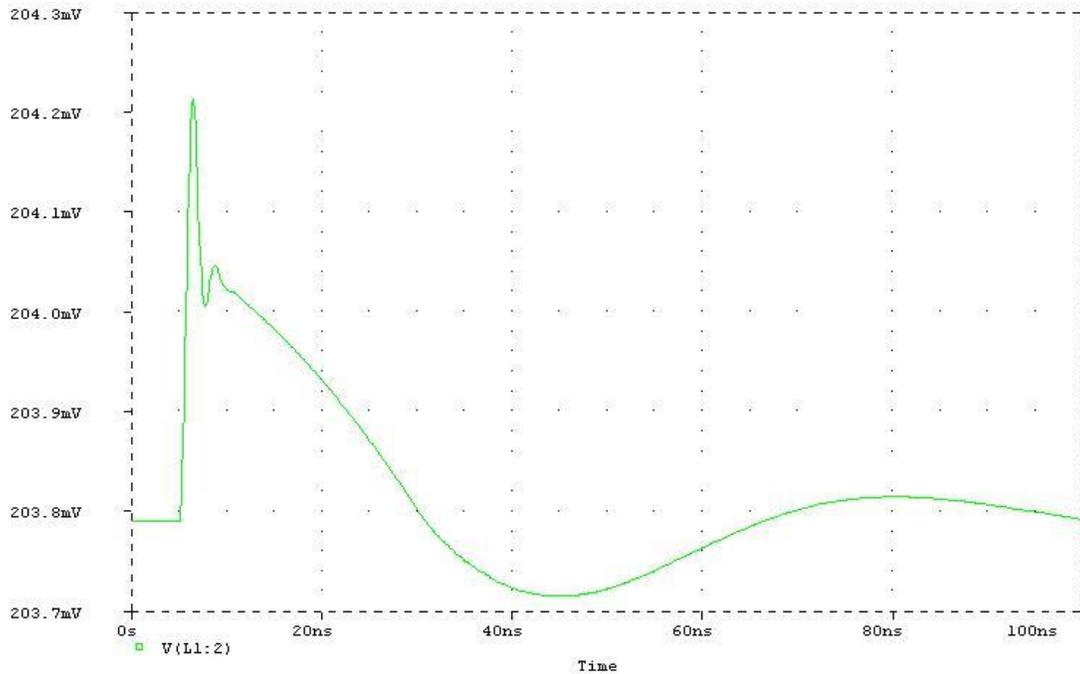


Figure 5-5: Input pulse as it is fed into the first stage MGA AGILENT amplifier

The output of the front-end analog part, as it is simulated in SPICE is shown in figure 5-6. The rise time of the output is very short and the baseline restoration is much faster than that of the input pulse. However, an overshoot can be observed towards the end of the falling edge of the pulse. This is due to the sensitivity of the SPICE amplifier model to the small second spike observed in the input pulse. The SPICE models of the amplifiers also exhibit an increased sensitivity to the amplification of the falling edge and the baseline restoration of the pulse.

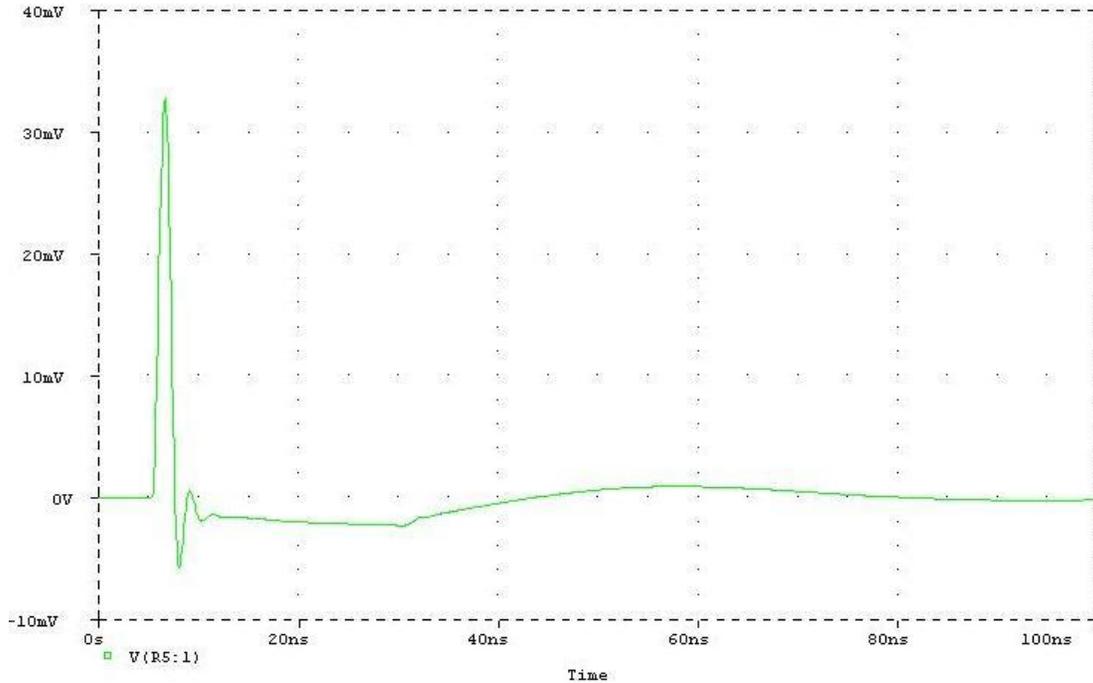


Figure 5-6: Output of the front-end analog part SPICE simulation

5.4 Pulser circuits and SPICE simulation

During operation the front-end analog electronics receive signals from the detector modules, which in turn are sent amplified into the next system on the BCM chain. However, when ATLAS is not operating and there is no beam, the front-end electronics are inactive. A lot of tests and calibrations in all the BCM subsystems are needed to be performed using the pulser, as discussed in chapter 4. In order to operate the front-end electronics even when there is no beam and produce pulses in all BCM channels is to use a pulser circuit before the amplification stage. This provides pulses that pass through all the BCM subsystems, thus allowing to test and calibrate the whole BCM system, simulating accurately normal operation.

SPICE was used in order to simulate 3 different pulser circuits that could potentially be used as mentioned above. In all these cases the idea is that a very fast square pulse generator will be used and the signal will be passed through a differentiator circuit

that would output derivatives of the initial input signal thus creating the spike pulse needed.. This pulser system should be fast enough and able to create pulses similar to the real pulses coming from detectors during operation. Moreover, it should be radiation hard as it would be placed inside the copper boxes 5cm from the beampipe.

5.4.1 Active differentiator with operational amplifier

The first pulser system to be discussed is an active differentiator made using an operational amplifier. The resistor placed at the loop of the amplifier and the capacitor at the inverting input (as shown in figure 5-7) yield the following equations:

$$I = C \frac{dV}{dt} \quad (5.1)$$

Equation 5.1 is the relation of voltage in respect to the current in a capacitor. V in equation 5.1 represents V_{in} of the amplifier shown in figure 5-7. The output voltage V_{out} is related to the current I as given from Ohm's law:

$$I = \frac{V_{out}}{R} \quad (5.2)$$

Combining the equations 5.1 and 5.2 we have the equation 5.3 for the amplifier circuit operating as differentiator:

$$V_{out} = RC \frac{dV_{in}}{dt} \quad (5.3)$$

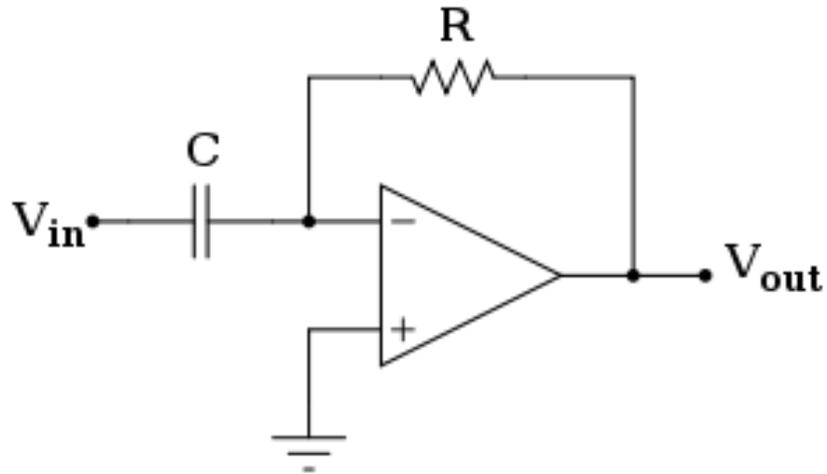


Figure 5-7: Circuit schematic of a differentiator using operational amplifier

In this circuit we input a wide square pulse with rise and fall time of 1 ns created by a SPICE pulse generator. The expected output of this circuit is two very short spikes, from which the first one is positive pulse similar to the diamond detector output pulses. In figure 5-8 the schematic of the differentiator and the pulse generator connected to the BCM front-end amplifiers is illustrated. The inductance and the capacitors before the amplifiers were included so that the response of the amplification stage remained unchanged. The values of the differentiator capacitor and resistance were set to values that would minimize the fall time and the baseline restoration without creating distortion to the incoming signal.

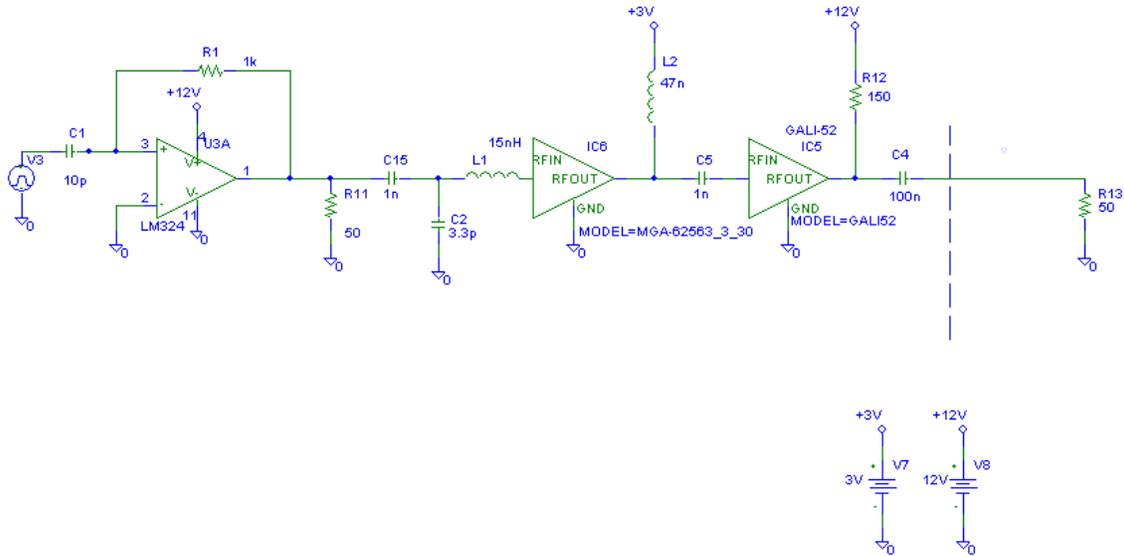


Figure 5-8: Circuit schematic of the differentiator connected to the BCM front-end amplifiers

As amplifier a LM324 low power operational amplifier was selected, whose model was already included within SPICE libraries. The square pulse used as input to the differentiator circuit is shown in figure 5-9. It is a square pulse of width 200ns, amplitude 2mV and rise and fall times 1ns.

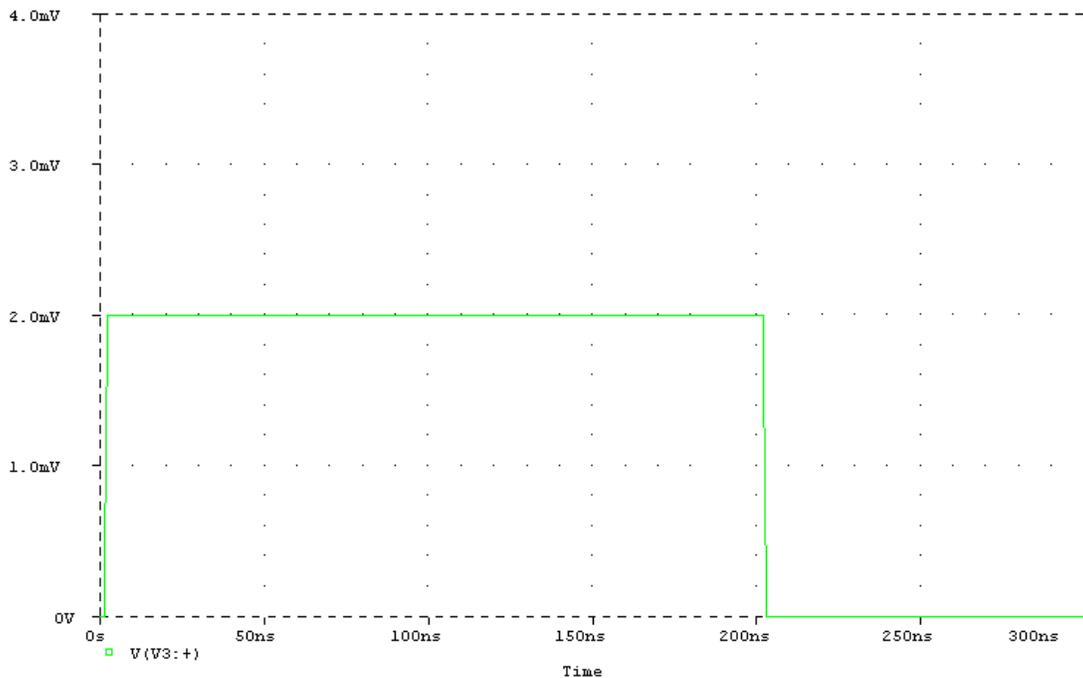


Figure 5-9: Input pulse from the pulse generator to the differentiator circuit

The output of the differentiator is shown in figure 5-10. Only the positive spike is illustrated, since it is the only one needed for the purposes of these simulations. Although the pulse has a desirable short rise time, the fall time is not as short. However this does not present a problem, as discussed in the previous paragraphs, since the BCM amplifier the inductors and capacitors placed before the amplifiers are able to compensate for the longer fall time. A small second spike is also observed, created by the small capacitance used as compensation for the expected longer fall time.

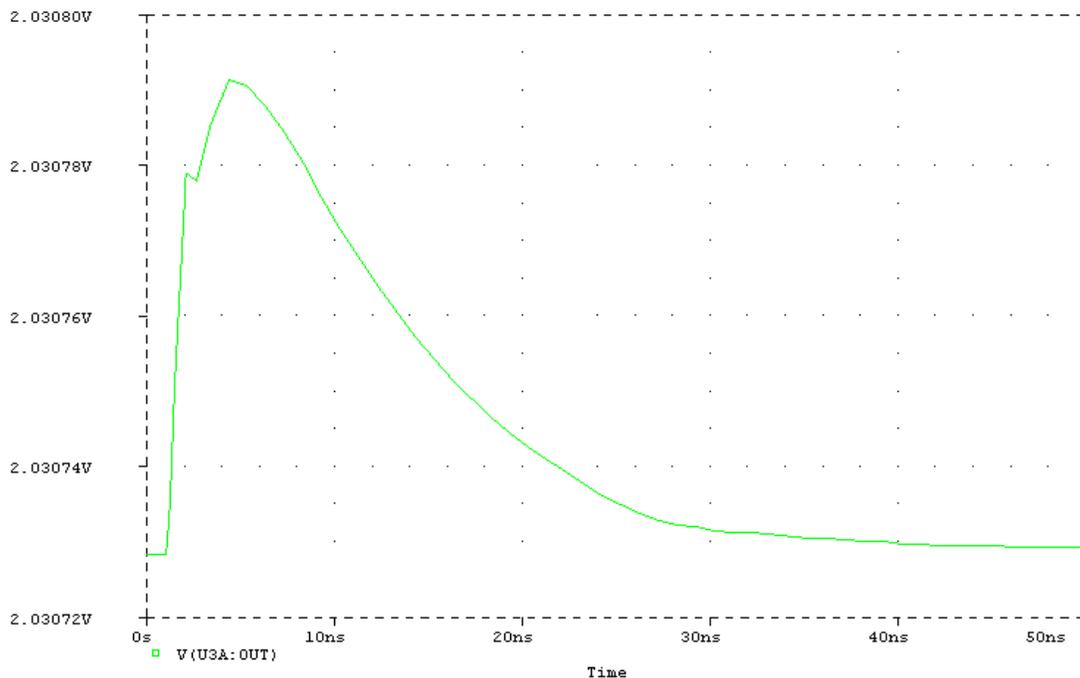


Figure 5-10: Output of the differentiator circuit

The voltage offset of the pulse is close to 2 V, however the capacitor before the amplification stage will cut-off that DC offset. The pulse before the first amplifier and at the output of the whole BCM amplification system is illustrated in figures 5-11 and 5-12 respectively. In those figures it can be seen that the curve of the pulse is smoothed and that the fall time is reduced.

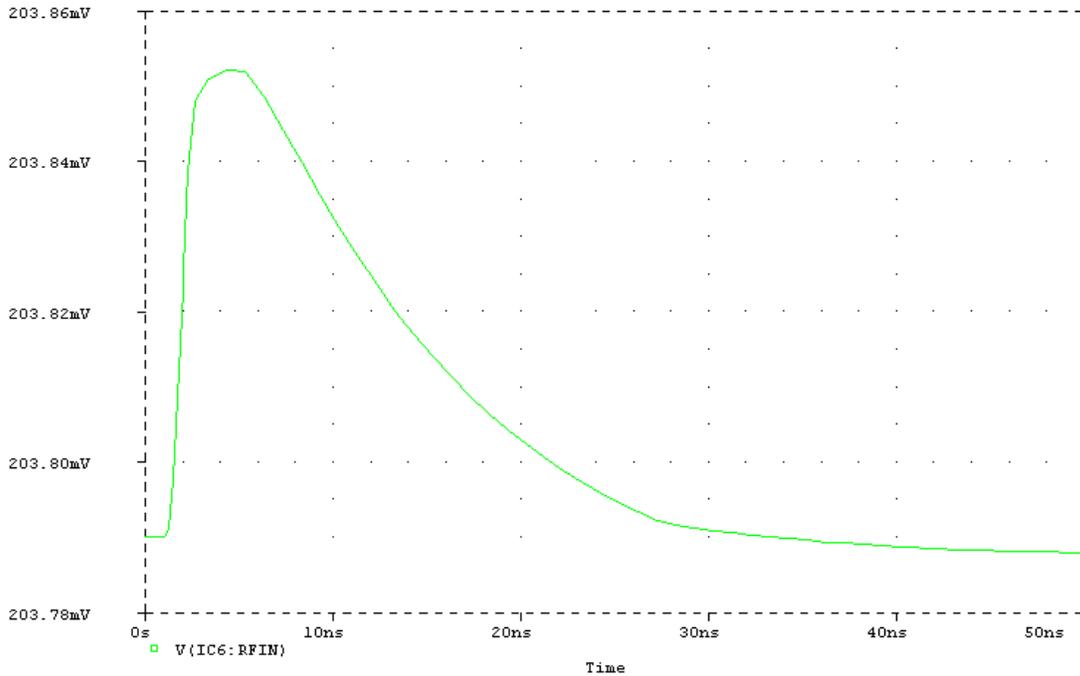


Figure 5-11: Pulse just before the Agilent first stage amplifier

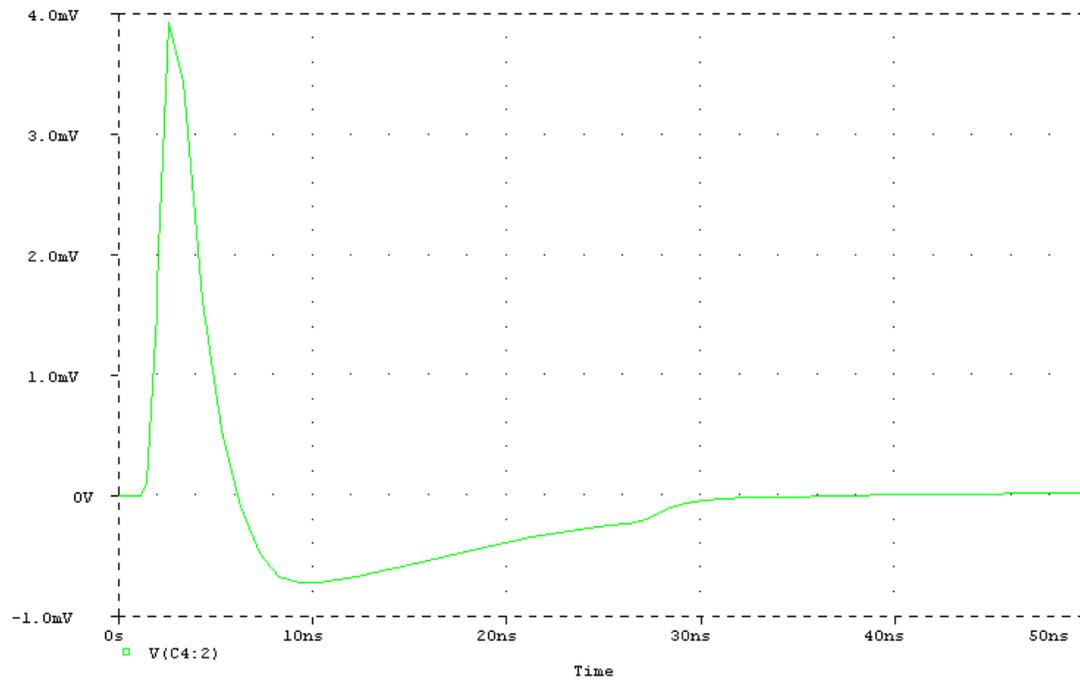


Figure 5-12: Output pulse after the 2 stages of amplification

The output pulse has low amplitude, as expected since the input pulse also has a very low amplitude as it has been defined by the pulse generator. The rise time of the pulse

is very small and the overshoot within normal levels. Finally, the baseline restoration is also fast and the curve is smooth with no secondary spikes.

The advantage of this circuit is that, due to the amplifier, the resulting curve is very smooth and linear in respect to curves resulting from other differentiator circuits. Furthermore the system is not affected by the capacitors and the inductors before the BCM amplifiers as much in other differentiator circuits. However, the use of the amplifier as shown here has also disadvantages, since the amplifier has a slower response and it is difficult to be made radiation tolerant. In the next two paragraphs passive circuits that are not based on amplifiers will be discussed.

5.4.2 Passive differentiator using a capacitor

In this differentiator circuit only a capacitor and a resistor, coupled to the ground, are being used. This circuit also fulfills the role of a first order high pass filter.

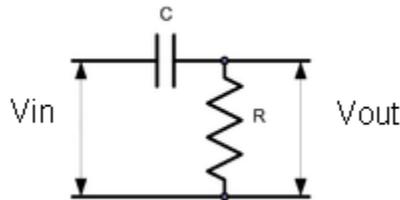


Figure 5-13: A RC passive differentiator circuit

The transfer function of the circuit is:

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1 + (1/R\omega C)^2)^{1/2}}, \quad \text{where } \omega = \frac{1}{RC} \quad (5.4)$$

The schematic of the circuit is illustrated in figure 5-13 and the values of the parameters are set to 30pF and 1KOhm, found through trial and error to be the best combination in order to create the necessary pulse.

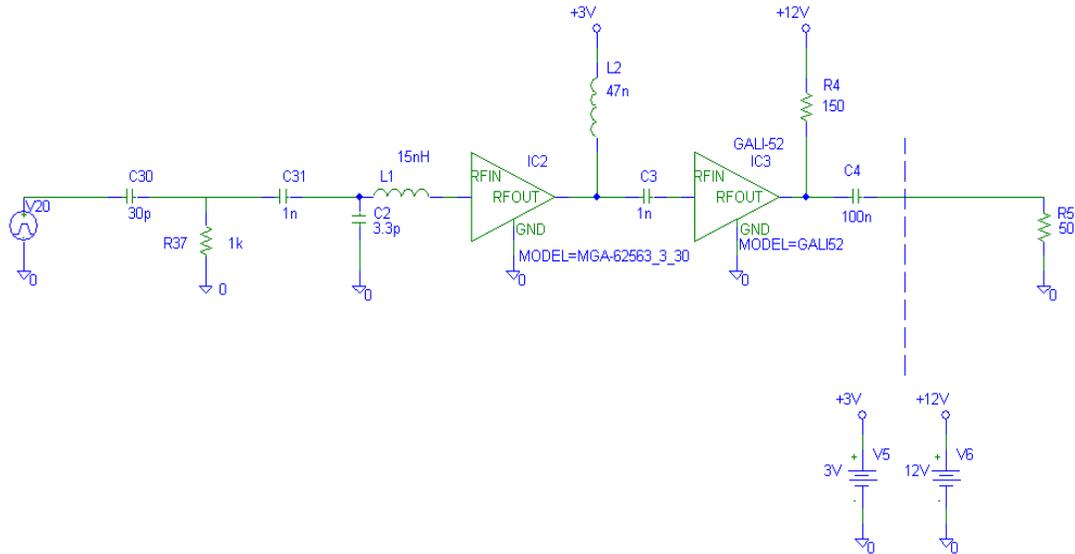


Figure 5-14: Circuit schematic of the capacitor based passive differentiator

In this differentiator circuit, the capacitors and the inductors have a strong influence to the response of the system. The pulse is much more distorted and it is similar to the pulse the SPICE model used for the diamond detectors, as shown in figure 5-5. The output of the differentiator with the same input pulse can be seen in figure 5-14 and it is can be seen that the curve is not as smooth as in case presented above, where the circuit uses an operational amplifier. The fall time of the pulse is not so short and the baseline restoration is not within acceptable limits. The output of the BCM amplifiers is also similar to the output of the BCM model as that is shown in figure 5-6. The output pulse has a smooth curve, with the only disadvantage being its relatively high overshoot, as this illustrated in figure 5-15.

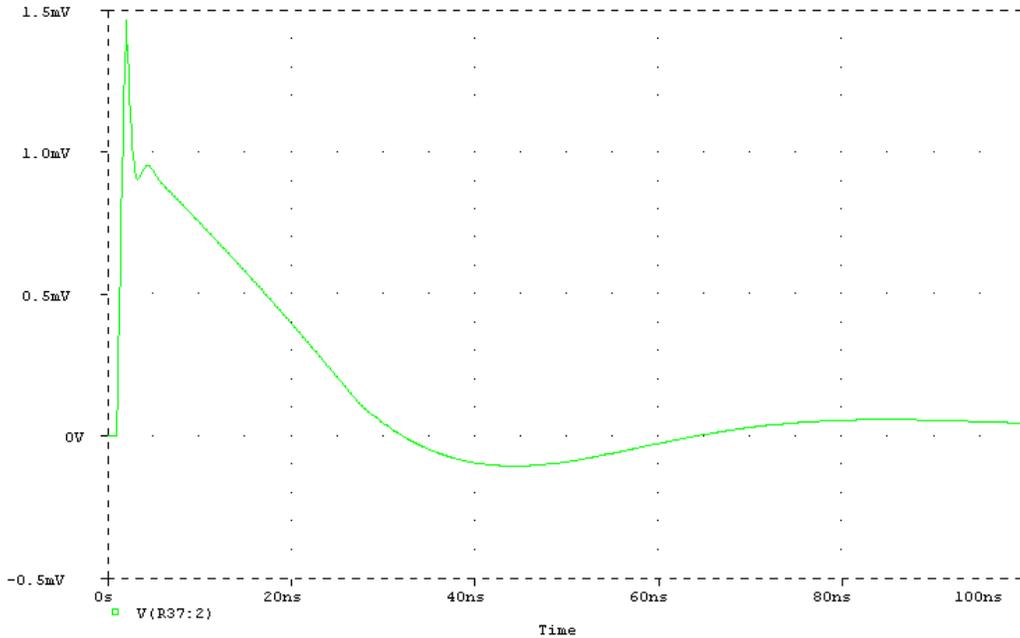


Figure 5-15: Output pulse of the differentiator circuit using capacitor

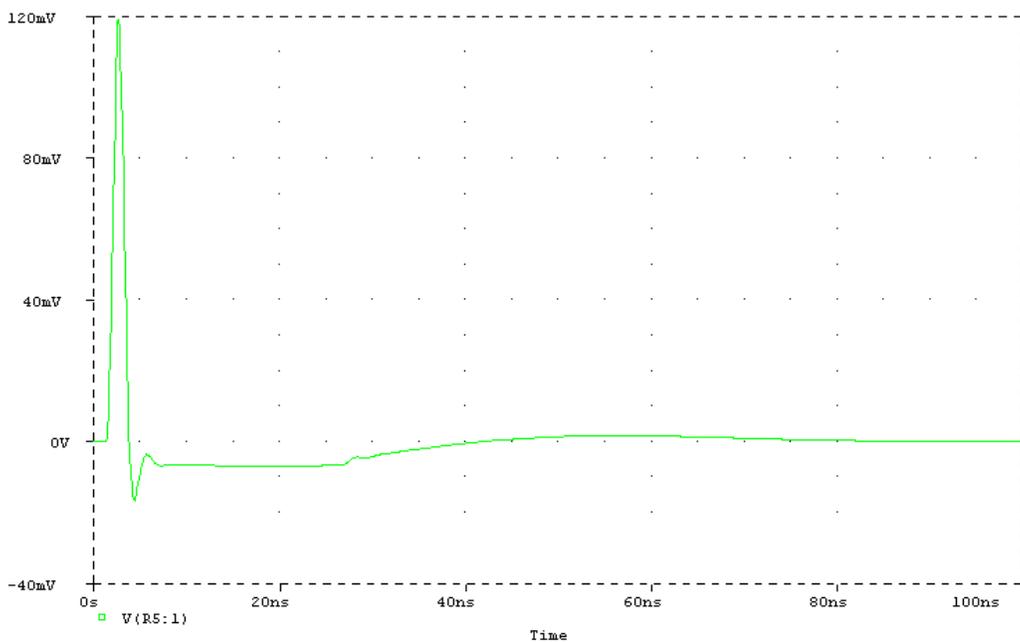


Figure 5-16: Output pulse after the 2 stages of amplification

It is noteworthy that the amplitude of the output pulse is very high in respect to the previous circuit, and that is due to the fact that the resistor is coupled to the ground and the impedance of the capacitor is low. The advantage of this circuit is in the fact that no amplifier is being used and it can be made radiation hard with relative ease.. The

disadvantages, however, as discussed above are that the output pulse curve is not as smooth and the restoration in the falling edge is very slow.

5.4.3 Passive differentiator with use of inductance

The last circuit to be discussed is a passive differentiator using an inductor. The response of the system is illustrated in figure 5-17.

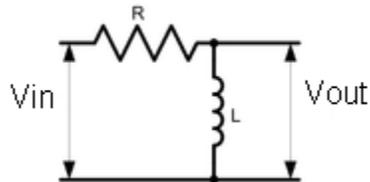


Figure 5-17: A RL passive differentiator circuit

The transfer function for this circuit is:

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1 + (R / \omega L)^2)^{1/2}}, \quad \text{where } \omega = \frac{R}{L} \quad (5.5)$$

The schematic of the circuit is illustrated in figure 5-16. The values were set as $R=50$ Ohm and $L=1\mu\text{H}$, found through trial and error in order to produce a fast response and low oscillation in the pulse amplitude.

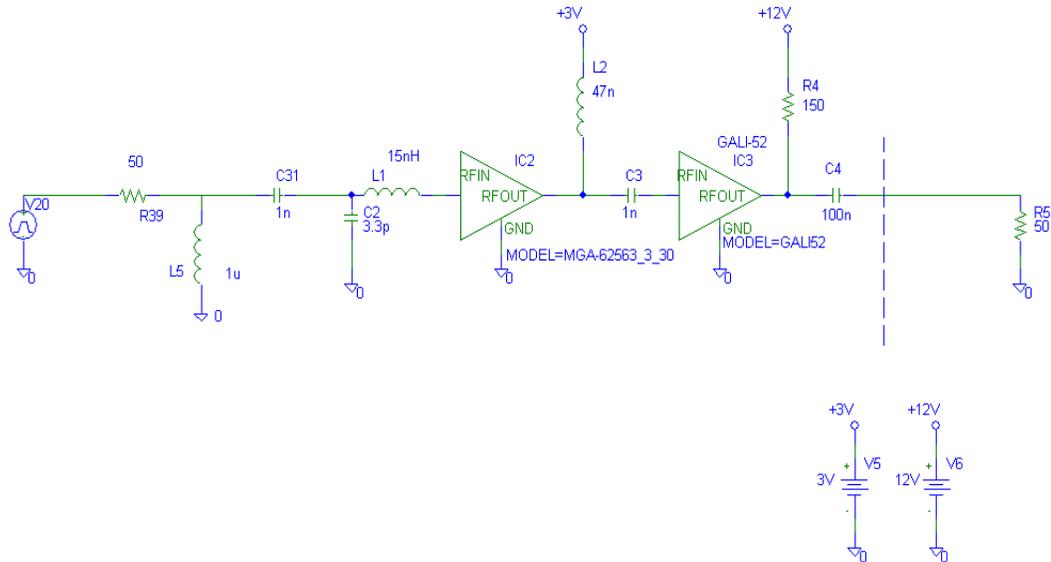


Figure 5-18: Circuit schematic of the inductance based passive differentiator

This circuit is heavily influenced by the inductor and the two capacitors that follow it. Amongst the circuits tested and presented in this these, this is the one with the largest falling time. Any attempt reducing the falling time resulted in heavy distortion of the pulse. The input pulse is the same to the previous tests and the output pulse is illustrated in figure 5-19.

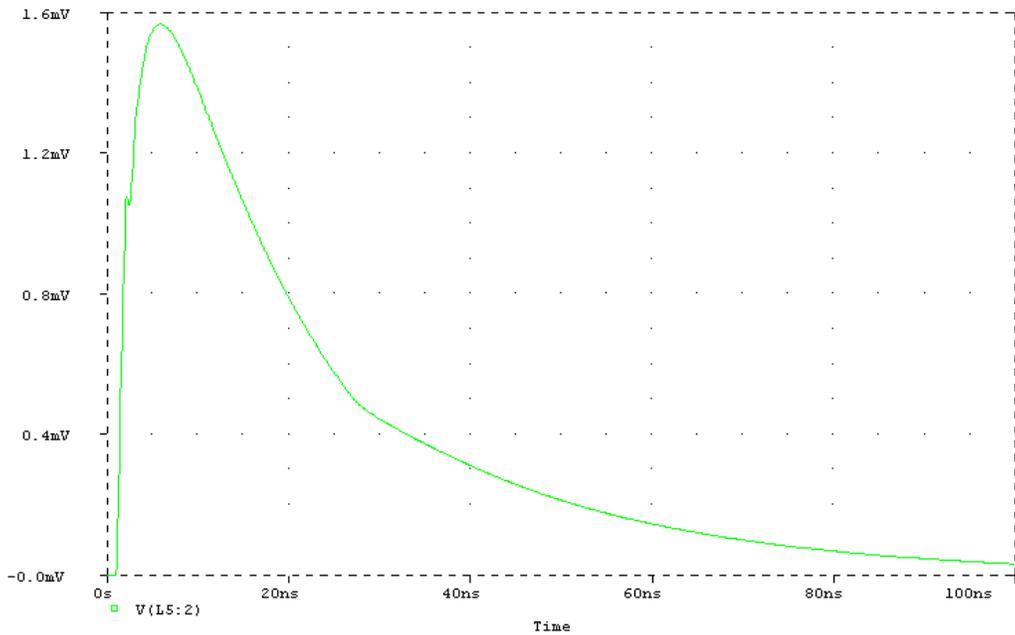


Figure 5-19: Output pulse of the differentiator circuit using inductance

It can be seen from figure 5-19 that the falling time is far bigger than the encountered in previous circuits. The curve of the pulse is smooth except for a small secondary spike within the rise time. The output of the entire circuit is shown in figure 5-20.

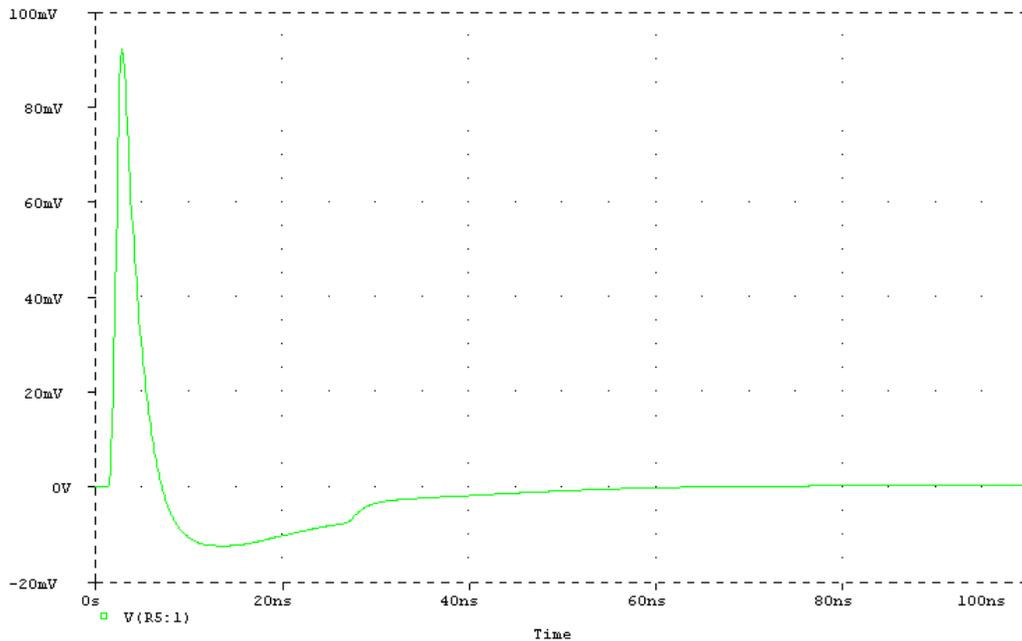


Figure 5-20: Output pulse after the 2 stages of amplification

The output signal has a very small rise time and the overshoot within acceptable limits. The baseline restoration and falling times are reduced as well compared to previous circuits. The advantages of the RL circuit are: a) it can become radiation hard with relative ease (not using an operational amplifier) and b) it exhibits low impedance. However its disadvantages are: a) unstable baseline restoration as well as b) large falling of the baseline restoration time on the circuit output pulse.

In all the aforementioned differentiator circuits a pulse generator is used to produce the input pulse. This pulse generator fulfills the timing requirements presented earlier, of which the very short rise time is the most important one. Moreover, the pulse generator should be radiation hard, as in reality it would be placed very close to the beam pipe. It is

also noteworthy that any discussion or proposal for improvements in the BCM front-end part has to take into account the fact that no intervention inside the Inner Detector is planned for the following years.

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[ISE] Iseg Spezialelektronik GmgH, D-01454 Radeberg/OT Rossendorf Germany.

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Appendix A

Trigger adder test plots

In this appendix the trigger adder test plots are presented in order to provide a more detailed outlook on the trigger adder operation.

Tests with asynchronous LHC CLK

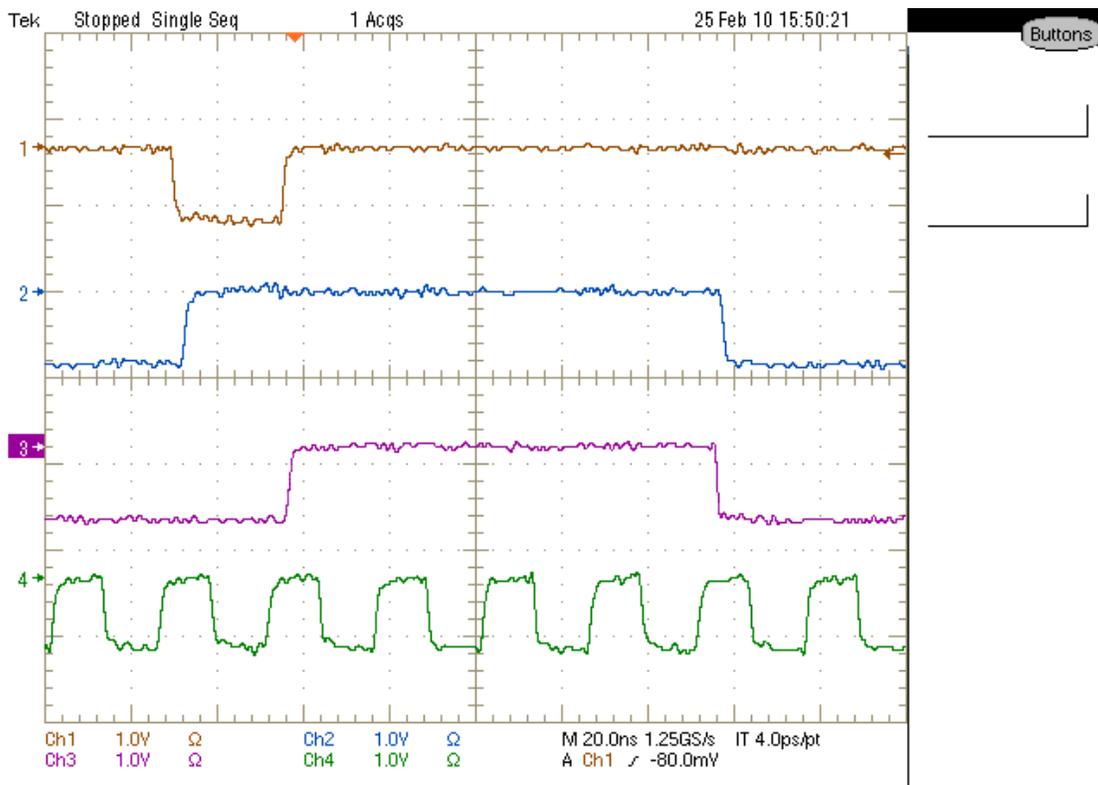


Figure A-3: A 3+3 result with wrong output at the first BC due to asynchronous inputs

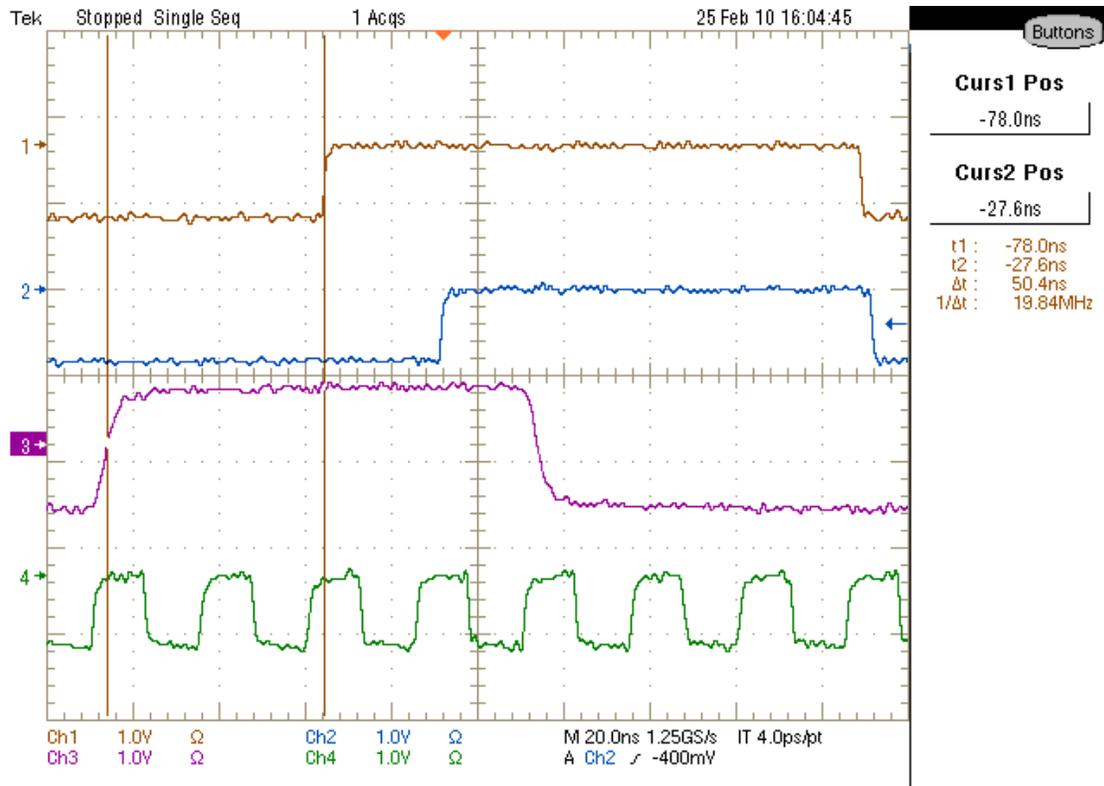


Figure A-2: Delay between the input (channel 3) and the outputs

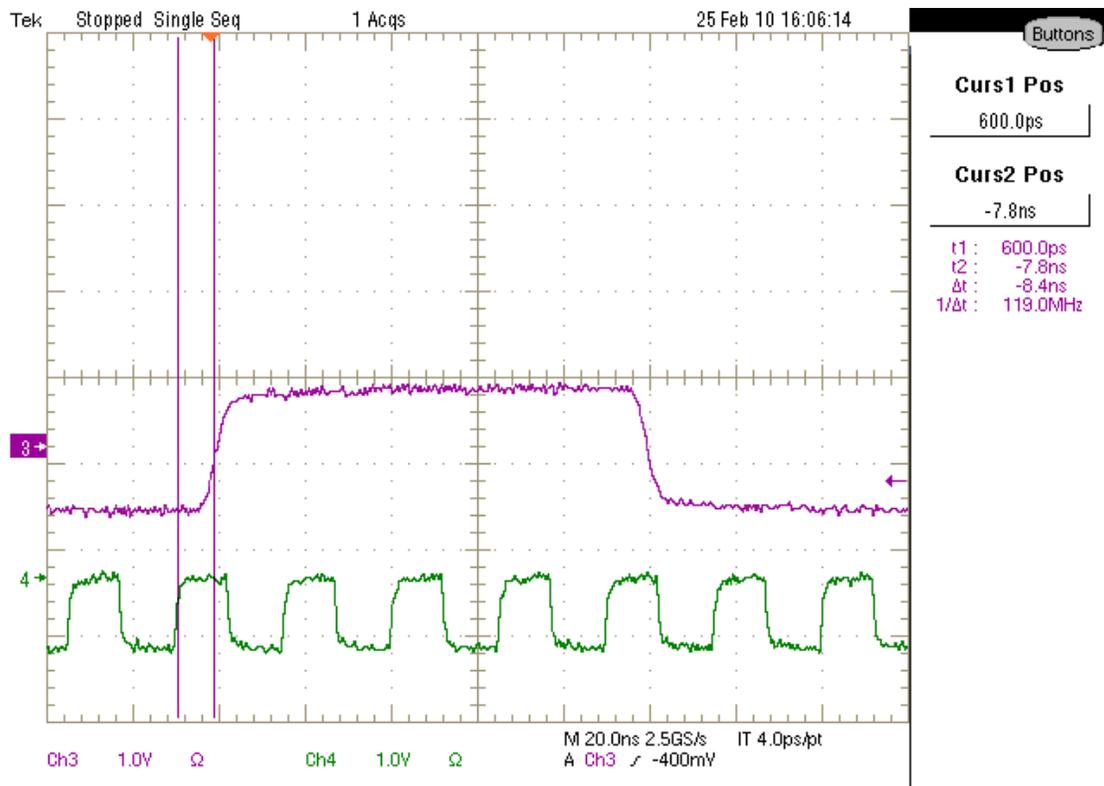


Figure A-3: A Input pulse-CLK delay different to the one shown in figure 3-5

Tests with synchronous 10MHz CLK

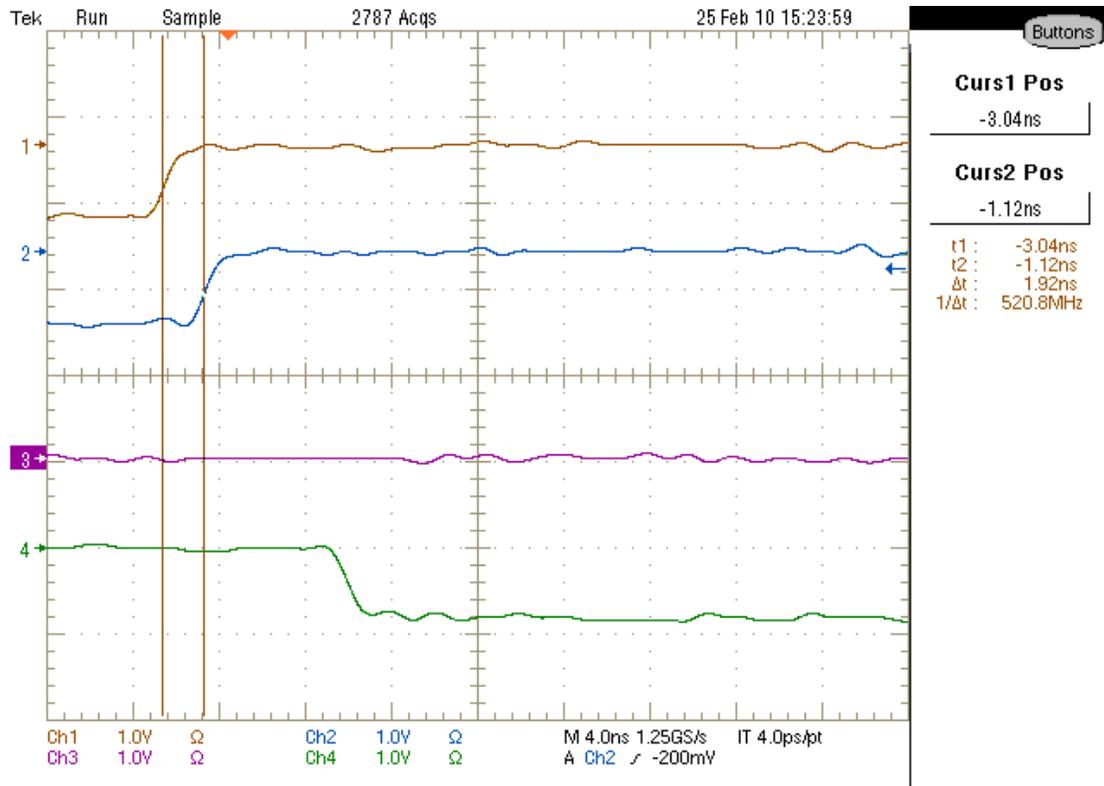


Figure A-4: Delay between the inputs due to different cable lengths

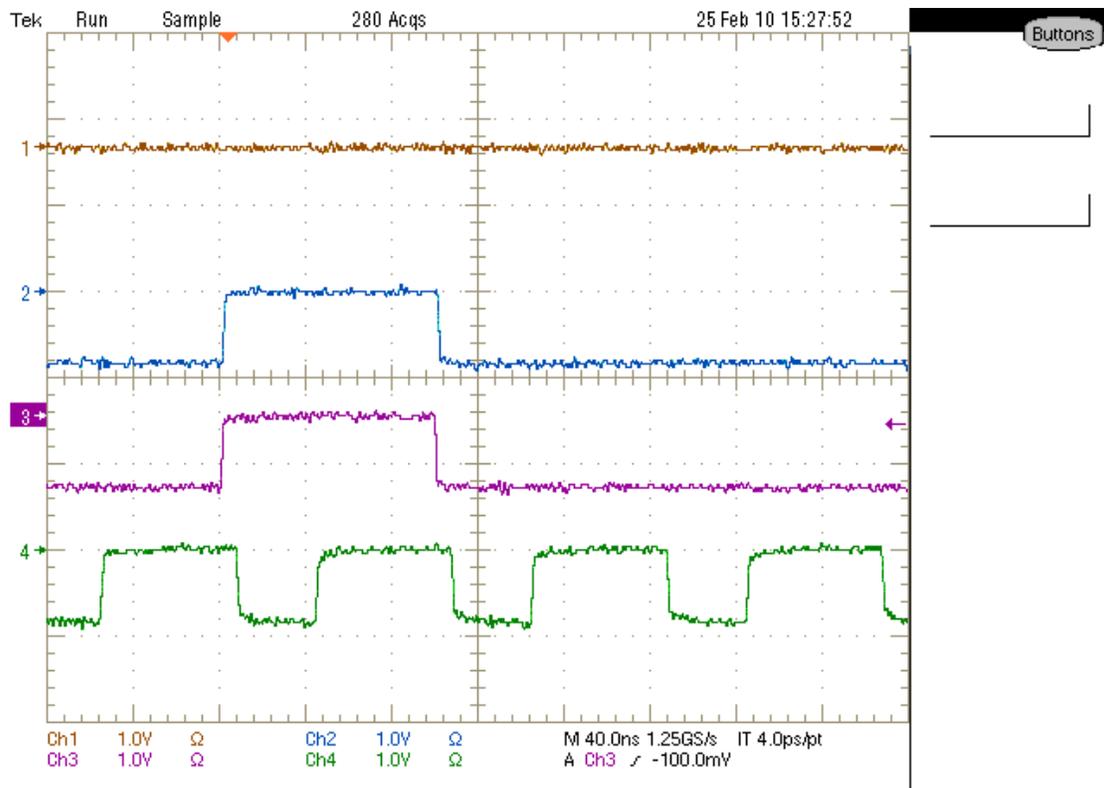


Figure A-5: A 3+3 result with the outputs in phase with the CLK falling edge

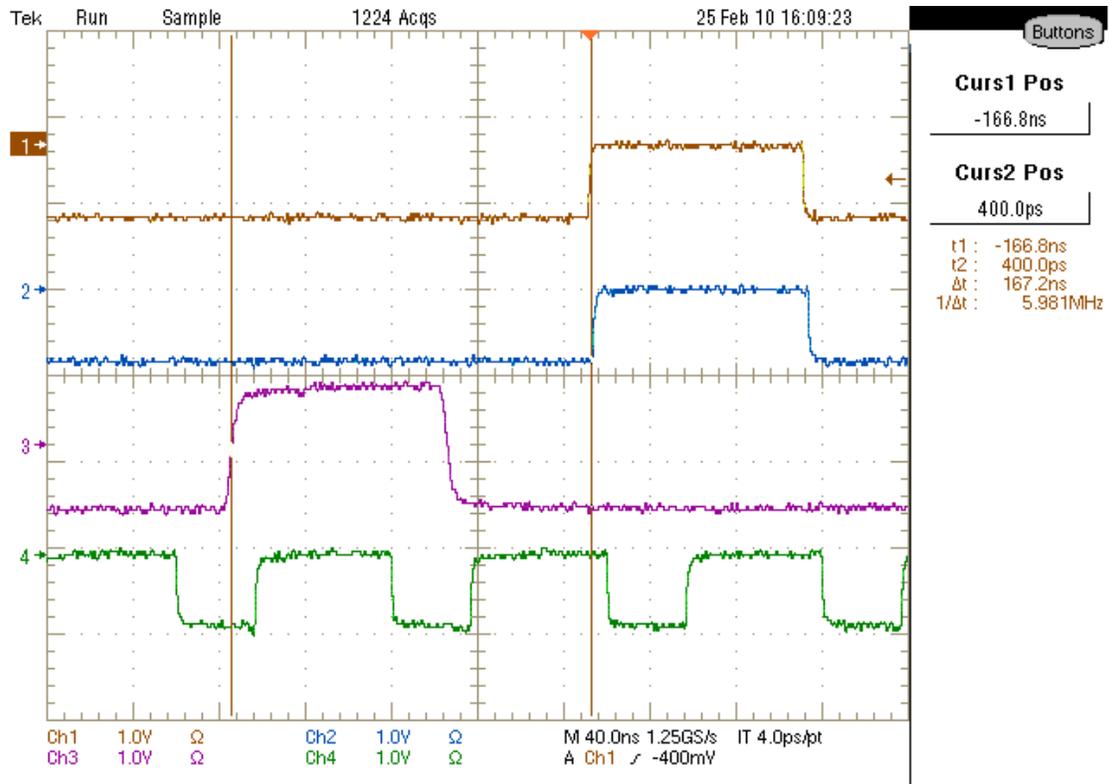


Figure A-6: Delay between the input (channel 3) and the outputs

Tests with synchronous 40MHz CLK

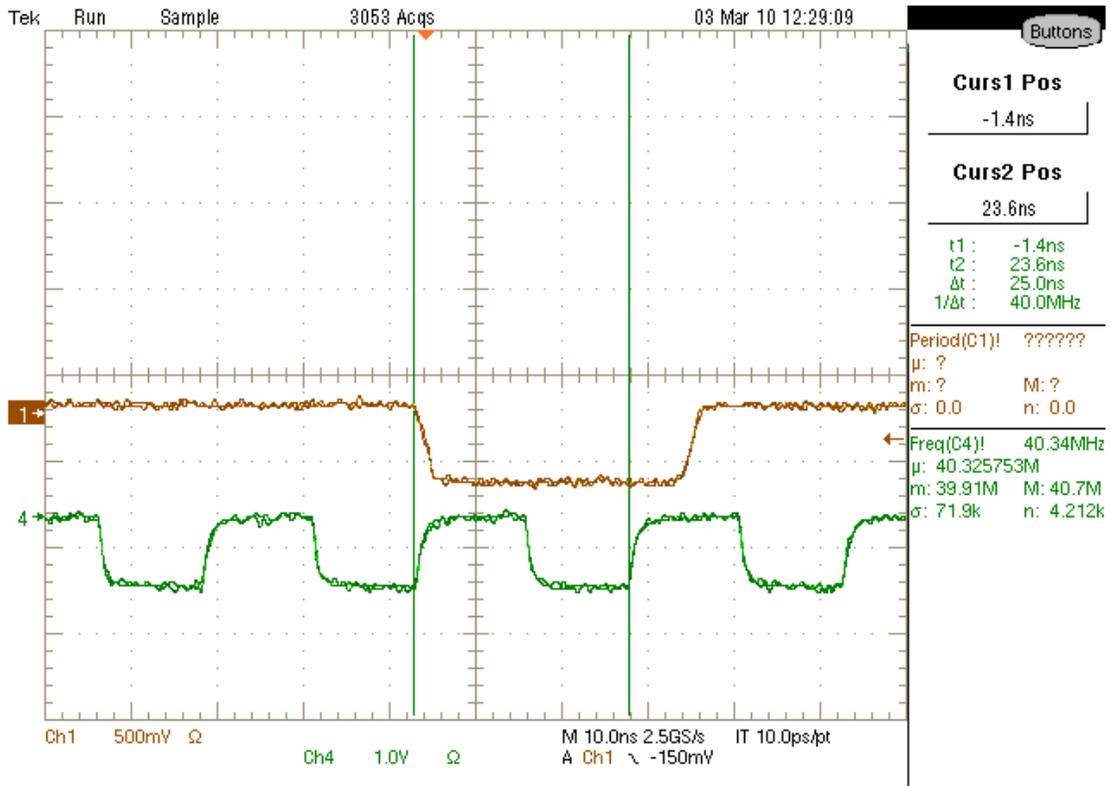


Figure A-7: The 40 MHz CLK in phase with the rising edge of the input pulse

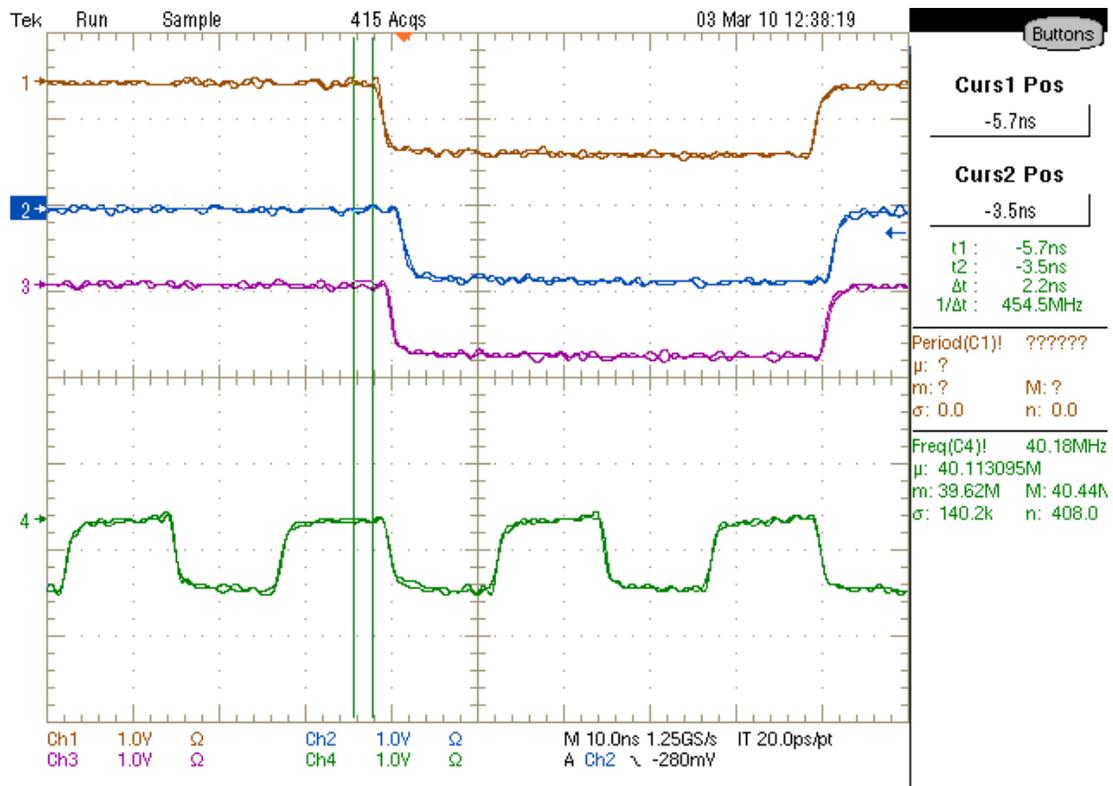


Figure A-8: Output of the board when at least one high-threshold input is high

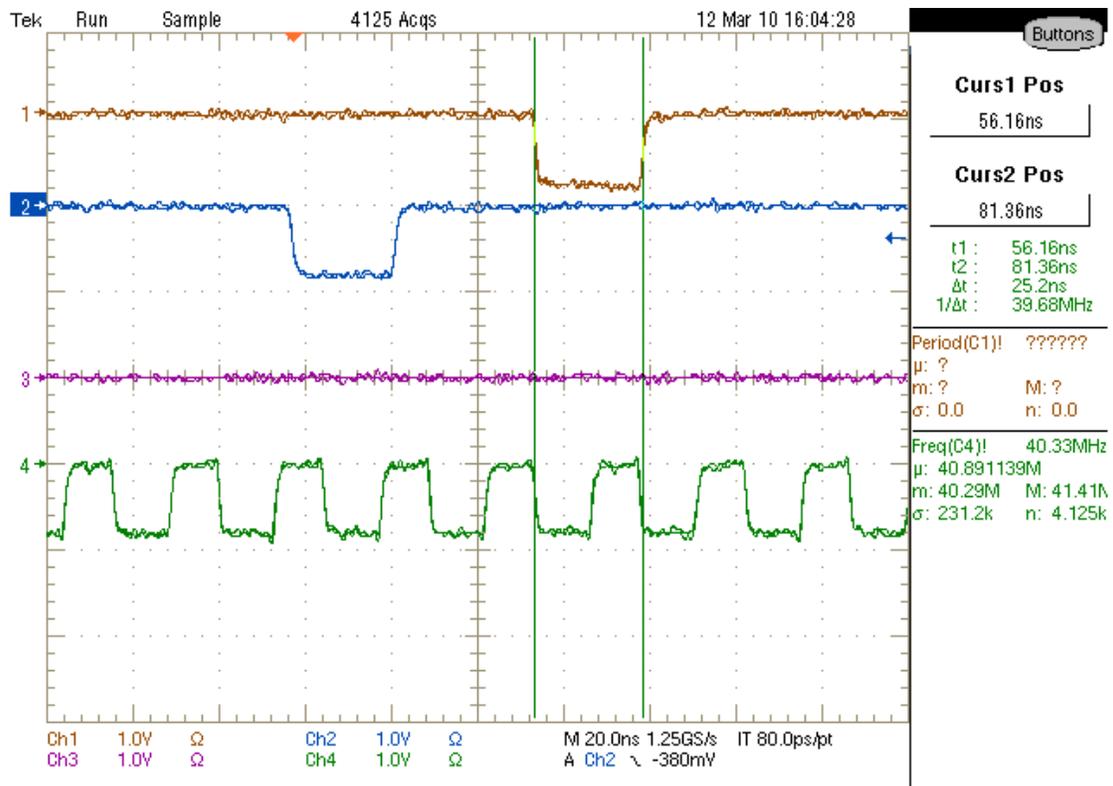


Figure A-9: 25.2 ns width of an output pulse

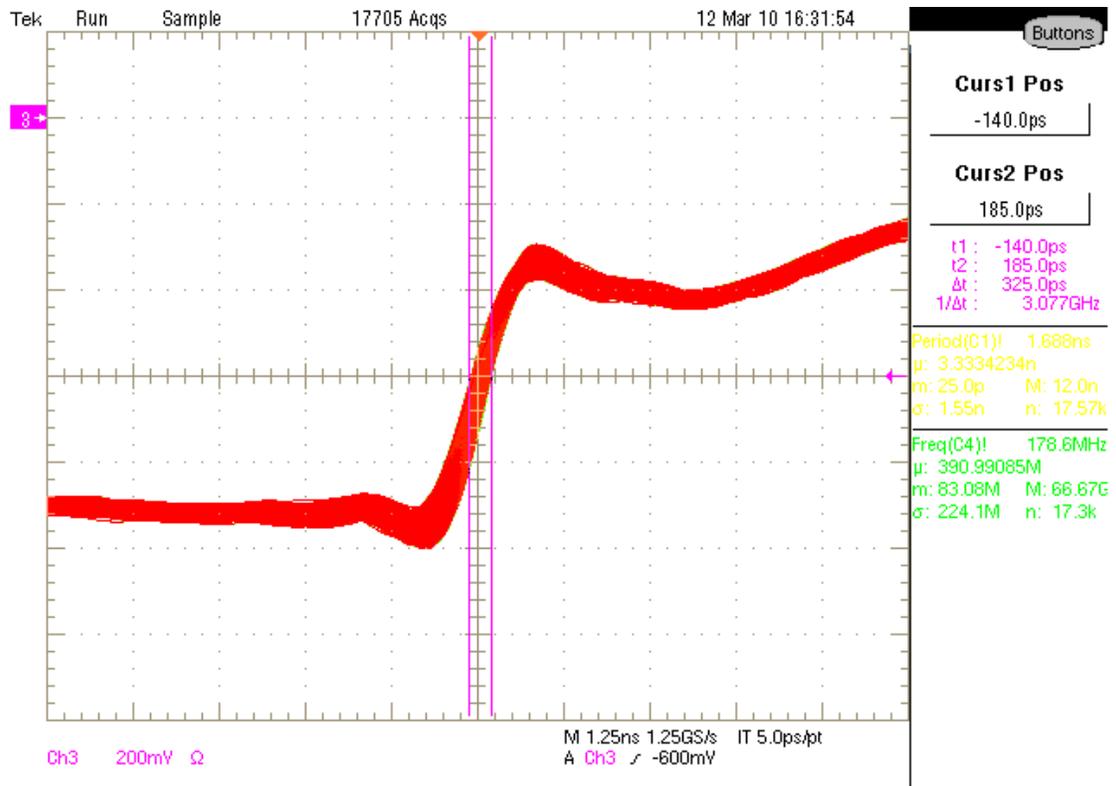


Figure A-10: Jitter of the oscilloscope used

Appendix B

Beam abort algorithms tests

In this appendix the beam abort algorithms' test plots are presented in order to provide a more detailed outlook on the operation of the algorithms

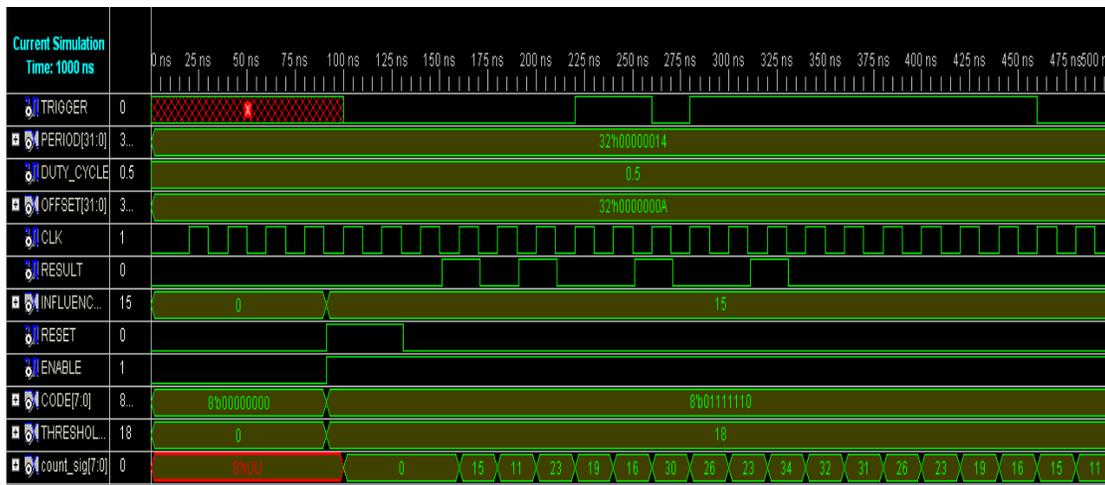


Figure B-1: Test of the FF algorithm with CHIPSOCPE fires a beam abort signal as shown in TRIGGER signal

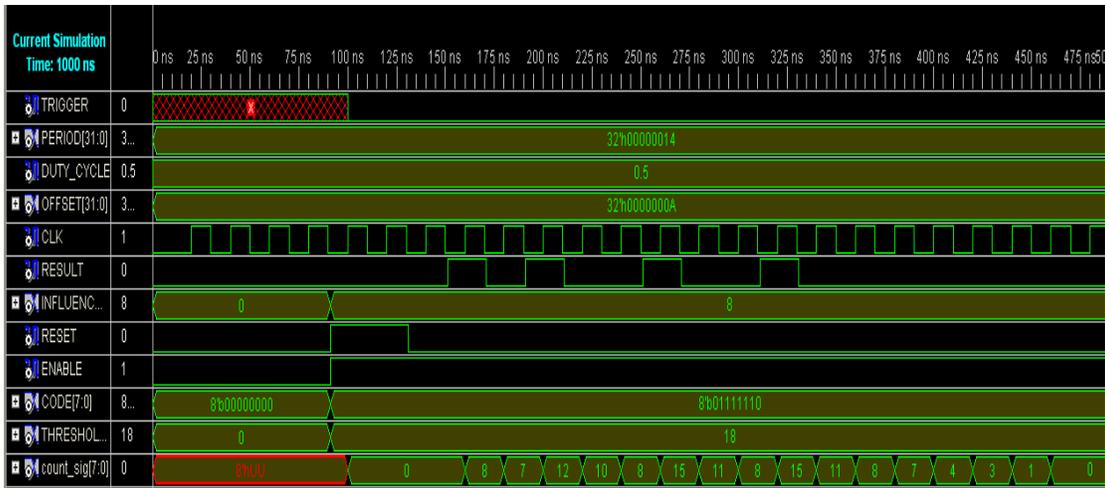


Figure B-2: Test of the FF algorithm with the same pattern as in figure B-1 but different parameter values does not fire a beam abort

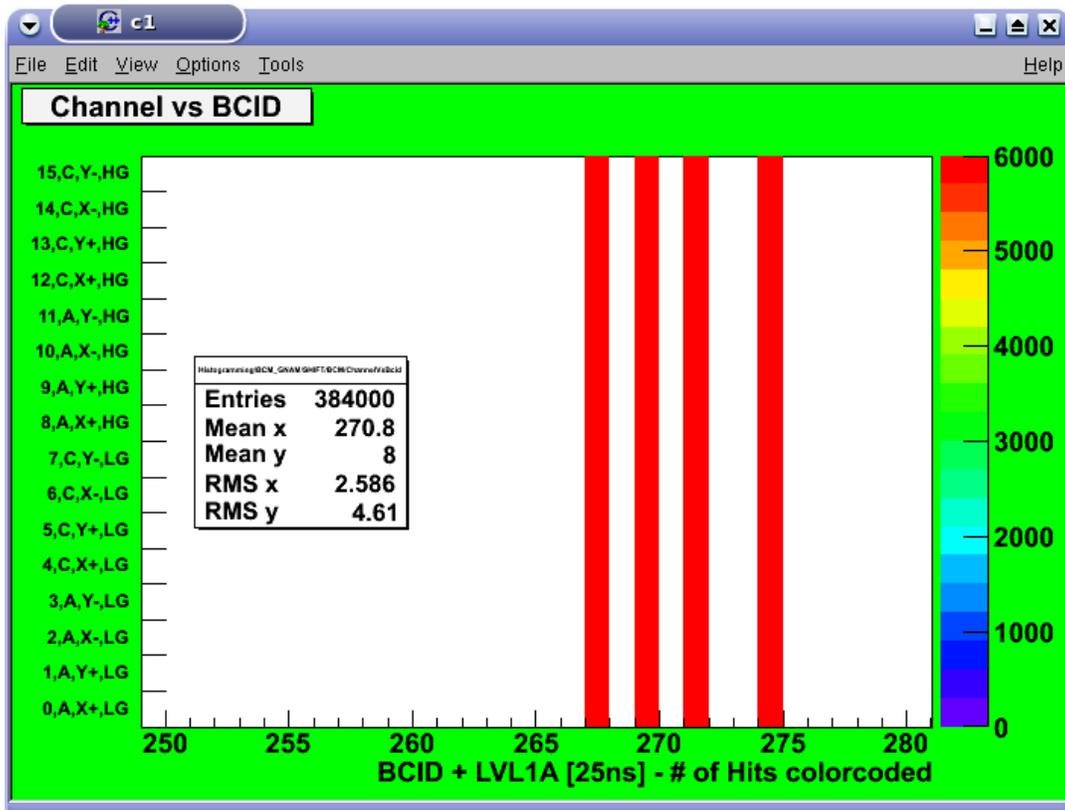


Figure B-3: Pulsar run pattern that fired a beam abort monitored in the OHP BCID window

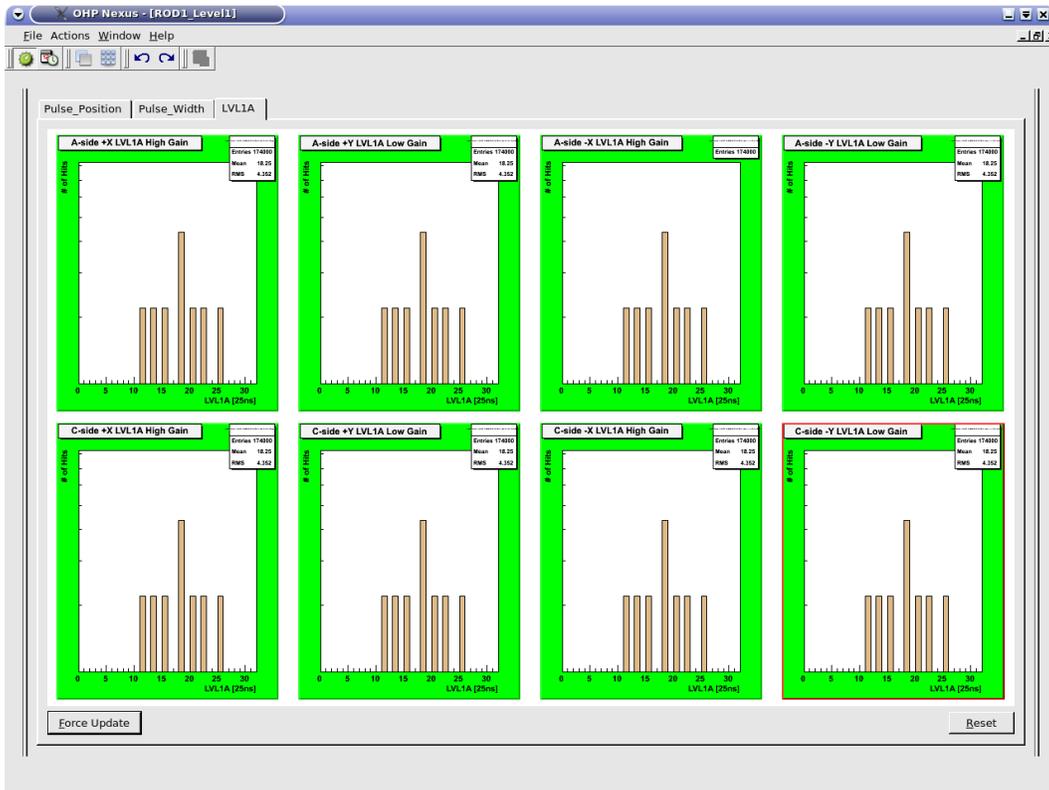


Figure B-4: The same pattern as in figureB-3 monitored in the OHP trigger window. The patterns is doubled as the L1A triggers twice for the pattern

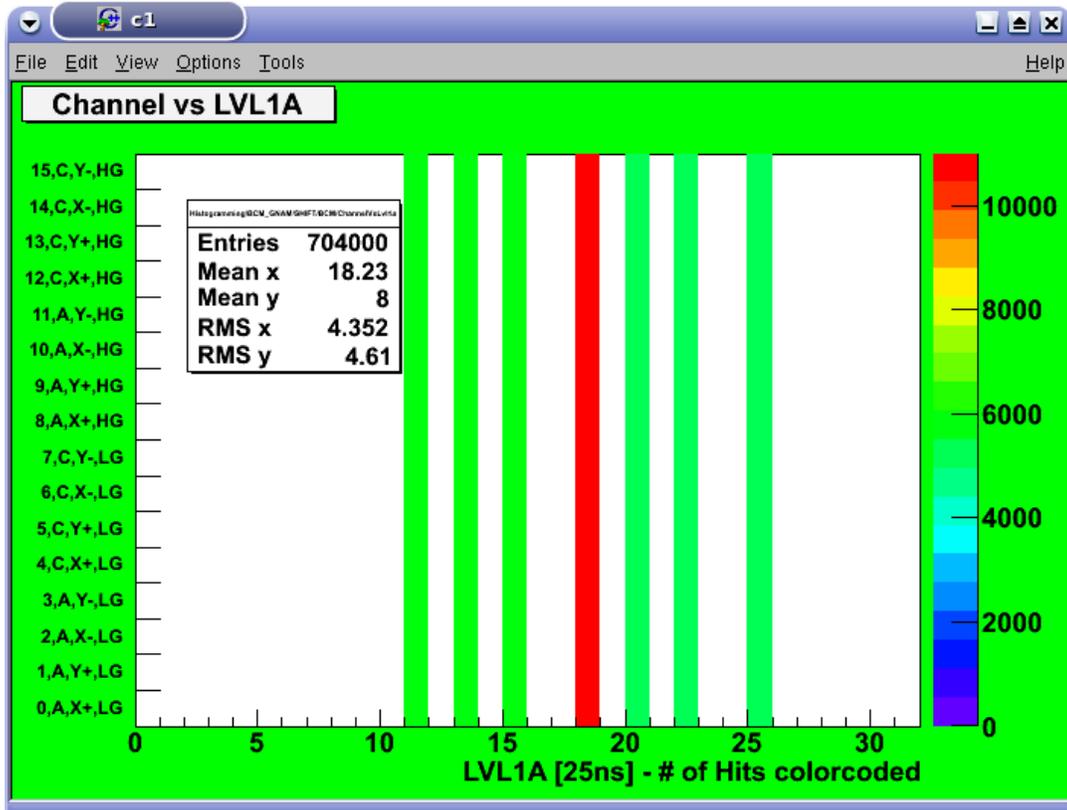


Figure B-5: Pattern that fired a beam abort monitored as double pattern in the OHP LV1A window

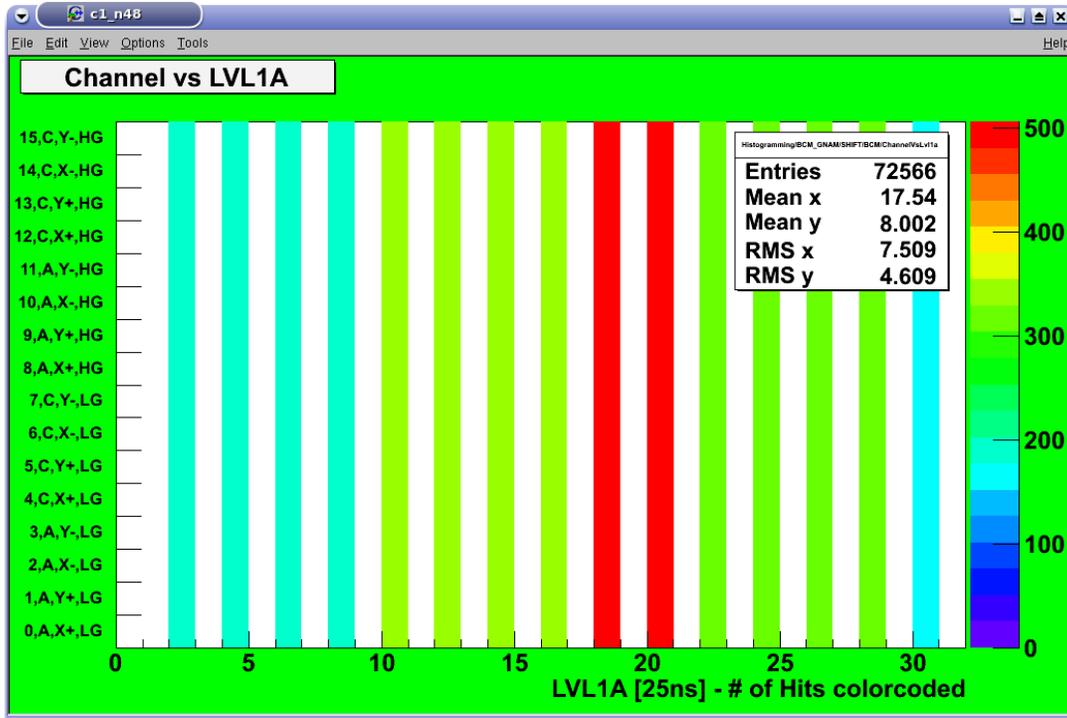


Figure B-6: The same pattern as in figure 4-15 that fired a beam abort is shown as triple pattern in the OHP LV1A window

Appendix C

VHDL code for beam abort algorithms and the trigger adder board

In this appendix the main parts of the VHDL code used for the beam abort algorithms and the trigger adder board are presented.

X out of Y algorithm

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity x_of_y_algo is
  Port (
    CLK : in  STD_LOGIC;
    RESULT : in  STD_LOGIC;
    TRIGGER : out  STD_LOGIC;
    FRAME_Y : in  STD_LOGIC_VECTOR (15 downto 0) := "1010101010101010";
    RESET : in  STD_LOGIC;
    ENABLE : in  std_logic;
    THRESHOLD_X      : in          STD_LOGIC_VECTOR      (15          downto
0) := "0000000010101010"
  );
```

```

end x_of_y_algo;

architecture Behavioral of x_of_y_algo is

    component Bitram IS
        port (
            addr_a: IN std_logic_VECTOR(13 downto 0);
            addr_b: IN std_logic_VECTOR(13 downto 0);
            clka: IN std_logic;
            clk_b: IN std_logic;
            dina: IN std_logic_VECTOR(0 downto 0);
            dout_b: OUT std_logic_VECTOR(0 downto 0);
            wea: IN std_logic);
    END component;

    signal activation : std_logic := '0';
    signal count : std_logic_vector(7 downto 0);
    signal address_in : std_logic_vector(13 downto 0);
    signal address_out : std_logic_vector(13 downto 0);
    signal past_result : std_logic;

begin

    algorithm_sample : process (CLK)
    begin
        if RESET = '1' then
            activation <= '0';
            count <= x"00";
            TRIGGER <= '0';
            address_in <= (others => '0');
            address_out <= (others => '0');
        else
            if (CLK'event and CLK = '1') and ENABLE = '1' then
                address_in <= address_in + 1;
                if (address_in = FRAME_Y) then
                    activation <= '1';
                end if;
            if ( activation = '1' ) then

```

```

        address_out <= address_out + 1;
        if (RESULT = '1' and past_result = '0') then
            count <= count + 1;
        --here we look at result and past_result
        elsif (RESULT = '0' and
past_result = '1') and (count >= "00000001") then
            count <= count - 1;
        end if;
    else
        if RESULT = '1' then
            count <= count + 1;
        --we only look at result
        end if;
    end if;
    if count >= THRESHOLD_X then
        TRIGGER <= '1';
    else
        TRIGGER <= '0';
    end if;
end if;

end process;

ram_Comp : Bitram
    port map(
        addra => address_in,
        addrb => address_out,
        clka => CLK,
        clkb => CLK,
        dina(0) => RESULT,
        doutb(0) => past_result,
        wea => ENABLE
    );

end Behavioral;

```

Bitram used for the X out of Y algorithm

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
-- synthesis translate_off
Library XilinxCoreLib;
-- synthesis translate_on
ENTITY Bitram IS
    port (
        addra: IN std_logic_VECTOR(13 downto 0);
        addrb: IN std_logic_VECTOR(13 downto 0);
        clka: IN std_logic;
        clkb: IN std_logic;
        dina: IN std_logic_VECTOR(0 downto 0);
        doutb: OUT std_logic_VECTOR(0 downto 0);
        wea: IN std_logic);
END Bitram;

ARCHITECTURE Bitram_a OF Bitram IS
-- synthesis translate_off
    component wrapped_Bitram
        port (
            addra: IN std_logic_VECTOR(13 downto 0);
            addrb: IN std_logic_VECTOR(13 downto 0);
            clka: IN std_logic;
            clkb: IN std_logic;
            dina: IN std_logic_VECTOR(0 downto 0);
            doutb: OUT std_logic_VECTOR(0 downto 0);
            wea: IN std_logic);
    end component;

-- Configuration specification
```

```

    for      all      :      wrapped_Bitram      use      entity
XilinxCoreLib.blkmemdp_v6_3 (behavioral)
    generic map(
        c_reg_inputsb => 0,
        c_reg_inputsa => 0,
        c_has_ndb => 0,
        c_has_nda => 0,
        c_ytop_addr => "1024",
        c_has_rfdb => 0,
        c_has_rfda => 0,
        c_ywea_is_high => 1,
        c_yena_is_high => 1,
        c_yclka_is_rising => 1,
        c_yhierarchy => "hierarchy1",
        c_ysinita_is_high => 1,
        c_ybottom_addr => "0",
        c_width_b => 1,
        c_width_a => 1,
        c_sinita_value => "0",
        c_sinitb_value => "0",
        c_limit_data_pitch => 18,
        c_write_modeb => 0,
        c_write_modea => 2,
        c_has_rdyb => 0,
        c_yuse_single_primitive => 0,
        c_has_rdya => 0,
        c_addra_width => 14,
        c_addrb_width => 14,
        c_has_limit_data_pitch => 0,
        c_default_data => "0",
        c_pipe_stages_b => 0,
        c_yweb_is_high => 1,
        c_yenb_is_high => 1,
        c_pipe_stages_a => 0,
        c_yclkb_is_rising => 1,
        c_yydisable_warnings => 1,
        c_enable_rlocs => 0,
        c_ysinitb_is_high => 1,

```

```

        c_has_web => 0,
        c_has_default_data => 1,
        c_has_sinitb => 0,
        c_has_wea => 1,
        c_has_sinita => 0,
        c_has_dinb => 0,
        c_has_dina => 1,
        c_ymake_bmm => 0,
        c_sim_collision_check => "NONE",
        c_has_enb => 0,
        c_has_ena => 0,
        c_depth_b => 16384,
        c_mem_init_file => "mif_file_16_1",
        c_depth_a => 16384,
        c_has_doutb => 1,
        c_has_douta => 0,
        c_yprimitive_type => "32kx1");

-- synthesis translate_on
BEGIN
-- synthesis translate_off
U0 : wrapped_Bitram
    port map (
        addra => addra,
        addrb => addrb,
        clka => clka,
        clkb => clkb,
        dina => dina,
        doutb => doutb,
        wea => wea);

-- synthesis translate_on

END Bitram_a;

```

Forgetting factor Algorithm

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity forgetting_factor_algo is
  Port(
    CLK : in std_logic;
    RESULT : in STD_LOGIC;
    INFLUENCE : in std_logic_vector (7 downto 0) := "00001111";
    RESET : in std_logic;
    ENABLE : in STD_LOGIC;
    CODE : in STD_LOGIC_VECTOR (7 downto 0) := "10101010";
    THRESHOLD_F : in STD_LOGIC_VECTOR (7 downto 0) := "01010101";
    TRIGGER : out STD_LOGIC
  );
end forgetting_factor_algo;

architecture Behavioral of forgetting_factor_algo is

  signal count_sig : std_logic_vector (7 downto 0);

begin
```

```

factor_pro : process(CLK)

    variable sum : integer := 0;
    variable count_var : integer;
    -- variable trig_var : integer :=0;

begin
    if RESET = '1' then
        count_sig <= x"00";
        TRIGGER <= '0';
    -- trig_var := 0;
    else
        if (CLK'event and CLK = '1') and ENABLE = '1' then
            sum := 0;
            count_var := CONV_INTEGER(count_sig);

            if CODE = "11111111" then
-- If CODE is "11111111" then FACTOR = COUNT (the previous COUNT)
                sum := count_var;
            elsif CODE = "00000000" then
-- If CODE is "00000000" then FACTOR = 0
                sum := 0;
            else
                if CODE (6)= '1' then
                    count_var :=
CONV_INTEGER(count_sig (7 downto 1));

                    sum := sum + count_var;

-- add to factor 0.5

                end if;

                if CODE (5)= '1' then
                    count_var :=
CONV_INTEGER(count_sig (7 downto 2));

                    sum := sum + count_var;

-- add to factor 0.25

                end if;
                if CODE (4)= '1' then

```

```

count_var :=
CONV_INTEGER(count_sig (7 downto 3));
sum := sum + count_var;
-- add to factor 0.125
end if;

if CODE (3)= '1' then
count_var :=
CONV_INTEGER(count_sig (7 downto 4));
sum := sum + count_var;
-- add to factor 0.0625
end if;

if CODE (2)= '1' then
count_var :=
CONV_INTEGER(count_sig (7 downto 5));
sum := sum + count_var;
-- add to factor 0.03125
end if;

if CODE (1)= '1' then
count_var :=
CONV_INTEGER(count_sig (7 downto 6));
sum := sum + count_var;
-- add to factor 0.015625
end if;

if CODE (0)= '1' then
count_var :=
CONV_INTEGER(count_sig (7 downto 7));
sum := sum + count_var;
-- add to factor 0.0078125
end if;
end if;

if (RESULT = '0') then

count_sig <= CONV_STD_LOGIC_VECTOR(sum, 8 );

```

```

-- If RESULT is 0 (low) count= FACTOR
    else

count_sig <= CONV_STD_LOGIC_VECTOR(sum , 8 ) + INFLUENCE ;
-- If RESULT is 1 (high) count= FACTOR + INFLUENCE
    end if;
    if (count_sig >= THRESHOLD_F) then
        TRIGGER <= '1';
-- Fires Abort When THRESHOLD_F is overpassed
-- trig_var := 1;
    else
        TRIGGER <= '0';
    end if;
end if;
end process;

end Behavioral;

```

Trigger adder board

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.std_logic_unsigned.all;
USE ieee.std_logic_misc.all;  -- Use OR_REDUCE function

USE work.v1495pkg.all;

ENTITY Two_Bit_Adder IS
    PORT(
        LCLK          : IN      std_logic;
        -- CERN Clock
        RESET         : IN      std_logic;
        D_DIN         : IN      std_logic_vector(31 downto 0) ;
        -- D Mezzanine Input, only bits 0-7 used
        F_DIN         : IN      std_logic_vector(31 downto 0) ;
        -- D Mezzanine Input, only bits 0-7 used
        E_DOUT        : OUT     std_logic_vector(31 downto 0)
        -- E Mezzanine Output, only bits 0-7 used
    );
END Two_Bit_Adder;

ARCHITECTURE rtl OF Two_Bit_Adder IS

    signal number1          : std_logic_vector(2 downto 0);
    signal number2          : std_logic_vector(2 downto 0);
    signal result           : std_logic_vector(6 downto 0);
    signal hthres           : std_logic_vector(1 downto 0);
    signal AtoC             : std_logic_vector(1 downto 0);
    signal CtoA             : std_logic_vector(1 downto 0);
    signal Wide             : std_logic_vector(1 downto 0);

BEGIN
```

```

adder : process (LCLK, RESET)
begin
  if RESET ='0' then
    result <= (others=>'0');
    number1 <= (others=>'0');
    number2 <= (others=>'0');
    hthres <= (others=>'0');
    AtoC <= (others=>'0');
    CtoA <= (others=>'0');
    Wide <= (others=>'0');
  elsif LCLK'event and LCLK = '1' then
    number1 <= '0' & D_DIN(1 downto 0);
    number2 <= '0' & D_DIN(4 downto 3);
    hthres <= D_DIN (7 downto 6);
    AtoC <= F_DIN (1 downto 0);
    CtoA <= F_DIN (4 downto 3);
    Wide <= F_DIN (7 downto 6);
    result(3) <= AtoC(1) or AtoC(0);
    result(4) <= CtoA(1) or CtoA(0);
    result(5) <= Wide(1) or Wide(0);
    result(6) <= D_DIN(7) or D_DIN(6);

    if hthres= "00" then

      result(2 downto 0) <= number1 + number2;

    else

      result(2 downto 0) <= "111";
    end if;
  end if;
end process;

E_DOUT(6 downto 0) <= result;
E_DOUT(7) <= LCLK;

END rtl;

```