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Τομέας Ηλεκτρικής Ισχύος
Εργαστήριο Ηλεκτρικών Μηχανών και Ηλεκτρονικών Ισχύος

Προβλεπτικός Έλεγχος Αντιστροφέων Τριών Επιπέδων για Σύνδεση στο Δίκτυο με LCL Φιλτρο

Model Predictive Control of Grid Connected Neutral Point Clamped Converters through LCL filters

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ABSTRACT

The objective of this thesis is the development of a grid connected control system of a three level Neutral Point Clamped converter interfacing the grid through LCL filters with switching losses minimization and active damping of the filter resonance. In order to achieve optimum efficiency, an online Model Predictive optimization strategy is considered minimizing switching losses, namely Model Predictive Direct Power Control(MPDPC), and is properly extended to meet active damping of LCL filter requirements. As an outcome of the online optimization process, switching frequency of the converter is variable, thus it is compared in simulation environment with the traditional Direct Power Control(DPC) technique. DPC with and without LCL output filter are thoroughly presented and an analytical way of DPC lookup table design is proposed based on virtual flux quantities. Moreover an effective three-level hysteresis controller design is proposed in order to smooth spikes present in reactive power with conventional DPC. While presenting the MPDPC solution algorithm utilized in this thesis, two new techniques are introduced, aiming at lowering the computational effort required for conventional MPDPC reach a solution. Finally, MPDPC with LCL filters and active damping is evaluated in a broad range of operating points, and proof of concept hardware is implemented. The main conclusions drawn from this study is that high performance converters can be designed utilizing MPC concepts making use of today computational power, while providing a framework for traditional techniques, i.e active damping, to be integrated with Online Optimization Controllers.

Keywords: Neutral Point Clamped Converter(NPC), Model Predictive Control(MPC), Direct Power Control(DPC), Model Predictive Direct Power Control(MPDPC), LCL filter, Active Damping, Virtual Flux, Online Predictive Control, Receding Horizon

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CONTENTS

CHAPTER

ONE

INTRODUCTION

1.1 Background

Ever since industrial revolution, energy demand is constantly growing, based largely on fossil fuel resources. Electric power is mostly produced by steam powered electric generators through fossil fuel combustion, like coal, natural gas, or petroleum and other non renewable energy sources. Combination of both of these facts and continuous rise of fossil fuels price paralleled to the potential ecological catastrophe that over-exploitation of available resources imply, make massive adoption of renewable energy sources into large scale energy production urgent, towards a sustainable equilibrium.

Such a change is happening and can easily be depicted by many statistics illustrating rapid growth of new energy sources, such as figure 1.1, summarizing electricity production from renewable energy sources rise in Europe.

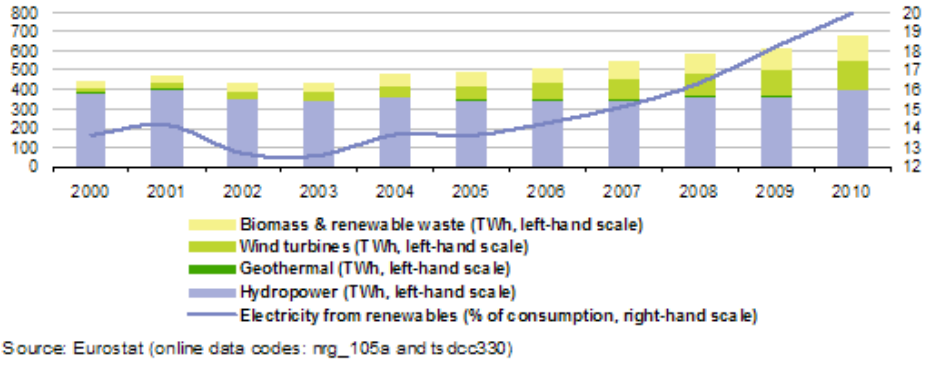


Figure 1.1: Electricity generated from renewable energy resources in Europe for previous decade

Renewable energy sources such as wind, sunlight, tides, waves, biomass, geothermal heat etc., can accommodate for a much larger ratio in electric power generation, if related technological advances are made and constraints, mainly related with intermittent availability and efficient storage, are surpassed. Moreover, with the rise of fossil fuels price, investing on renewable energy electricity production is getting more potent than the past, boosting development of new technologies. Of great importance is the fact that with growth of Distributed Generation Systems, the main picture of centralized electricity production changes, allowing rapid growth of sustainable electricity generation. Moreover for developing countries, renewable energy sources are of great importance, as a way to provide electricity to remote areas and support local economy by natural resources readily available.

All this technological advances needed in the energy domain are closely related to power electronics research area, since modern power converters with efficient operation, and capability of complex implementations, are empowering changes boosting utilization of renewable energy sources. Power converters are the key mechanism allowing different energy sources to connect together and integrate in a larger power distribution network.

1.2 Thesis Objectives

The main objective of this thesis is the study and development of a grid connected high efficiency - high performance system, fig 1.2. In high power-high voltage applications, with rise of applied voltage, switching losses have a greater impact on overall performance and are linearly related to switching frequency. Thus, minimization of switching frequency leads to more efficient power systems by decreasing switching losses of the converter. For this reason a more sophisticated Model Based Predictive Control approach is adopted, targeting switching losses minimization.

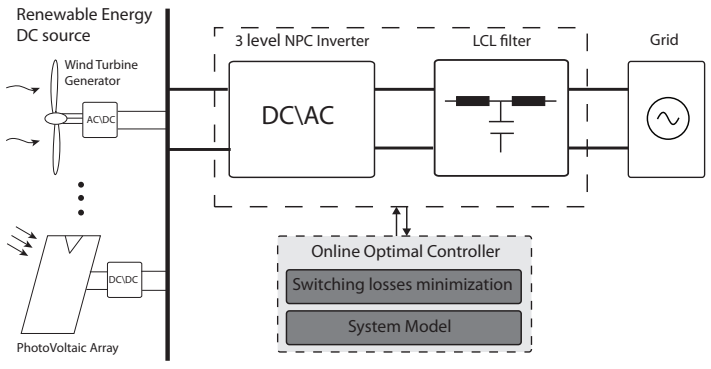


Figure 1.2: Online Predictive Control system block diagram

Neutral Point Clamped converters are utilized in a variety of applications, such as electrical energy transmission systems and active front ends for medium voltage drives. Selection of a multilevel power converter topology in this thesis, such as a three-level NPC, is made due to the proved advantages over conventional two level converters. Multilevel topologies are more efficient, more suitable for high power applications and control algorithms developed for one level can be expanded to higher level topologies due to their modular nature.

One main challenge met in this thesis, is utilization of LCL filter for the grid connection. Since studied control methods produce variable switching frequency, overall system might exhibit strong resonance leading to overall instability. As a result an active damping approach is followed for all studied techniques, and is properly expanded to fit in the Model Predictive Control method used.

1.3 Thesis Outline

In order to maintain consistency and provide a continuous reading flow, this thesis is divided in three parts.

In part I the literature review covered during this thesis is presented, in an attempt to situate studied topologies and control techniques in current research and present state of the art, at addressed topics.

Chapter 2 Multilevel converter topologies are discussed, with a focus on three level Neutral Point Clamped converters, which is the topology utilized in second part. Prevailing topologies are presented and an overview of multilevel converter advantages and tradeoffs are given.

Chapter 3 Active and Reactive Power control techniques are reviewed, making clear to the reader the necessity of sophisticated control systems for power converters,

Chapter 4 A basic classification of Predictive control is presented, with a review of main categories, familiarizing the reader with predictive control concepts and setting the background for the predictive control techniques studied in the next part.

Chapter 5 LCL output filter design for power converters is reviewed, and an approach to passive and active damping techniques through extension of existing control method is given, in an attempt to clarify the benefits and perils of high-order filter utilization.

In part II main study of Direct Power Control and Model Predictive Direct Power Control grid connection techniques follows, with the intention to cover in depth the suggested MPDPC - LCL method as an extension of all previous method analyzed:

Chapter 6 the classic Direct Power Control method is reviewed, with an in depth analysis of all its components, with simulation and experimental results are presented and reviewed.

Chapter 7 DPC method studied in previous chapter is extended in order to incorporate an LCL output filter and actively damp generated resonant harmonics. Simulation results are presented as well.

Chapter 8 a hybrid technique of Model Predictive Control and Direct Power Control studied in chapter 6 is presented, Model Predictive Direct Power Control. An in depth analysis of the problem formulation, system modeling and solution algorithm implementation is provided to the reader, allowing for a practitioners approach to sophisticated MPC techniques. Chapter finishes with simulation and experimental results.

Chapter 9 MPDPC method is extended in order to incorporate LCL filter with active damping, as for DPC in chapter 7. A framework for adapting cascaded loops in existing MPC algorithms is suggested, and simulation results are presented.

Chapter 10 An evaluation of four main control techniques studied in previous chapters is made through simulations in steady state for a broad range of operating points. A concluding table and proper graphs illustrate performance acquired of all control techniques evaluated.

Chapter 11 Conclusions drawn from previous chapters are expressed, following the comparative analysis of four studied control methods and evaluation of the proposed MPDPC-LCL technique.

In part III an overview of the hardware setup utilized in the experimental part of this thesis is given, and a description of hardware developed specifically for this part is presented. The following Appendix contains useful matlab scripts developed during this thesis.

Part I

Literature review - State of the art

CHAPTER
TWO

MULTILEVEL CONVERTERS

Use of multilevel converters have increased in high voltage-high power applications due to the main benefits of high voltage capability and low losses that they present. The main concept of all multilevel topologies is to synthesize their output voltage from several voltage levels in a staircase waveform fashion in contrast to conventional two level inverters. In this chapter the three more common topologies of multilevel converters are presented with an emphasis on Neutral Point Clamped converter which is the topology utilized in the following part.

2.1 Diode Clamped - NPC Multilevel Inverter

In a three phase *m-level* NPC as proposed in [1] each leg is composed of $2(m-1)$ series connected switches and $(m-1)$ dc link capacitors charged with a voltage level equal to $\frac{Vdc}{m-1}$. In a 3 level NPC each phase leg is composed of 4 series connected switches ,2 dc link capacitors splitting the dc bus voltage in half and 2 clamping diodes. A basic schematic diagram of a 3 level NPC is shown in figure 2.1.

In general, control strategies employed to a 3 level converter can be extended to higher level topologies due to their modular nature. Obviously the higher the level of one topology the better the output quality is expected to be, with a trade-of in system cost and complexity. One major limitation of higher multilevel implementations is the reverse voltage capability of the clamping diodes, which should be proportional to the level for which they are used to employ clamping action, thus making implementation of high level multilevel converters difficult. In this thesis the case of a 3level NPC converter is considered as the simplest abstraction of multilevel topologies.

In a 3 level NPC inverter the output voltage of each phase leg can be set to $\frac{V_{dc}}{2}$, 0, or $\frac{-V_{dc}}{2}$. In that way, each phase leg of the NPC inverter can be seen as a three-state switch able to take values between $1, 0, -1$ as illustrated in figure

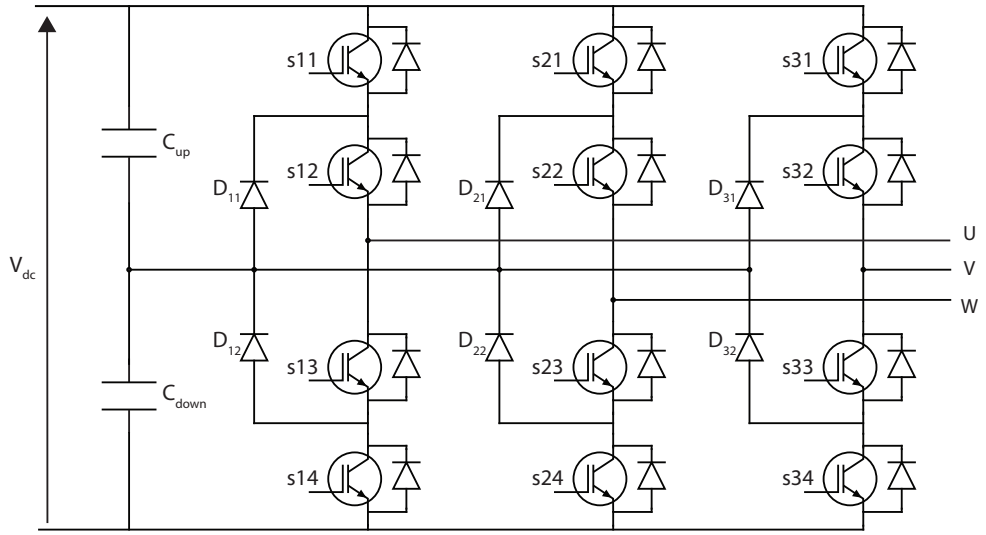


Figure 2.1: 3 level NPC schematic diagram.

2.2. The input voltage V_{dc} is equally divided by the dc link capacitors C1,C2 and the output of each phase is referenced to the capacitor connection point, the midpoint, thus balancing the capacitor voltages is critical for proper operation.

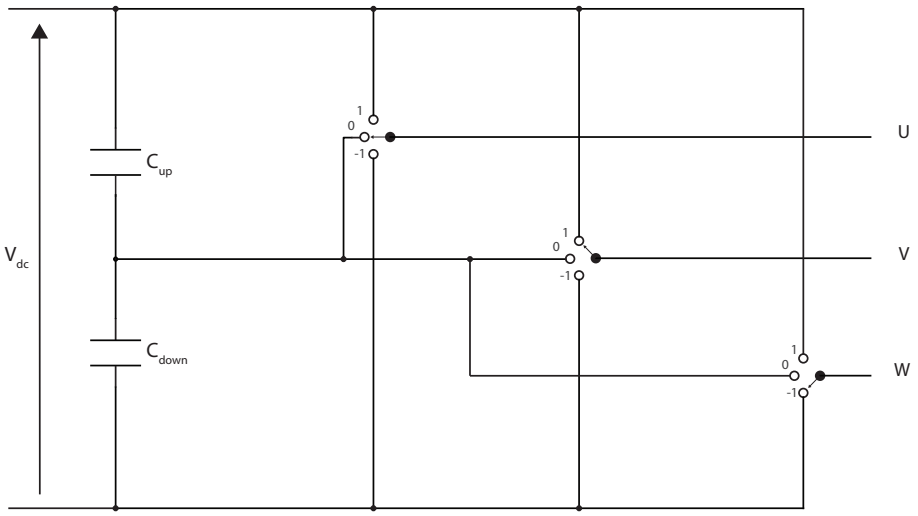


Figure 2.2: 3 level NPC phase leg as three-state switch

Given the schematic diagram of figure 2.1, in order to generate a voltage output of $\frac{Vdc}{2}$ on phase U, switches S11 and S12 are closed while S13 and S14

remain open. In this case the clamping diode D12 balances the voltage sharing between S13 and S14 with S13 blocking the voltage across C1 and S14 the voltage across C2. To generate a voltage output of $\frac{-Vdc}{2}$ on phase U, switches S13 and S14 are closed while S11 and S12 remain open. In this case the clamping diode D11 balances the voltage sharing between S11 and S12 with S11 blocking the voltage across C1 and S12 the voltage across C2. to generate a voltage output of 0Volt on phase U, switches S12 and S13 are closed while S11 and S14 remain open. In this case diode D11 clamps switch S11 to block the voltage across C1 ans D12 clamps switch s14 to block the voltage across C2. The same switching action exists for the rest of the phases and they can be summarized in table 2.1. The three possible switching states as already described are illustrated in figure 2.3

Voltage level	Switching States S1	S2	S3	S4	Sr
$\frac{Vdc}{2}$	1	1	0	0	1
0	0	1	1	0	0
$\frac{-Vdc}{2}$	0	0	1	1	-1

Table 2.1: 3 level NPC switching states

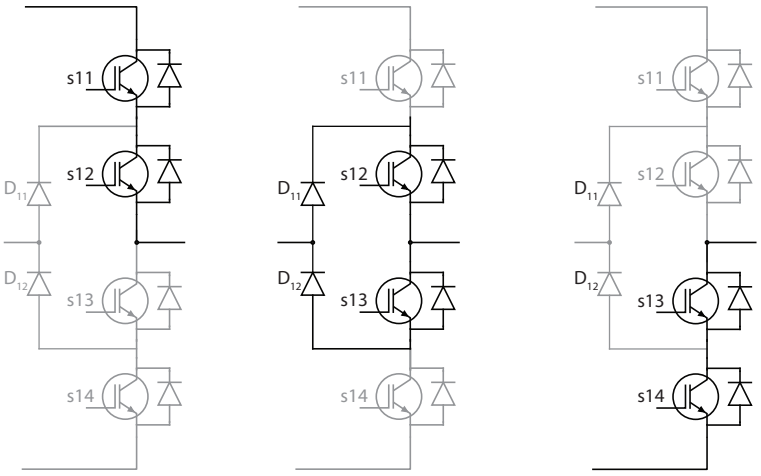


Figure 2.3: NPC converter possible switching actions

2.1.1 NPC switching vectors $\alpha\beta$ plane analysis

Considering previous switching state analysis for the 3 level NPC, it is very useful for further analysis to consider the representation of all possible output voltage vectors of the converter, related to switches state, transformed from the three phase system,$V_{inv_{abc}} = [V_{inva}, V_{invb}, V_{invc}]^\intercal$ to $\alpha\beta 0$ static reference plane $Vinv_{\alpha\beta} = [V_{inv\alpha}, V_{inv\beta}]^\intercal$ using the Clarke-Parke transformation 2.1

$$V_{inv\alpha\beta} = \frac{2}{3} \cdot P \cdot V_{invabc} \tag{2.1}$$

where P is the transformation matrix:

$$P = \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.2}$$

All possible voltage outputs in phase and magnitude are depicted in figure 2.4. A hexagon is formed containing 27 voltage vectors with sets of,in terms of magnitude, 6 large vectors(5,9,13,17,21,25),6 medium vectors(2,6,10,14,18,22), 12 small(3,4,7,8,11,12,15,16,19,20,23,24) vectors and 3 zero vectors(0,1,26). Zero Vectors are not considered as normal operating switching positions and are mainly used to halt the converter or for other operational functions.

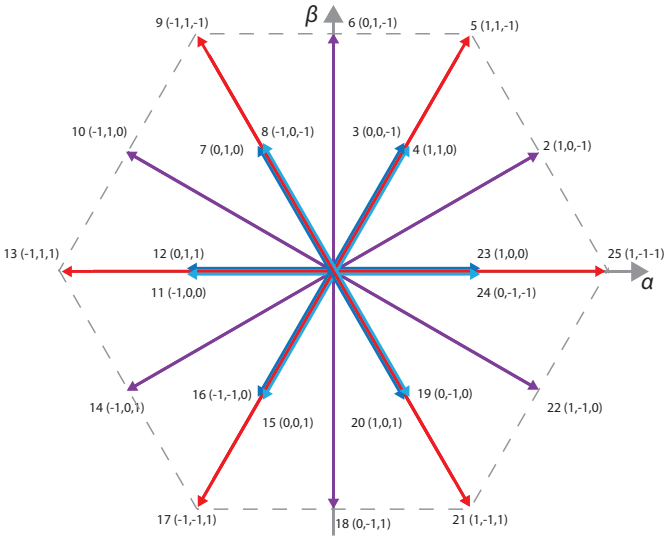


Figure 2.4: 3 level NPC voltage vectors in $\alpha\beta$ plane.

Of great importance is the fact that small vectors come in pairs. These are redundant states meaning that when employed, same output voltage is achieved and this the key mechanism for midpoint capacitor voltage balancing in the NPC as it will be explained in the direct power control description.

Since in terms of voltage output capacity the NPC inverter bears only 18 states, the voltage vector numbering can be reduced to 18, with three different switching states for the zero state, and two for each small voltage vector. The new voltage vector indexing is addressed in table 2.2. This new voltage vector indexing is a simple way to minimize computation effort to calculations that only magnitude of outpout voltage is of interest.

U_n	S_R	S_S	S_T
U_1	1	0	0
	0	-1	-1
U_2	0	0	-1
	1	1	0
U_3	0	1	0
	-1	0	-1
U_4	-1	0	0
	0	1	1
U_5	0	0	1
	-1	-1	0
U_6	0	-1	0
	1	0	1

Small

U_n	S_R	S_S	S_T
U_8	1	0	-1
U_{10}	0	1	-1
U_{12}	-1	1	0
U_{14}	-1	0	1
U_{16}	0	-1	1
U_{18}	1	-1	0

Medium

U_n	S_R	S_S	S_T
U_7	1	-1	-1
U_9	1	1	-1
U_{11}	-1	1	-1
U_{13}	-1	1	1
U_{15}	-1	-1	1
U_{17}	1	-1	1

Large

U_n	S_R	S_S	S_T
	0	0	0
U_0	1	1	1
	-1	-1	-1

Zero

Table 2.2: Zero, Small, Medium and Large Converter Output Voltage Vectors Indexing

2.2 Capacitor Clamped - Flying Capacitor Multilevel Inverter

Flying Capacitor multivel inverters [2] are a similar topology to the NPC converter previously presented by the fact that instead of utilizing diodes to provide clamping action, capacitors are used to maintain voltage levels to the desired values. For the same reason, capacitor voltage levels increase quadratically as the number of levels implemented grows.

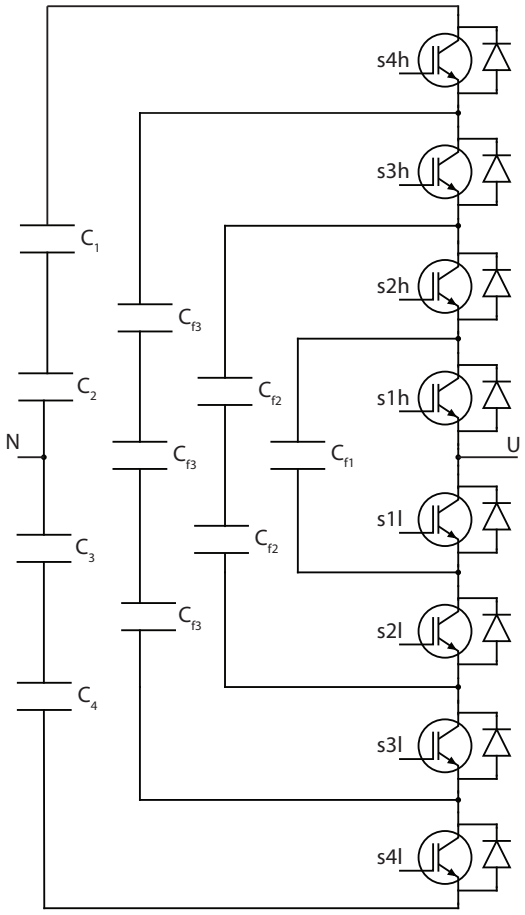


Figure 2.5: phase leg of a 5 level Flying Capacitor Inverter

For a *m-level* Flying Capacitor inverter phaseleg, *m-1* cells are connected in series, where each cell represents a pair of switches separated by one flying capacitor, resulting to *2(m-1)* semiconductor switches and *m-2* flying capacitors chargef at m different voltage levels. By relevant switching action, capacitors are serially connected to the phase output, forming a staircase waveform of m

levels. One limitation similar to NPC topology is that at each cell only one of the switches can be closed or else different voltage level capacitors are paralleled resulting in a short circuit.

In figure 2.5 a *5-level* flying capacitor multilevel converter phaseleg is illustrated and in table 2.3 switching action of the converter relevant to voltage level output are summarized. h and l indexes denote high and low switches of each cell pair and number of capacitors at each cell denotes their voltage rating ratio.

Voltage level	Switching States							
	$S4_h$	$S3_h$	$S2_h$	$S1_h$	$S4_l$	$S3_l$	$S2_l$	$S1_l$
$\frac{Vdc}{2}$	1	1	1	1	0	0	0	0
$\frac{Vdc}{4}$	1	1	1	0	1	0	0	0
	0	1	1	1	0	0	0	1
	1	0	1	1	0	0	1	0
	1	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0
	1	0	0	1	0	1	1	0
	0	1	0	1	0	1	0	1
	0	1	1	0	1	0	0	1
$\frac{-Vdc}{4}$	1	0	0	0	1	1	1	0
	0	0	0	1	0	1	1	1
	0	0	1	0	1	0	1	1
	0	1	0	0	1	1	0	1
$\frac{-Vdc}{2}$	0	0	0	0	1	1	1	1

Table 2.3: 5 level Flying Capacitor switching states

2.3 Cascaded H-bridge Multicell Inverter

This topology is a different approach in considering other multilevel topologies previously described. A number of full bridge two level inverter is cascaded using separate isolated dc sources, in a modular setup, in order to synthesize the multilevel output [3]. The number of levels m is proportional to the number of dc sources,thus H-bridges, utilized n as: $m = 2n+1$. In figure 2.6 a 7-level three phase converter is illustrated, by properly connecting three H-bridge converters at each phase.

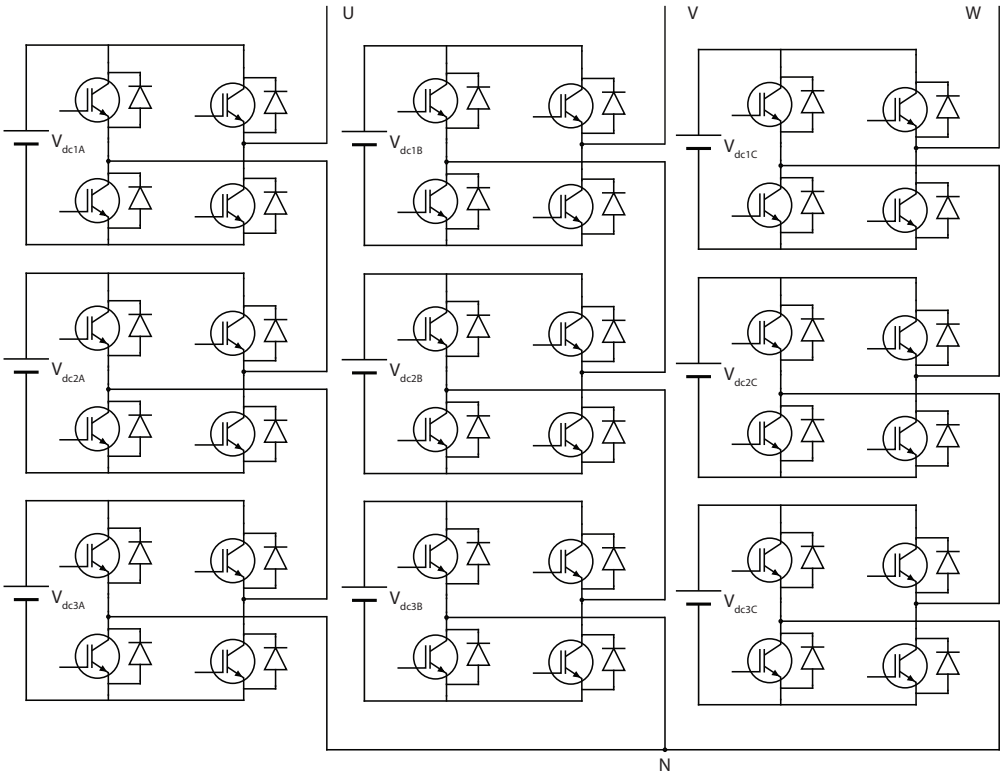


Figure 2.6: 7-level Cascaded H-bridge Multilevel Inverter

Features of this topology are the reduced number of semiconductor components required compared to other topologies already presented, and the fact that no clamping elements exist, either diodes or capacitors. These benefits, in combination with the modular nature of the topology, makes ideal for higher level multilevel converters realization and allows easy expansion of existing converters to higher level output. Especially in applications where multiple dc voltage sources exist, such as photovoltaic applications, battery operated systems, and fuel cells, integration of such a modular architecture is very intuitive and beneficial.

On the other hand, if multiple isolated dc sources are not available, realization of such a topology tends to be hard to implement, thus avoided. For this reason several other modular multilevel converter topologies operating from common dc source have been implemented, such as Reversing Voltage Mutilevel Inverter (RVMI) and Modular Multilevel Inverter (M2I).

2.4 Overview

Multilevel Converters present many advantages over conventional two level power converters, most important among them are:

High quality waveforms as their voltage output is synthesized from several voltage levels. Lower voltage semiconductor switches also allow adoption of more efficient semiconductor technologies.

Low switching losses due to the fact that switching action is shared among a larger number of semiconductor switches, making them ideal for a low switching frequency implementation. Utilization of semiconductors at lower voltage levels allow for even lower switching losses

High voltage capability as seen from the previous analysis a well balanced system can operate at double the voltage ratings of the semiconductors and capacitors used.

Low EMI interference due to lower $\frac{dV}{dt}$ stress of the semiconductor switches. Also due to the non constant switching frequency applied throughout this thesis, harmonics generated are less concentrated around specific frequencies, thus produce less noise in specific harmonics leading to reduction of EMI and audible noise, in a similar way to the spread spectrum EMI reduction techniques .

Common-mode Voltage present in multilevel inverters is minimal and can be totally eliminated by proper control techniques in contrast to two level converters. This is a useful aspect in electrical drives industry as common mode voltage produces stress on the machine bearings and may cause over-voltage stress to the winding insulation, affecting its lifetime.

Input Current that a multilevel converter draws is of reduced harmonic distortion, making their design more easy to adopt to power quality standards.

On the other hand, multilevel converters have design trade-offs, such as high number of semiconductor and clamping devices, and more complex control techniques since with rise of switching elements, the number of possible switching actions of the converter is augmented as well.

Since for a high power-high voltage system which is the case of most grid connected systems, a 3 level NPC converter will be evaluated in the following part, as the simplest abstraction of multilevel converters.

CHAPTER
THREE

PQ CONTROL

3.1 Introduction

In order to effectively utilize the growing number of alternative energy resources, electric power generated is paralleled to the main power distribution network so as to be made remotely available to an extended consumers network, in contrast to isolated power systems where there is no provision for energy storage. This Distributed Generation scheme, becomes attractive due to the sustainable and pollution free properties that exploitation of renewable energy sources presents. Main challenge of DG systems is the proper arrangement and operation of this network oriented scheme, and can be achieved by use of modern power converters capable of:

Grid side:

- Synchronization to mains grid frequency
- Control of mains Voltage
- Control of Active Power flow to the grid
- Control and Compensation of Reactive Power to and from the grid .
- Guarantee current and voltage waveform quality complying to standards

Energy source side:

- Efficient utilization of energy source, i.e solar MPPT applications
- DC voltage supervision at the converter input

A typical system of a grid connected wind turbine system is illustrated in figure 3.1, illustrating the nested functions that the controller of the power converter perform from basic to supervisory functions. This thesis concentrates on

the grid connection part, thus the case of dc/ac Power control techniques are reviewed in this chapter.

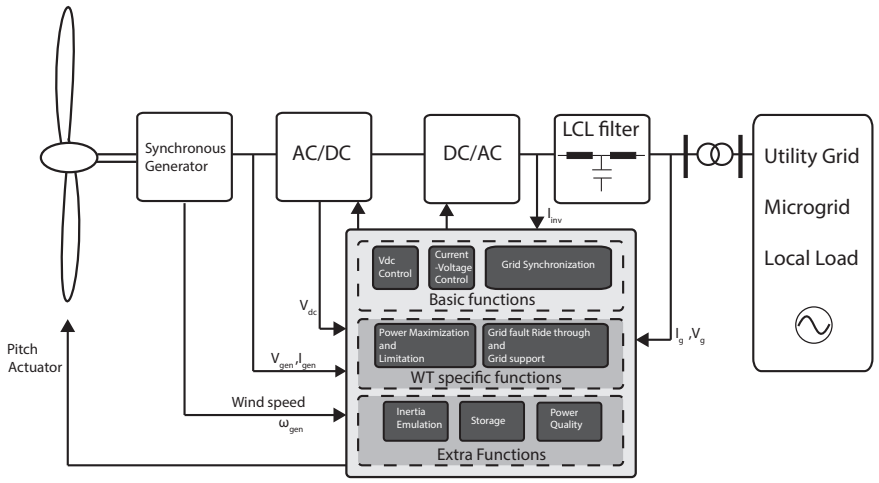


Figure 3.1: overview of a typical System of grid connected wind turbine system

Grid connected control systems have to provide power in an accepted quality, and many control techniques exist. A preliminary classification is whether there exists a communication link between central grid and remote DG system. Main Control techniques of DG systems can be summarized as:

With communication link:

- Active and Reactive power control - PQ control
- Distributed Control
- One cycle control

Without communication link:

- Droop control

Droop Control is one of the most popular techniques used in literature [4] [5] and is commonly known as Voltage - frequency droop control. Main concept is that power delivered to the grid mimics characteristics of synchronous generators used in centralized power plants. This characteristics depend on synchronous generator rotor inertia which limit frequency variation and natural coupling between frequency and power delivered to the grid. Since active and reactive power of a grid connected inverter can be defined by :

$$P = \frac{3V_{inv}V_g}{X}\sin\delta$$
$$Q = \frac{3V_g}{X}(V_{inv}\cos\delta - V_g)$$

Inverter Active and Reactive power demand is described by droop coefficients m,n of a specific power converter, wich can be illustrated in figure 3.2

$$\omega = \omega_0 - m \cdot P$$
$$V = V_0 - n \cdot Q$$

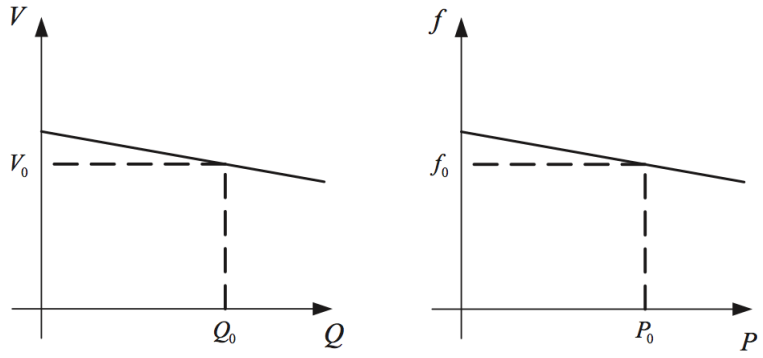


Figure 3.2: Droop control V-f charactheristics

This method accomplishes acceptable performance only if existing grid voltage is free of distortion and balanced. Moreover it presents drawbacks such as slow transient response, trade off between Voltage output regulation, and frequency and phase deviation that in many applications make this method impractical.

Distributed control as introduced in [6] sets power references of the inverter through a communication network. In this network smart metering of the interconnected loads transceive information with power generation units in order to properly coordinate power generation at every DG system. This method is highly depended in a complex by nature bidirectional communication system.

One cycle control This technique as presented in [7] takes advantage of the pulsed and nonlinear nature of switching converters and achieves instantaneous control of the average value of the chopped voltage or current, in contrast to power converter characteristics linearization of simple droop control. This

method is favored for its simple control implementation, but restricts its use to specific control strategies. In parallel operation this control method of the DG system might lead to circulating current between phases.

Active and Reactive Power Control in contrast to voltage - frequency control or other current control techniques, sets directly the active and reactive power reference to the power converter. Usually Active power is set by a PI control loop from the dc Voltage input at the inverter so as the grid absorb as much active power as possible, while Reactive power compensation is possible by adjusting the reference value. This method can be classified in three categories depending on the control method employed to regulate Active and Reactive power of the inverter:

- Direct Power Control - DPC
- Virtual Flux based control
- Current Control techniques

A brief overview of main control techniques of PQ control will be presented in the following section.

3.2 PQ control methods of grid connected converter

Active and Reactive power control is based on instantaneous power theory as presented in [8], and power calculations in rotating and stationary frame can be summarized by:

$$p = \frac{3}{2}(e_{gd}i_{gd} + e_{gq}i_{gq})$$
$$q = \frac{3}{2}(e_{gq}i_{gq} - e_{gd}i_{gd})$$

$$p = \frac{3}{2}\omega(e_{g\alpha}I_{g\beta} - e_{g\beta}I_{g\alpha})$$
$$q = \frac{3}{2}\omega(e_{g\alpha}I_{g\alpha} + e_{g\beta}I_{g\beta})$$

3.2.1 Current control techniques - synchronous frame VOC

An easy way to achieve active and reactive power control to a power converter is to incorporate power references to an existing current control scheme. Synchronous frame VOC is a simple to implement control scheme, using a current

controller implemented in dq rotating frame and a power calculating stage acting as feedback.Current component references can be calculated by:

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \frac{1}{V_{gd}^2 + V_{gq}^2} \begin{bmatrix} V_{gd} & -V_{gq} \\ V_{gq} & V_{gd} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} \tag{3.1}$$

An overall block diagram of the implemented control is illustrated in figure 3.3

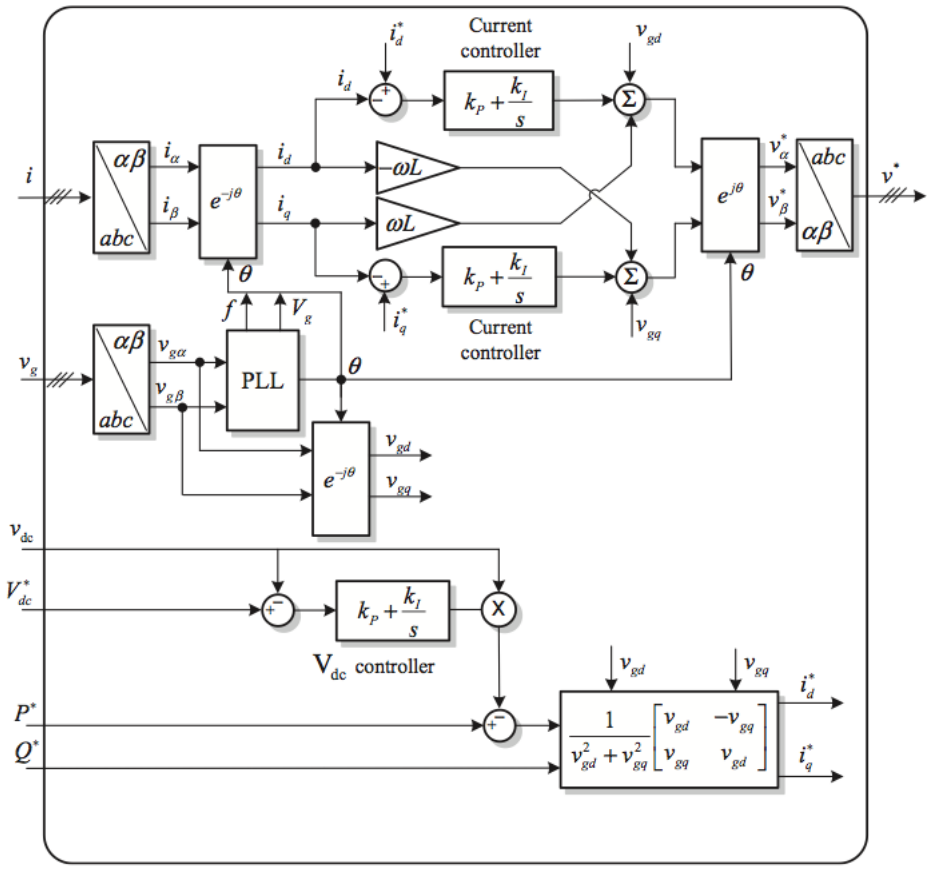


Figure 3.3: PQ open loop Voltage Oriented Control based on the synchronous dq frame [9]

Many variations of this technique exist, replacing synchronous frame calculation with static reference coordinate transformations, using PI closed loop controller to adjust the duty cycle of the converter. This technique utilizes a modulator and yields a steady switching frequency output waveform.

3.2.2 Virtual flux based Control

As an alternative to the aforementioned VOC, another scheme utilizing virtual flux concept has been developed. Originally Virtual Flux concept has been proposed for Direct Power Control implementations but can be incorporated to VOC techniques. Due to the resemblance of grid connection to the equivalent schematic of an AC machine, a virtual quantity is considered, that of virtual flux and can be derived by equations:

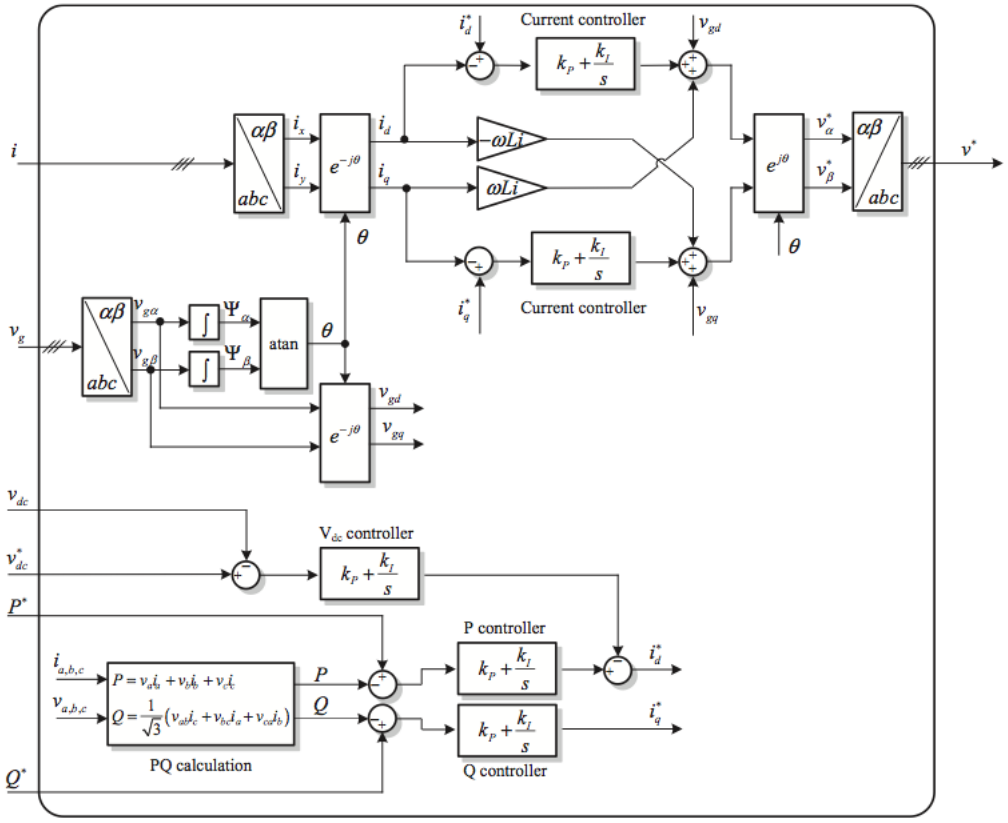


Figure 3.4: Virtual Flux based Voltage Oriented block diagram [9]

$$\psi_{g\alpha} = \int V_{g\alpha}\,\mathrm{d}t$$
$$\psi_{g\beta} = \int V_{g\beta}\,\mathrm{d}t$$
$$\sin(\theta) = \frac{\psi_{g\beta}}{\sqrt{\psi_{g\alpha}^2 + \psi_{g\beta}^2}}$$
$$\cos(\theta) = \frac{\psi_{g\alpha}}{\sqrt{\psi_{g\alpha}^2 + \psi_{g\beta}^2}}$$

Virtual flux quantities are thus estimated by current feedback of the system and knowledge of the converter output voltage, and can be used for Power Estimation and to replace PLLs for grid synchronization. A more analytical study of Virtual Flux quantity will be presented in the next part of this thesis in the section of Direct Power Control, as it is a very important aspect of all studied Control techniques.

Block diagram of the VOC using the virtual flux concept is illustrated in figure 3.4 and incorporates closed loop PI current controllers. This technique yields also a steady switching frequency since a modulator is used at the output of the control.

3.2.3 Direct Power Control

Direct Power Control presented in [10] originates from Direct Torque Control developed for AC machines drives. Utilizing the Virtual Flux concept, power delivered to the grid is estimated and compared to reference values. Depending on power errors, a switching action is selected based on a pre calculated Look-up table. In this essence, DPC is a predictive control technique of Active and Reactive power, where prediction stage is calculated offline and reflected in the utilized Look-up table. Since no modulator is used, this technique results in variable switching frequency. Benefits of DPC are simple control algorithm and fast response, while there is a trade of in need for a high sampling frequency of the overall system. Many variations of the proposed technique have been developed, some of which incorporate a modulator in order to achieve constant switching frequency.

This technique will be more analytically presented in the respective chapter of DPC control of 3 level NPC inverter. Since this technique yields a variable switching frequency, it is selected as a benchmark to evaluate results of the proposed predictive technique.

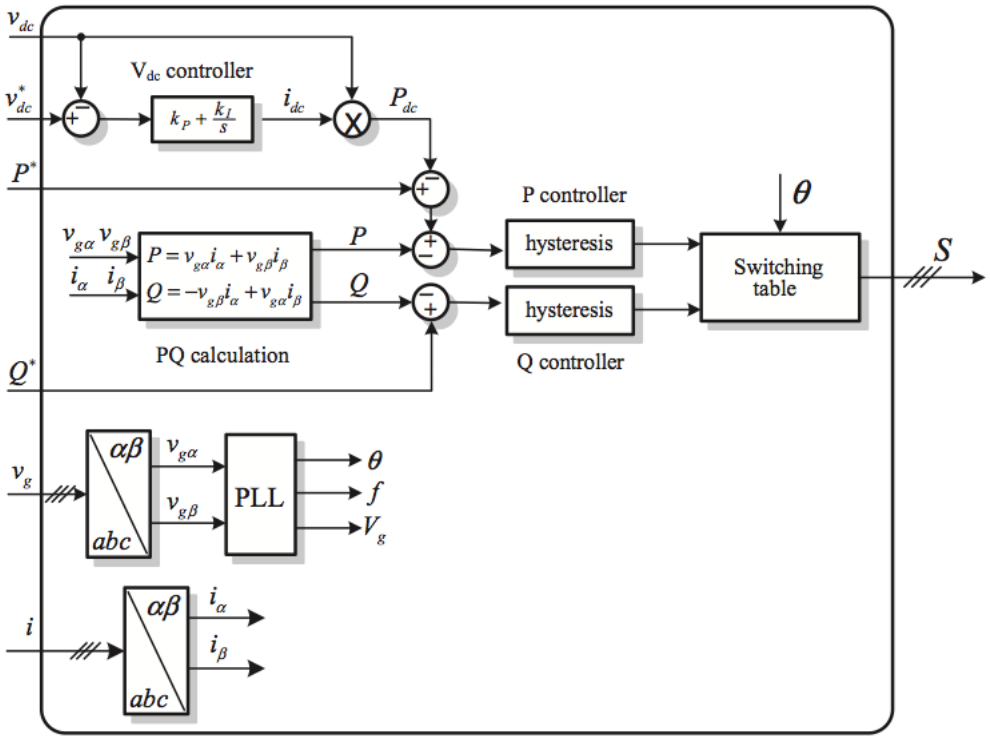


Figure 3.5: Direct Power Control block diagram [9]

CHAPTER
FOUR

PREDICTIVE CONTROL

4.1 Introduction

With the increased use of power converters and demand of more complex control schemes, many converter control techniques have been developed. A general classification of the control techniques described in literature is illustrated in figure 4.1. From conventional linear PWM techniques and hysteresis controllers, control methods are evolving to more advanced schemes like fuzzy logic and predictive controllers, utilizing processing power and speed of modern hardware.

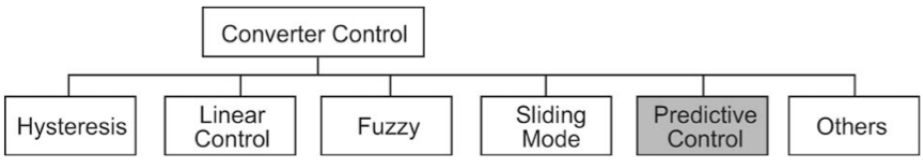


Figure 4.1: Classification of converter control methods [11]

Predictive control has lately being adopted in power converters control concepts, and already represents a wide range of various techniques developed. Following presentation and analysis of predictive control in power electronics in [11],[12] a principal classification of existing techniques is presented in figure 4.2. Main concept of all predictive control techniques is that decision of the controller is not based on past state of the controlled system but on predicted behavior of the state variables and proper selection of the controlled variables after an optimization stage either offline, meaning precalculated, or online. Despite the hard to implement nature of predictive techniques, main concept is very simple and intuitive to the control designer and has proved adequate for power converters control. One of the biggest advantage over other techniques

is that in predictive control, a MIMO (multiple input multiple output) system can be controlled by a single control loop in contrast to other techniques where cascaded control schemes must be implemented.

Moreover, especially for the case of MPC (Model Predictive Control) nonlinearities of the controlled system can easily be implemented in the model used, and additional restrictions of the system can easily be incorporated in the control algorithm and optimization strategy. A brief presentation is following for every predictive technique concepts focusing on Model Predictive Control.

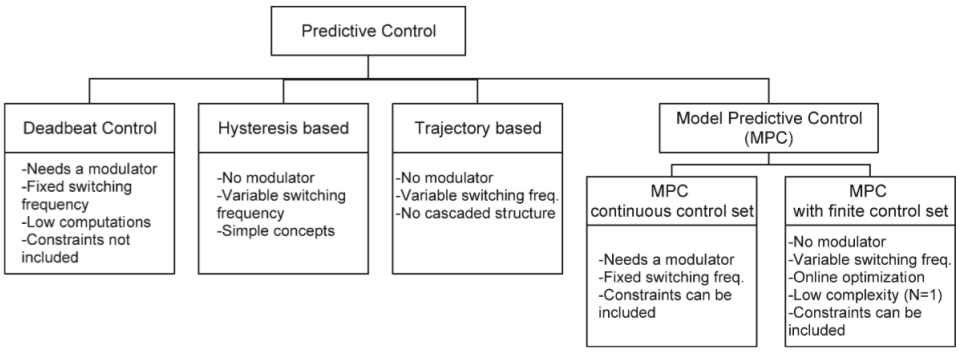


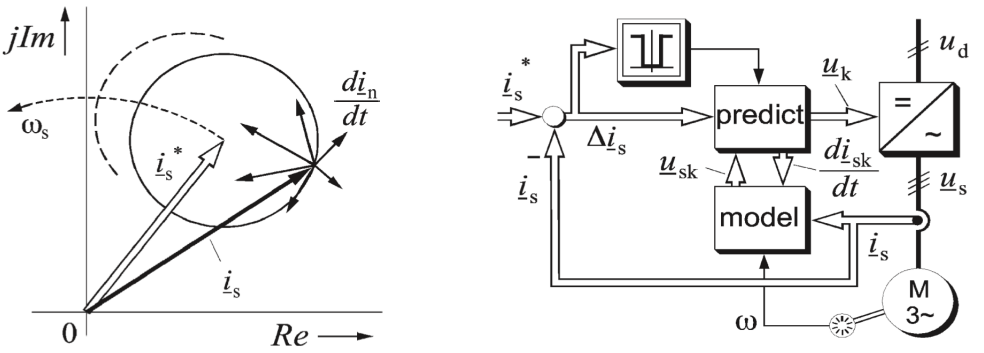
Figure 4.2: Clasification of predictive control method used in power electronics [11]

4.2 Overview of Predictive Control Techniques

4.2.1 Hysteresis based Predictive Control

Hysteresis Based predictive control strategies main concept, is to maintain controlled values of the system between certain bounds, while an optimality criterion is achieved by prediction of system states. Block diagram of hysteresis-based predictive current control is shown in figure 4.3b. Given allowed error boundaries as set by control designer, future switching actions are determined by predictive current control. In figure 4.3b the circular bounded region denotes the allowed area of the controlled variables in dq space, as set by the reference values. When the current reaches the boundaries, switching action of the converter is determined by prediction and optimization stages.

In the prediction stage, trajectory of all possible switching vectors are calculated based on machine model equations and time to reach the boundary line is penalized respectively. In the optimization stage, most promising trajectory based on optimality criterion is selected and applied in next time instant. If



(a) Predictive current control, boundary circle, and space vector

(b) Hysteresis-based predictive control

Figure 4.3: Hysteresis based control system description [11]

minimization of switching frequency, thus switching losses is the targeted objective of the control, which is common for high power converters, trajectory that is predicted to keep current vector inside bounded area for the longest time interval is selected and applied.

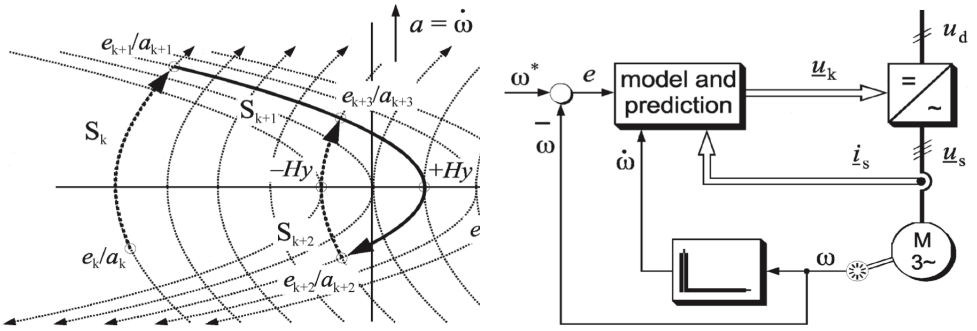
Maximum allowed switching frequency is bounded by the computation time of the algorithm which determines the optimal switching state vector. Many variations of basic hysteresis predictive control, targeting current distortion, emitted EMI, Torque ripple etc. or by altering the bounded area definition.

4.2.2 Trajectory based Predictive Control

Trajectory Based control concept, is to drive the controlled variables of the system, onto precalculated trajectories. Many implementations based on this idea have been presented, like Direct Self Control, Direct mean Torque control and many others like Sliding Mode control and Direct Torque Control, which are a hybrid form of trajectory and hysteresis based predictive control.

Unlike cascaded control, predictive control algorithms offer the possibility to directly control multiple system values. DSPC, shown in figure 4.4a, utilizes no external control loop for speed control, and the switching states applied in the inverter are calculated in a way where speed is directly controlled in a time-optimal manner.

Similar to the methods of [13] and [10], the switching states of the inverter are classified as torque increasing, slowly torque decreasing, or rapidly torque decreasing. For small time intervals, the inertia of the system and the derivatives of machine and load torques are assumed as constant values. The behavior of the system leads to a set of parabolas in the speed error versus acceleration area as shown in figure 4.4b.



(a) Predictive current control, trajectory based principle

(b) Trajectory-based predictive control scheme

Figure 4.4: Trajectory based control system description [11]

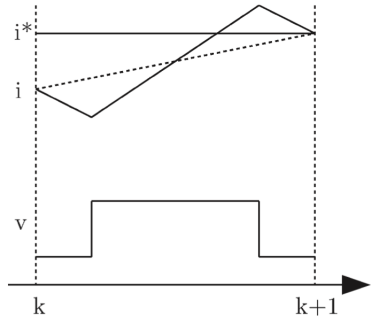
The example of DSPC, illustrates the difference of predictive controllers to linear control systems, that instead of linearizing non linear parts of the controlled system so as to be controllable by PI controllers, precalculated optimal solutions are applied depending on knowledge of the system parameters and state variables. Avoidance of cascaded loops leads to more robust control, capable to drive more complex systems in an optimal way.

4.2.3 Deadbeat Control

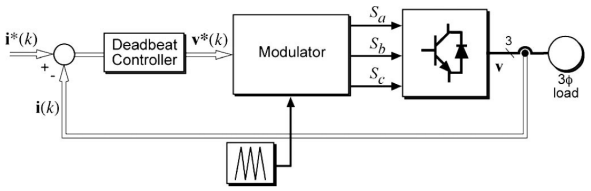
Deadbeat Control can be considered as a different form of predictive controller. Basic principle of this method, is that at every time instant, based on error between reference and measured values of controlled variable, switching state to be applied is selected so as to ideally eliminate the error in next time step, or at least approach the reference value as fast as possible. This kind of predictive controller is used when very fast dynamic response is needed, but has many limitations as unmodeled delays and other errors in the model often deteriorate system performance and may even give rise to instability and non linearities of the controlled system are difficult to incorporate to the control.

In Figure 4.5b a deadbeat current control system is illustrated. This topology is of great resemblance to classic PID control, but instead of the modulator been controlled by the linear controller, it is activated by a deadbeat controller. Main logic of a current deadbeat controller is illustrated in figure 4.5a. At every time instant k, error between measured value and reference value is considered and respective output voltage is selected so as the measured current reaches the reference value in the next time instant k+1.

In real implementations of deadbeat control many issues have to be compensated, with main attention to delays introduced by computation time and



(a) Predictive current control, deadbeat control principle



(b) deadbeat predictive control scheme

Figure 4.5: Deadbeat control system description [11]

modulation. Also another pitfall of deadbeat control is sensitivity to system parameter variation which might lead to instability. Many variations of simple deadbeat implementation exist and many solutions for deadbeat control drawbacks have been proposed.

4.2.4 Model based Predictive Control

Model Predictive Control is the most advanced predictive control technique capable to drive multivariable systems with hard constraints on their output. MPC is also referred as receding horizon control,as the main concept is to mimic an infinite prediction horizon solution by continuously sliding the prediction horizon [14]. Main parts of MPC control are illustrated in figure 4.6. Main difference between finite set and continuous set Model Based MPC is that optimization is done in the relevant space,continuous or discrete. For the case of power converters, the continuous optimization output is passed to a modulator and then translated to a switching state with an optimum duty cycle while the FS-MPC optimization stage outputs directly the optimum switching state for the next time interval. As a consequence CS-MPC yields a constant switching frequency while FS-MPC results to variable switching frequency.

System Model is the most important part of Model Predictive Control. More often model of the plant is derived as the state space model describing the controlled system. In other cases more advanced statistical models might be utilized, i.e ARMAX, but then expression of the system should be given in a transfer function form rather than a state space model representation. An MPC setup is expected to be as successful as the model describing the main plant is. In a finite set MPC is usually described as :

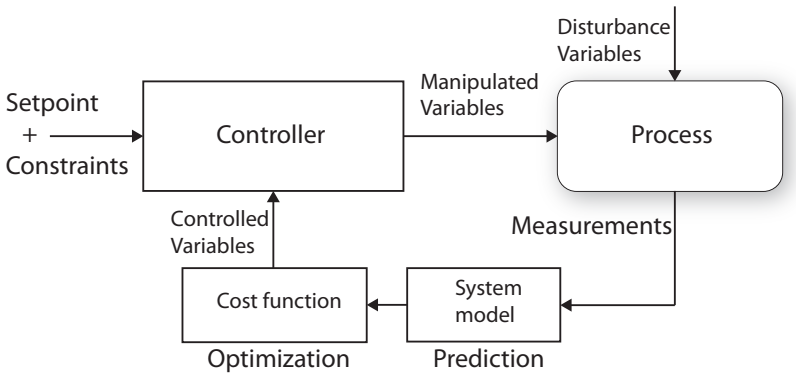


Figure 4.6: MPC generalized block diagram

$$x[k+1] = Ax[k] + Bu[k]$$
$$y[k] = Cx[k] + Du[k]$$

Or in a more general expression, the model is used so as to predict future state by present state and input variables,:

$$x[k+1] = f(x[k], u[k]) \qquad , k \in 1, 2, 3, \ldots$$

To complete the system description the set of constraints imposing on state and input variables must be described. Especially in the case of power electronics where the discrete nature of switching actions denotes absolute constraints in the input variables, constraints description is a key mechanism in the optimization process. In the case of Constrained Model based Predictive Control, a set of constraints for the output variables should be devised as well.

$$u(k) \in \mathcal{U} \subseteq \mathcal{R}^p$$

In continuous set MPC the input variable will reflect a value that belongs in a continuous set, i.e $\mathcal{U} = [0, 1]^p$ where u denotes the pwm duty cycle. In FS-MPC the input will reflect a value that belongs to a discrete set,i.e one of the finite possible switching actions of the power converter. State constraints depend on physical limitations of the described system.

$$x(k) \in \mathcal{X} \subseteq \mathcal{R}^n$$

Cost Function is the heart of the optimization stage that takes place inside the MPC controller. Based on the optimality criterion set by the control

designer, an solution of the MPC algorithm is considered optimal when it minimizes a certain cost function. This function may take several forms and complexity, but the general can be described as present and predicted state and input variable dependent:

$$\mathcal{J} = V(x(k), u(k)) = F(x(k+N)) + \sum_{l=k}^{k+N-1} L(x(l), u(l), u(l-1))$$

Where N is the length of the prediction horizon, and F, L weighting functions which serve to penalize predicted system behavior. Once the optimum solution for the given horizon has been accomplished, it is passed to the output of the controller and the solution algorithm is executed for the next time instant with the prediction horizon has moved by one timestep. The idea of the receding horizon is depicted in figure 4.7

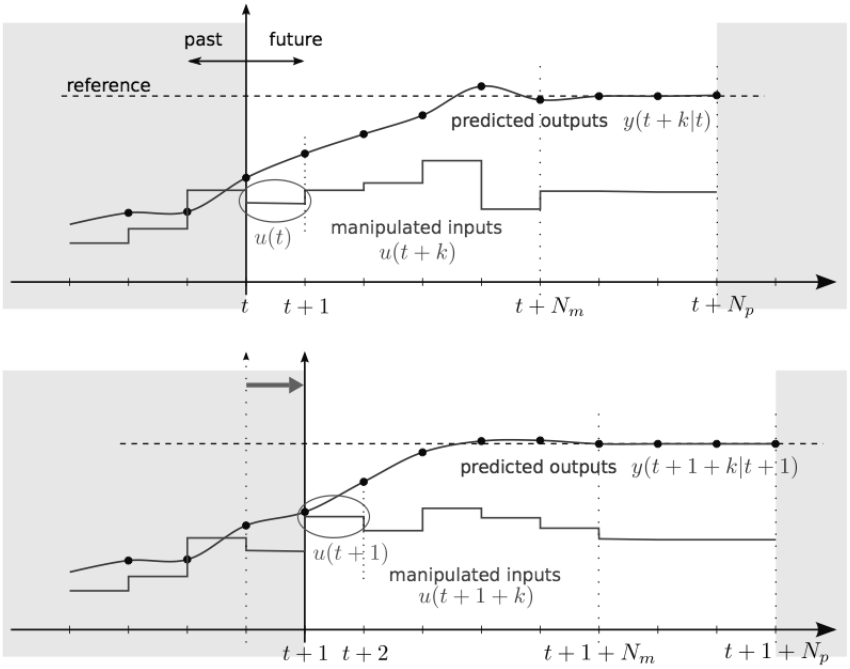


Figure 4.7: MPC Receding Horizon concept [14]

Implementation of FS-MPC solution algorithm will be analytically presented in the following part where the case of Model Predictive Direct Power Control (MPDPC) is presented and analyzed in depth.

CHAPTER

FIVE

LCL FILTER AND DAMPING TECHNIQUES

Filters are used in all power converter systems to interface the grid side, from simple first order inductor to more complex high order filters. LCL filters present great performance in current ripple attenuation but introduce a resonance frequency in the system, which should be compensated in order to guarantee stability of the overall system. Several techniques exist for LCL filter damping, but main categorization is amon passive and active damping.

For reasons of completeness a brief overview of the main characteristics of an LCL filter and the design procedure followed in this thesis is described in the next two sections. A matlab script will be provided in the Appendix where calculations of transfer function characteristics and the design procedure will be automatically generated by input system parameters and specifications and an overview of filter resonance damping techniques will follow

5.1 LCL Filter Overview

An LCL filter consists of 2 series inductors L_{inv}, L_g and one parallel capacitor C_f connected as in figure 5.1. The LCL filter interfaces the converter output to the grid, so the inverter voltage V_{inv} output is depicted as the filter input and the grid voltage V_g on the filter output. By applying Kirchhoff voltage and current equations, 5.1, while considering grid voltage as an ideal voltage source meaning that for the filter analysis it will be considered as a short-circuit for harmonic frequencies, $V_g = 0$, the transfer function of the filter can be derived by equation 5.2. R_{inv}, R_g, R_C are parasitic elements of filter components.

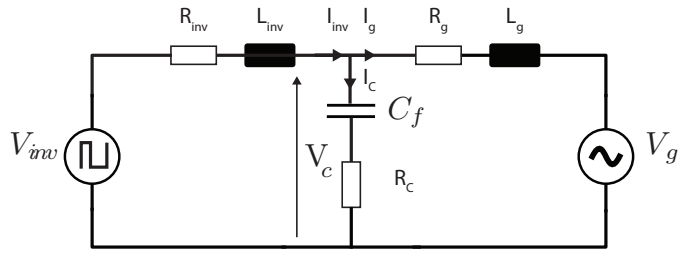


Figure 5.1: LCL output filter schematic

$$
\begin{aligned}
&I_{inv} = I_C + I_g \\
&V_{inv} = I_{inv}(sL_{inv} + R_{inv}) + V_C \\
&V_C = I_g(sL_g + R_g) + V_g \\
&V_C = I_C(\frac{1}{sC_f} + R_{inv}) \\
&V_g = 0
\end{aligned}
\tag{5.1}
$$

$$
\frac{I_g}{V_{inv}} = \frac{sR_CC_f + 1}{\begin{aligned}s^3L_gL_{inv}C_f + s^2C_f(L_g(R_C + R_{inv}) + L_{inv}(R_C + R_g)) + R_g + \\ s(L_g + L_{inv} + C_f(R_cR_g + R_cR_{inv} + R_gR_{inv})) + R_{inv}\end{aligned}} \tag{5.2}
$$

Which for neglecting R_{inv}, R_g, R_C as small, can be expressed as:

$$
\frac{I_g}{V_{inv}} = \frac{1}{s^3L_gL_{inv}C_f + s(L_g + L_{inv})} \tag{5.3}
$$

In figure 5.2 magnitude and phase bode diagrams of an LCL filter transfer function are shown. As it gets obvious a resonance effect occurs at a specific frequency. This resonance frequency can be calculated by equation 5.4 and any harmonics generated by the inverter around this frequency should be avoided or they will be augmented, leading to performance deterioration and possibly to instability.

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_{inv} + L_g}{L_{inv} L_g C_f}} \tag{5.4}$$

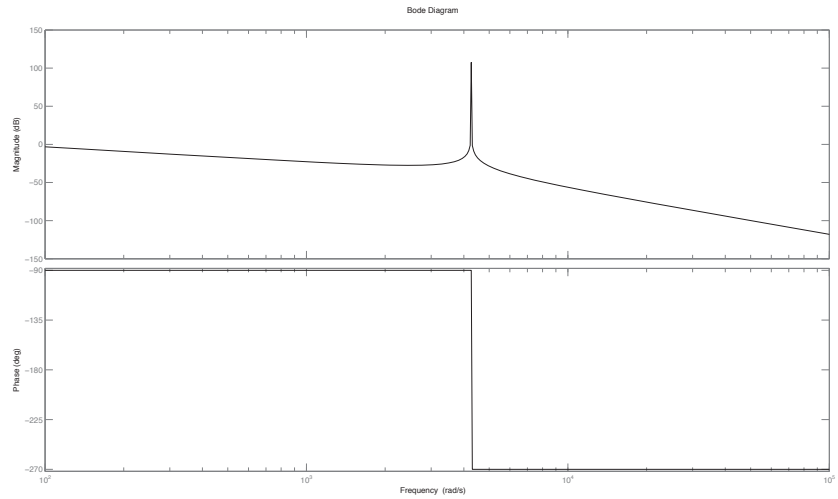


Figure 5.2: Magnitude and Phase response of an LCL filter

5.2 LCL Filter Design

Designing an output LCL filter for an inverter in a systematic approach has been described in [15],[16], and for the three-level NPC converter specifically in [17]. In all cases the design was set for steady switching frequency PWM converters. Since DPC employs variable switching frequency, the LCL filter will be designed for the average switching frequency expected.

First, parameters of the inverter and the grid should be considered. DC link voltage, average switching frequency of the converter, grid line voltage, grid frequency, and output power desired.

Second, resonance frequency of the filter is selected .As a general guideline, the resonance frequency is selected to be at least ten times the fundamental frequency of the generated output and at least half of the average switching frequency[18] .

Then the inverter side inductor is calculated based on the desirable maximum current ripple ΔI_{Lmax} at the inverter output, equation 5.5

$$Linv = \frac{V_{dc}}{16 f_{sw} \Delta I_{Lmax}} \tag{5.5}$$

Current ripple ΔI_{Lmax} refers to the difference between the instantaneous value of the waveform and its fundamental frequency and considering the switching nature of the converter can be calculated by equation 5.6 as a percentage p_L,where P_N is the nominal power of the inverter and V_{ph} the grid phase voltage. A good starting point is a 10% ripple, $p_L = 0.1$.

$$\Delta I_{Lmax} = p_L(\%)\frac{P_N\sqrt{2}}{3V_{ph}} \tag{5.6}$$

After that,filter capacitor value can be selected. The value of the capacitance is limited by the decrease of power factor that occurs, which should remain below 5% at rated power, $p_C = 0.05$. In this particular application where reactive power compensating for the power factor decrease due to the filter capacitor is generated, higher percentage can be used leading to even smaller inductors used in final filter design, as long as current ripple remains acceptable. E_N is the line to line rms voltage and S_N the nominal power.

$$C_f = p_C(\%) \cdot C_b \tag{5.7}$$

$$C_b = \frac{1}{\omega_N Z_b} \tag{5.8}$$

$$Z_b = \frac{E_N^2}{S_N} \tag{5.9}$$

At last grid side inductance can be calculated, such as resonance frequency of the filter defined by equation 5.4 is accomplished. Grid side and inverter side inductance are related with a ratio r, $r = \frac{L_{inv}}{L_g}$, and the relation between the harmonic current generated by the inverter and the current injected into the grid can be calculated as in equation 5.10.

$$\frac{I_g(h)}{I_{inv}(h_{sw})} = \frac{1}{L_g C_f|\omega_{res}^2 - \omega_{sw}^2|} = \frac{1}{|1 + r[1 - (L_{inv}C_f\omega_{sw}^2) \cdot p_C]|} \tag{5.10}$$

When designing output filter of a power converter for grid connected applications, compatibility with grid regulations should be taken into account. Among other factors such as reactive power level, grid short circuit current, voltage fluctuations and flicker, harmonic content of the delivered current should be under

specific limits. This set of limits and regulations is thoroughly described in the IEEE Standard 519-1992, and presents the limits of total harmonic distortion of currents, for voltage levels below 69kV, table 5.1. The limits in the table are calculated for six pulse rectifiers, so when converters with another number of pulses (q) are used, the limits of the harmonic order are increased by a factor $\sqrt{\frac{q}{6}}$ which in the case on the 3 level NPC will be $\sqrt{2}$.

Maximum Harmonic Current Distortion in Percent of I_L Individual Harmonic Order (Odd Harmonics)						
I_{sc}/I_L	< 11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 25$	$35 \leq h$	TDD
< 20	4.0	2	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1	0.5	8.0
$50 < 10$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5	2	1	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonics limits above.						

Table 5.1: Current distortion limits described by IEEE Standard 519-1992

5.3 Passive Damping

Passive damping of the resonant frequency of the filter is achieved by adding a resistance in series or in parallel with the capacitance or inductance of the filter. The four possible positions are shown in figure 5.3 where no parasitic values of the filter are considered.

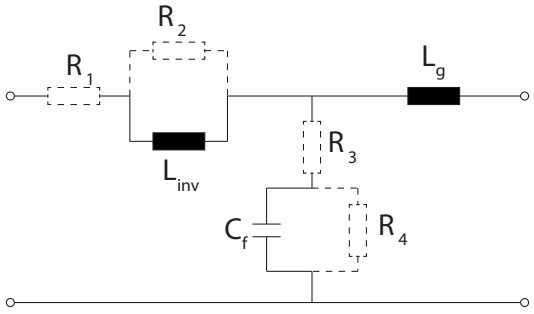


Figure 5.3: possible topologies for passive damping

The effect of the damping resistance placed in each of the four positions is shown in figure 5.4. By observing the bode diagrams, for critical damping values, the parallel to filter capacitor damping resistor, and the the series to converter side inductor damping resistor placement respond as expected, by following the filter response throughout whole frequency range, except the resonance frequency. Also both damping resistor topologies introduce minimal delay compared to the others.

Power losses on a damping resistor R_d can be calculated by:

$$P_d = 3R_d \sum_h [i_i(h) - i_g(h)]^2$$

Since extra power losses on the power converter chain lead to low power efficiency, other methods to actively damp resonant frequency of the filter should be considered. In the next section, three main approaches to active damping through extra control loops in the existing control scheme are reviewed.

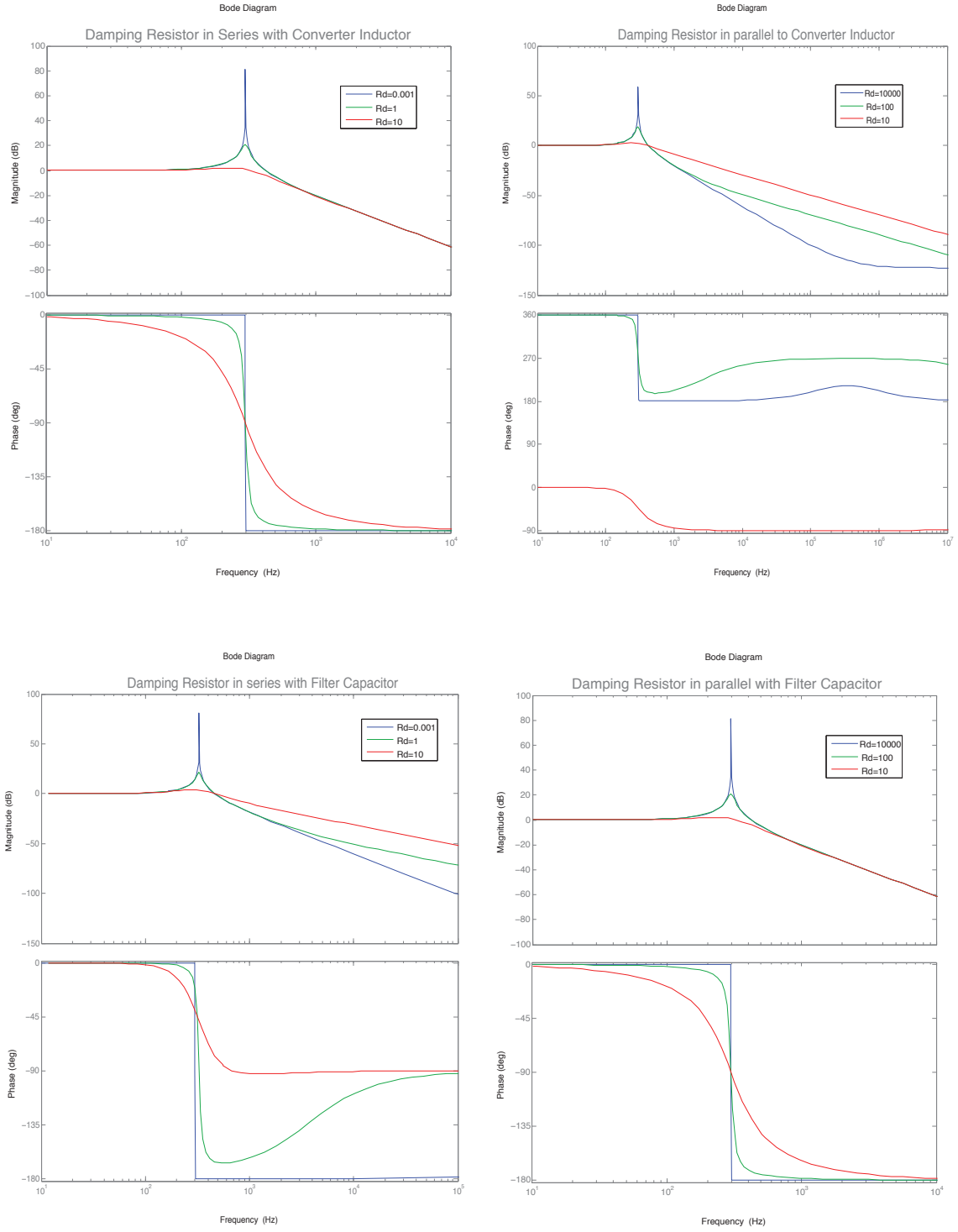


Figure 5.4: Bode plots of LCL filter with passive damping

5.4 Active Damping

5.4.1 Virtual Resistor method

One approach to actively damp unwanted resonant content of the output current due to the LCL filter transfer characteristics, is to mimic the behavior of passive damping resistor previously described, by introducing a virtual resistor in the control loop. Through this extension, damping current that would dissipate onto the damping resistor is calculated and forwarded to the reference value, avoiding physical power losses on the resistor.

As for passive damping, there are four places for the damping resistor to be placed, or a combination of them. Depending on the virtual resistor placement, an extra sensor will be needed, a current sensor if the virtual resistor is considered in series with filter inductor or capacitor, and a voltage sensor if it is considered in parallel.

By considering from the filter equivalent schematic with damping resistor R_d virtually connected parallel to filter capacitor ,figure 5.5, converter side inductor and converter voltage act as a current controlled source, and we can express the transfer function of the system as :

$$\frac{I_g}{I_{inv}} = \frac{\frac{1}{L_g C}}{s^2 + s\frac{1}{R_d C} + \frac{1}{L_g C}}$$

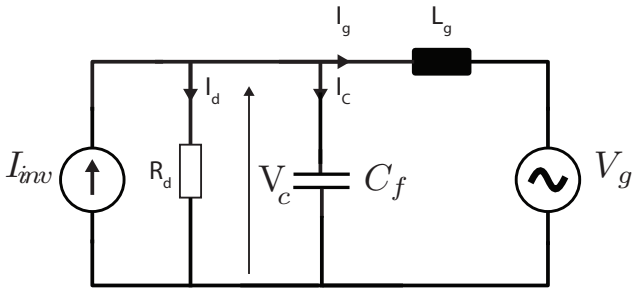


Figure 5.5: LCL filter diagram with converter output and inductor as a current source

Damping current of the virtual resistor is calculated as, $I_d = \kappa_d V_c$, where K_d is the gain $\kappa_d = \frac{1}{R_d}$ of the controllable current source and controls the amount of filter resonance damping applied. By examining filter transfer function as a general form second order system, the undamped natural frequency of the system and damping factor can be calculated based on the filter parameters C, L_g and damping ratio ζ.

$$\omega_n = \sqrt{\frac{1}{L_g C}}$$

$$\kappa_d = 2\zeta\sqrt{\frac{C}{L_g}} = \frac{1}{R_d}$$

An example of a current controlled power converter incorporating virtual resistor concept block diagram is illustrated in figure 5.6

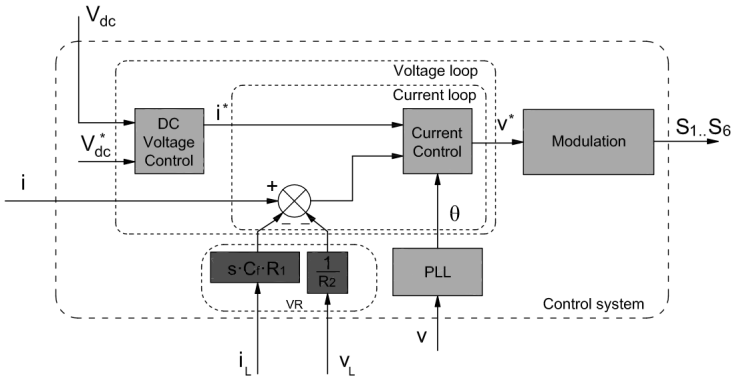


Figure 5.6: Virtual Resistor method Active Damping block diagram [18]

5.4.2 Lead-Lag compensator method

The shift in the phase angle introduced by the filter can be compensated with an lead-lag compensator. The lead compensator has the following equation :

$$L(s) = k_d \frac{T_d s + 1}{\alpha T_d s + 1}$$

The lead compensator adds positive phase to the system. The compensator needs to be tuned to the resonance frequency of the filter.

An active damping method using a lead-lag compensator is described in [19]. This method uses a lead-lag element in the synchronous reference frame applied to the feedback from the capacitor voltage, figure 5.7

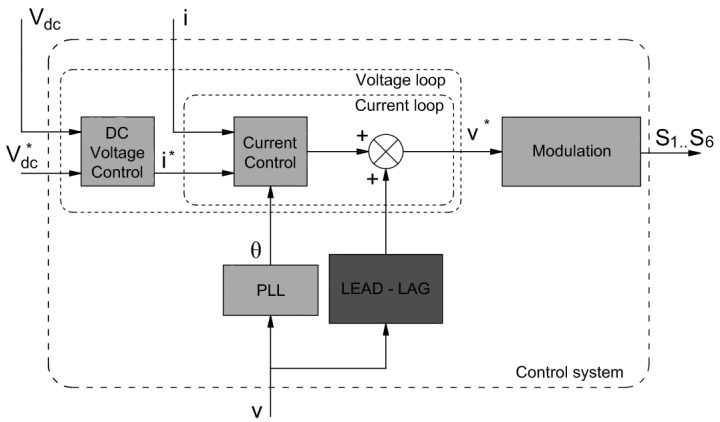


Figure 5.7: Lead-Lag compensator method Active Damping block diagram [18]

The grid voltages are used both for the grid synchronization and for the active damping. First, they are transformed in the reference frame the controller works with and then inputed to a lead-lag block. Then, the output from the lead-lag block are added to the output of the current regulators and then processed to obtain the duty cycles to be sent to the inverter.

5.4.3 Notch Filter method

This method consists of adding a filter in series with the reference voltage of the modulator, figure 5.8

The basic idea can be explained in the frequency domain by introducing a negative peak (notch) in the system, that compensates for the resonant peak due to the LCL filter [20]. This can be done by adding a notch filter in the current loop. The frequency of the Notch filter has to be tuned at the resonance frequency of the LCL filter, in order to provide a good damping.

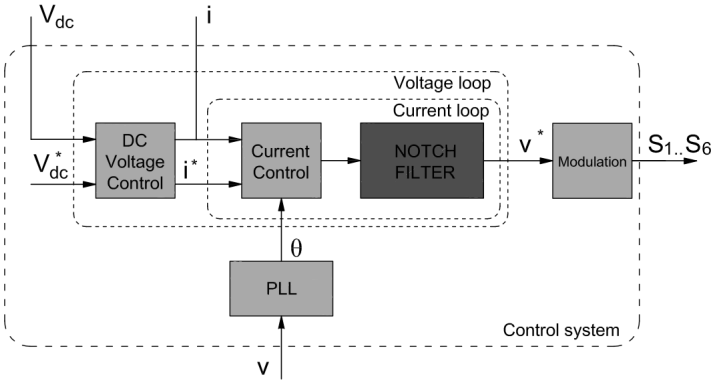


Figure 5.8: Notch Filter method Active Damping block diagram [18]

Part II

Analysis and Comparative Study of DPC and MPDPC techniques

CHAPTER

SIX

DIRECT POWER CONTROL

Direct Power Control of DC/AC inverter stems from the well known Direct Torque Control of AC machines,based on the similarity of an induction motor's electric equivalent circuit to the output load and the grid connection equivalent of a DC/AC inverter. Basic principles of DTC are incorporated in the DPC technique in order to control active and reactive power at the inverter terminals, in the same manner as torque and flux of an induction motor are controlled in DTC. Key differences of DPC from vector control are that no modulator is used,leading to a variable switching frequency output, and that current is regulated indirectly, in terms of active and reactive power.

The basic control scheme of DPC is that, active and reactive power are calculated and are fed to hysteresis controllers whose output, together with grid voltage angle information select the optimum switching state from a predefined lookup table. As it is obvious, both accurate calculation of active-reactive power and correct design of the switching table is critical. System quality parameters can be tuned through the hysteresis controllers, either by utilizing a multilevel controller or by tightening them bounds, or through a different design approach of the lookup table. More control loops might exist, like midpoint voltage balancing as in the case of 3 level NPC inverter but a more in depth analysis of the case specific DPC scheme will be presented in the next section. Usually active power reference of the P hysteresis controller is set by a PI loop monitoring the DC bus voltage and the reactive power reference of the Q hysteresis controller is set to zero to assure unity power factor at the converter terminals.

6.1 DPC of 3 level NPC

Direct Power Control of a 3 level NPC inverter is shown on the block diagram in figure 6.1 .

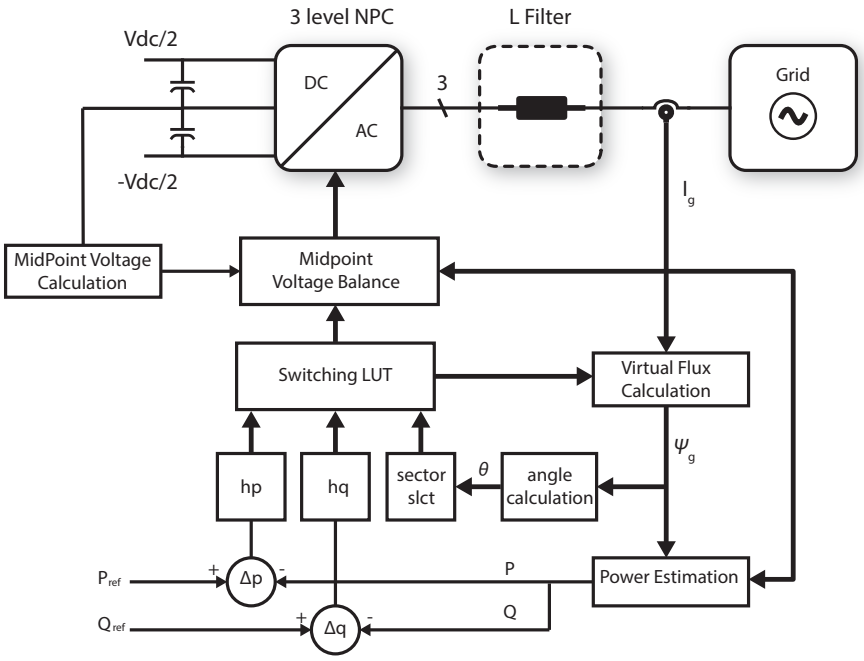


Figure 6.1: 3 level NPC Direct Power Control Block Diagram

Measurements of current in the three phases of the VSI [1] and voltage across two DC link capacitors are performed. A *virtual flux estimator* is employed, to calculate virtual flux at the output of the inverter, based on current measurements and voltage output of the inverter which can be estimated from the switching state and the DC link voltage. Based on virtual flux, active and reactive power are estimated in a *PQ estimator* and are fed to the P and Q *hysteresis controllers*. Also angle information of the connected grid voltage is acquired from virtual flux which is fed to a *sector decision control block* where it is determined in which sector of the $\alpha\beta$ plane the virtual flux vector is moving. From the hysteresis controllers and the sector decision control block outputs the next switching output,or better the next inverter voltage vector in the $\alpha\beta$ plane , is selected from an existing *switching Look Up Table*. The inverter voltage vector is fed in a *midpoint voltage balancing* control block where it gets translated to the switching control signals, in respect to the voltage balancing action.

As it gets obvious, the control loop must be executed very fast in order to have a properly functioning system with accurate power estimation and fast switching state determination, demanding a control system with fast processing resources which might be a serious drawback of the DPC control method in certain applications. On the other hand use of virtual flux and absence of dq coordinate transformations allow for very fast control loop of a DPC imple-

[1] only two phase current measurements are needed if the system is considered balanced

mentation with most modern processors available. Next each control block is analysed in depth.

6.1.1 Virtual Flux

Due to the resemblance of a grid connected NPC inverter to the stator equivalent of an AC motor with resistance and inductance of grid side connection resembling the stator resistance and leakage inductance, while grid voltage is similar to motor's electro-motive force, a virtual measurement can be considered, that of virtual flux. Virtual flux is defined in the same way as magnetic stator flux linkage would be, by integrating stator voltage, hence grid side virtual flux can be estimated by integrating grid voltage,as in equation 6.1. Without the use of virtual flux concept, when calculating active and reactive power, derivation of the grid side current would be needed which would lead to added distortion due to extra noise present in the control loop.

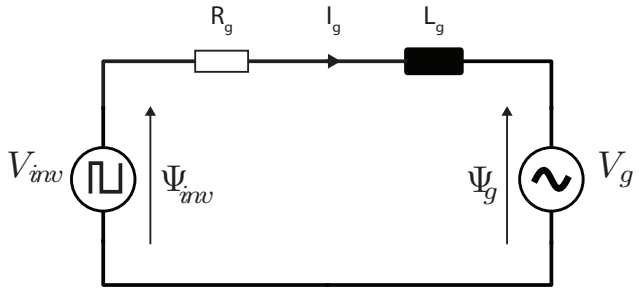


Figure 6.2: grid connected VSI equivalent circuit

$$\psi_g = \int V_g \, \mathrm{d}t \tag{6.1}$$

$$\psi_g = \int (V_{inv} - R_g \cdot I_g) \, \mathrm{d}t - L_g \cdot I_g \tag{6.2}$$

Which for neglecting series resistance transforms to:

$$\psi_g = \int V_{inv} \, \mathrm{d}t - L_g \cdot I_g \tag{6.3}$$

Voltage inverter V_{inv} can be estimated by the measured DC link voltage and knowledge of the current switching state, and after the $\alpha\beta$ transformation

inverter output voltage can be calculated by:

$$\begin{aligned} V_{invR} &= S_R \cdot V_{dc} \\ V_{invS} &= S_S \cdot V_{dc} \\ V_{invT} &= S_T \cdot V_{dc} \end{aligned}$$

$$\begin{aligned} V_{inv\alpha} &= \frac{V_{dc}/2}{3}(2S_R - S_S - S_T) \\ V_{inv\beta} &= \frac{V_{dc}/2}{\sqrt{3}}(S_S - S_T) \end{aligned} \tag{6.4}$$

And Virtual Flux can finally be estimated by equations:

$$\begin{aligned} \psi_{g\alpha} &= \int V_{inv\alpha}\,\mathrm{d}t - L_g \cdot I_{g\alpha} \\ \psi_{g\beta} &= \int V_{inv\beta}\,\mathrm{d}t - L_g \cdot I_{g\beta} \end{aligned} \tag{6.5}$$

In practice when integrating a measured voltage, a dc value is present, which in steady state can be calculated as $\frac{V_{dc}}{\omega_s}$. In order to avoid rounding errors of dc offset subtraction and make the virtual flux calculation less immune to noise the pure integrator is replaced by a first order low pass filter with a cut off frequency at 5 Hz. Phase and magnitude compensation is followed as presented in [21] and [22] for virtual flux estimation in a induction machine stator.
Calculating inverter flux with pure integration in the frequency domain

$$\psi_{inv} = \frac{V_{inv}}{j\omega} \tag{6.6}$$

Calculating inverter flux with low pass filter with a cut off frequency f_c:

$$\psi'_{inv} = \frac{V_{inv}}{j\omega + \omega_s} \tag{6.7}$$

Solving equation 6.7 for V_{inv} and replacing in equation 6.6 we can relate the calculated inverter flux from the pure integrator with the low pass filter technique as

$$\psi_{inv} = \psi'_{inv} - j\frac{\omega_c}{\omega}\psi'_{inv} \tag{6.8}$$

Which in the $\alpha\beta$ plane can be expressed as in equation 6.9 and the implemented control block can be summarized in figure 6.3 where grid flux is derived by subtracting quantity $L_g \cdot I_g$ from the calculated inverter flux, as described in equation 6.3

$$\begin{aligned} \psi_{inv\alpha} &= \psi'_{inv\alpha} + \frac{\omega_c}{\omega}\psi'_{inv\beta} \\ \psi_{inv\beta} &= \psi'_{inv\beta} - \frac{\omega_c}{\omega}\psi'_{inv\alpha} \end{aligned} \tag{6.9}$$

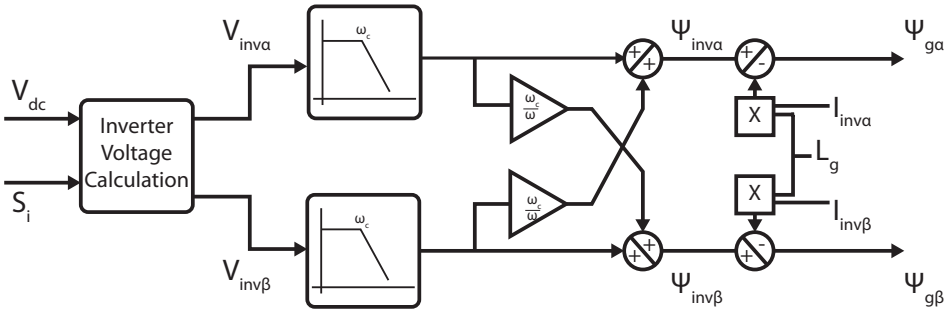


Figure 6.3: Virtual flux calculation block diagramm

6.1.2 Power Calculation

As previously explained, fast and accurate estimation of active and reactive power is critical in Direct Power Control. In order to avoid complex calculations and rotating coordinate transformations, power is calculated in the $\alpha\beta$ reference frame from virtual flux already calculated by the previously described estimator. According to the space vector theorem, instantaneous power can be calculated by real and imaginary product of voltage vector and the conjugate current vector:

$$p = \frac{3}{2}\Re\{\vec{V_g}\vec{I_g^*}\}$$
$$q = \frac{3}{2}\Im\{\vec{V_g}\vec{I_g^*}\} \tag{6.10}$$

Grid Line voltage can be expressed by virtual flux $\vec{\psi_g} = \psi_g e^{j\omega t}$ as:

$$\vec{V_g} = \frac{d}{dt}\vec{\psi_g} = \frac{d}{dt}\psi_g e^{j\omega t} = \frac{d\psi_g}{dt}e^{j\omega t} + j\omega\psi_g e^{j\omega t} = \frac{d\psi_g}{dt}e^{j\omega t} + j\omega\vec{\psi_g} \tag{6.11}$$

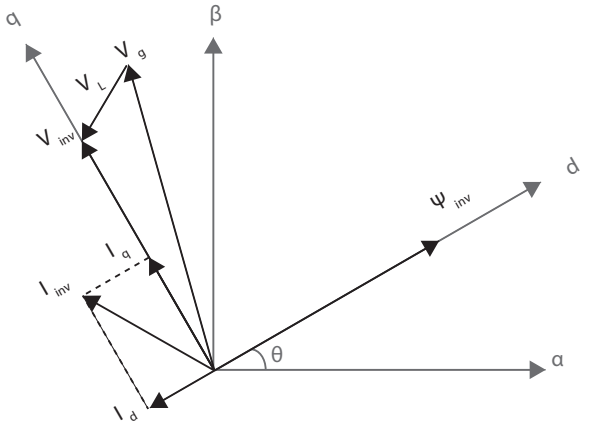


Figure 6.4: Reference coordinates and vectors

Replacing equation 6.11 in equations 6.10 considering the dq coordinates where $\vec{\psi_g} = \psi_{gd}$ instantaneous power is calculated by:

$$p = \frac{3}{2}[\frac{d\psi_{gd}}{dt}i_{gd} + \omega\psi_{gd}i_{gq}]$$
$$q = \frac{3}{2}[-\frac{d\psi_{gd}}{dt}i_{gq} + \omega\psi_{gd}i_{gd}] \tag{6.12}$$

which for sinusoidal and balanced line voltages, where $\frac{d\psi_{gd}}{dt} = 0$ are simplified to:

$$\begin{aligned} p &= \frac{3}{2}\omega\psi_{gd}i_{gq} \\ q &= \frac{3}{2}\omega\psi_{gd}i_{gd} \end{aligned} \tag{6.13}$$

In a same manner considering $\alpha\beta$ coordinates, line voltage V_g is expressed by equation 6.14 and instantaneous power can be calculated by equations 6.16 which for sinusoidal and balanced line voltages, where $\frac{d\psi_g}{dt} = 0$ is simplified to equation 6.17

$$\vec{V_g} = \left.\frac{d\psi_g}{dt}\right|_\alpha + j\left.\frac{d\psi_g}{dt}\right|_\beta + j\omega(\psi_{g\alpha} + j\psi_{g\beta}) \tag{6.14}$$

$$\vec{V_g}\vec{I_g^*} = \left[\left.\frac{d\psi_g}{dt}\right|_\alpha + j\left.\frac{d\psi_g}{dt}\right|_\beta + j\omega(\psi_{g\alpha} + j\psi_{g\beta})\right](I_{g\alpha} - jI_{g\beta}) \tag{6.15}$$

$$\begin{aligned} p &= \frac{3}{2}\left[\left.\frac{d\psi_g}{dt}\right|_\alpha I_{g\alpha} + \left.\frac{d\psi_g}{dt}\right|_\beta I_{g\beta} + \omega(\psi_{g\alpha}I_{g\beta} - \psi_{g\beta}I_{g\alpha})\right] \\ q &= \frac{3}{2}\left[\left.\frac{d\psi_g}{dt}\right|_\alpha I_{g\beta} + \left.\frac{d\psi_g}{dt}\right|_\beta I_{g\alpha} + \omega(\psi_{g\alpha}I_{g\alpha} + \psi_{g\beta}I_{g\beta})\right] \end{aligned} \tag{6.16}$$

$$\begin{aligned} p &= \frac{3}{2}\omega(\psi_{g\alpha}I_{g\beta} - \psi_{g\beta}I_{g\alpha}) \\ q &= \frac{3}{2}\omega(\psi_{g\alpha}I_{g\alpha} + \psi_{g\beta}I_{g\beta}) \end{aligned} \tag{6.17}$$

For comparison, instantaneous power calculations from voltage quantities are noted ,as presented in [23]. Equation 6.10 considering the abc three phase system is transformed to:

$$p = v_a i_a + v_b i_b + v_c i_c$$
$$q = \frac{1}{\sqrt{3}}(v_{bc} i_a + v_{ca} i_b + v_{ab} i_c) \tag{6.18}$$

which for a voltage sensorless system can be transformed to:

$$p = L\left[\frac{di_a}{dt} i_a + \frac{di_b}{dt} i_b + \frac{di_c}{dt} i_c + V_{dc}(s_a i_a + s_b i_b + s_c i_c)\right]$$
$$q = \frac{1}{\sqrt{3}}\left[3L(\frac{di_a}{dt} i_c - \frac{di_c}{dt} i_a) - V_{dc}[s_a(i_b - i_c) + s_b(i_c - i_a) + s_c(i_a - i_b)]\right] \tag{6.19}$$

6.1.3 Hysteresis Controllers

The estimated active and reactive power P,Q are fed to the hysteresis controllers, where they are compared with their respective reference values. Depending on number of levels and type of the hysteresis controllers their output varies. Normally reactive power reference is set to zero, so as to guarantee unity power factor at the converter terminals, and active power reference is usually set by an external PI controller with feedback from the dc link voltage measurement.

Following the investigation on different hysteresis controllers and switching tables for DPC done by [24] ,[25] and since main objective of the thesis is minimization of switching losses, the 2 level p hysteresis and 2 level q hysteresis control of conventional DPC were adopted in first place. While maintaining a low switching frequency, and stable dV/dt switching operation the simple 2 level implementation of the q hysteresis controller results in periodic spikes and notches of reactive power Q, which increase linearly with active power. In order to maintain reactive power bounded, a 3 level asymmetric hysteresis controller was used ,in a similar way as described for DTC in [26]. Output of P,Q hysteresis controllers h_p, h_q is summarized by the following equations

$$\Delta p = p_{ref} - p$$
$$\Delta q = q_{ref} - q$$

$$h_p = \begin{cases} 1 & \text{if } \Delta p \geq P_{bound} \\ 1 & \text{if } -P_{bound} \leq \Delta p \leq P_{bound}\ AND\ \frac{d\Delta p}{dt} < 0 \\ 5 & \text{if } -P_{bound} \leq \Delta p \leq P_{bound}\ AND\ \frac{d\Delta p}{dt} > 0 \\ 5 & \text{if } \Delta p \leq -P_{bound} \end{cases}$$

$$h_q = \begin{cases} 2 & \text{if } \Delta q < -2Q_{bound} \\ 2 & \text{if } \Delta q < 0\ AND\ \frac{d\Delta q}{dt} > 0 \\ 1 & \text{if } -2Q_{bound} < \Delta q < -Q_{bound}\ AND\ \frac{d\Delta q}{dt} < 0 \\ 1 & \text{if } 0 < \Delta q < Q_{bound}\ AND\ \frac{d\Delta q}{dt} > 0 \\ 0 & \text{if } -Q_{bound} < \Delta q < 0\ AND\ \frac{d\Delta q}{dt} < 0 \\ 0 & \text{if } Q_{bound} < \Delta q < 2Q_{bound}\ AND\ \frac{d\Delta q}{dt} > 0 \\ -1 & \text{if } \Delta q > 2Q_{bound} \\ -1 & \text{if } \Delta q > 0\ AND\ \frac{d\Delta q}{dt} < 0 \end{cases}$$

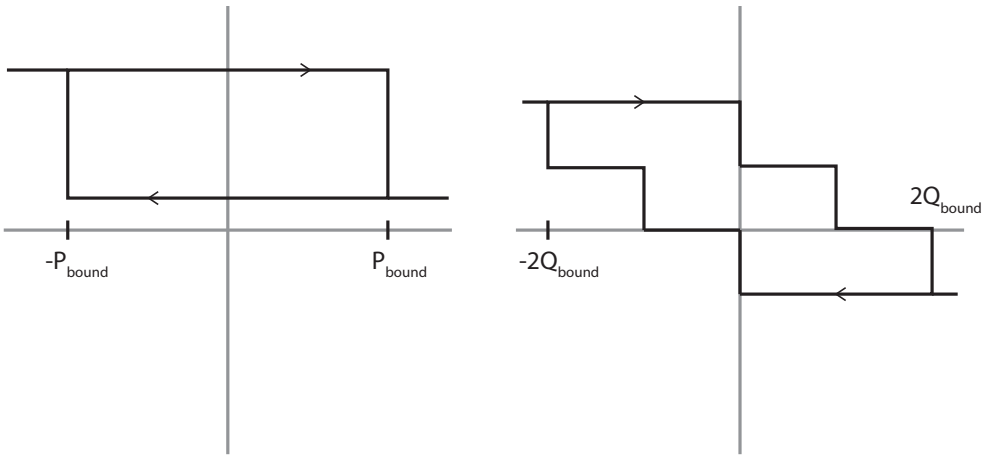


Figure 6.5: Behavior of p,q hysteresis controllers

Where P_{bound} and Q_{bound} are the p,q hysteresis controller bounds respectively, set by the programmer. Once the DPC switching table has been designed, width of the hysteresis controllers ,area from negative to positive bound,

plays a major role in DPC and is the main mechanism to control quality parameters such as power pulsation, current harmonic distortion, average switching frequency and power losses, with a trade of among the two first with the two last mentioned.

6.1.4 Sector decision

As explained in the three-level NPC section, there is a set of 27 voltage vectors an NPC inverter can deliver, and each inverter voltage vector, or similarly virtual flux vector, can alter active and reactive power in a different way depending on position of grid voltage vector, or virtual flux vector similarly. So in order to make a decision on which voltage vector to switch, knowledge of the grid voltage or virtual flux vector position,is needed.Due to the discrete nature of DPC, the $\alpha\beta$ plane is divided in 12 sectors of 30^o resolution as in figure 6.6, and depending on grid virtual flux angle estimation the sector that the virtual flux is moving in is selected.

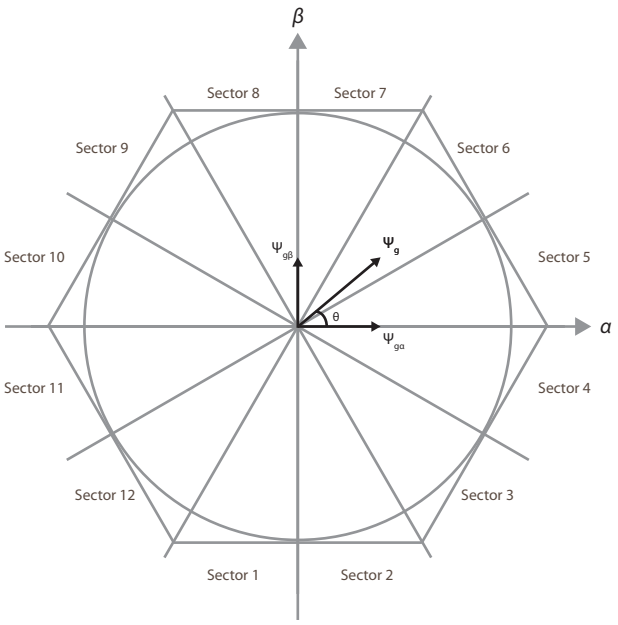


Figure 6.6: $\alpha\beta$ plane divided into 12 sectors

Since a virtual flux estimator is utilized, the grid virtual flux position is tracked by calculating the angle θ of the vector with the α axis, by calculating the arctangent of $\frac{\psi_\beta}{\psi_\alpha}$. For reasons of easier computation the atan2 standard function is used.

$$\theta = atan2(\frac{\psi_\beta}{\psi_\alpha}) \quad , 0 \leq \theta \leq 360 \tag{6.20}$$

And the sector n in which the virtual flux vector lies can be defined by equation 6.21

$$(n-4)\frac{\pi}{6} \leq sector\ n \leq (n-3)\frac{\pi}{6} \quad \text{where n=1,2 ... 12} \tag{6.21}$$

In case of a distorted grid voltage,the previously described method of synchronizing inverter voltage output to the grid, would be problematic. In such a case, use of a more accurate technique, like using a pll to continuously track grid virtual flux frequency, would be imperative. Since no case of distorted grid situations will be evaluated in this thesis, the angle estimation is left as is.

6.1.5 Switching Table

Design of the Lookup switching table is the main ingredient of a DPC algorithm. The main DPC control loop, every time instant it is executed, depending on the hysteresis controllers and the sector decision block ,selects the more adequate next switching state. As so the switching look up table is a 2 dimensional table which one dimension is determined by sector number and the other by hysteresis controllers combined output.

For each sector that grid virtual flux vector might lie, an analysis of how each possible inverter voltage vector influences active and reactive power is performed, and Switching table is predetermined before the online application. The mechanism in which inverter voltage vector to be applied alters the overall inverter flux can be shown with an example. As mentioned in [22] if we consider every time instant very small, the applied inverter voltage vector will create a difference in inverter virtual flux with the same direction as the inverter voltage vector and its magnitude proportional to the time length it is applied:

$$\Delta\vec{\psi}_{inv} = \vec{V_{inv}} \cdot \Delta t \tag{6.22}$$

If ψ_{inv}^{t+1} is the total inverter virtual flux in the next time instance after the selected inverter voltage vector has been applied, and ψ_{inv}^{t} the previous total inverter flux, then:

$$\psi_{inv}^{t+1} = \psi_{inv}^{t} + \Delta\psi_{inv} \tag{6.23}$$

Previously described flux modulation, can be depicted for sector one and for switching vector 5 in figure 6.7. The new total virtual flux of the inverter will yield a different power output. Examining the previous and current Current vectors $\vec{i^t}, \vec{i^{t+1}}$ and their dq counterparts, by instantaneous power theorem equations 6.13 and the fact that in the dq plane the grid virtual flux is synchronously rotating with the d axis, an evaluation of the active and reactive power variation can be made.

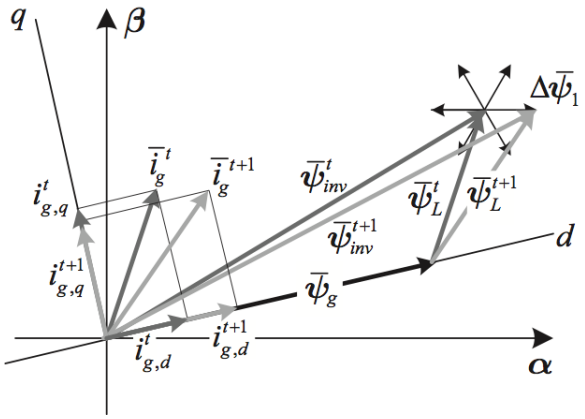


Figure 6.7: Effect of inverter output switching vector on virtual flux, active and reactive power, figure from [22]

Using the mentioned vector analysis, an evaluation of how each inverter switching vector affects active and reactive power on each sector can be made and set up the switching table of the DPC technique according to hysteresis controllers demands. A more analytical approach can be done in same way presented in [27] for voltage based power calculations, by considering rate of change in active and reactive power $\frac{dP}{dt}, \frac{dQ}{dt}$ that every inverter switching vector presents while in each sector.

By differentiating equations 6.17 while considering a balanced symmetrical grid such as equations 6.24 are true, the power variations can be expressed by equations 6.25.

$$\left.\begin{aligned}\psi_{g\alpha} &= \psi_g \sin(\omega t)\\ \psi_{g\beta} &= -\psi_g \cos(\omega t)\end{aligned}\right\} \Rightarrow \quad \begin{aligned}\frac{d\psi_{g\alpha}}{dt} &= -\omega\psi_{g\beta}\\ \frac{d\psi_{g\beta}}{dt} &= \omega\psi_{g\alpha}\end{aligned} \tag{6.24}$$

$$\begin{aligned}\frac{dP_g}{dt} &= \frac{3\omega}{2}\left(\frac{d\psi_{g\alpha}}{dt}I_{g\beta} + \psi_{g\alpha}\frac{I_{g\alpha}}{dt} + \frac{d\psi_{g\beta}}{dt}I_{g\beta} + \psi_{g\beta}\frac{I_{g\beta}}{dt}\right)\\ \frac{dQ_g}{dt} &= \frac{3\omega}{2}\left(\frac{d\psi_{g\alpha}}{dt}I_{g\alpha} + \psi_{g\alpha}\frac{I_{g\beta}}{dt} - \frac{d\psi_{g\beta}}{dt}I_{g\alpha} - \psi_{g\beta}\frac{I_{g\alpha}}{dt}\right)\end{aligned} \tag{6.25}$$

Applying Kirchhoff's voltage law on the simplified grid connected converter circuit, figure 6.2, while neglecting series resistance as small, current derivatives can be expressed by equation 6.26.

$$\begin{aligned}\frac{dI_\alpha}{dt} &= \frac{1}{L}(V_{inv\alpha} - V_{g\alpha}) = \frac{\omega}{L}(\psi_{g\beta} - \psi_{inv\beta})\\ \frac{dI_\beta}{dt} &= \frac{1}{L}(V_{inv\beta} - V_{g\beta}) = \frac{\omega}{L}(\psi_{inv\alpha} - \psi_{g\alpha})\end{aligned} \tag{6.26}$$

Where $\alpha\beta$ component of voltage have been transformed to virtual flux by simply considering that voltage is leading 90^o degrees in the static reference frame as seen in figure 6.8 ,equations 6.27

$$\begin{aligned}\psi_{inv\alpha} &= \frac{V_{inv\beta}}{\omega}\\ \psi_{inv\beta} &= -\frac{V_{inv\alpha}}{\omega}\end{aligned} \tag{6.27}$$

Substituing 6.26,6.24 and 6.17 in 6.25, it can be reduced to equation 6.28

$$\begin{aligned}\frac{dP_g}{dt} &= -\frac{3\omega^2}{2L}\left[\psi_{g\alpha}^2 + \psi_{g\beta}^2 - (\psi_{g\alpha}\psi_{inv\beta} + \psi_{g\beta}\psi_{inv\beta})\right] - \omega Q\\ \frac{dQ_g}{dt} &= -\frac{3\omega^2}{2L}\left[(\psi_{g\beta}\psi_{inv\alpha} - \psi_{g\alpha}\psi_{inv\beta})\right] + \omega P\end{aligned} \tag{6.28}$$

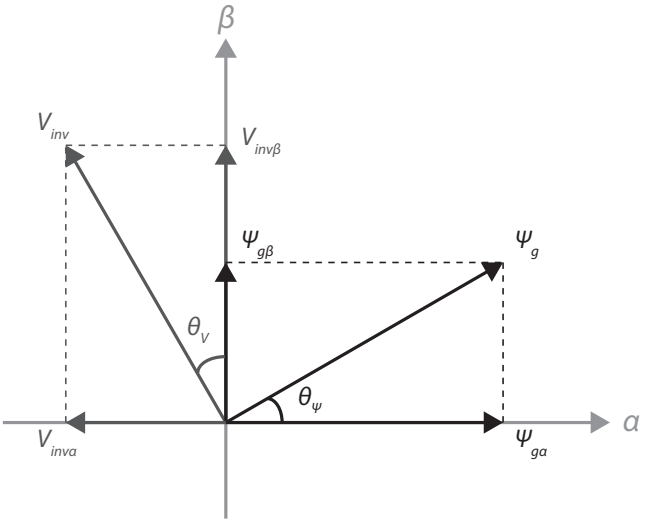


Figure 6.8: Voltage and Virtual Flux relation

Number of sectors	12
Grid Line Voltage	380V
DC bus Voltage	600V
Grid Frequency	50Hz
per phase Inductance	10mH

Table 6.1: grid characteristics for power variation evaluation example

Evaluating active and reactive power derivatives in every sector for every switching vector is a tedious task, so a matlab script has been used. The script divides the plane in N sectors ,depending on resolution needed, and calculates P,Q derivatives in each sector for every switching vector assuming that grid virtual flux vector lies in the middle of the specific sector. Although grid parameters like frequency, grid voltage and grid inductance are needed, most important aspect is the ratio of dc bus voltage to grid line voltage. This ratio is indicating the analogy of grid virtual flux to inverter virtual flux, and the radius grid flux covers in the static reference frame in relation to small and large inverter voltage hexagons as formed by inverter voltage vectors.

Using the previously mentioned script, an evaluation of variation rates of active and reactive power is made for a grid connected converter with the following characteristics, table 6.1 , and the results can be visualised by vector map 6.9 and surface plot 6.11 for active power and 6.10 ,6.12 for reactive power.

The surface plots are done for 360 sectors, so as to obtain a one degree

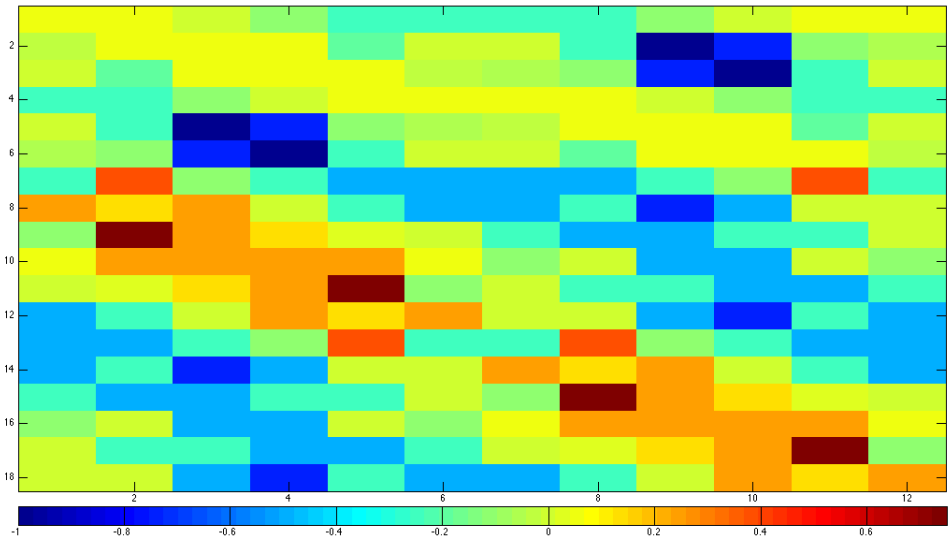


Figure 6.9: Active Power variation vector map

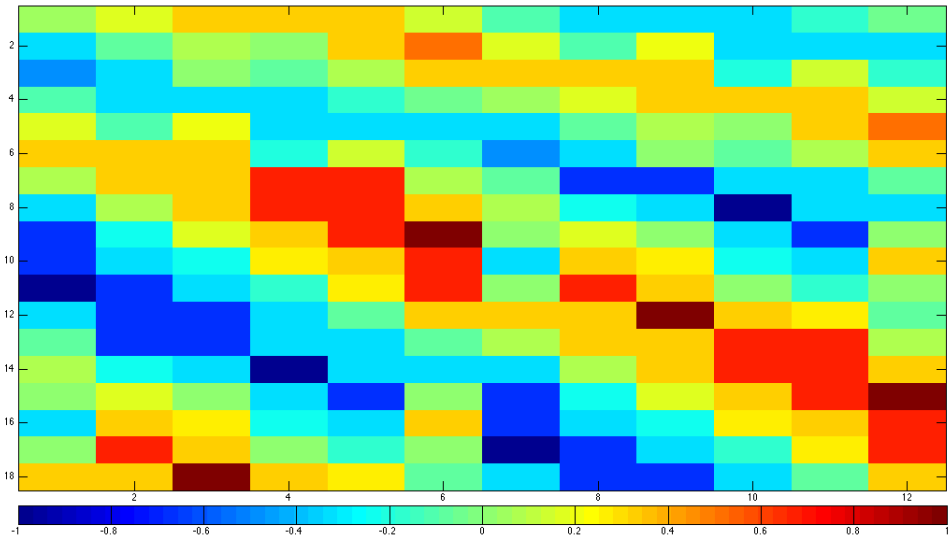


Figure 6.10: Reactive Power variation vector map

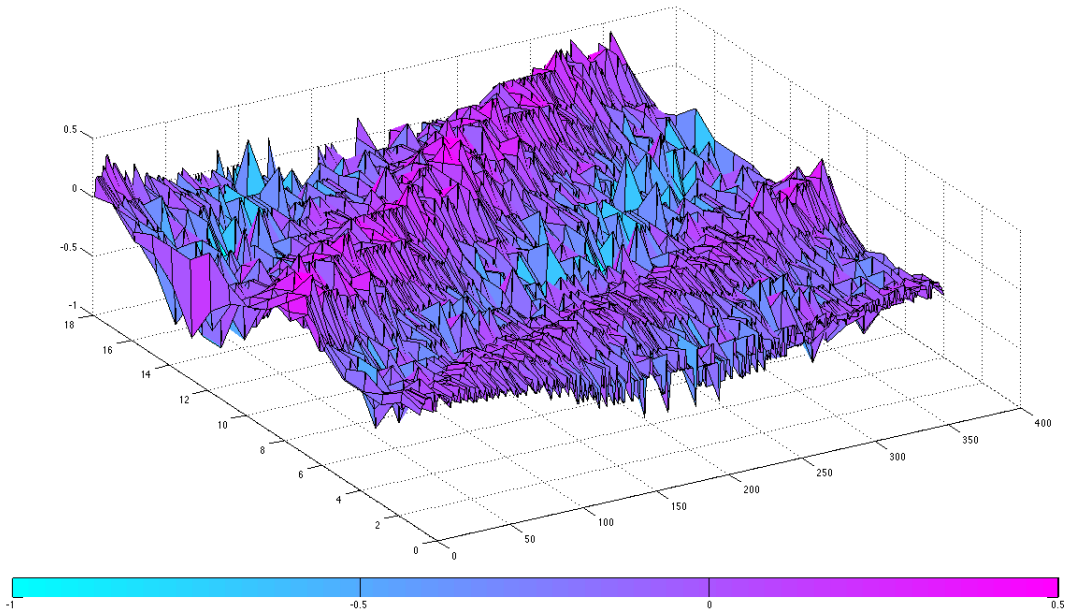


Figure 6.11: 360 sector resolution surface plot of Active power variation

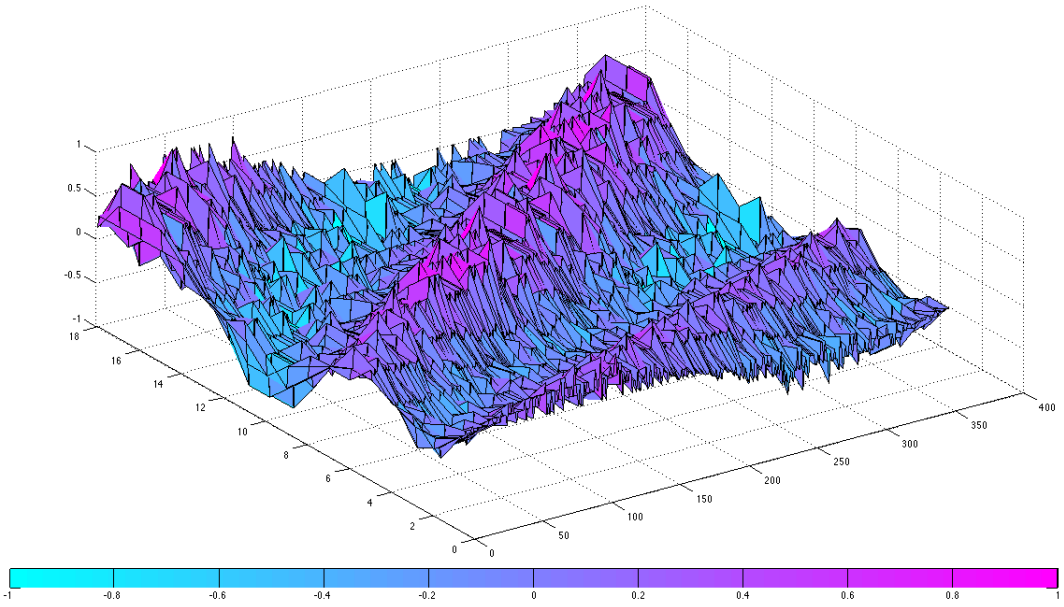


Figure 6.12: 360 sector resolution surface plot of Reactive power variation

resolution, during a whole period. Power variation magnitude is normalized to maximum power variation in each case. The script also attempts to automatically design the final switching lookup table, considering a combination among higher variation rates, inverter transition rules(high dV/dt, neighbouring vectors etc.) and switching transitions cost. The whole matlab script and more comments on it are available on the appendix. Using previous analysis, we can form the final switching table ,table 6.2 each inverter voltage vectors will be selected during each sector. Line index is obtained by the sum of p,q hysteresis controllers $LineIndex = h_p + h_q$ and column index by sector recognition, equation 6.21.

Power Demand	Sector Number PQindex	1	2	3	4	5	6	7	8	9	10	11	12
$P+Q++$	0	7	8	9	10	11	12	13	14	15	16	17	18
$P+Q+$	1	7	8	9	10	11	12	13	14	15	16	17	18
$P+Q-$	2	8	9	10	11	12	13	14	15	16	17	18	7
$P+Q--$	3	8	9	10	11	12	13	14	15	16	17	18	7
$P-Q++$	4	15	17	17	7	7	9	9	11	11	13	13	15
$P-Q+$	5	1	1	2	2	3	3	4	4	5	5	6	6
$P-Q-$	6	2	2	3	3	4	4	5	5	6	6	1	1
$P-Q--$	7	9	10	11	12	13	14	15	16	17	18	7	8

Table 6.2: proposed Lookup table

6.1.6 Midpoint Voltage Balancing

Balancing voltage across dc link capacitors, the considered neutral point reference voltage which will be referred as midpoint voltage, is critical in DPC and plays a major roll in overall system performance and stability.

A hysteresis control loop is employed in order to keep midpoint voltage between specific bounds. Even though a hysteresis control loop will introduce an amount of dc ripple in the output, this amount is controllable by the bounds set and it assures that no extensive switching will be applied in the attempt of midpoint voltage balancing.

When any of the phases connect the load to neutral point, a non zero mid point current is induced. Depending on polarity of mid point current the upper or the lower dc link capacitor is discharged, so any inverter voltage vectors with 0 state switches affect the midpoint. This can be expressed by equation 6.29 where m_p is 1 if the respective phase is connected to the midpoint, otherwise it is zero .

$$I_{mp} = mp_R \cdot I_R + mp_S \cdot I_S + mp_T \cdot I_T \tag{6.29}$$

	positive small vectors	I_{mp}	negative small vectors	I_{mp}
U1	(0,-1,-1)	I_{invR}	(1, 0, 0)	$-I_{invR}$
U2	(1, 1, 0)	I_{invT}	(0, 0,-1)	$-I_{invT}$
U3	(-1, 0,-1)	I_{invS}	(0, 1, 0)	$-I_{invS}$
U4	(0, 1, 1)	I_{invR}	(-1, 0, 0)	$-I_{invR}$
U5	(-1,-1, 0)	I_{invT}	(0, 0, 1)	$-I_{invT}$
U6	(1, 0, 1)	I_{invS}	(0,-1, 0)	$-I_{invS}$

Table 6.3: NPC Converter small switching vector taxonomy

$$mp_R = 1 - |S_R|$$
$$mp_S = 1 - |S_S|$$
$$mp_T = 1 - |S_T|$$

By observing this it is obvious that only small and medium switching vectors affect midpoint current and midpoint voltage can be balanced by the redundancy of small vectors. As previously reviewed every small vector is paired with another one which share same inverter voltage output in the $\alpha\beta$ plane. But what the two voltage vectors differ is the direction in which midpoint voltage is affected. So they can be grouped in positive and negative small voltage vectors. For a balanced three phase network where total Current is zero ,equation 6.30, small vectors can be categorized as in table 6.3

$$I_R + I_S + I_T = 0 \tag{6.30}$$

As shown in figure 6.13 for the two redundant states of small voltage vector 1, one is discharging the upper capacitor while letting the lower capacitor to charge, and the other acts in a complementary way. By using this redundancy, capacitor voltage can be balanced without compromising output voltage selection.

Voltage across two capacitors is continuously measured and voltage balance is checked by equation 6.31 where U_{Cup} is the measured voltage across upper dc link capacitor and U_{Cdown} the low one. The result is fed to a hysteresis

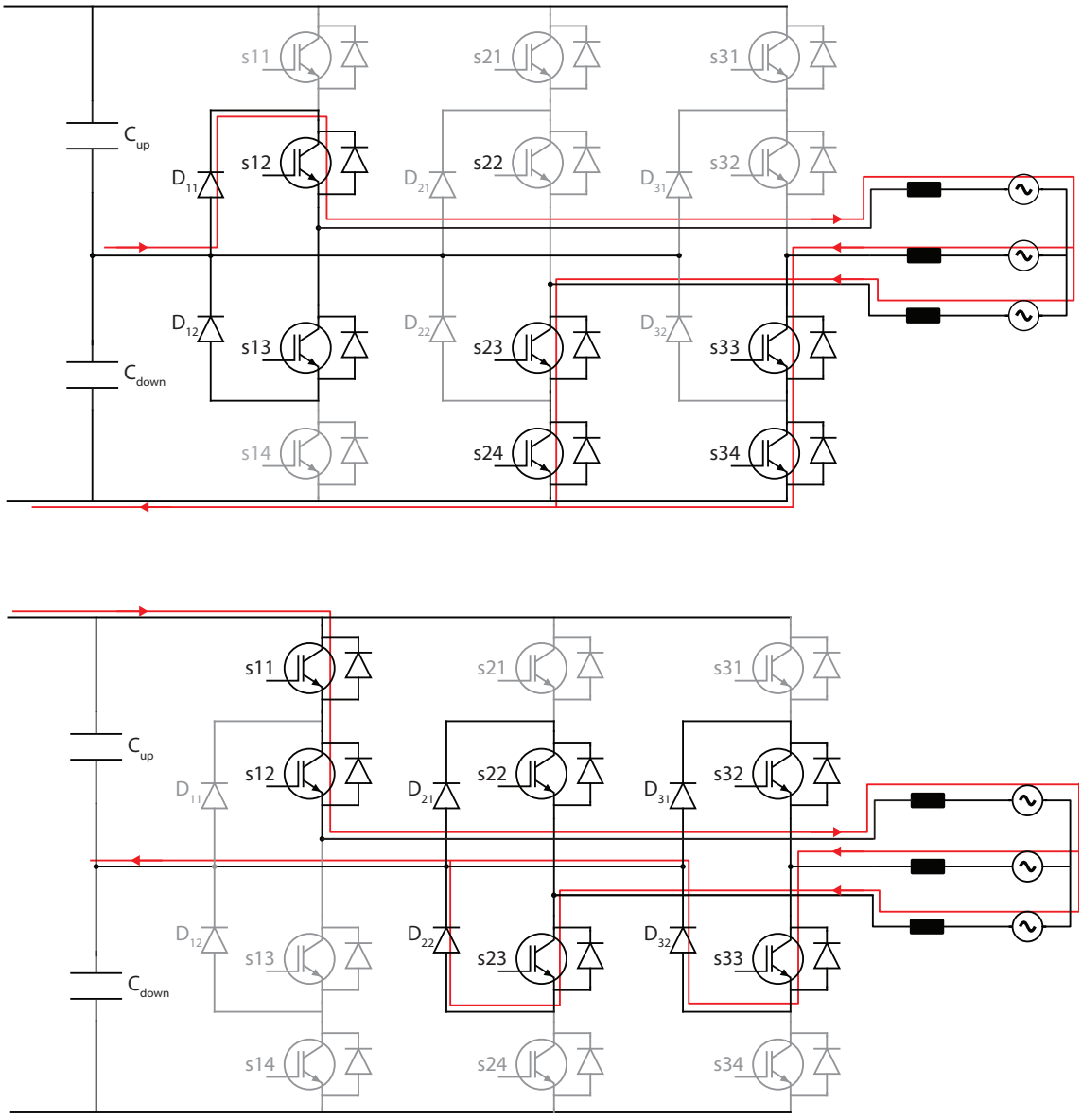


Figure 6.13: 3 level NPC redundant states and capacitor balancing.

controller which is tuned to allow a certain amount of dc ripple at the midpoint, as previously explained.

$$\Delta U_c = U_{Cup} - U_{Cdown} \tag{6.31}$$

$$h_{Uc} = \begin{cases} 1 & \text{if } \Delta U_c \geq U_{Cbound} \\ 0 & \text{if } \Delta U_c \leq -U_{Cbound} \end{cases}$$

Midpoint point balancing control scheme is summarized in figure 6.14.

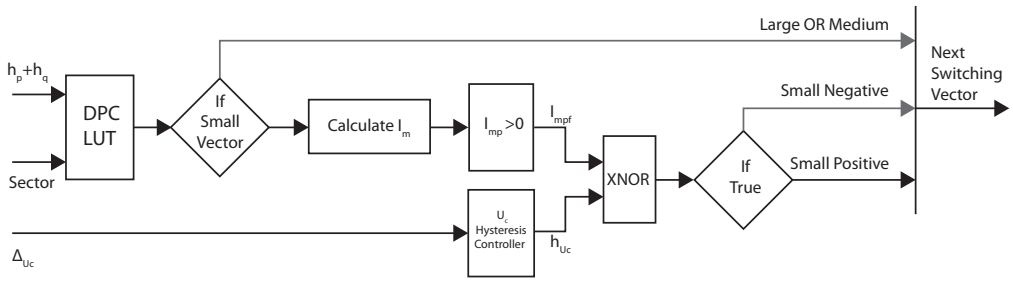


Figure 6.14: voltage balancing control scheme

After the next voltage vector to be applied has been selected by power hysteresis controllers and sector decision control block, assuming negative small voltage vectors (if a small vector has been selected) a midpoint current short-term prediction is made by equation 6.29. With knowledge of midpoint current direction and information from the voltage balancing hysteresis controller, a final decision is made whether a positive or negative voltage vector will be applied in next time instance. Truth table of Voltage balance hysteresis controller and mid point current direction is described in table 6.4 and can be performed in boolean algebra as a XNOR between h_{Uc}, I_{mpf}.

$$I_{mpf} = \begin{cases} 1 & \text{if } \ I_{mp} \geq 0 \\ 0 & \text{if } \ I_{mp} < 0 \end{cases}$$

Disregarding high frequency ripple present in the waveform of neutral point potential, an alternative way to predict whether a positive or negative mid point

I_{mpf}	h_{Uc}	XNOR
0	0	1
0	1	0
1	0	0
1	1	1

Table 6.4: voltage balance truth table

current should be induced, is by variation rate of midpoint voltage balancing as described by equation 6.32

$$I_{mp} = C_{dc}\frac{d(U_{Cup} - U_{Cdown})}{dt} \tag{6.32}$$

6.2 Simulation Results

In order to evaluate the presented control technique, a simulation of a grid connected system was set up in the Simulink environment. A 1KW NPC Inverter is interfacing a 200V DC link to a grid Network 70V 50Hz, through 8.5mH inductors and 1000uF DC link Capacitors. The system represents a low scale prototype and is tested in two reference step changes, one for active power while reactive power is kept constant, and one for reactive power while active power is kept constant.

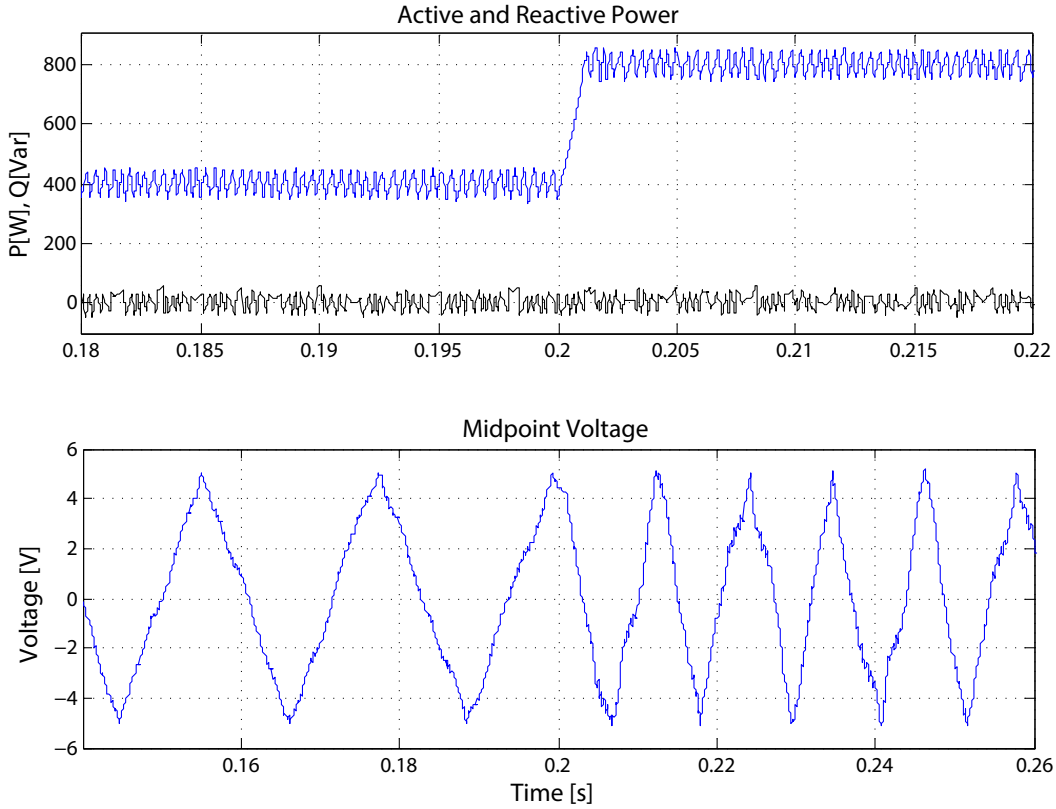


Figure 6.15: DPC controlled variables - Active Power Reference step change

Active and Reactive Power are maintained between predefined bound and no spikes or notches are present in reactive power control, which is the case of typical DPC. Midpoint Voltage is also balanced around a certain offset, avoiding excessive switching while assuring that the inverter will never exceed the allowed voltage balance level.

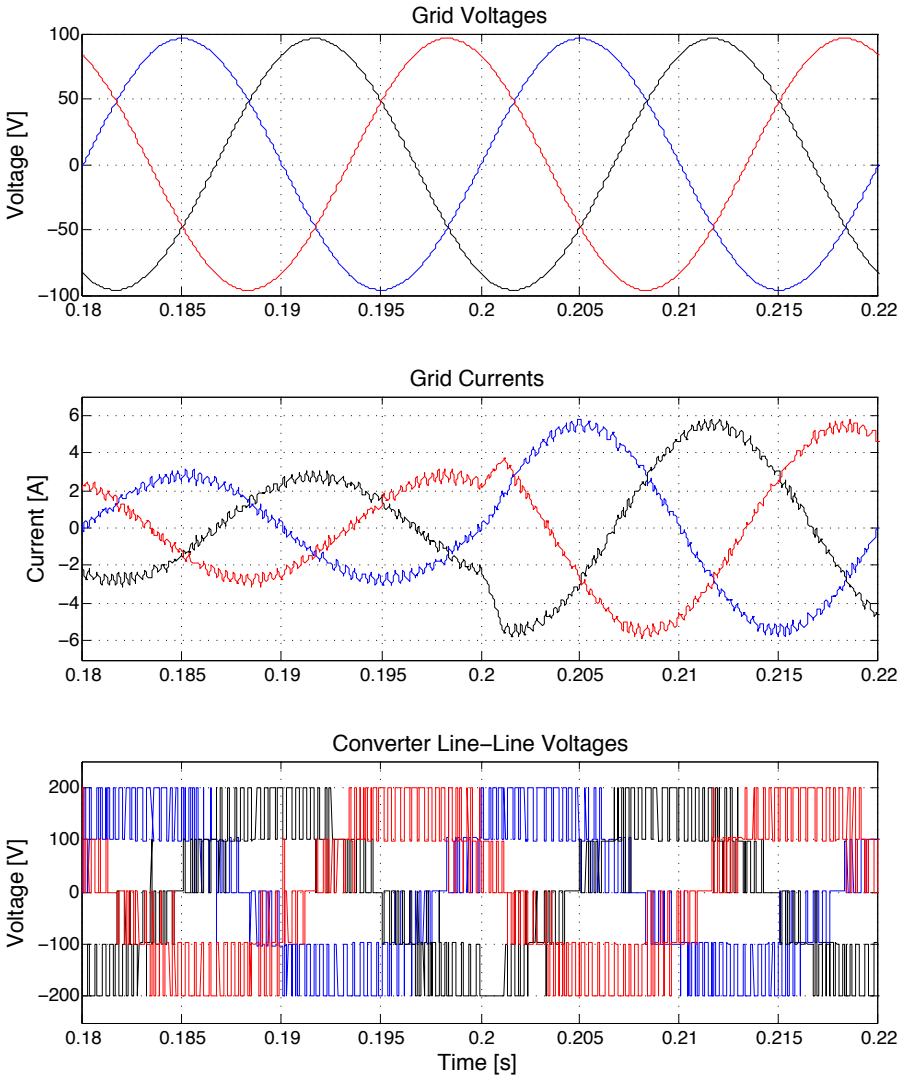


Figure 6.16: DPC grid 3 phase measurements - Active Power Reference step change

Observing the output current wafevorm, high frequency component is the result of hysteretic control,and can be diminished by tightening the hysteresis controllers bounds. Such a change would augment switching frequency which as seen from the inverter output voltage waveforms is kept low and was measured around $1.17 - 1.21KHz$ with a current THD of 3.5%..

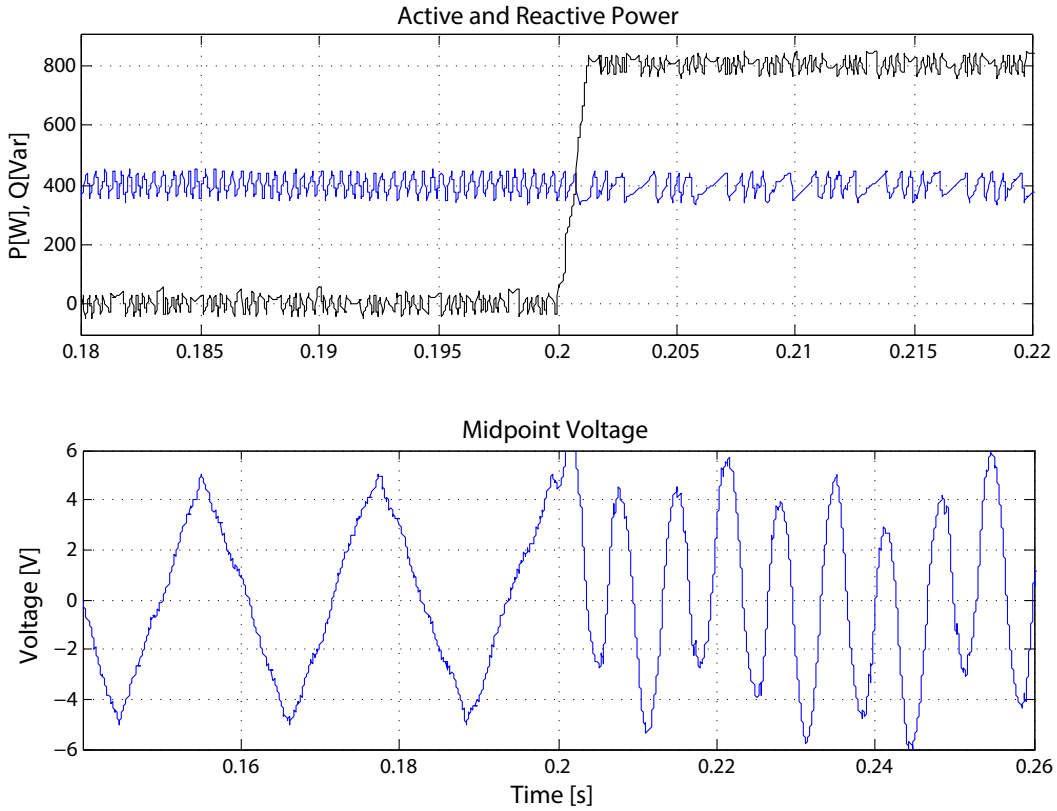


Figure 6.17: DPC controlled variables - Reactive Power Reference step change

Same is the case for reactive power reference step change. The suggested DPC technique manages to drive the controlled variables, P,Q and midpoint voltage, between predefined bounds avoiding extensive switching and prohibited switch transitions. Remarkable is the fact that there is little or no coupling between controlled variables as well as the fast response in step reference change in both cases.

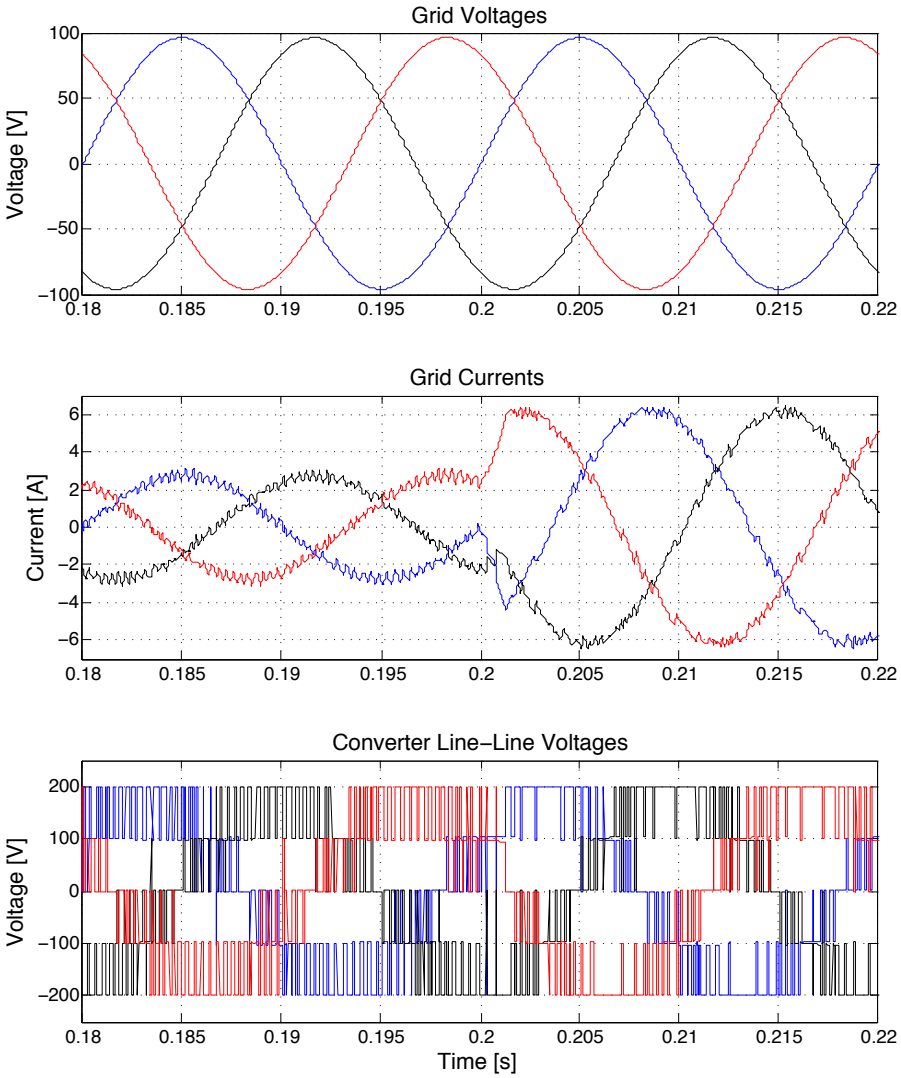


Figure 6.18: DPC grid 3 phase measurements - Reactive Power Reference step change

6.3 Experimental Results

In order to verify the proposed DPC technique, a small scale prototype was set up utilizing an already existing NPC converter, and BoomBox, the integrated control platform of LEI, for the implementation of the control loop algorithm. In order to properly Interface the NPC card to the Boombox platform, an interface card was designed. More on the Hardware setup in the appendix at the end of the thesis. The Overall system characteristics are summarized in :

$$L_g = 8.5\,mH$$
$$V_{dc} = 70\,V$$
$$C_{dc} = 1000\,\mu F$$
$$V_s = 20\,V$$
$$f_s = 50\,Hz$$

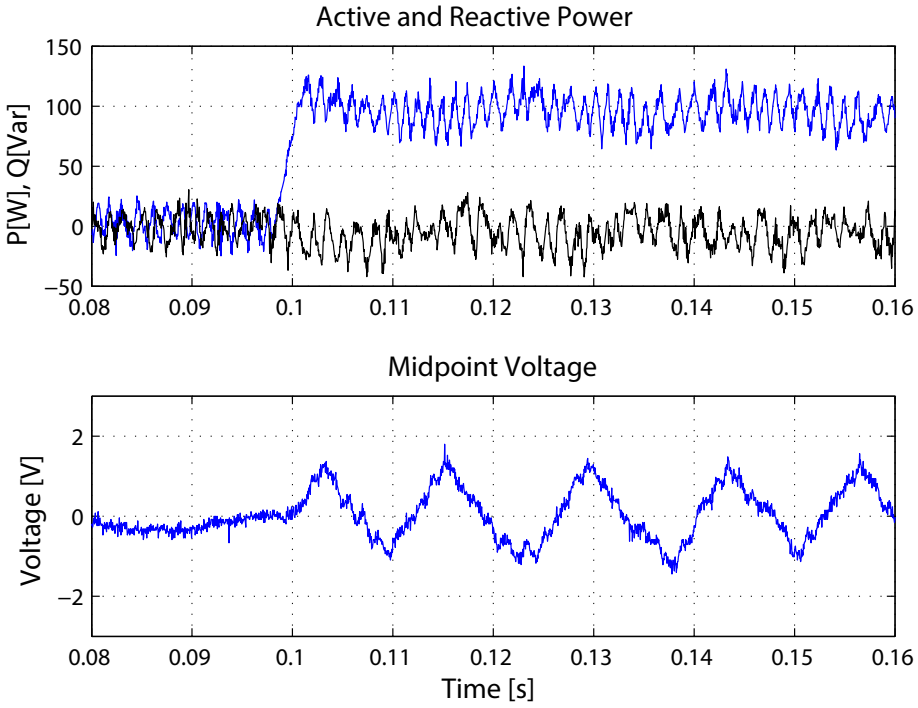


Figure 6.19: DPC controlled variables - Active Power Reference step change

As a first test, reactive power reference is set to zero and active power refer-

ence is changed from zero to 100 W. The system response is depicted in figure 6.19. The system resembles the simulated system to the point that the expected hysteretic behavior is present but the bounds of the controlled variables are continuously violated resulting in overly distorted current waveform. Grid voltage, current and NPC inverter voltage output are shown in figure 6.20. Even though switching frequency is maintained in low levels, grid current is severely distorted.

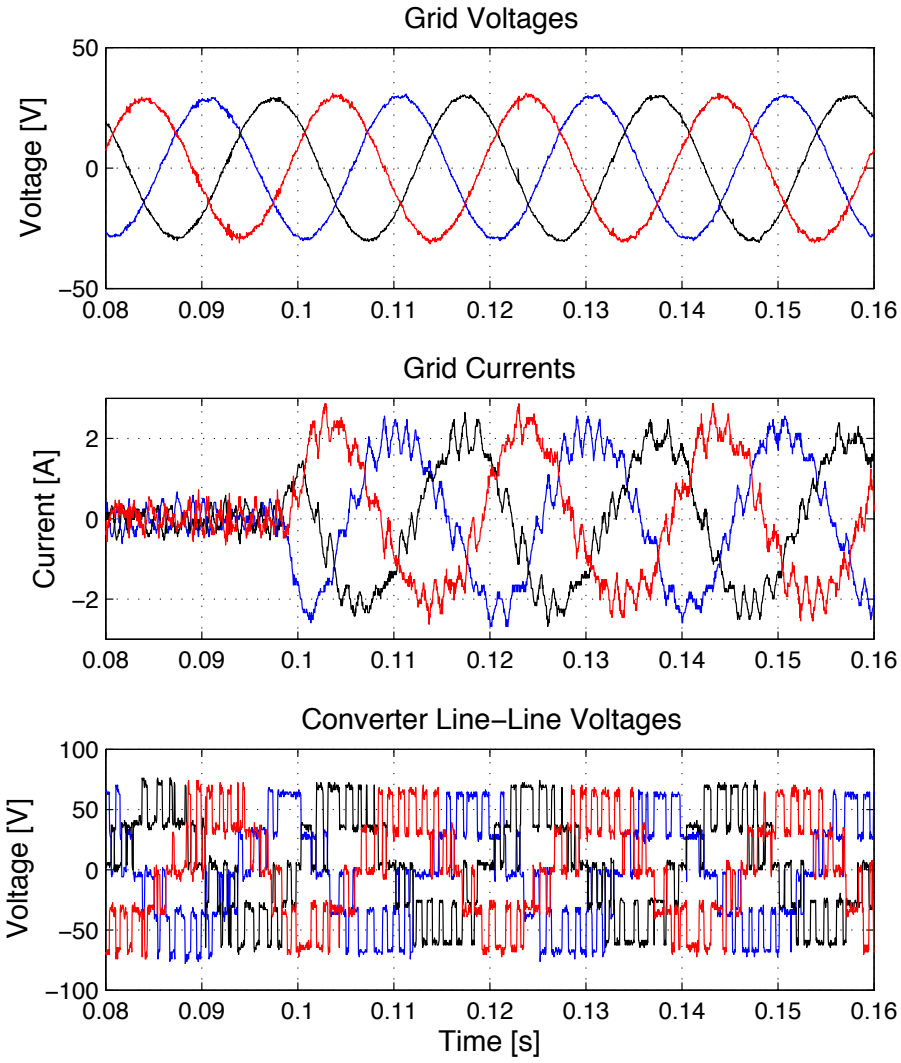


Figure 6.20: DPC grid 3 phase measurements - Active Power Reference step change

This system instability possibly occurs due to noise present in the measurement stage, due to the fact that the whole system is designed for high capacity

current sensors and calibrated for so, leading to a low signal to noise ratio for the specific application. Possible solutions to this is either recalibrating current sensors for specific test either augmenting current demand in a new test.

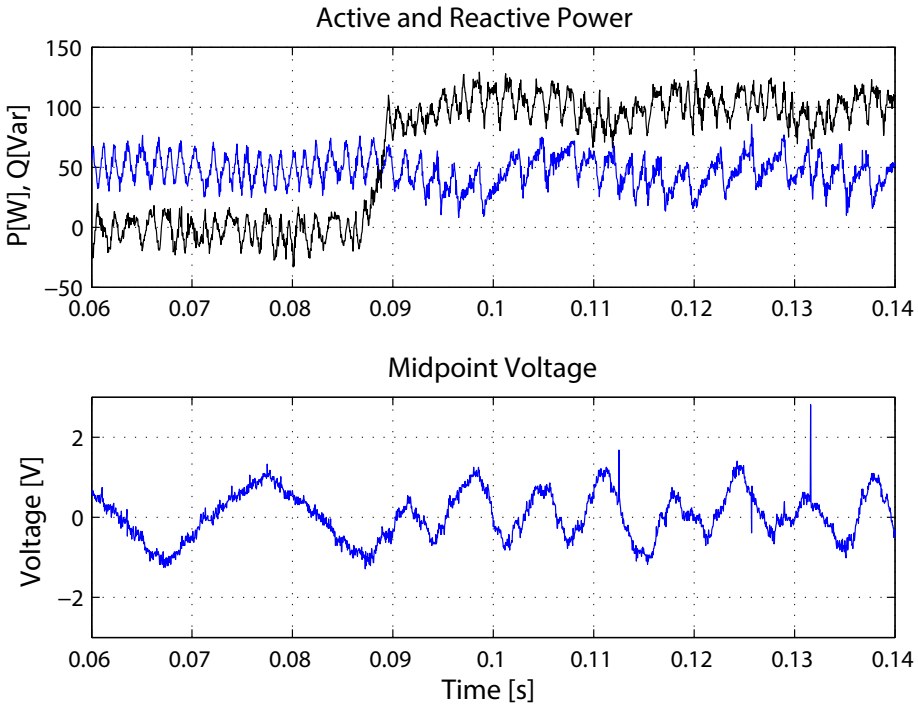


Figure 6.21: DPC controlled variables - Reactive Power Reference step change

The second test is for constant active power reference at $50\,W$ and a step change in reactive power from zero to $100\,Var$. The following figures present the results. As previously observed, the system follows the power references and manages to balance midpoint voltage but bounds are severely violated and grid current distorted.

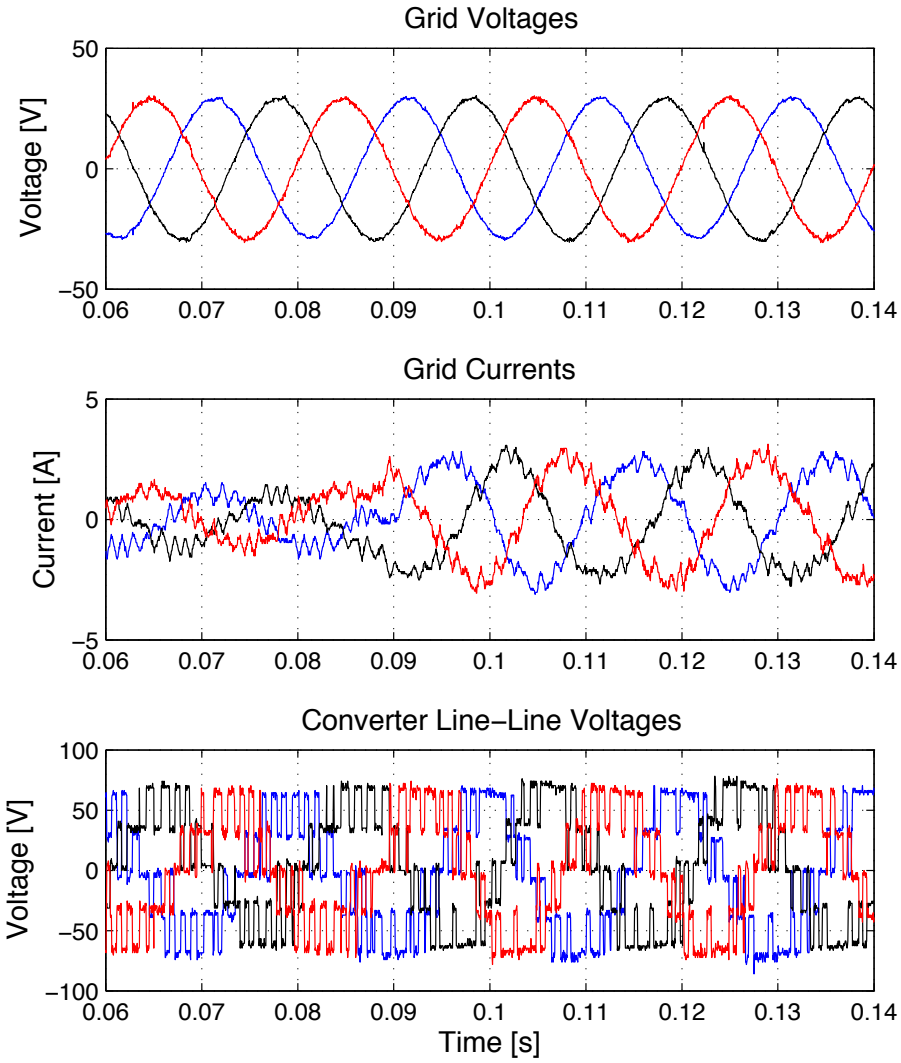


Figure 6.22: DPC grid 3 phase measurements - Reactive Power Reference step change

CHAPTER
SEVEN

DPC WITH LCL OUTPUT FILTER

The already presented DPC setup, utilizes a simple inductor to interface the NPC inverter to the grid. Even though simplicity of both setup and control design, in high power applications the inductance value needed for a first order low pass filter to maintain harmonic distortion of the current output at low levels, may lead to bulky and non cost effective designs. Another disadvantage of the simple inductor filter is that the control algorithm employed is highly depended on grid line inductance, or the inductive load connected to the NPC inverter's output.

A solution is the use of a higher order output filter, such as an LCL 3rd order filter. By interfacing the converter to the grid through an LCL filter, due to the filters steeper transfer function, same harmonic content can be rejected by a lower total inductance, achieving desired current ripple attenuation. Moreover the control algorithm gets far more independent from grid side inductance assuring better performance, robustness and a broader range of applications.

However with the use of LCL filter certain difficulties have to be encountered. Most important is to ensure that no harmonics will be generated at or near the resonance frequency of the output filter by the converter, which contrasts to the variable switching frequency of DPC method already presented. This is achieved by actively damping the aforementioned harmonic power avoiding any extra power losses by extensive current ripple or by damping resonant harmonic currents through passive power resistors.

7.1 DPC of three-level NPC with LCL Output Filter

The new DPC VSI with LCL output filter block diagram is presented in figure 7.1. Since the output equivalent circuit changes, virtual flux and power estimation are altered too. New Control blocks are also added for active damping of resonant harmonics and capacitor reactive power compensation.

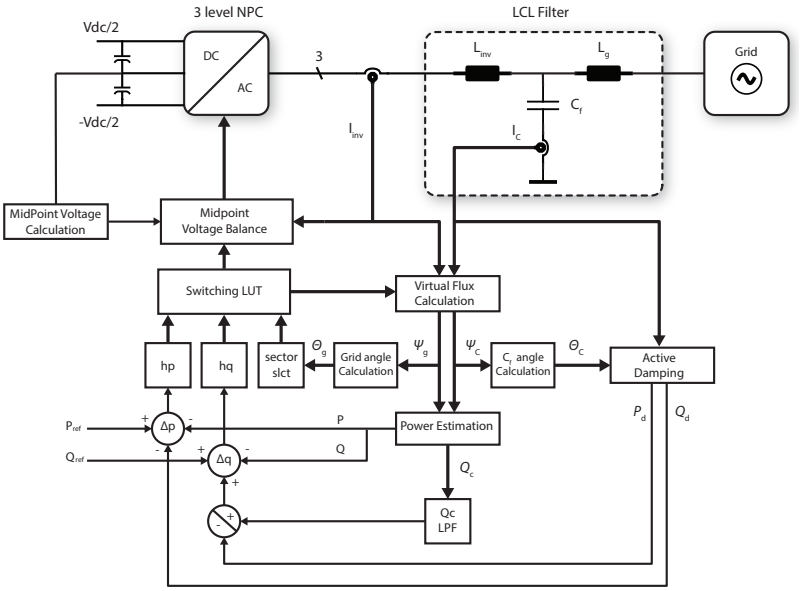


Figure 7.1: DPC with LCL block diagram

7.1.1 Virtual Flux and Power estimation

Virtual flux and Power are estimated in the same way as for simple inductor filter, with minor changes adapting calculations to the new LCL filter. Examining the filter diagram in figure 5.1, virtual flux to the grid can be calculated by equation 7.1

$$\psi_g = \psi_c - L_g(I_{inv} - I_c) \tag{7.1}$$

Where ψ_c is the virtual flux of filter capacitor and can be calculated by equation 7.2

$$\psi_c = \int V_{inv}dt - L_{inv}I_{inv} \tag{7.2}$$

Using the same decoupling method of low pass filtering instead of a simple integrator, virtual flux calculation can be described by block diagram in figure 7.2

Based on previous analysis of instantaneous power calculation and considering that ,for low frequencies, output filter can be approximated by an inductor

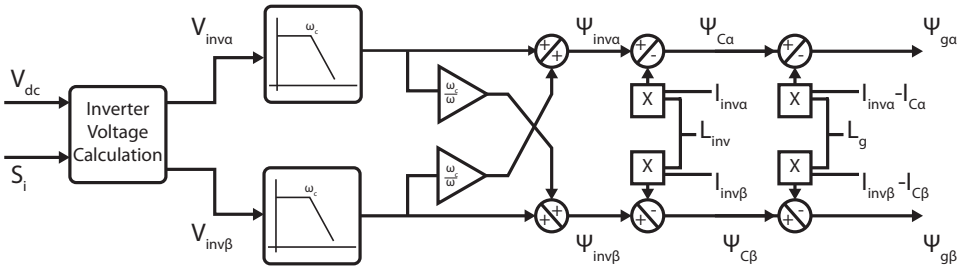


Figure 7.2: Virtual Flux calculation block diagramm with LCL output filter

and active and reactive power can be calculated by:

$$p = \frac{3}{2}\omega(\psi_{g\alpha}I_{inv\beta} - \psi_{g\beta}I_{inv\alpha})$$
$$q = \frac{3}{2}\omega(\psi_{g\alpha}I_{inv\alpha} + \psi_{g\beta}I_{inv\beta}) \tag{7.3}$$

Inverter side measurements are utilized, since grid side quantities will be more smooth, containing significant lower harmonic content due to filtering, rendering them more difficult to track and control.

7.1.2 Active damping

The strategy employed to actively damp resonant content of the output current is the well known method of virtual resistor [28] [29]. Since the inverter side current is controlled, inverter side inductor and inverter voltage output can be conceived as a controllable current source as in figure 7.3. By connecting a resistor parallel to the filter capacitor , transfer function of the filter alters as in equation 7.4 and through value selection of this damping resistor the amount of filter resonance damping is controlled. Major drawback of passive damping is power losses on the damping resistor lowering the total efficiency of the converter.

$$\frac{I_g}{I_{inv}} = \frac{\frac{1}{L_g C}}{s^2 + s\frac{1}{R_d C} + \frac{1}{L_g C}} \tag{7.4}$$

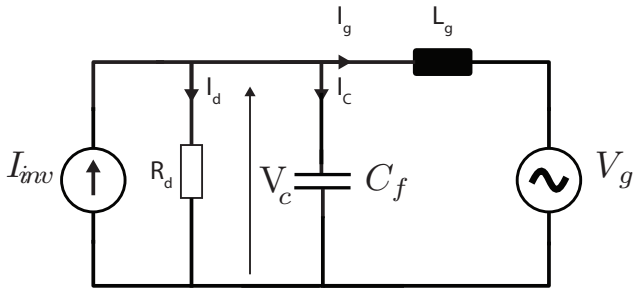


Figure 7.3: LCL filter diagram with converter output and inductor as a current source

Instead of using a real resistor, a current source proportional to filter capacitor voltage, $I_d = \kappa_d V_c$, parallel to the filter capacitor is emulated by the controller as in figure 7.4 which is later used to calculate resonant active and reactive components to be damped. By determining the gain $\kappa_d = \frac{1}{R_d}$ of the controllable current source the amount of filter resonance damping is controlled.

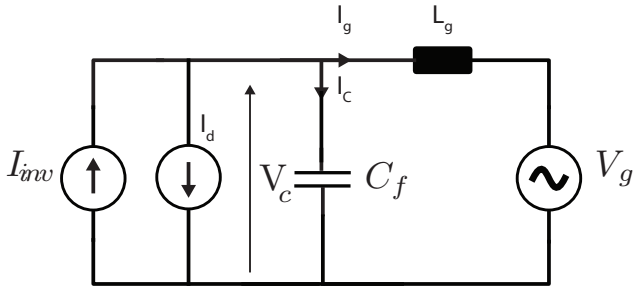


Figure 7.4: virtual current source I_d

Examining filter transfer function as a general form second order system, the undamped natural frequency of the system and damping factor can be calculated based on the filter parameters C, L_g and damping ratio ζ.

$$\omega_n = \sqrt{\frac{1}{L_g C}} \tag{7.5}$$

$$\kappa_d = 2\zeta\sqrt{\frac{C}{L_g}} = \frac{1}{R_d} \tag{7.6}$$

In order to calculate active and reactive power to be compensated, knowledge of filter capacitor is needed, wich can be derived by a capacitor current integrator. In case of a sensorless system, capacitor current can be estimated by equation 7.7 [28]

$$\begin{aligned} I_c &= C\frac{d}{dt}V_c = C\frac{d^2}{dt^2}\psi_c \\ V_c &= V_{inv} - L_{inv}\frac{dI_L}{dt} \end{aligned} \tag{7.7}$$

Capacitor voltage is transformed to alpha beta reference frame components and in order to form the resonance damping current it is passed through a notch filter with a center frequency at 50 Hz. Output of the filter is transformed to the dq0 components rotating synchronously to the capacitor voltage and then multiplied by κ_d, to form the virtual resistor damping current dq components I_{dd}, I_{dq}. The non filtered capacitor voltage is also transformed to the dq0 reference plane V_{cd} and is passed through a low pass filter in order to attenuate higher order harmonics. At last, active and reactive power to be damped are calculated by equations 7.8 and whole active damping power calculation is described in block diagram of figure 7.5. As previously mentioned, generated active and reactive damping power are subtracted from their respective references in order to compensate for any filter resonance taking effect in the converter output current.

$$\begin{aligned} p_d &= \frac{3}{2}V_{c,d}I_{d,d} \\ q_d &= -\frac{3}{2}V_{c,d}I_{d,q} \end{aligned} \tag{7.8}$$

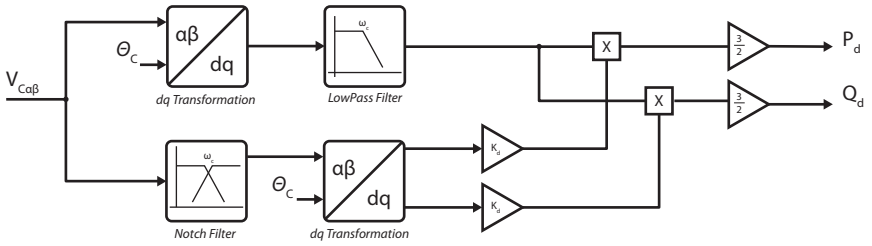


Figure 7.5: active damping block diagram

7.1.3 Filter Capacitor Reactive Power Compensation

Since converter side power is controlled, reactive power consumed to filter's capacitor should also be generated by the inverter, so as the reactive power reference is reflecting the grid side expected reactive power level. Filter capacitor reactive power to be compensated is calculated by equation 7.9, passed through a first order low pass filter so as to dispose off any extra harmonic content, and then is added to reactive power reference.

$$q_c = \frac{3}{2}\omega(\psi_{c\alpha} I_{c\alpha} + \psi_{c\beta} I_{c\beta}) \tag{7.9}$$

Another benefit of this reactive power compensation of the filter stage is that when designing the output filter a higher value of filter capacitor can be selected leading to smaller total inductance in the final design.

7.2 Simulation Results

The system that was simulated for evaluation of the DPC technique, is extended as described in this chapter to interface the grid through an LCL filter. Following the design procedure previously described an LCL filter was composed for the simulated system.Total Inductance of LCL filter is kept the same as in the case of simple L filter so as to have comparable results and correctly evaluate benefits of using an LCL filter. The final design of the filter for an average expected frequency of $1.2KHz$ resulted in the following components values:

$$L_{inv} = 6.5\,mH$$
$$L_g = 2.0\,mH$$
$$C_f = 47\,uF$$
$$f_{res} = 580\,Hz$$

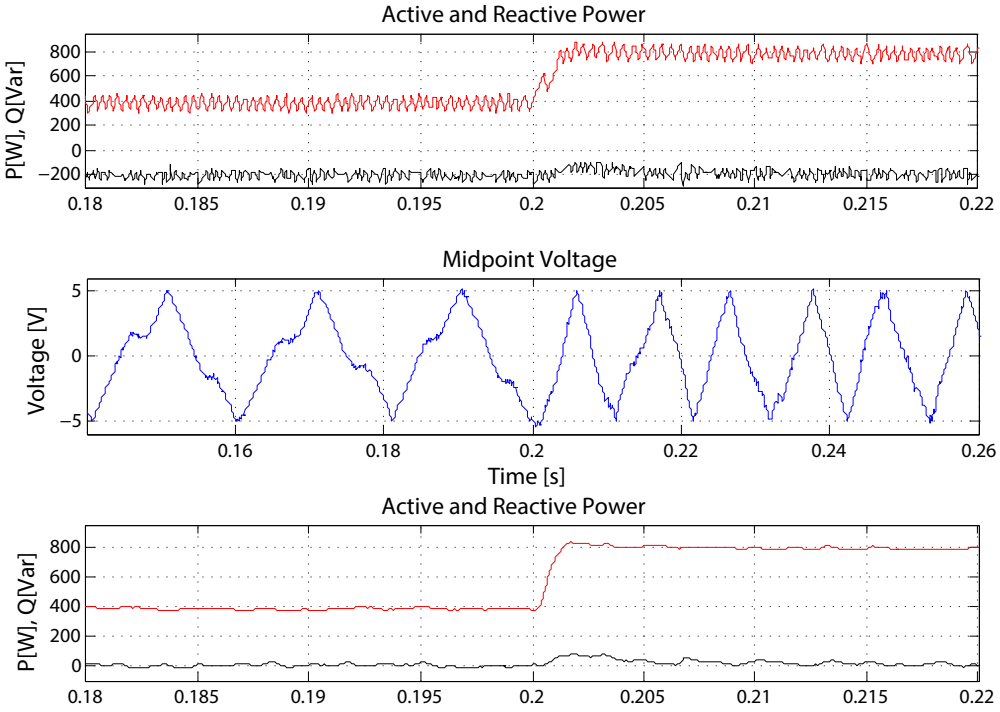


Figure 7.6: DPC-LCL control p step

In figure 7.6 the first plots represent the directly controlled converter side active and reactive power, while the last plot represent the grid side delivered

power. Obviously grid side power, both active and reactive, are much smoother, free of high frequency ripple compared to DPC with L filter. This means that in order to achieve same power output as in simple DPC with L filter, boundaries of PQ hysteresis controllers can be widened yielding a lower switching frequency. Midpoint Voltage balance control as expected behaves in the same way, since changes made to the control algorithm do not affect midpoint voltage balance control loop.

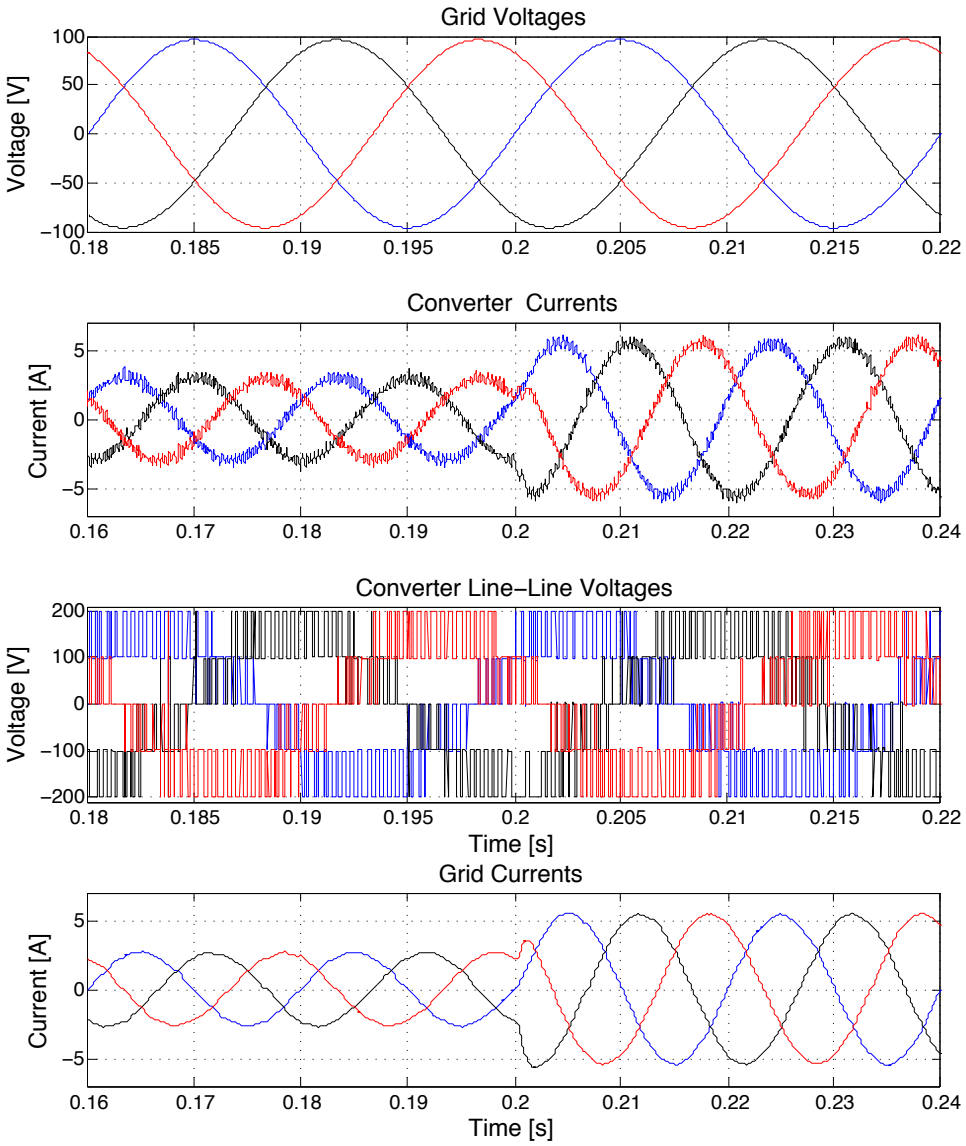


Figure 7.7: DPC-LCL 3 phase p step

Grid side Current is much cleaner, free of high order harmonics, with a THD of 1.58% for an average switching frequency of $1.34 - 1.4\,KHz$. Also when the active damping control is employed with a high damping ratio, an increase in low harmonic content, especially 5th, is observed. In a case that this low harmonic distortion is so intense to be of a problem, special harmonic compensation can be employed in an outer loop as presented in [29],[30] in order to selectively eliminate targeted harmonic distortion.

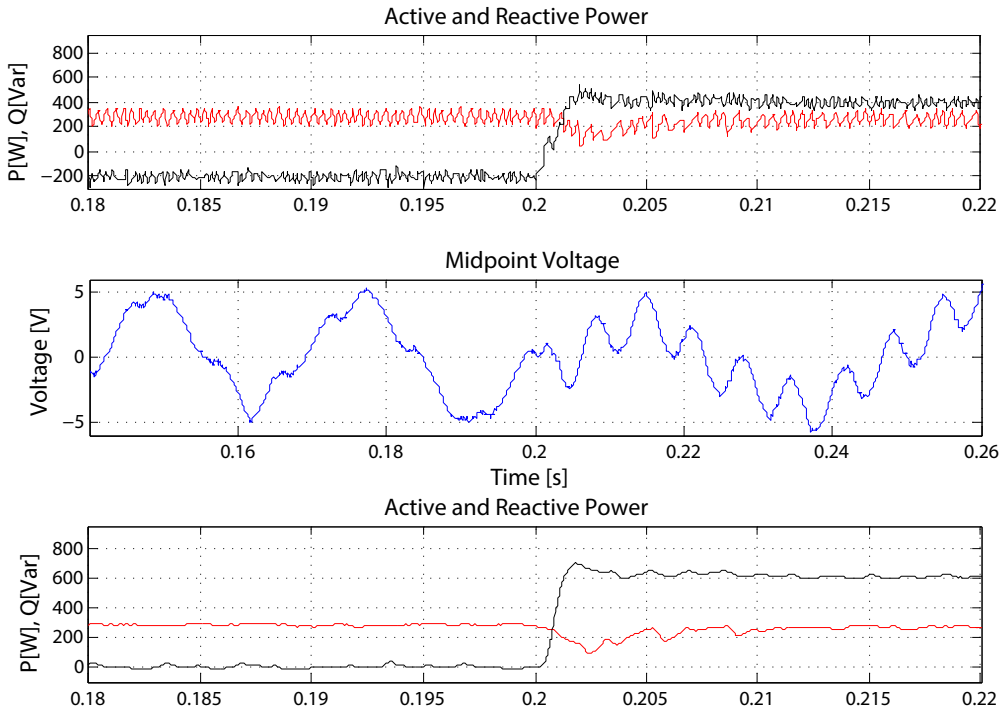


Figure 7.8: DPC-LCL control q step

In both step reference changes, P and Q, it is observed, that a slightly slower response compared to simple DPC, but in overall the system maintains fast response characteristics. Another point to consider is that the LCL system seems to exhibit more intense coupling between Active and reactive controlled variables, but this may be due to the filter capacitor, whose compensation is directly proportional to total output grid current.

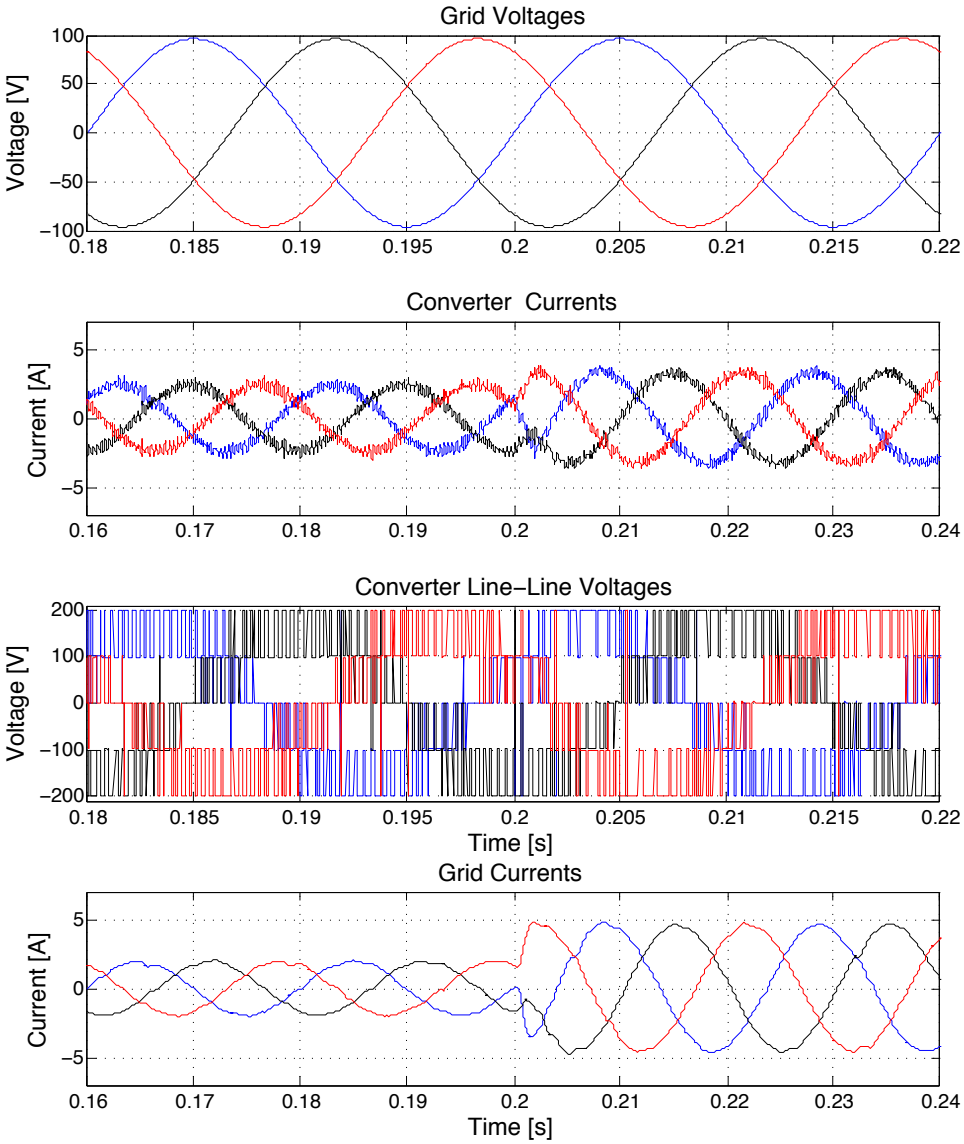


Figure 7.9: DPC-LCL 3 phase q step

In both step reference changes, controlled variables are driven between predefined boundaries, yielding a smooth output power, while midpoint voltage is properly balanced and no extreme switching transitions are allowed.

In order to visualize more clear the way that active damping acts, a simulation scenario was set, where damping ratio K_d is changed from zero to 0.707. As depicted in figure 7.10, strong harmonic distortion occurs at the excited resonant frequency of the filter, which is effectively eliminated by employing the active damping control technique.

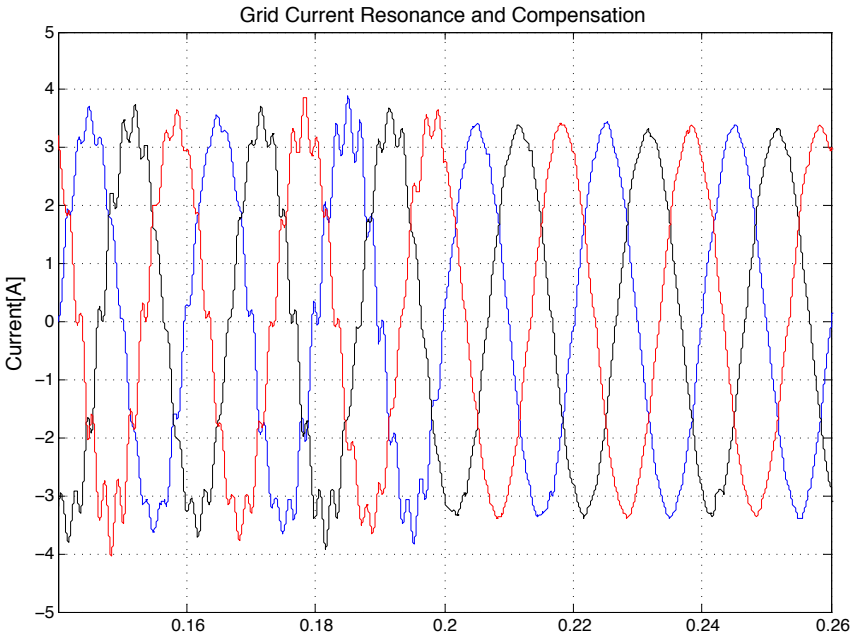


Figure 7.10: Grid Current Resonance with and without active damping.

CHAPTER

EIGHT

MODEL PREDICTIVE DIRECT POWER CONTROL

The idea underlying MPDPC as described in [31], is to replace the switching table in conventional DPC, with an online constrained optimal controller with a receding horizon policy [32][33][14][34]. The control objectives are to keep converter's Active and Reactive Power within predefined hysteresis bounds, which is referred to as the feasible region. With three-level neutral point clamped inverters, it is also desired to balance the neutral point of the inverter, the midpoint voltage balance as previously described. In [12] there is a categorization of predictive control methods, in trajectory based strategies, hysteresis based strategies, like common DPC, and model based strategies like the one described here. The general control scheme can be seen in figure 8.1.

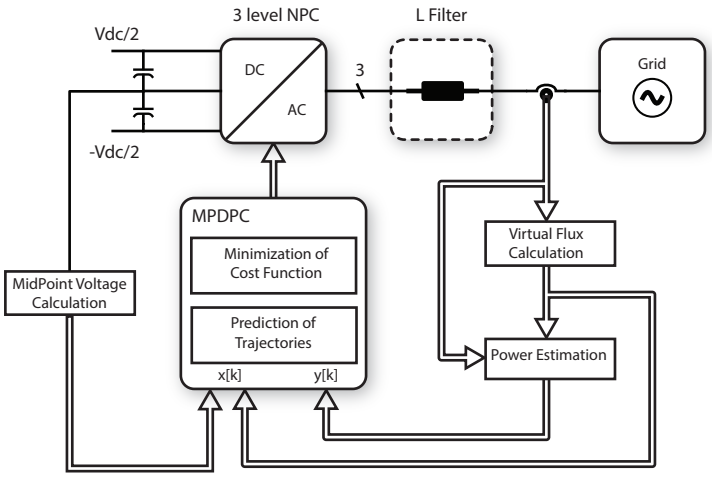


Figure 8.1: MPDPC scheme for a grid connected npc converter

In the same way that MPDTC extends on DTC, Model Predictive Direct Power Control (MPDPC) can be viewed as an extension of DPC, replacing the switching table with an online-optimization stage. Using the virtual flux concept, instant active and reactive power are estimated, and fed to the MPC controller, which drives the switches of the three-level NPC converter. For that reason power calculations and general characteristics of NPC inverter remain the same as described in previous section and will not be re-examined.

For the optimal controller, a model of the inverter has to be derived. This is done by the state space model formed with the differential equations describing the system. Also a cost function has to be formed, which should be minimized or maximized for the optimal input. Moreover input, output and state vector constraints should be described.

8.1 Discrete time physical modeling

Considering differential equations 6.26 of grid Current as previously derived by grid connected NPC converter operation equivalent circuit, figure 6.2, voltage to flux relation described by equation6.27 , and differential equations of virtual flux 6.24, state vector $x = [I_\alpha, I_\beta, \Psi_\alpha, \Psi_\beta]^\intercal$ description is formed. With $y = [P, Q]^\intercal$ as the output vector and $u = [V_{inv\alpha}, V_{inv\beta}]^\intercal$ the input vector, the state space model is set up.

$$\begin{aligned}
\frac{d\psi_{g\alpha}}{dt} &= -\omega\psi_{g\beta} \\
\frac{d\psi_{g\beta}}{dt} &= \omega\psi_{g\alpha} \\
\frac{dI_\alpha}{dt} &= \frac{1}{L}(\omega\psi_{g\beta} + V_{inv\alpha}) \\
\frac{dI_\beta}{dt} &= \frac{1}{L}(-\omega\psi_{g\alpha} + V_{inv\beta})
\end{aligned}$$

The output vector, active and reactive power, is calculated in the same way as in conventional DPC,equation 6.17

$$\begin{aligned}
p &= \frac{3}{2}\omega(\psi_{g\alpha}I_{g\beta} - \psi_{g\beta}I_{g\alpha}) \\
q &= \frac{3}{2}\omega(\psi_{g\alpha}I_{g\alpha} + \psi_{g\beta}I_{g\beta})
\end{aligned}$$

While input vector u, is the inverter voltage output, calculated as in equation 6.4.

From this set of equations and assuming zero order hold for input vector, system is moved to discrete time domain using forward euler method where $\frac{1}{s}$ is approximated by $\frac{T_s}{z-1}$ in the Laplace domain, with T_s the sampling time of conversion. This procedure yields the discrete physical model of the system, described by set of equations 8.1 and will be used as the internal prediction model for the MPC controller realization.

$$\begin{aligned}
\psi_{g\alpha}[k+1] &= \psi_{g\alpha}[k] - T_s\omega\psi_{g\beta}[k] \\
\psi_{g\beta}[k+1] &= \psi_{g\beta}[k] + T_s\omega\psi_{g\alpha}[k] \\
I_{\alpha}[k+1] &= I_{\alpha}[k] + \frac{T_s}{L}(\omega\psi_{g\beta}[k] + V_{inv\alpha}[k]) \\
I_{\beta}[k+1] &= I_{\beta}[k] + \frac{T_s}{L}(-\omega\psi_{g\alpha}[k] + V_{inv\beta}[k]) \\
p[k+1] &= p[k] + \frac{3}{2}\omega(\psi_{g\alpha}[k]I_{g\beta}[k] - \psi_{g\beta}[k]I_{g\alpha}[k]) \\
q[k+1] &= q[k] + \frac{3}{2}\omega(\psi_{g\alpha}[k]I_{g\alpha}[k] + \psi_{g\beta}[k]I_{g\beta}[k])
\end{aligned} \tag{8.1}$$

8.2 Problem Formulation

In order to be able to control the midpoint voltage U_{mp} and balance the three-level NPC inverter, it should be properly expressed and incorporated into the output vector. The dynamics of mid point voltage can be described by equation 8.3 , as derived by equation 8.2, with midpoint current measured as in equation 6.29 by using knowledge of the switches state. Midpoint voltage should be described by existing state variables thus it can be incorporated into the existing model, adding another set of constraints, that of maintaining U_{mp} between specified boundaries.

$$\left.\begin{aligned} C_{up}\frac{d(V_+ - U_{mp})}{dt} &= I_{Cup} \\ C_{down}\frac{d(U_{mp} - V_-)}{dt} &= I_{Cdown} \end{aligned}\right\} \Rightarrow \quad \begin{aligned} \frac{dU_{mp}}{dt} &= \frac{1}{C_{up}}I_{Cup} \\ \frac{dU_{mp}}{dt} &= \frac{1}{C_{down}}I_{Cdown} \end{aligned} \tag{8.2}$$

Adding vertically expressions of $\frac{dU_{mp}}{dt}$, while considering that upper and lower dc link capacitor values are the same $C_{up} = C_{down} = C_{dc}$, and that midpoint cur-

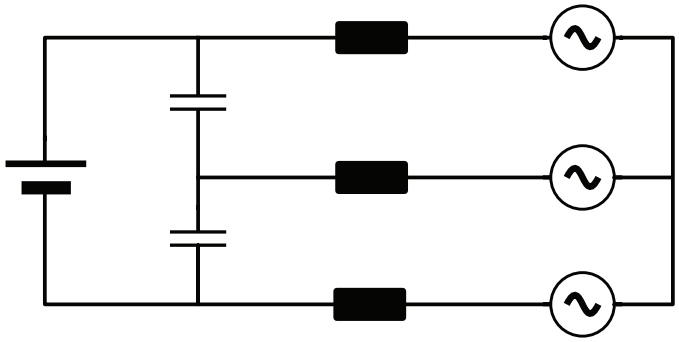


Figure 8.2: Mid point voltage connection equivalent circuit

rent is the algebraic sum of two dc link capacitors current $I_{mp} = I_{Cup} + I_{Cdown}$,

$$\frac{dU_{mp}}{dt} = \frac{1}{2C} I_{mp} = \frac{1}{2C} \left[(1 - |S_R|) \cdot I_R + (1 - |S_S|) \cdot I_S + (1 - |S_T|) \cdot I_T \right] \quad (8.3)$$

Where I_R, I_S, I_T can be derived by inverse Parke transform of α, β grid Currents:

$$I_{RST} = \frac{2}{3} P^{-1} \cdot I_{\alpha\beta} \quad (8.4)$$

The dynamics of midpoint voltage can finally be properly expressed as in equation 8.5 enabling its use in state vector $x = [I_\alpha, I_\beta, \Psi_\alpha, \Psi_\beta, U_{mp}]^\intercal$

$$\frac{dU_{mp}}{dt} = \frac{1}{2C} ||1 - I \cdot S_{abc}||_1 \frac{2}{3} P^{-1} \cdot I_{\alpha\beta}$$

$$\frac{dU_{mp}}{dt} = \frac{1}{6C} \left[\left[2(1 - |S_R|) - (1 - |S_S|) - (1 - |S_T|) \right] I_\alpha + \sqrt{3} \left[(1 - |S_S|) - (1 - |S_T|) \right] I_\beta \right] \quad (8.5)$$

Which in its discrete form can be rewritten as :

$$\begin{aligned} U_{mp}[k+1] = U_{mp}[k] &+ \frac{T_s}{6C} \left[2(1 - |S_R[k]|) - (1 - |S_S[k]|) - (1 - |S_T[k]|) \right] \cdot I_\alpha[k] \\ &+ \frac{T_s}{6C} \sqrt{3} \left[(1 - |S_S[k]|) - (1 - |S_T[k]|) \right] \cdot I_\beta[k] \end{aligned} \quad (8.6)$$

Where factors of I_α, I_β can be precalculated and stored for every possible switching vector.

P is the transformation matrix:

$$P = \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{8.7}$$

Which for a balanced system where $I_R + I_S + I_T = 0$ can be reduced to:

$$P = \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{8.8}$$

And P^{-1} the P inversion, used for moving from static reference frame to rotating

$$P^{-1} = \begin{bmatrix} \frac{2}{3} & 0 & \frac{2}{3} \\ \frac{-1}{3} & \frac{\sqrt{3}}{3} & \frac{2}{3} \\ \frac{-1}{3} & \frac{-\sqrt{3}}{3} & \frac{2}{3} \end{bmatrix} \tag{8.9}$$

Which for a balanced system where $I_0 = 0$ can be rewritten as:

$$P^{-1} = \begin{bmatrix} \frac{2}{3} & 0 \\ \frac{-1}{3} & \frac{\sqrt{3}}{3} \\ \frac{-1}{3} & \frac{-\sqrt{3}}{3} \end{bmatrix} \tag{8.10}$$

Since Inverter Voltage components $V_{inv\alpha\beta}$ are directly proportional to inverter switch vector, the input vector can be altered from inverter voltage output $V_{inv\alpha\beta} = [V_{inv\alpha}, V_{inv\beta}]$ to inverter switches state $u = S_{abc} = [S_R, S_S, S_T] \quad , (S_R, S_S, S_T) \in (-1, 0, 1)$. Output voltage of the inverter can be calculated by equation 8.12 and

all previous state variables can be expressed in terms of inverter switches state. Obviously inverter voltage output can be pre-calculated for every possible inverter switch vector considering knowledge of dc voltage input.

After some term rearrangements, final state space representation is given by

$$x(k+1) = \left(I + \begin{bmatrix} A & 0 \\ 0 & 0 \end{bmatrix} T_s\right) x(k) + \begin{bmatrix} B_1 \\ 0 \end{bmatrix} T_s u(k) + \begin{bmatrix} 0 \\ B_2(x(k)) \end{bmatrix} T_s |u(k)| \tag{8.11}$$

$$y(k) = g(x(k))$$

Where:

$$B_1 = \frac{V_{dc}}{2} \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} P, \quad B_2(x(k)) = \frac{1}{2C} x^{\intercal} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} P^{-\intercal},$$

$$A = \begin{bmatrix} 0 & -\omega_s & 0 & 0 \\ \omega_s & 0 & 0 & 0 \\ 0 & \frac{\omega_s}{L} & \frac{-R}{L} & 0 \\ \frac{-\omega_s}{L} & 0 & 0 & \frac{-R}{L} \end{bmatrix}$$

$$g(x(k)) = \begin{bmatrix} \frac{3}{2}\omega_s(x_1(k)x_4(k) - x_2(k)x_3(k)) \\ \frac{3}{2}\omega_s(x_1(k)x_3(k) + x_2(k)x_4(k)) \\ x_5(k) \end{bmatrix}$$

$$\begin{aligned} V_{inv\alpha\beta} &= \frac{V_{dc}}{2}\frac{2}{3} P S_{abc} \\ V_{inv\alpha} &= \frac{V_{dc}}{6}(2S_R - S_S - S_T) \\ V_{inv\beta} &= \frac{V_{dc}}{2\sqrt{3}}(S_S - S_T) \end{aligned} \tag{8.12}$$

In order to the controller takes optimal decisions, a cost function must be formed. This function is minimized for the optimum decision and since in this

application, target is to minimize switching losses, while driving the output vector $y = [p, q, U_{mp}]$ between predefined boundaries, the following cost function is formed:

$$J^*(U(k), x(k), u(k-1)) = \min_{U(k)} \frac{1}{N_p} \sum_{l=k}^{k+N-1} C_{sw}(x(l), u(l), u(l-1)) \tag{8.13}$$

$$x(l+1) = Ax(l) + Bu(l) \tag{8.14}$$

$$y(l) = g(x(l)) \tag{8.15}$$

$$y(l) \in \mathcal{Y} \tag{8.16}$$

$$u(l) \in \mathcal{U}, \quad max|\Delta u(l)| \leq 1 \tag{8.17}$$

$$\forall l = k, ..., k+N-1 \tag{8.18}$$

Supposing a receding horizon policy of length N, at time instant k, optimal controller makes predictions of state and output vectors $x_i[k+1]...x_i[k+N], y_i[k+1]...y_i[k+N]$ for all possible input sequences $U_i(k) = [u(k), ..., u(k+N-1)]$, where i is the number of all possible input sequences as imposed by allowed switching transitions of the inverter model. After that,switching cost C_{sw} for all feasible, feasible by the meaning that output constraints $\mathcal{Y}$ are fulfilled throughout the input sequence , are evaluated,and the input sequence with minimum cost is chosen. The cost function is evaluating switching frequency indirectly by choosing the input sequence that drives output vector inside feasible region for the longest time, meaning that no new switching action will be generated by the optimal controller for a longer time period. For a high voltage-high power system where switching losses are linearly dependent on switching frequency, the indirect switching loss calculation utilized here proves to be sufficient. A more analytic approach in calculating switching losses is presented in [35] and can be directly incorporated in the existing cost function but with added complexity and computational effort.

8.3 Solution Algorithm

The solution algorithm through which optimal controller makes decision of next input for a receding horizon policy of $N = 2$ steps is summarized in block diagram ,figure 8.3.

The routine is repeated at each time step k, depending on time that a solution takes to be calculated. Given that for an online controller this time step should be as fast as possible, computational efficiency of the solution algorithm is essential. For that reason precalculated values are used whenever possible and other numerical optimization techniques are taken into consideration. Maximum

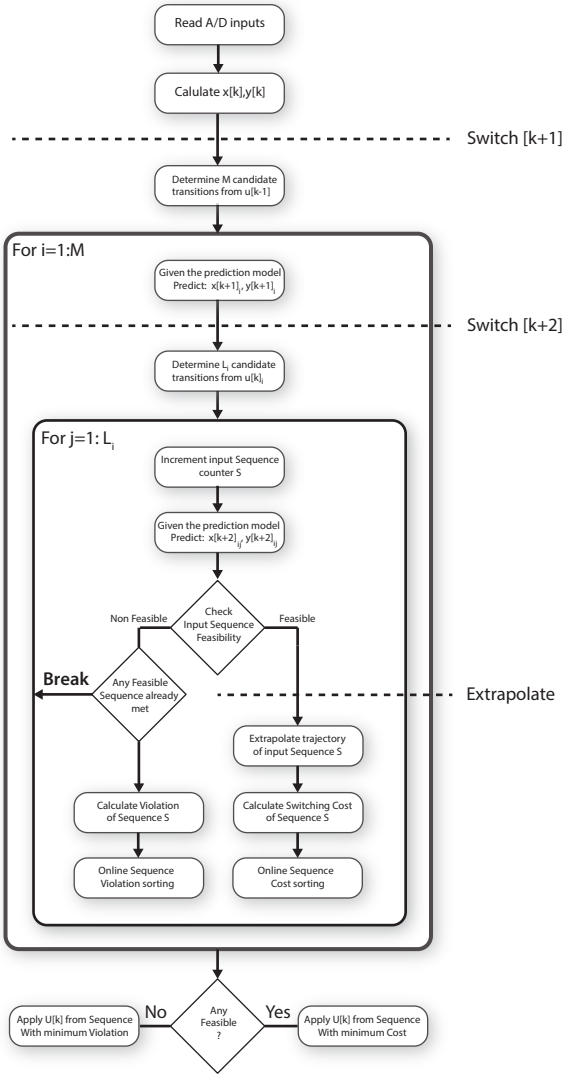


Figure 8.3: MPC flow diagram

time allowed for a decision to be taken from the optimal controller is proportional to the output inductor and stability should be guaranteed [33].

8.3.1 Timestep k ,Present State

At time step k measurements of grid current are taken, transformed into the $\alpha\beta$ reference frame and estimations of grid virtual flux are made in the same way as in conventional DPC. In order to complete the present state vector, measurement of mid point voltage is needed $U_{mp}[k]$. Output vector $y[k]$,active and reactive power, is calculated and stored same as in conventional DPC.

8.3.2 Timestep k+1, Horizon=1

Based on switching state selected at previous time step k-1, $u[k-1]$, a set of possible switching transitions is set to be explored in next time instant $k+1$. Allowed transitions are posed by physics of the inverter, so as the three-level NPC inverter is never allowed to switch in the same phase from $\frac{Vdc}{2}$ to $-\frac{Vdc}{2}$ protecting active devices from over-voltage and avoiding extensive switching. Allowable transitions for a 3 level NPC can be visualized in figure 8.4.

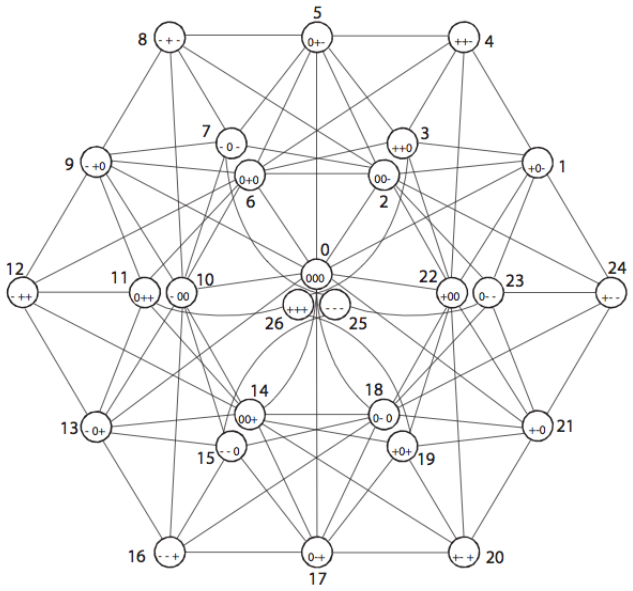


Figure 8.4: NPC allowed state transition map (Courtesy of ABB ATDD, Switzerland)[36]

At first the algorithm forms recursively a tree of all possible input sequences.

At time step $k+1$, for every i candidate input $u[k]_i$ as selected in previous step, predictions are made for state vector $x[k+1]_i$ and estimation of output

vector $y[k+1]_i$ using difference equations of discrete model, forming a tree of candidate switching sequences .

8.3.3 Timestep k+2, Horizon=2

At time step $k+2$, as for previous time step, all new candidate states $u[k+1]_{ij}$ of previously derived switching sequences, are evaluated, and used to predict and store state and output vectors $x[k+2]_{ij}, y[k+2]_{ij}$. The tree of candidate switching sequences (figure 8.5) now has a depth of $N = 2$.

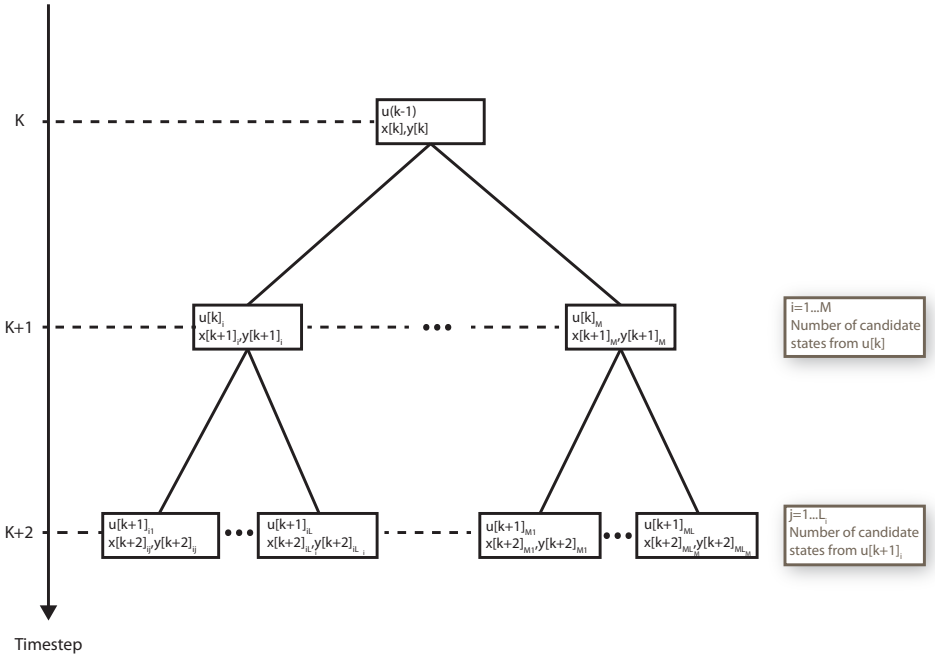


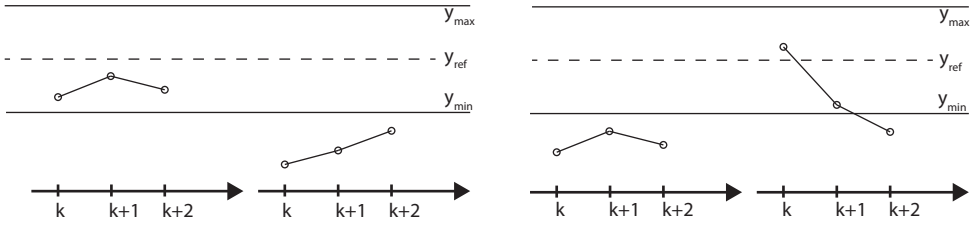
Figure 8.5: Candidate Input Sequences tree

8.3.4 Sequence Feasibility Sorting

Next the algorithm evaluates feasibility of all candidate sequences. A switching sequence is considered feasible when constraints posed on output vector are satisfied during all time steps (Hard Constraints) , or they are pointing to the right direction. Pointing to the right direction means that even if either of the output is outside of its predefined bounds, the input sequence drives the output towards the respective reference value.

An example of feasible sequence is given in figure 8.6. If at any time step for a given input sequence, any output variable lies outside of predefined boundaries, the trajectory direction of this variable for $U_i[k+1]$ to $U_i[k+2]$ is examined.

If the variable is moving towards the reference point the sequence is considered feasible, otherwise the respective input sequence is considered non feasible.



(a) Trajectories that are either feasible or pointing inbounds

(b) Trajectories that are neither feasible nor pointing inbounds

Figure 8.6: example of feasible and non feasible trajectories

8.3.5 Extrapolation of Feasible sequences

At the end of candidate sequences sorting, trajectories of output variables of feasible input sequences,if any, are extrapolated linearly in time until they reach out of bounds,"emulating" a longer prediction horizon. By doing so an approximation of how long a switching sequence will keep the output variables inside the feasible region is made. There are other ways to extrapolate output variables in time, thoroughly presented in [34], but simple linear extrapolation provides a good enough and computationally efficient method.In figure 8.7 an example of trajectory extrapolation is depicted. The slope of the extrapolated line from the last two trajectory points, $y[k+1], y[k+2]$ can be calculated as:

$$\lambda = \frac{y[k+2] - y[k+1]}{(k+2) - (k+1)} = y[k+2] - y[k+1] \tag{8.19}$$

and the number of steps until the trajectory is out of bounds of all output variables $ny_i = [np_i, nq_i, nU_i]$:

$$ny_i = \begin{cases} \frac{y_{max} - y[k+2]}{\lambda} & \text{if } \lambda \geq 0, \quad y_{max} = y_{ref} + y_{bound} \\ -\frac{y_{min} + y[k+2]}{\lambda} & \text{if } \lambda < 0, \quad y_{min} = y_{ref} - y_{bound} \end{cases}$$

For each sequence, the maximum number of steps before a new switching action will be generated by the controller is the minimum steps number of all three output variables.

$$n_i = \min(np_i, nq_i, nU_i) \tag{8.20}$$

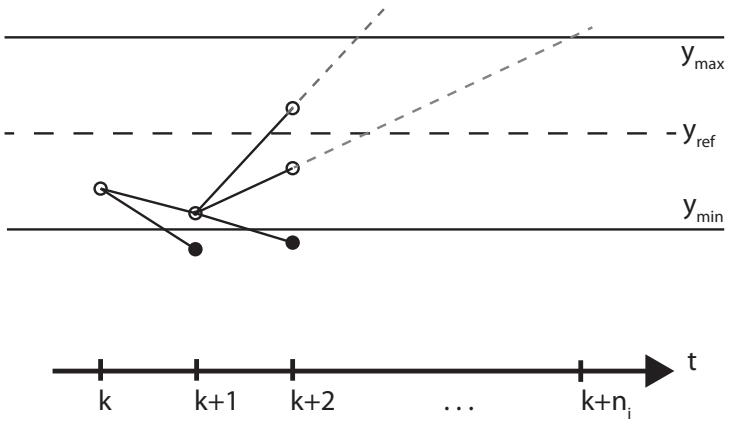


Figure 8.7: linear extrapolation of output variable

8.3.6 Cost Calculation

For each extrapolated output variable trajectory of each feasible input sequence i, the shorter number of steps until driven out of bounds n_i is stored and used for the calculation of cost c_i. That physically means that each feasible input sequence will remain feasible for n_i steps until a new switching event will be trigerred. The cost function can be expressed as:

$$c_i = \frac{s_i}{n_i} \tag{8.21}$$

where s_i is the number of switching actions between state transitions of input sequence i expressed as:

$$s_i = \sum_{l=k}^{k+N-1} ||u_i(l) - u_i(i-1)||_1 \tag{8.22}$$

After cost has been calculated for all feasible input sequences, the one with minimum cost is selected, and $u[k+1]$ of optimal sequence is applied during next time step and set as $u[k]_{new}$.

8.3.7 Handling Infeasibilities

If no feasible input sequence exists, then the violations that occur in output vectors at first prediction time step, $y[k+1]$, are evaluated, and the one with minimum violation v_i is selected. Violation of output vector $vy_i = [vp_i, vq_i, vU_i]$ of sequence U_i is calculated as the distance of the output variable from the closest bound.

$$vy_i = \begin{cases} y[k+1] - y_{max} & \text{if } y[k+1] > y_{max}, \quad y_{max} = y_{ref} + y_{bound} \\ y_{min} - y[k+1] & \text{if } y[k+1] < y_{min}, \quad y_{min} = y_{ref} - y_{bound} \end{cases}$$

Maximum violation of output vector variable is set as the violation v_i of input sequence: U_i

$$v_i = \max(vp_i, vq_i, vU_i) \tag{8.23}$$

8.3.8 First Check and Delay Compensation

In order to minimize switching frequency and speed up next time step input calculation a test if no switching is necessary for the next horizon length time is carried. Before the algorithm starts to search for the next optimal solution, it is checked whether application of previously applied input, throughout whole horizon length, an input sequence where $u[k+2] = u[k+1] = u[k]$, is a feasible input sequence thus driving the output inside the feasible region . If this is true, no further optimization is executed, since this input sequence represents a zero cost solution and it guarantees minimization of cost function.

In practical implementation of the MPDPC algorithm, non optimal behavior of the controller might be observed in case of delay mismatch in the control loop. A technique proposed and presented in [37], compensates for this delay by utilizing the internal prediction model and shifting in time present state measurements $x[k]$, by N_c timesteps , so as:

$$x[k]' = x[k + N_c] \tag{8.24}$$

8.3.9 Branch and bound

Branch and Bound as presented in [38] is a common technique to speed up optimal controller's decision time. The main concept is before beginning to explicitly calculate the cost that an input sequence will yield, an estimation of the optimum cost is made and if this input sequence is a promising one, meaning

that the optimum cost to be met at the end of sequence exploration is better than the one already calculated, it is explored otherwise it is bypassed.

Main control mechanisms of branch and bound technique are optimum cost calculation of a candidate input sequence based on its present state, and maximum amount of calculations allowed for the optimum cost calculation before the final descision is taken. As it gets obvious, in order to yield significant execution speed gain, the branch and bound should be warm started, meaning that a low cost is acquired in the beginning so as many as possible input sequences are not necessarily explored. In worst case scenario, if maximum number of allowed calculations is not met, all candidate input sequences are explored with no speed gain at all,and if maximum number of allowed calculations is met, solution provided by the optimal controller is the best from every other candidate input met, but probably not the optimum.

8.4 Heuristic MPDPC

8.4.1 External Midpoint Balancing

Since for a short horizon of $N = 2$ steps branch and bound optimum cost calculation computational effort gain is not considerable, a different approach was set in order to lower computational effort of the optimal controller. The main concept is to remove the midpoint Voltage balancing from the optimal controller, reducing computational effort in the solution algorithm and increasing execution speed.

Midpoint Voltage balancing is achieved by an external loop as in conventional DPC described in section[Midpoint Voltage Balancing]. Calculating current flowing in the midpoint of two DC link capacitors and monitoring capacitor voltage difference, a hysteretic external control loop is employed, as in figure 8.8. By doing so, optimization process is called for two controlled variables, allowing for a much faster algorithm implementation. Moreover number of candidate sequences is decreased as more restrictions apply for switching transitions since positive small vectors, as defined in the NPC section, will be excluded when in search for candidate state transitions that reduce midpoint voltage and negative small vectors when in need to augment midpoint voltage .

Core idea is that midpoint needs just to be balanced between specific bounds for proper operation, without need of optimal driving . In the following simulations, it is obvious that this kind of state exploration reduction leads to slightly sub-optimal function of the converter, but with proper extensions and inclusion of medium switching vectors in the Midpoint Voltage control loop it is strongly believed that this abstraction can achieve similar performance to the full scale optimization process.

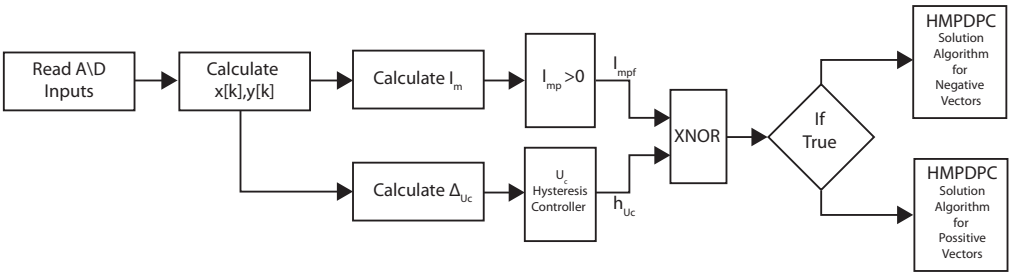


Figure 8.8: External Midpoint Control loop adoption

8.4.2 Active and Reactive Power Coupling - PQ-R

In an attempt to even lower optimal controller's solution computational effort , active and reactive power are combined in one variable leading to a single Positive Variable optimization. Main concept is that since active and reactive power components are naturally related, a common variable can be tracked in order for them to stay inbound given constraints.

Considering a complex space where Real axis is the measured Reactive Power deviation from reference set point Δq and Imaginary axis is the Active Power deviation from reference set point Δp, output state vector of the previously derived state space model of the converter can be described by a single complex number, whose magnitude R reflects deviation from the axis origin point.

$$\begin{aligned} \Delta p &= P_{ref} - P \\ \Delta q &= Q_{ref} - Q \\ \mathrm{Z} &= \Delta p + \Delta q \\ R &= |\mathrm{Z}| = \sqrt{\Delta p^2 + \Delta q^2} \end{aligned} \tag{8.25}$$

The described space is illustrated in figure 8.9. By equally bounding Active and Reactive power which is the case of constraints for the presented MPDPC, a circle with the maximum allowed magnitude is formed with radius $R_{max} = \sqrt{P_{bound}^2 + Q_{bound}^2}$. This is the area where one state described by the complex number previously defined, is considered to satisfy constraints of predictive controller.

MPDPC solution algorithm already presented can be executed for R instead of P, Q, as the midpoint voltage is controlled by the external loop previously described, which will simplify, feasibility sorting to a single comparison with R_{max}, and extrapolation step to a single,positive only, variable extrapolation.

So after state exploration, the sequence will be considered feasible if:

$$R[k+1] < R_{max} \quad \textbf{AND} \quad R[k+2] < R_{max} \qquad \text{,feasible}$$

OR

$$R[k+2] < R[k+1] \qquad \text{,pointing inbound}$$

And the number of steps until the trajectory is out of bounds after linear extrapolation of R ny_i:

$$ny_i = \frac{R_{max} - R[k+2]}{R[k+2] - R[k+1]} \tag{8.26}$$

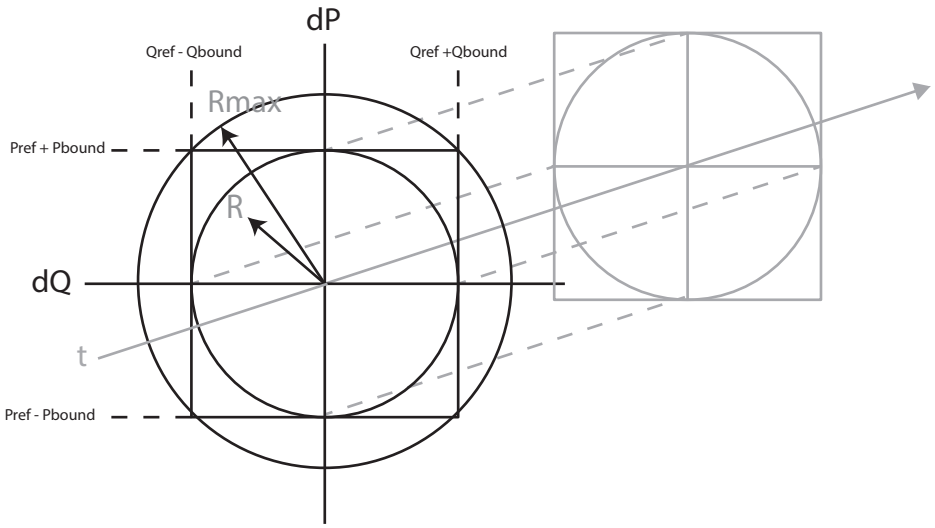


Figure 8.9: PQ-R concept

By depicting the axis perpendicular to the Complex level previously defined, as the time axis, one can illustrate trajectories of feasible sequences as those enclosed by the cylinder with radius R_{max} and height the timestep prediction horizon.

As it will be described in the simulations section of the suggested MPDPC technique simplification, despite the computation efficiency gain presented, performance is deteriorated compared to full scale MPDPC optimization, and results can relate only to DPC. Either a consequence of wrong implementation or as a natural consequence of Active and Reactive Power in one variable, coupling observed among the two controlled variables is a major drawback and probably renders this simplification of no use.

8.5 Simulation Results

A simulation was set up in matlab simulink in order to investigate the MPDPC algorithm and the proposed variations. At each case the system response is evaluated for a step change in one controlled variable while the other is remaining constant. The simulated system represents a 1KW 3-level inverter connected to a three phase grid of $70V_{rms}$ with a DC bus of 200 V. The midpoint Capacitance is 1000uF and the total filter inductance 8.5mH. The same system simulated for simple DPC technique is now evaluated for the MPDPC algorithm so as to have a reference point and properly compare the two control approaches.

8.5.1 MPDPC

First the MPDPC solution algorithm, as described in this chapter, is evaluated. A step reference change of active power is set while reactive power is set to zero.

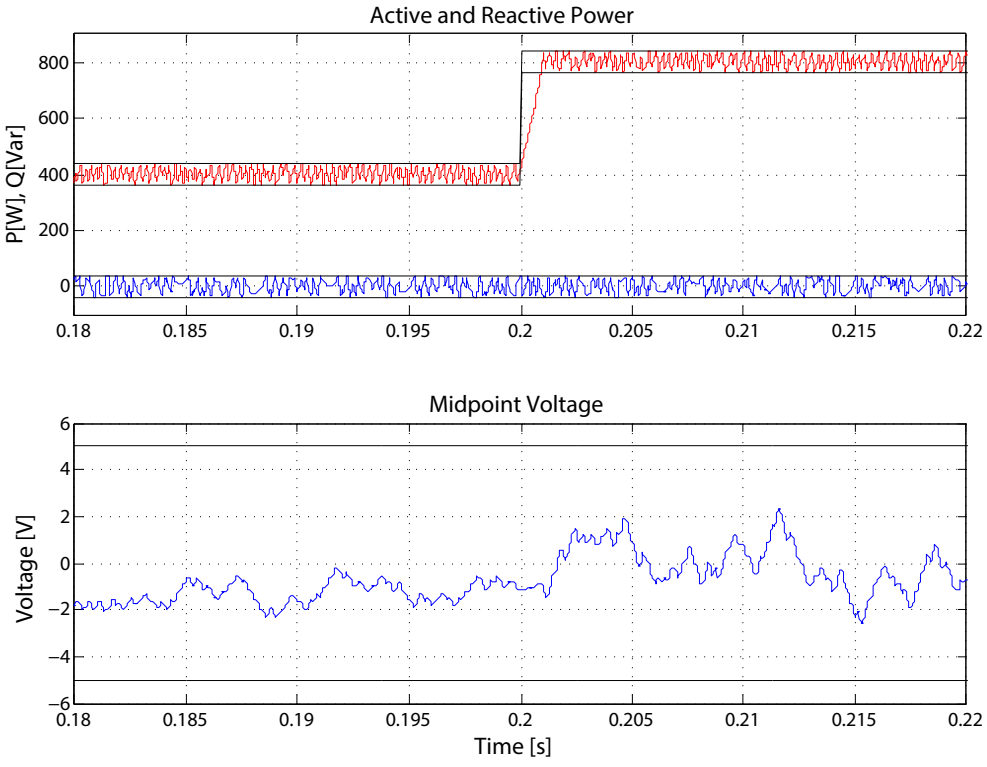


Figure 8.10: MPDPC controlled variables active power step change

Both controlled variables are tightly preserved between the desired bounds, which are also plotted in the same graph and preserve same responsiveness of DPC method as well as decoupling of controlled variables. Midpoint Voltage is

balanced in a more precise way than the hysteretic control of simple DPC.

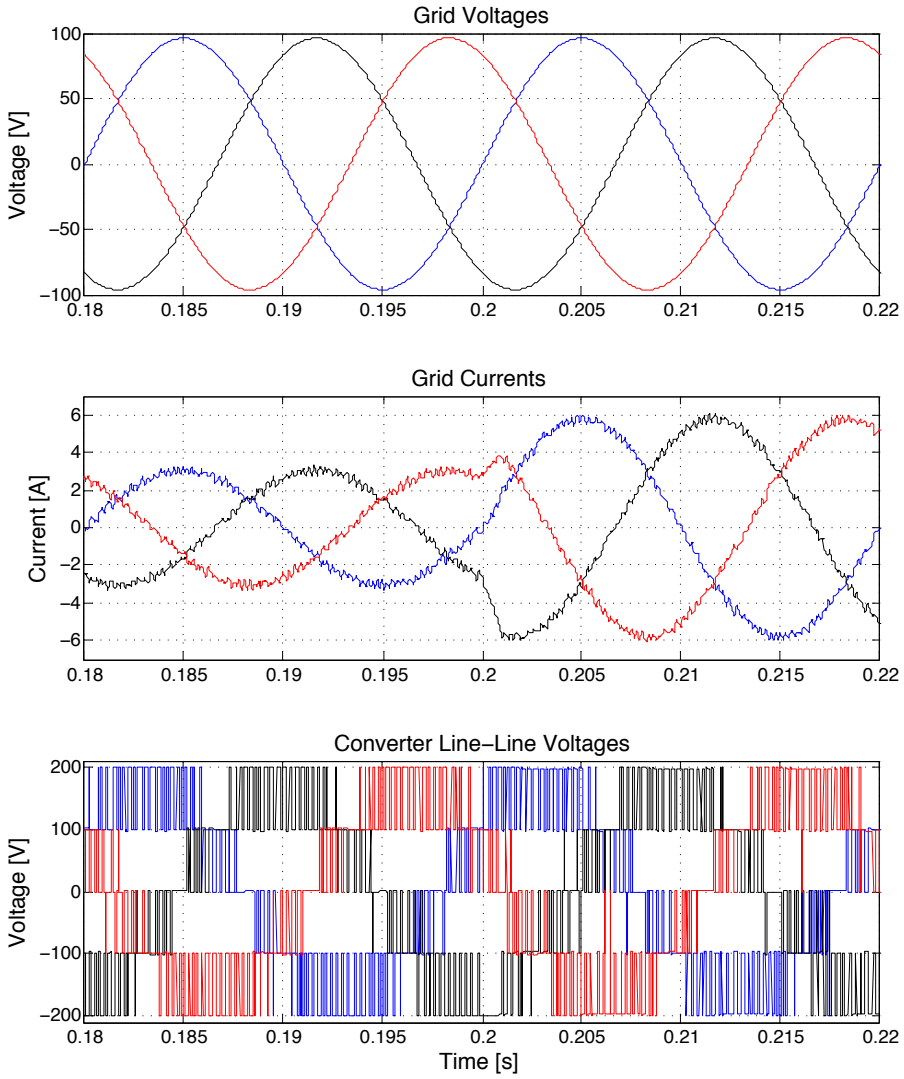


Figure 8.11: MPDPC 3 phase measurements - active power step change

Inverter Voltage Output are guaranteed to avoid extensive switching and prohibited transitions, while maintaining a significant lower average switching frequency of $880 - 900\ Hz$. As it gets obvious current waveforms are much cleaner than conentional DPC with a measured THD of 1.25%

In the reactive power reference step test, same observations are met. Reactive Power is driven always within specified bounds and the step change is made with a fast response.

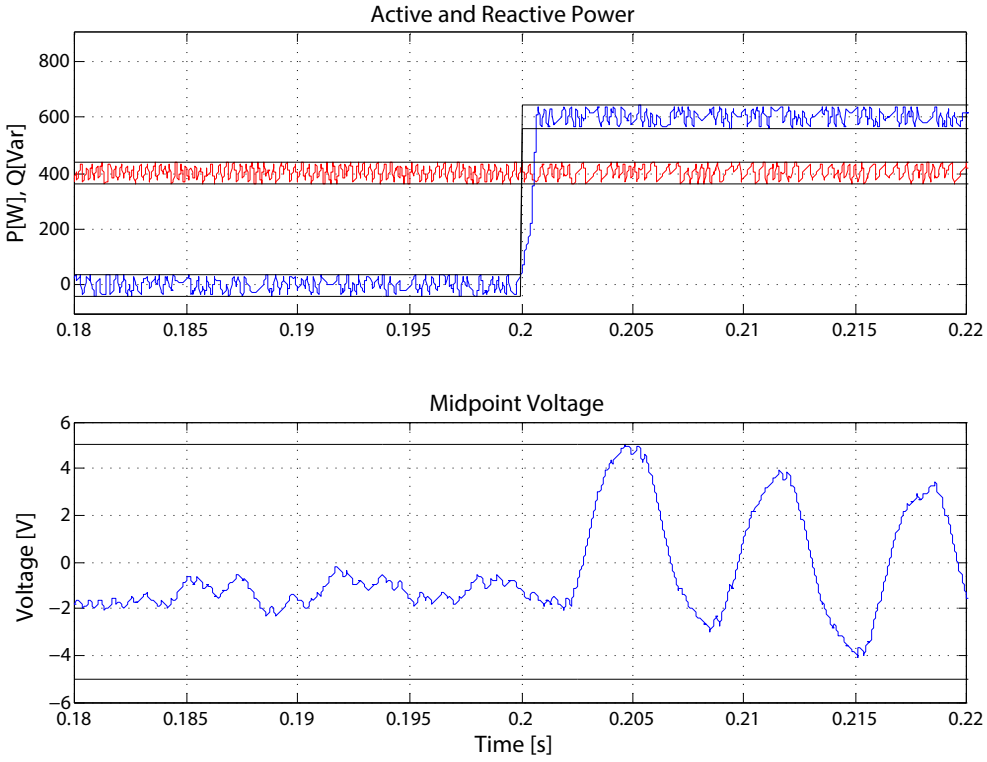


Figure 8.12: MPDPC controlled variables reactive power step change

In general, evaluated MPDPC technique resembles great response, and outperforms conventional DPC in all aspects with a great trade off in control complexity and computational effort required.

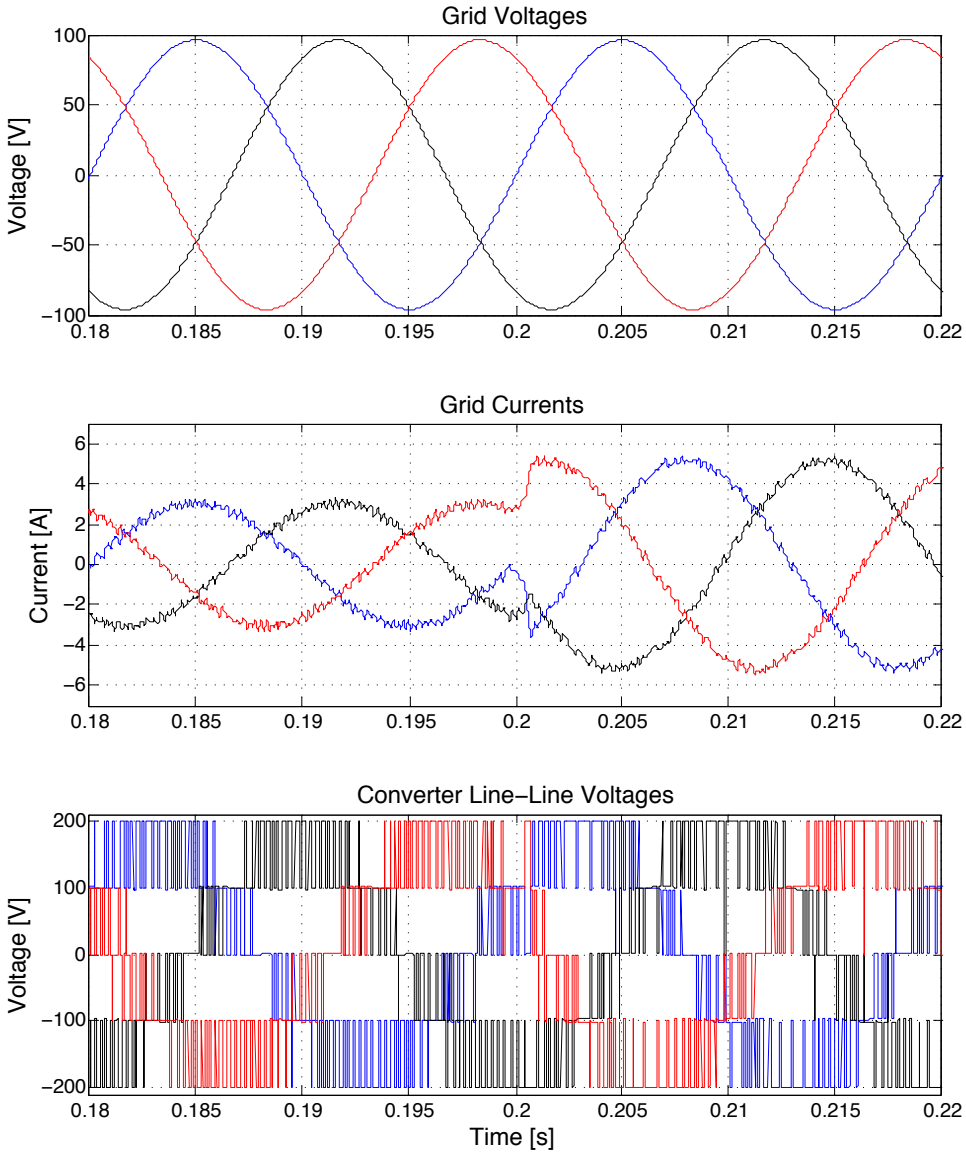


Figure 8.13: MPDPC 3 phase measurements - reactive power step change

8.5.2 HMPDPC with external midpoint balance

Same system simulated utilizing MPDPC technique, is extended to use the concept of external midpoint balancing as previously described. Again two step reference changes are evaluated as in previous simulations.

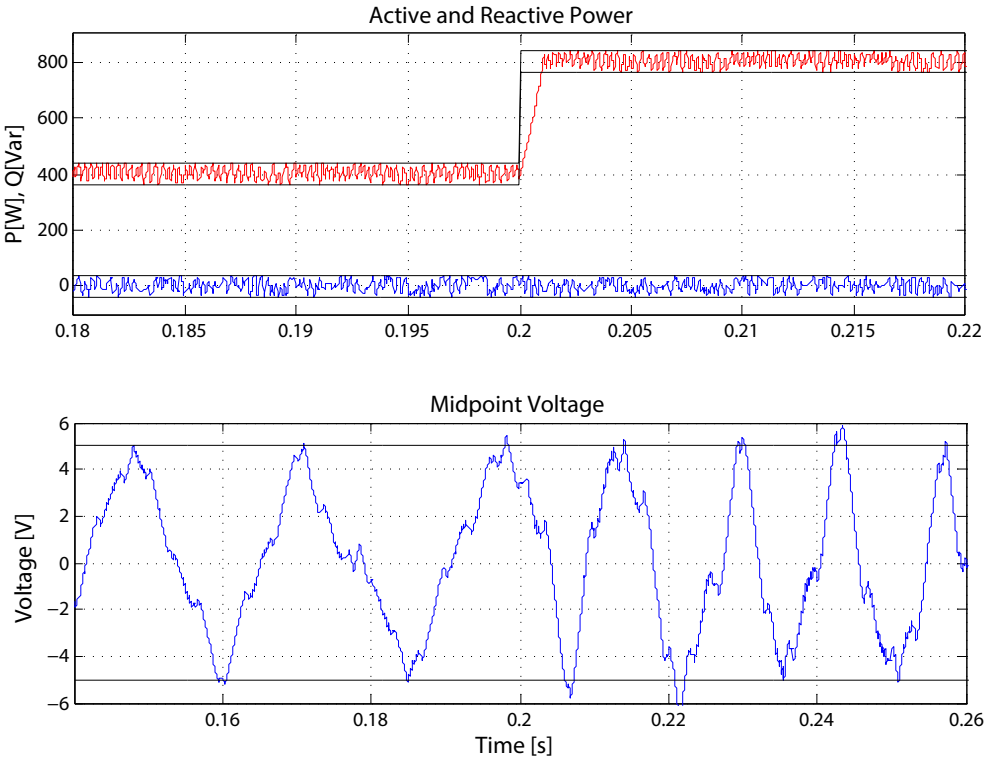


Figure 8.14: MPDPC controlled variables active power step change

In first test, active and reactive power are driven constantly in bounds and midpoint voltage balancing resembles the hysteretic behaviour met in DPC, but bound are violated in order to a low the controlled variable to change direction.

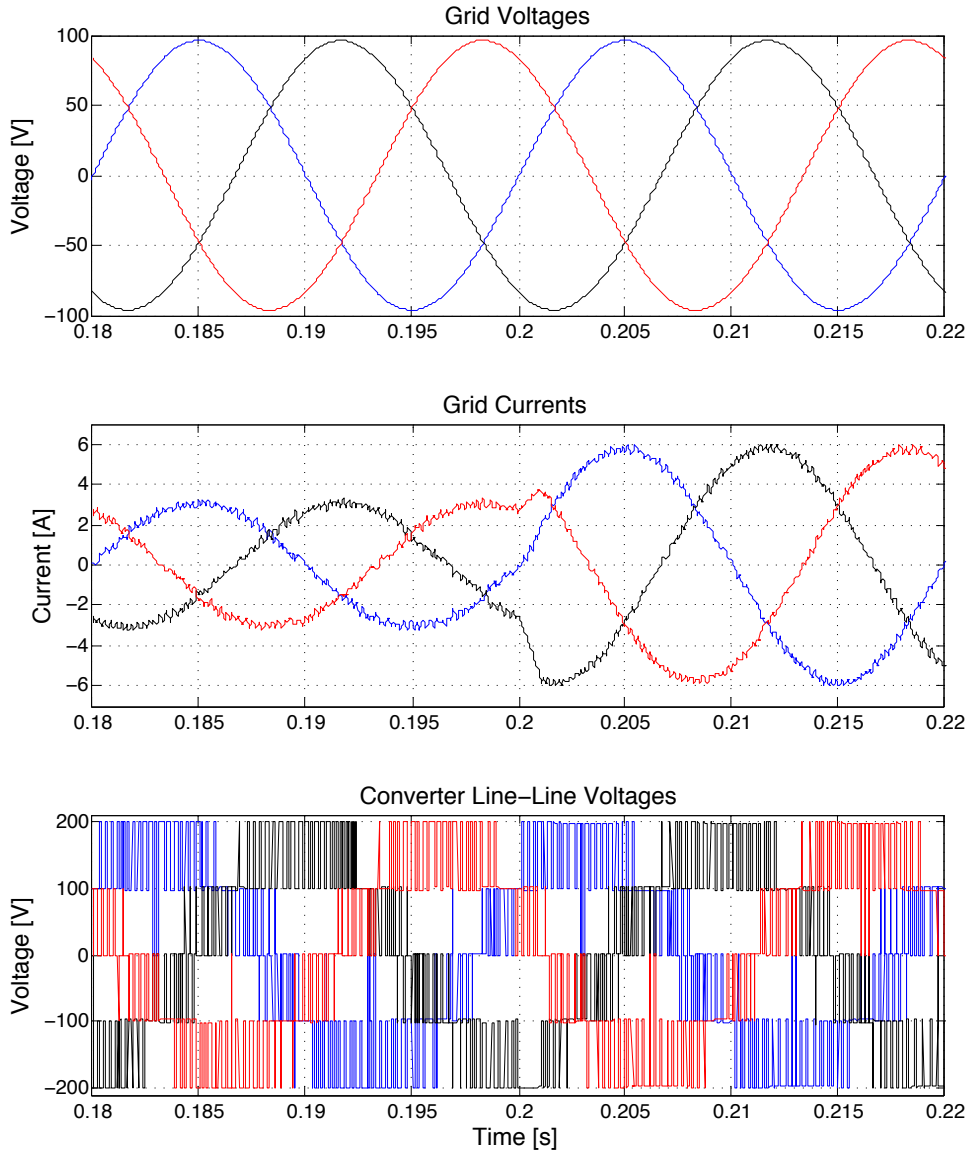


Figure 8.15: MPDPC 3 phase measurements - active power step change

Grid Current preserves a low THD of 2.1% with a slight increase in average switching frequency $880 - 900\,Hz$. Increase in switching frequency appears to be normal, since solutions of the HMPDPC algorithm might be sub-optimally compared to MPDPC previously described.

In second test as well, same conclusions can be made, that the HMPDPC technique performs well but sub optimal compared to MPDPC.

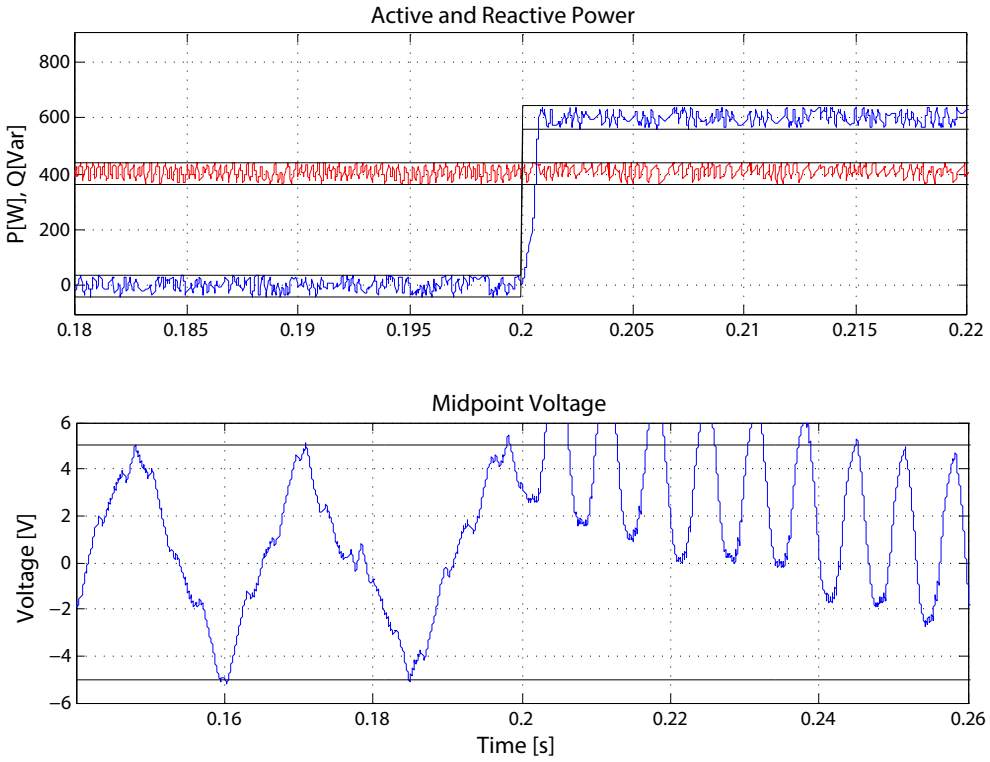


Figure 8.16: MPDPC controlled variables reactive power step change

A remark that should be made, is that with increase of output current, midpoint voltage bound violation tends to be more extensive, thus the HMPDPC technique might need extra protections in order to guarantee safe operating areas of semiconductors utilized.

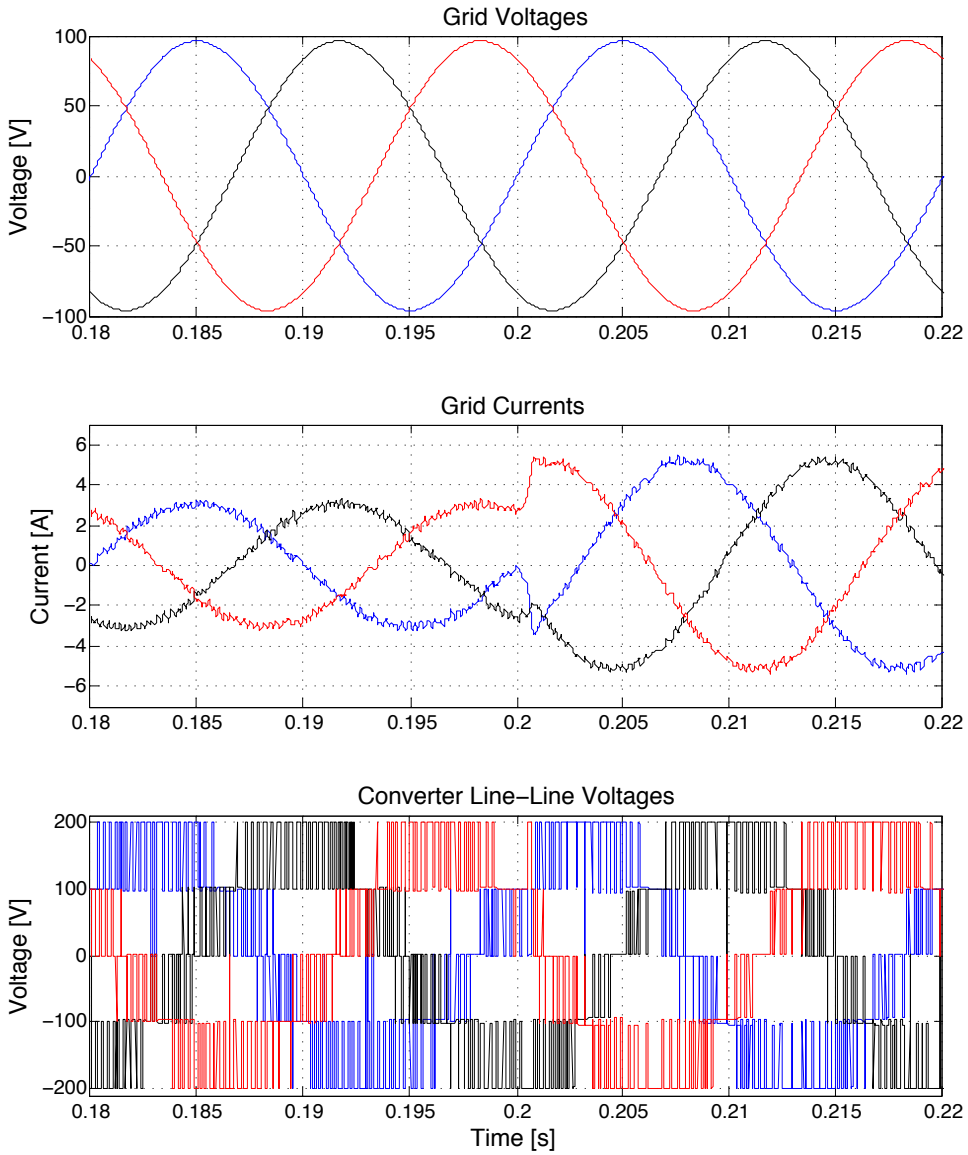


Figure 8.17: MPDPC 3 phase measurements - reactive power step change

8.5.3 HMPDPC with PQ coupling

The PQ coupling technique is evaluated in the same way as two previous MPDPC techniques were tested. In overall this technique is by far sub optimal compared to the two previous techniques, by means that it exhibits inherent coupling between the two controlled variables, but this is tolerated as the assumption was that this technique would be utilized in an application where active and reactive power are naturally coupled.

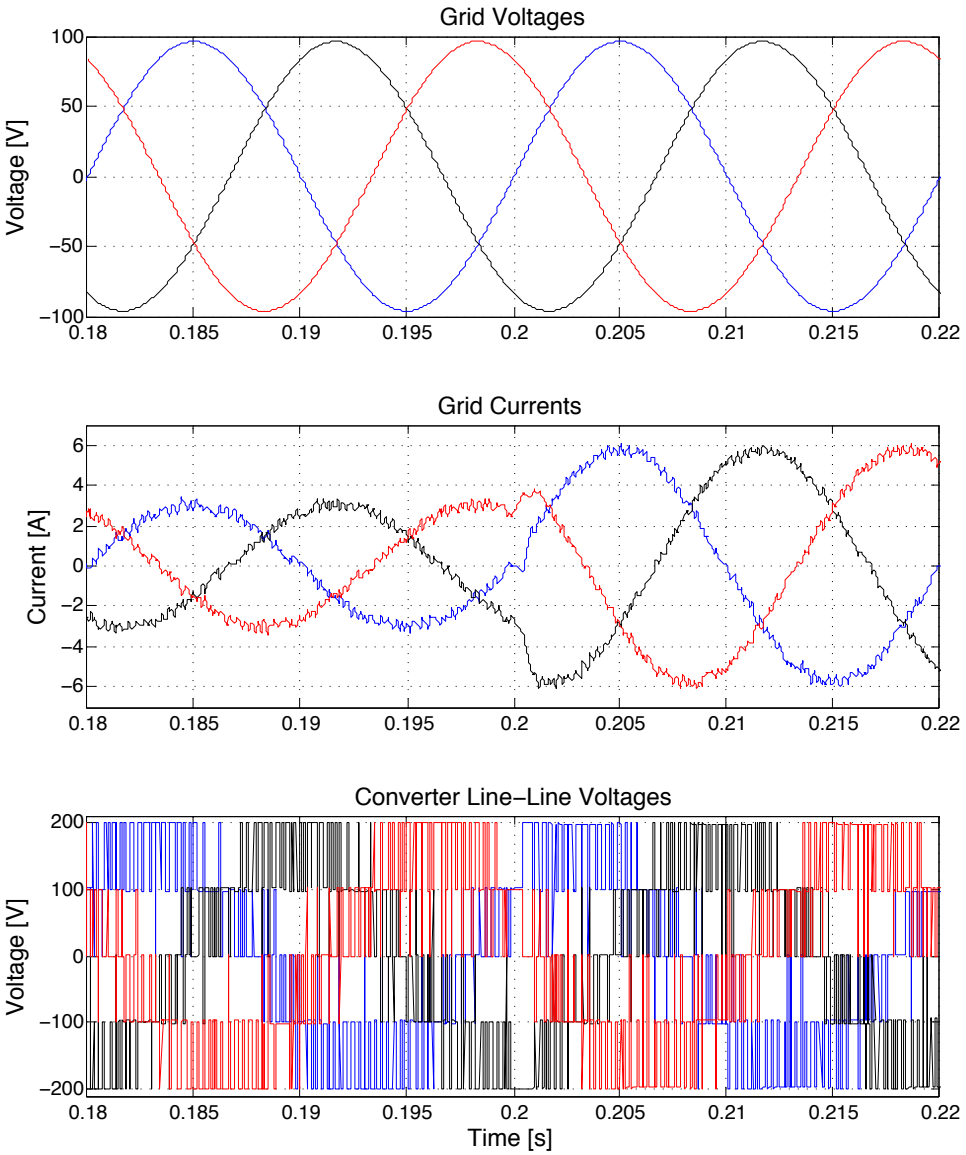


Figure 8.18: MPDPC 3 phase measurements - active power step change

Another drawback is that it preserves switching frequency in the same levels of conventional DPC $1260 - 1300\,Hz$, but compared to DPC it bears much cleaner output current with a THD measured at 1.44%. and with guaranteed switching solutions that would not violate switching transitions rules.

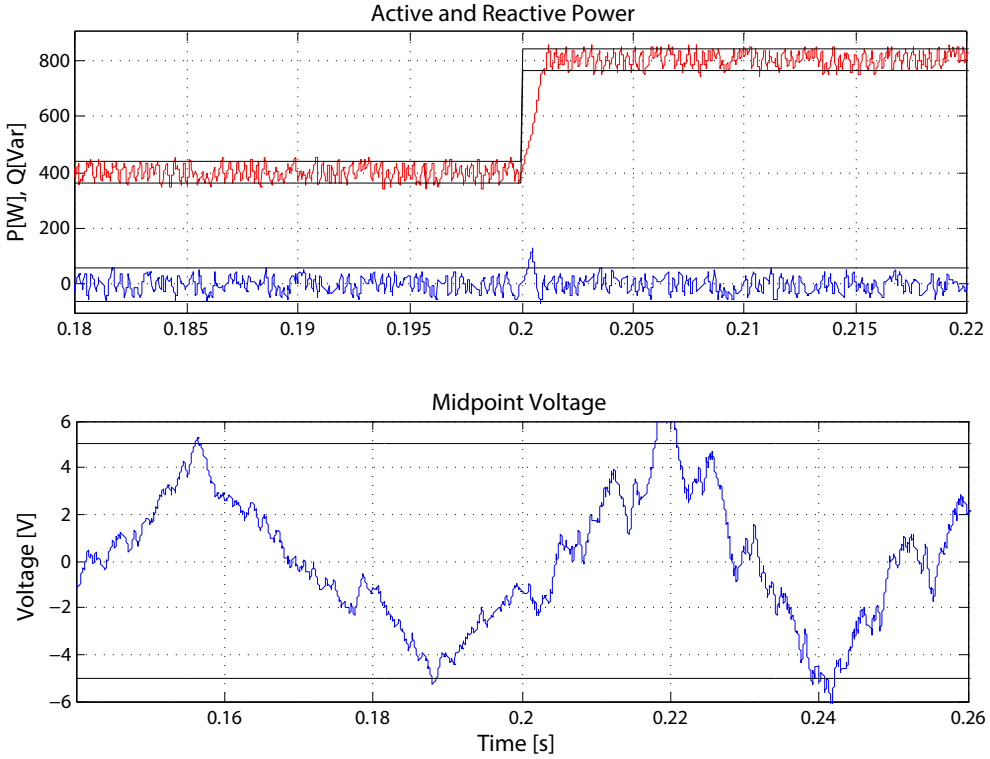


Figure 8.19: MPDPC controlled variables active power step change

In both test simulations the controlled variables are properly driven while midpoint voltage balance is maintained in the same hysteretic manner as in DPC. It appears that by selective tuning, the algorithm can outperform DPC, but only if controlled variables coupling is not an issue in the specific application. The proposed simplification of MPDPC as is, is by far sub optimal compared to conventional MPDPC, but might be utilized as part of a more complete MPC solution abstraction.

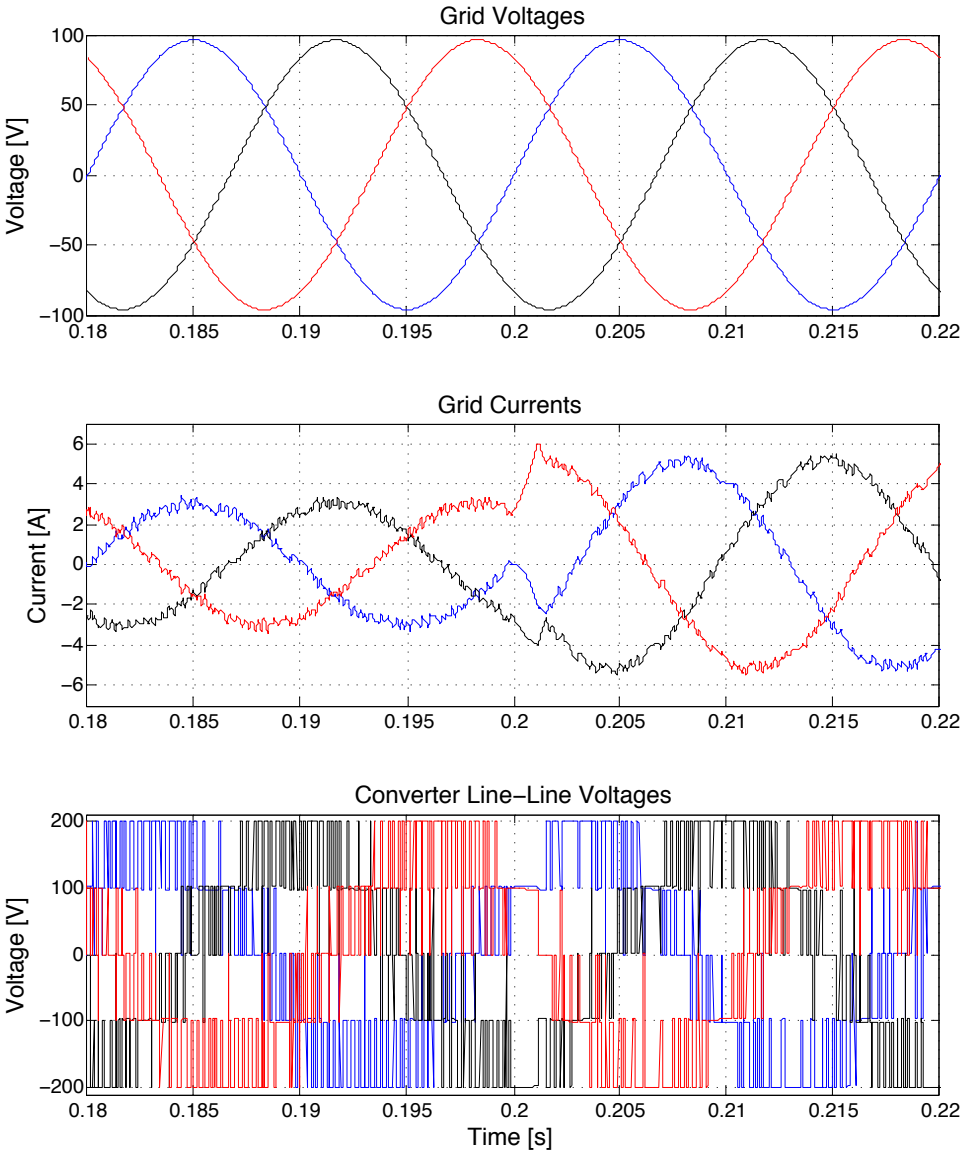


Figure 8.20: MPDPC 3 phase measurements - reactive power step change

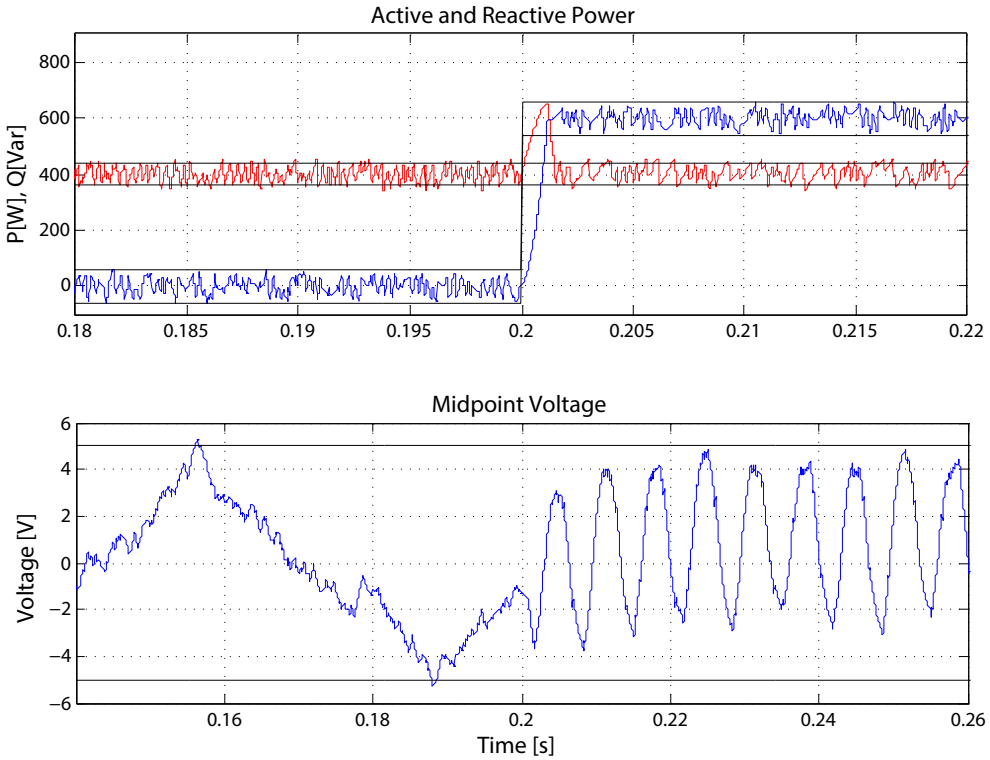


Figure 8.21: MPDPC controlled variables reactive power step change

8.6 Experimental Results

Hardware setup used for the DPC prototype is used to evaluate a low scale prototype of the NPC inverter running on MPDPC. Even though Boombox is a powerful platform, a DSP only implementation of a predictive controller is a task requiring a great amount of computational resources. Online Optimization problems and Online Predictive control especially call naturally for a parallel architecture approach in order to efficiently solve the optimization problem. Of course the Boombox also has a user configurable FPGA on board which can be configured to parallel the optimization stage of the solution algorithm, but such an implementation would be out of scope of this thesis. A serial-architecture approach on MPDPC implementation was adopted in order to evaluate the presented MPDPC technique, and with various optimization techniques the control loop execution time reached $80\mu Sec$, with $25\mu Sec$ being the original benchmark. The Boombox is definitely able to get control loop faster than that, especially if a parallel optimization stage is considered.

The setup parameters are synopsized as:

$$
\begin{aligned}
L_g &= 8.5\, mH \\
V_{dc} &= 70\, V \\
C_{dc} &= 1000\, \mu F \\
V_s &= 20\, V \\
f_s &= 50\, Hz
\end{aligned}
$$

As in simulation environment and as in DPC experimental part, two tests are done to the hardware setup. One step change in active power while maintaining reactive power reference zero, and one step change in reactive power reference while maintaining active power reference constant are performed. The following results are for the conventional MPDPC technique described in previous section. In figure 8.22, active power reference is changed from zero to $100W$ while reactive power is set to zero. Both controlled variables follow the reference values in the expected way, but boundaries are clearly violated in certain cases, while a low frequency offset appears in both active and reactive power. Such an effect can be contributed to the fact that the control loop execution is 3 times slower compared to the simulation environment, and low signal to noise ratio due to wider range of the calibrated current sensors as explained in the DPC experimental setup section. Midpoint Voltage balance is achieved and maintained.

Grid current and converter voltage output depicted in figure 8.23 are acceptable considering directly controlled variables performance, and in comparison to DPC experimental results it maintains a lower current THD and a low switching frequency.

For the second test, active power reference is set constant to $50\, W$ while reactive power reference is changed from zero to $100\, Var$. Same Observations

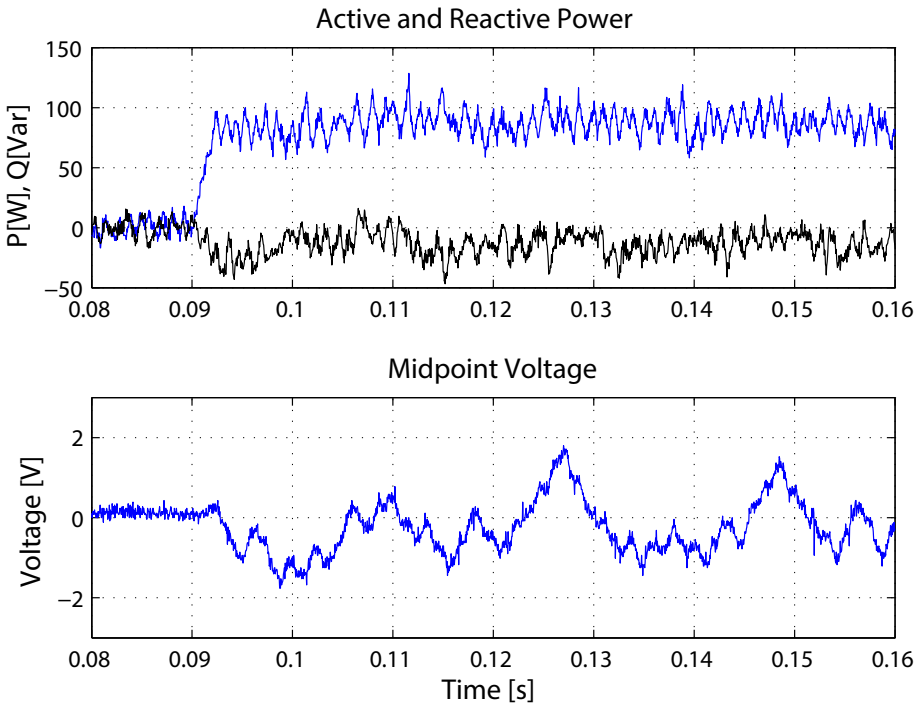


Figure 8.22: MPDPC controlled variables active power step change

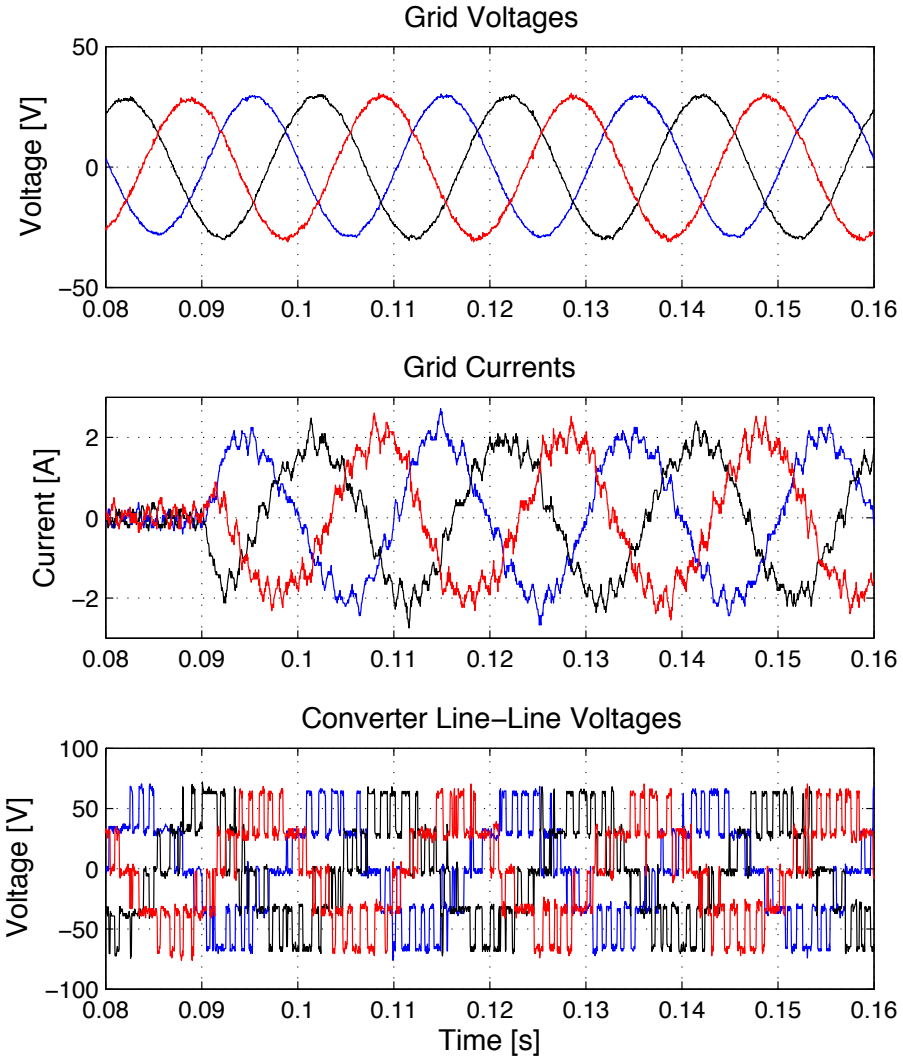


Figure 8.23: MPDPC 3 phase measurements - active power step change

made in previous test of the setup can be made here as well. While active and reactive power follow their respective references and midpoint voltage balance is maintained, figure 8.24, Low frequency oscillation offset is present and unexpected distortion at the grid output current, figure 8.25.

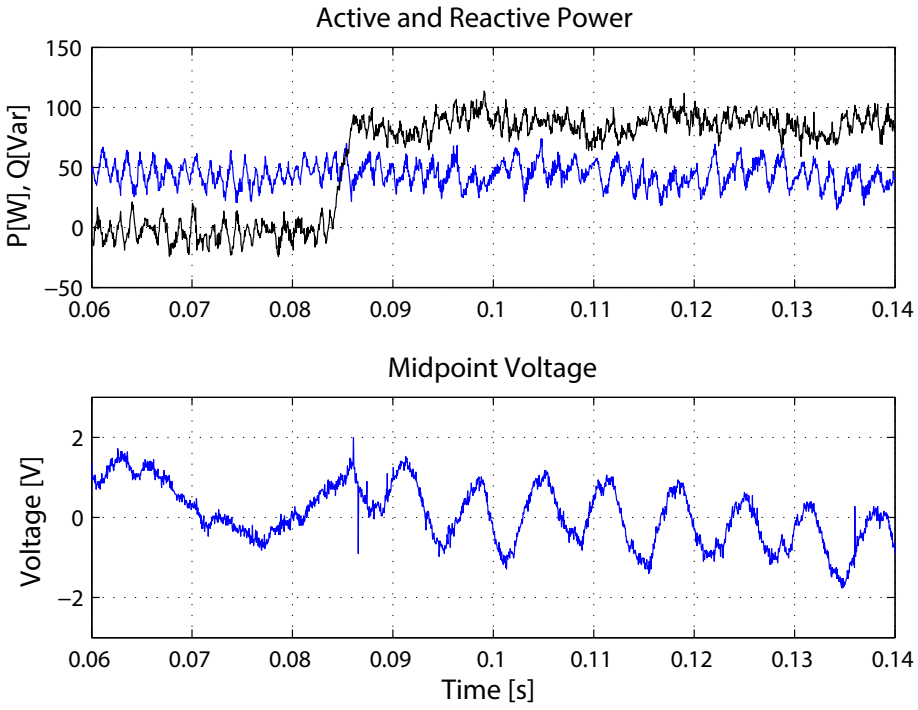


Figure 8.24: MPDPC controlled variables reactive power step change

Compared to DPC experimental results of the same system, MPDPC is proved to be superior, as apart from the expected gain in performance, MPDPC control,it also appears to be less immune to noisy measurement input. Even if not the prototype test measurements represent an elaborate MPDPC implementation, the presented setup can evaluate all the proposed MPDPC variations as proof of concept and illustrate superiority of online optimization versus conventional DPC.

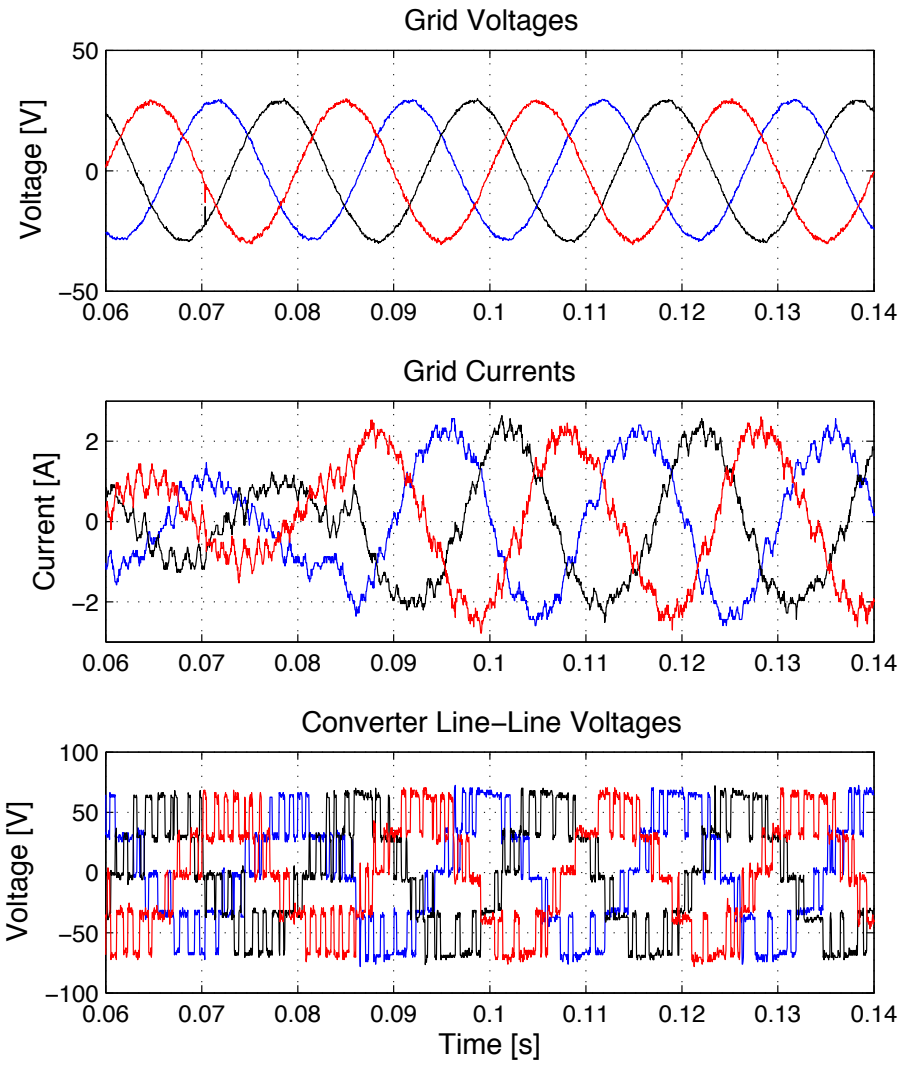


Figure 8.25: MPDPC 3 phase measurements - reactive power step change

CHAPTER

NINE

MPDPC WITH LCL FILTER

The concept of Model Predictive Direct Power Control with LCL output filter is to incorporate active damping to resonant frequencies of the filter and higher harmonic content when an LCL filter is used to interface the NPC converter to the grid. As in Direct Power Control the switching frequency generated by constrained optimal controller is varying, making it possible to generate harmonics at and around the resonant frequency of the filter, producing excessively distorted currents.

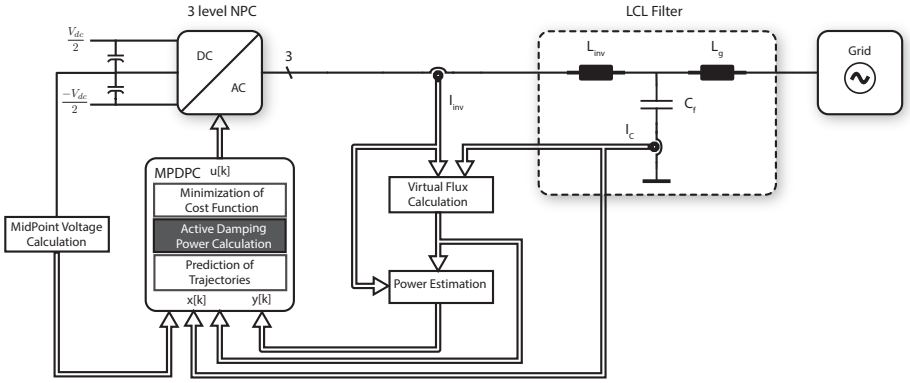


Figure 9.1: MPDPC with LCL scheme

The same strategy followed in conventional Direct Power Control is followed in MPC, as described in section [Active Damping]. In order to actively damp harmonic currents the idea of virtual resistor is adopted and an outer loop is formed, where harmonic active and reactive power to be compensated are calculated. As for conventional DPC, reactive power compensation due to presence of filter capacitor is still needed. The active and reactive power references together

with the active damping and compensation signals are fed into the optimal controller where the new bounds for the output vector constraints are calculated. Also the use of an extra voltage sensor, is needed, in order to monitor filter capacitor voltage. In case of a sensorless LCL filter system, filter capacitor current and voltage estimations can be made as previously presented in equation 7.7. A general overview of the MPDPC with LCL filter is illustrated in figure 9.1.

9.1 Physical Modeling

With the addition of the LCL output filter, the state space equations describing the physical model of the grid connected NPC inverter should be reformed. Using equivalent circuit,figure 9.2, and analysis presented in conventional DPC with LCL output filter the following differential equations describe the grid connected NPC inverter

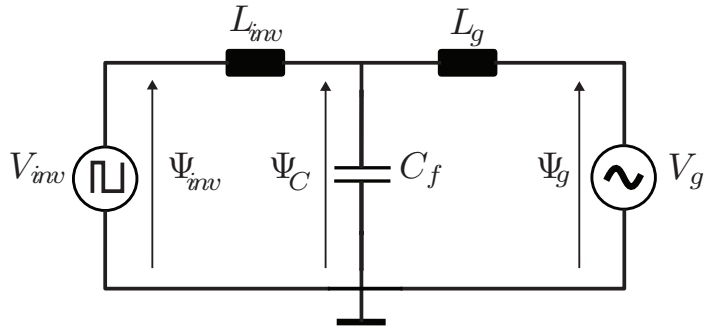


Figure 9.2: LCL output filter equivalent circuit

$$\frac{d\psi_{g\alpha}}{dt} = -\omega\psi_{g\beta}\,, \qquad \frac{dV_{C\alpha}}{dt} = \frac{1}{C_f}I_{c\alpha}\,,$$

$$\frac{d\psi_{g\beta}}{dt} = \omega\psi_{g\alpha}\,, \qquad \frac{dV_{C\beta}}{dt} = \frac{1}{C_f}I_{c\beta}\,,$$

$$\frac{dI_{inv\alpha}}{dt} = \frac{1}{L_{inv}}(V_{inv\alpha} - V_{C\alpha})\,, \quad \frac{dI_{C\alpha}}{dt} = (\frac{L_{inv}+L_g}{L_{inv}L_g} - \frac{1}{L_g})V_{inv\alpha} - \frac{L_{inv}+L_g}{L_{inv}L_g}V_{C\alpha} - \omega\psi_{g\beta}\,,$$

$$\frac{dI_{inv\beta}}{dt} = \frac{1}{L_{inv}}(V_{inv\beta} - V_{C\beta})\,, \quad \frac{dI_{C\beta}}{dt} = (\frac{L_{inv}+L_g}{L_{inv}L_g} - \frac{1}{L_g})V_{inv\beta} - \frac{L_{inv}+L_g}{L_{inv}L_g}V_{C\beta} - \omega\psi_{g\alpha}\,,$$

Which in their discrete form can be rewritten as:

$$
\begin{aligned}
\psi_{g\alpha}[k+1] &= \psi_{g\alpha}[k] - T_s\omega\psi_{g\beta}[k] \\
\psi_{g\beta}[k+1] &= \psi_{g\beta}[k] + T_s\omega\psi_{g\alpha}[k] \\
I_{inv\alpha}[k+1] &= I_{inv\alpha}[k] + \frac{T_s}{L_{inv}}(V_{inv\alpha}[k] - V_{C\alpha}[k]) \\
I_{inv\beta}[k+1] &= I_{inv\beta}[k]\frac{T_s}{L_{inv}}(V_{inv\beta}[k] - V_{C\beta}[k]) \\
V_{C\alpha}[k+1] &= V_{C\alpha}[k] + \frac{T_s}{C_f}I_{c\alpha}[k] \\
V_{C\beta}[k+1] &= V_{C\beta}[k] + \frac{T_s}{C_f}I_{c\beta}[k] \\
I_{C\alpha}[k+1] &= I_{C\alpha}[k] + T_s(\frac{L_{inv}+L_g}{L_{inv}L_g} - \frac{1}{L_g})V_{inv\alpha}[k] - T_s\frac{L_{inv}+L_g}{L_{inv}L_g}V_{C\alpha}[k] - T_s\omega\psi_{g\beta}[k] \\
I_{C\beta}[k+1] &= I_{C\beta}[k] + T_s(\frac{L_{inv}+L_g}{L_{inv}L_g} - \frac{1}{L_g})V_{inv\beta}[k] - T_s\frac{L_{inv}+L_g}{L_{inv}L_g}V_{C\beta}[k] - T_s\omega\psi_{g\alpha}[k]
\end{aligned}
$$

With input and output vector u, y same as in MPDPC with simple L filter, state vector x is augmented by the addition of filter capacitor Voltage and Current components:

$$
\begin{aligned}
x &= [\psi_{g\alpha}, \psi_{g\beta}, I_{inv\alpha}, I_{inv\beta}, V_{C\alpha}, V_{C\beta}, I_{C\alpha}, I_{C\beta}] \\
y &= [p, q, U_{mp}] \\
u &= [S_R, S_S, S_T]
\end{aligned}
$$

Voltage sensors for filter capacitors might be omitted, and their voltage can be estimated by capacitor current integration:

$$V_{Cf} = \frac{1}{C_f}\int I_{Cf}dt$$

9.2 Problem Formulation

As described in previous section for MPDPC without LCL output filter, the state space equations are reformed incorporating switch state as input and properly

expressing dc link capacitor midpoint voltage balance. After some term rearrangements the final state space representation is given by:

$$x(k+1) = \left(I + \begin{bmatrix} A & 0 \\ 0 & 0 \end{bmatrix} T_s \right) x(k) + \begin{bmatrix} B_1 \\ 0 \end{bmatrix} T_s u(k) + \begin{bmatrix} 0 \\ B_2(x(k)) \end{bmatrix} T_s |u(k)| \tag{9.1}$$

$$y(k) = g(x(k))$$

where:

$$B_1 = \frac{V_{dc}}{2}\frac{1}{3}\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \frac{2}{L_{inv}} & \frac{-1}{L_{inv}} & \frac{-1}{L_{inv}} \\ 0 & \frac{\sqrt{3}}{L_{inv}} & \frac{-\sqrt{3}}{L_{inv}} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 2\gamma & -\gamma & -\gamma \\ 0 & -\sqrt{3}\delta & \sqrt{3}\delta \end{bmatrix}, \quad B_2(x(k)) = \frac{1}{2C}\frac{1}{3}x^{\intercal}\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ -2 & 1 & 1 \\ 0 & -\sqrt{3} & \sqrt{3} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix},$$

$$A = \begin{bmatrix} 0 & -\omega_s & 0 & 0 & 0 & 0 & 0 & 0 \\ \omega_s & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{inv}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{inv}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_f} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_f} \\ -\omega_s & 0 & 0 & 0 & 0 & -\delta & 0 & 0 \\ 0 & -\omega_s & 0 & 0 & -\delta & 0 & 0 & 0 \end{bmatrix}$$

$$g(x(k)) = \begin{bmatrix} \frac{3}{2}\omega_s(x_1(k)x_4(k) - x_2(k)x_3(k)) \\ \frac{3}{2}\omega_s(x_1(k)x_3(k) + x_2(k)x_4(k)) \\ x_5(k) \end{bmatrix}$$

$$\gamma = \frac{L_{inv} + L_g}{L_{inv}L_g} - \frac{1}{L_g}, \qquad \delta = \frac{L_{inv} + L_g}{L_{inv}L_g}$$

The cost function is structured almost in the same as for MPDPC technique previously presented. The only difference is that with the use of the active damping module, the set of output vector constraints $\mathcal{Y}_l$ of active and reactive

power is now also depending on the horizon-depth of input sequence as it is continuously overridden by the active damping compensator:

$$J^*(U(k), x(k), u(k-1)) = \min_{U(k)} \frac{1}{N_p} \sum_{l=k}^{k+N-1} C_{sw}(x(l), u(l), u(l-1)) \tag{9.2}$$

$$x(l+1) = Ax(l) + Bu(l) \tag{9.3}$$

$$y(l) = g(x(l)) \tag{9.4}$$

$$y(l) \in \mathcal{Y}_l \tag{9.5}$$

$$u(l) \in \mathcal{U}, \quad max|\Delta u(l)| \leq 1 \tag{9.6}$$

$$\forall l = k, ..., k+N-1 \tag{9.7}$$

9.3 Solution Algorithm

With the introduction of active damping, the solution algorithm is slightly altered so as to incorporate the damping signals into the new active and reactive power references. All solution steps remain the same as described in previous section for MPDPC, but now at every time step of present and predicted states a calculation of resonant harmonic power generated by the filter is made, and power references are updated to new values as in equation 9.8 for active power and 9.9 for reactive power.

$$\begin{aligned} P'_{ref_i}[k+n] &= Pref - P_{damp_i}[k+n] \\ P'_{max_i}[k+n] &= P'_{ref_i}[k+n] + P_{bound} \qquad n = 0, 1, ..., N \\ P'_{min_i}[k+n] &= P'_{ref_i}[k+n] - P_{bound} \end{aligned} \tag{9.8}$$

$$\begin{aligned} Q'_{ref_i}[k+n] &= Qref - Q_{damp_i}[k+n] + Q_{comp_i}[k+n] \\ Q'_{max_i}[k+n] &= Q'_{ref_i}[k+n] + Q_{bound} \qquad n = 0, 1, ..., N \\ Q'_{min_i}[k+n] &= Q'_{ref_i}[k+n] - Q_{bound} \end{aligned} \tag{9.9}$$

Since computational effort of the solution algorithm is of great importance, the active damping strategy employed in the DPC solution, is slightly altered in order to avoid *dq* transformations which require many processing resources. The active and reactive compensation power values are calculated as in figure

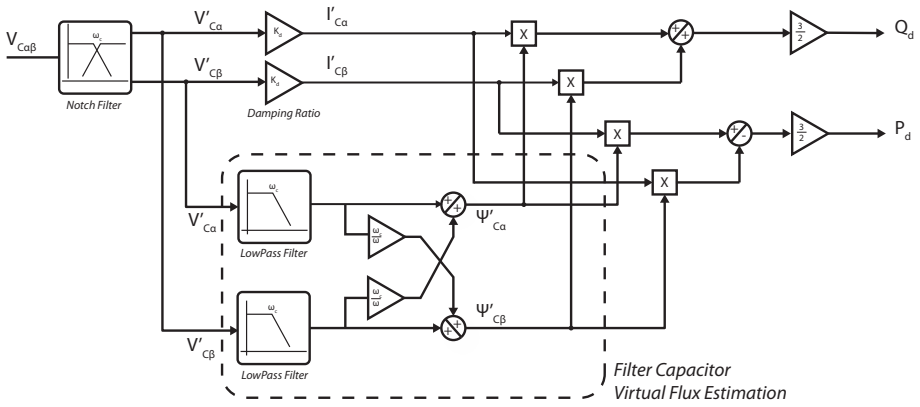


Figure 9.3: Active Damping Power Calculation

9.3. Capacitor virtual flux estimation is performed in the illustrated way only at the present state(timestep k), and for predicted states, it is calculated by:

$$\begin{aligned}\psi_{c\alpha}[k+n] &= \psi_{g\alpha}[k+n] - L_g(I_{inv\alpha}[k+n] - I_{c\alpha}[k+n]) \\ & \qquad\qquad n = 1, ..., N \\ \psi_{c\beta}[k+n] &= \psi_{g\beta}[k+n] - L_g(I_{inv\beta}[k+n] - I_{c\beta}[k+n])\end{aligned} \tag{9.10}$$

$$\begin{aligned}P_{damp} &= \frac{3}{2}\omega(\psi_{c\alpha}I'_{c\beta} - \psi_{c\beta}I'_{c\alpha}) \\ Q_{damp} &= \frac{3}{2}\omega(\psi_{c\alpha}I'_{c\alpha} + \psi_{c\beta}I'_{c\beta})\end{aligned} \tag{9.11}$$

Where:

$$\begin{aligned}I'_{c\alpha} &= V'_{c\alpha} \cdot K_d \\ I'_{c\beta} &= V'_{c\beta} \cdot K_d\end{aligned} \tag{9.12}$$

Also reactive power consumed at filter capacitor Q_{comp} is calculated and properly compensated as in DPC with LCL filter, but since rate of change is

relatively slow compared to the prediction horizon, it is calculated only for the present state and kept the same throughout whole exploration so as:

$$Q_{comp_i}[k+n] = Q_{comp}[k] \qquad n = 1, ..., N$$

$$Q_{comp}[k] = \frac{3}{2}\omega(\psi_{c\alpha}[k]I_{c\alpha}[k] + \psi_{c\beta}[k]I_{c\beta}[k])$$

An overview of the solution algorithm followed for MPDPC with LCL filter and active damping is described in flow diagram in figure 9.4.

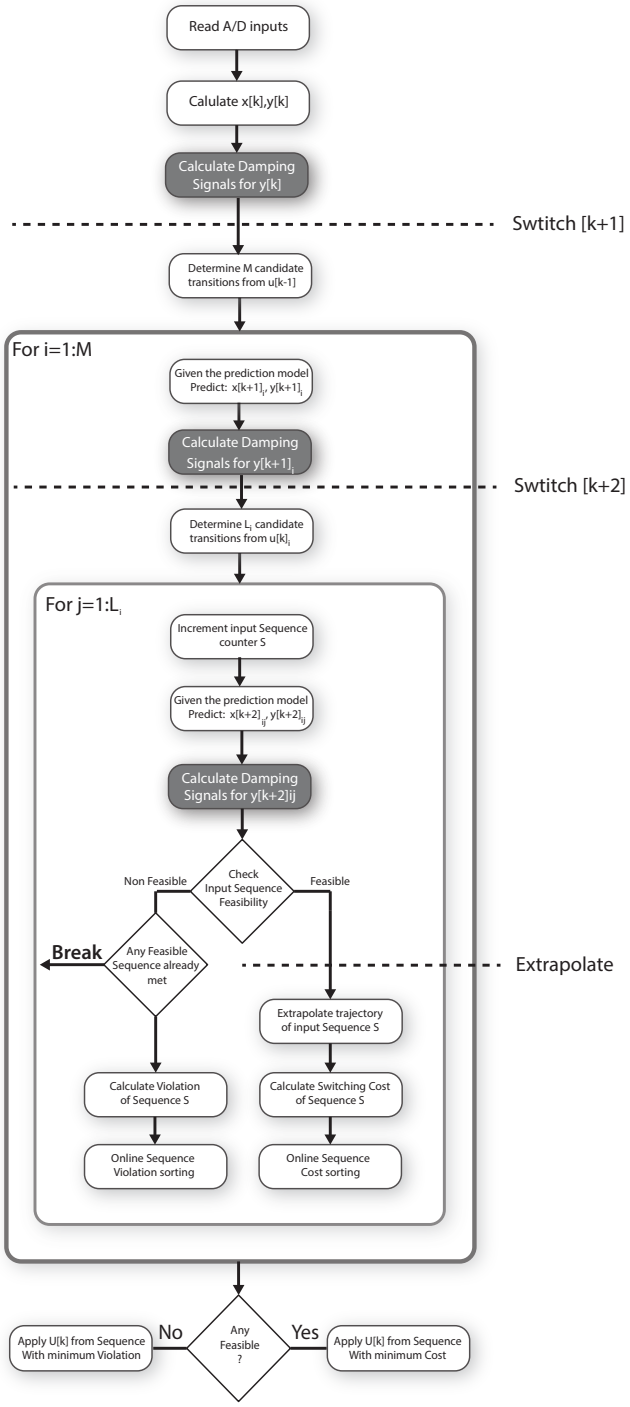


Figure 9.4: MPDPC with LCL Active Damping flow diagram

9.4 Simulation Results

The simulation system used to evaluate MPDPC algorithms with simple L filter is extended in order to interface the NPC converter to the grid through LCL filter. As in the case of the DPC with LCL filter the designed filter has the same total inductance used in simple MPDPC implementation and presents the following charachteristics:

$$L_{inv} = 6.5\,mH$$
$$L_g = 2.0\,mH$$
$$C_f = 47\,uF$$
$$f_{res} = 580\,Hz$$

Since execution time of the control loop is crucial for stability and optimal operation, two versions of the MPDPC with LCL algorithm are tested in simulation environment. In first case, damping signals are calculated for all steps of the solution algorithm thought whole prediction horizon, as described in this section. In the second case, based to the assumption that the prediction horizon is small compared to the rate of change of damping signals, one active damping calculation is made for the present state and is maintained the same for all predicted states, allowing for faster execution control loop. Both cases are evaluated and compared with conventional MPDPC.

9.4.1 MPDPC LCL with active damping throughout whole horizon

In first simulation test a reference step change from 400 to 800 watt is evaluated, while reactive power reference is maintained to zero. In figure 9.5 controlled variables are illustrated, active and reactive power in the converter side, midpoint voltage and power delivered to the grid. Active and Reactive power bounds are not constant since power reference values are continuously overridden by the active damping compensator of the LCL filter. As it can be seen, controlled variables are maintained inside their defined bounds, which are set to be wider than in MPDPC with simple L filter. This is done due to the fact that Power delivered to the grid is much smoother than in simple MPDPC and in order to have comparable results, control bounds are set so as to have equal power ripple in both simulations.

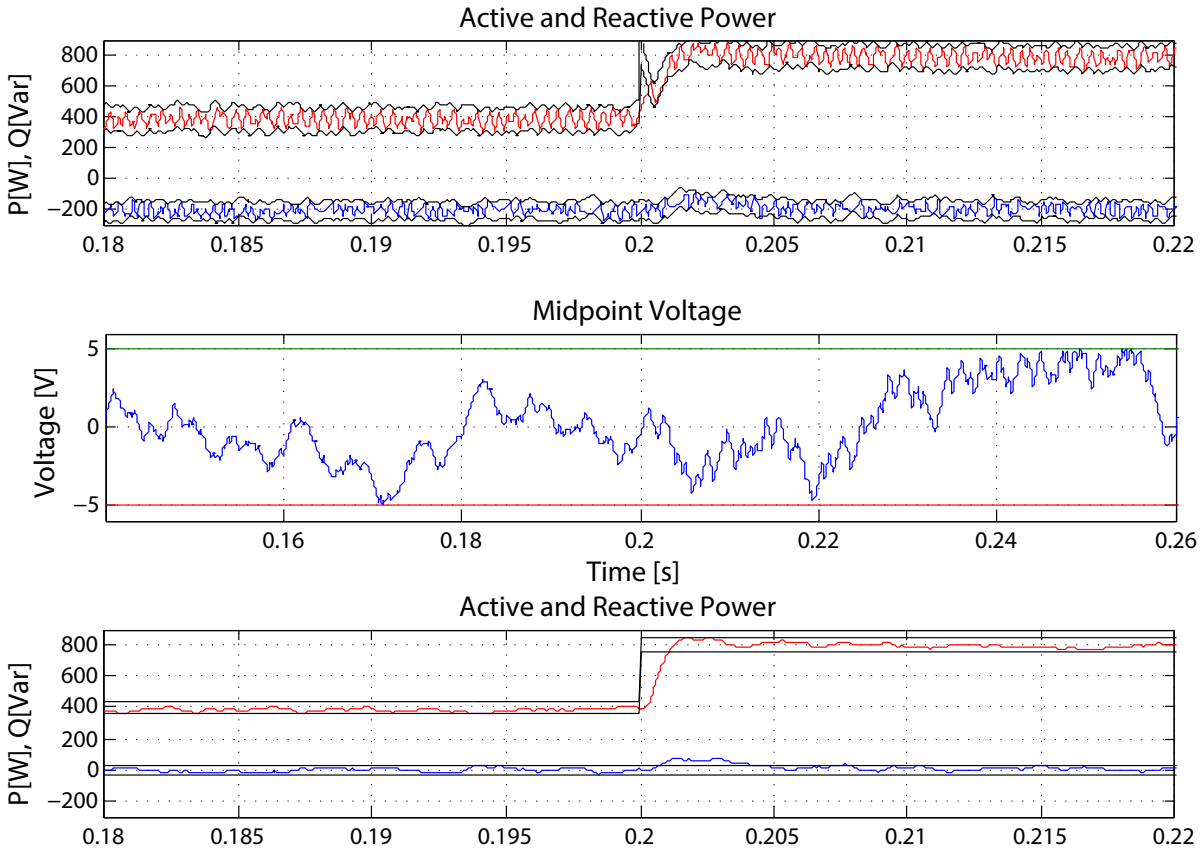


Figure 9.5: MPDPC LCL controlled variables active power step change

In figure 9.6, low switching frequency achieved at the inverter voltage output can be observed, as well as the high quality of grid current waveform. Average switching frequency was measured at $800 - 830\,Hz$ with a THD of grid current of 1.16%. Its clear that MPDPC with LCL filter outperforms simple MPDPC in all aspects utilizing the same total inductance.

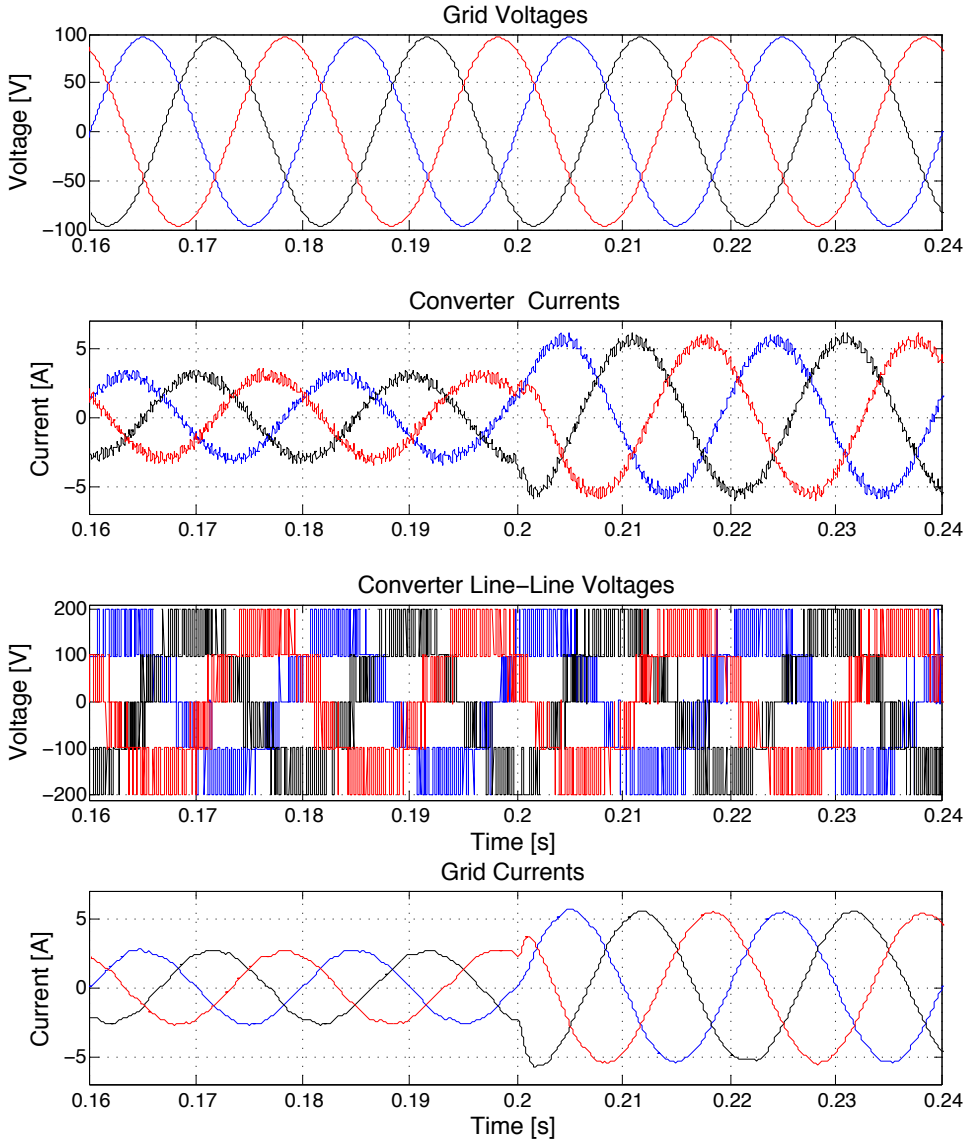


Figure 9.6: MPDPC LCL 3phase measurements - active power step change

In second simulation test of the system, reactive power reference is changed from zero to 600 Var while active power reference is kept constant at 300 $Watt$. Difference in reactive power between converter side and grid side is due to filter capacitor, which is properly compensated.

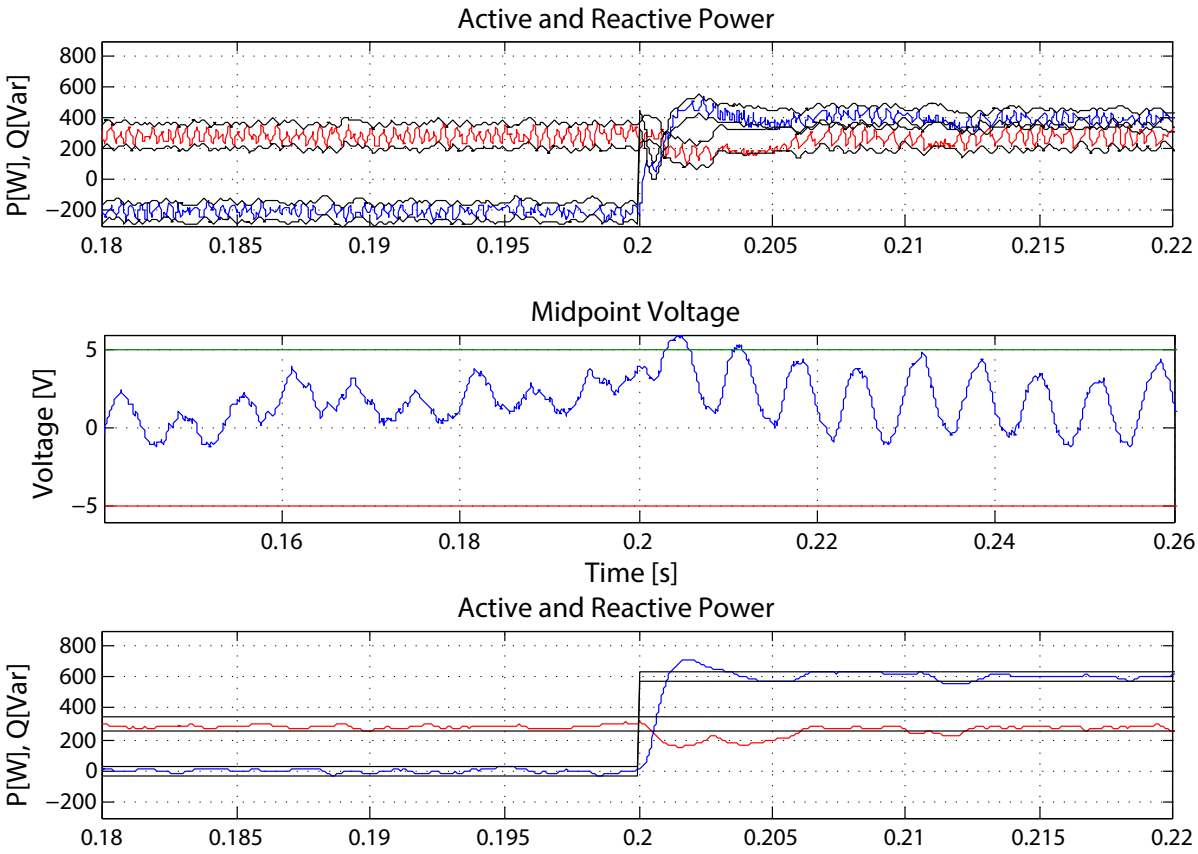


Figure 9.7: MPDPC LCL controlled variables reactive power step change

Observations remain the same for this simulation as well, that the MPC controller achieves to maintain all controlled variables between specified bounds while delivering high quality grid current with low switching frequency, thus lower switching losses.

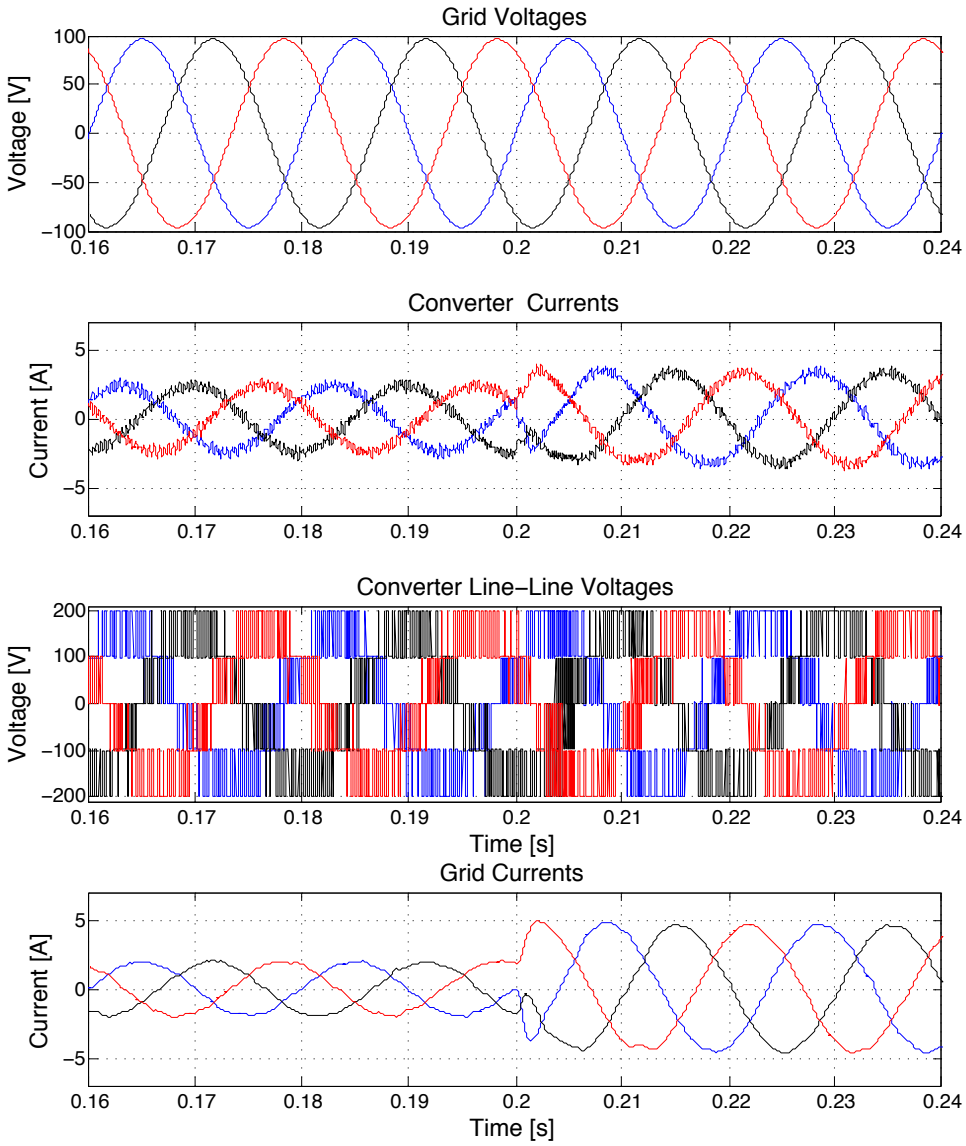


Figure 9.8: MPDPC LCL 3phase measurements - reactive power step change

In figure 9.9 grid current is shown, in a simulation of the system where damping ratio K_d was set from zero to 0.707. As it gets obvious, the system exhibits severe resonance during operation of this simulation, but when active damping control is employed, it effectively manages to eliminate resonant distortion.

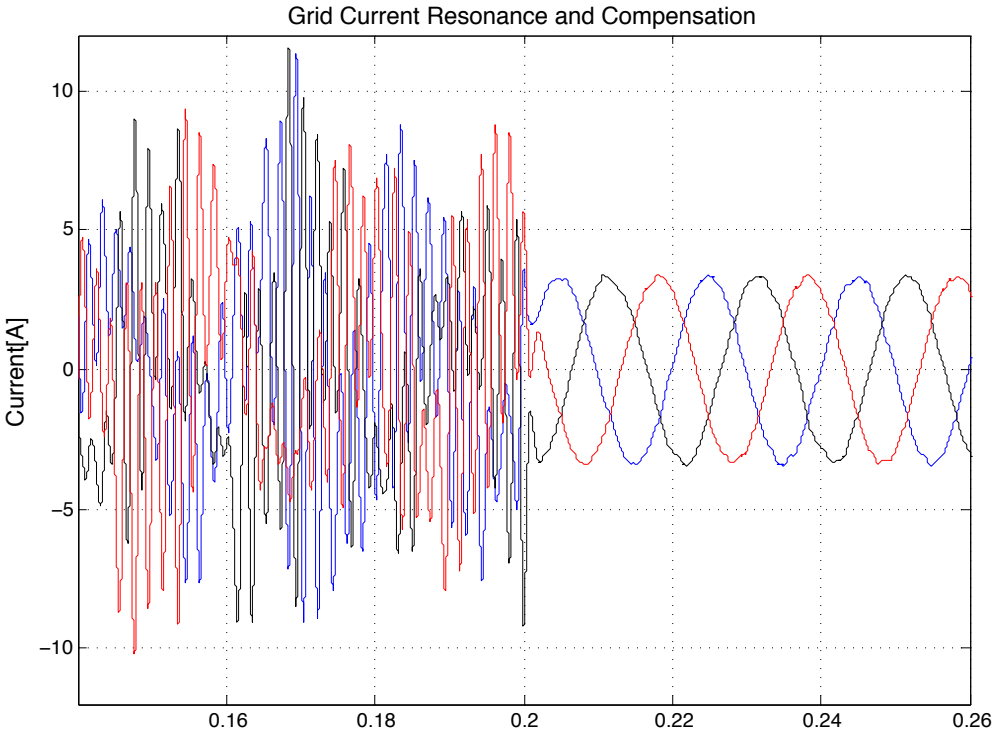


Figure 9.9: filter resonance

9.4.2 MPDPC LCL with active damping to present state only

With the addition of active damping in MPDPC algorithm, an increase in processing resources is needed. Apart from the extra predictions for the augmented state space model that was setup during the problem formulation, damping signals should be calculated for every switching sequence prediction. Such an approach adds significant burden to the online optimizer which grows significantly for larger prediction horizons.

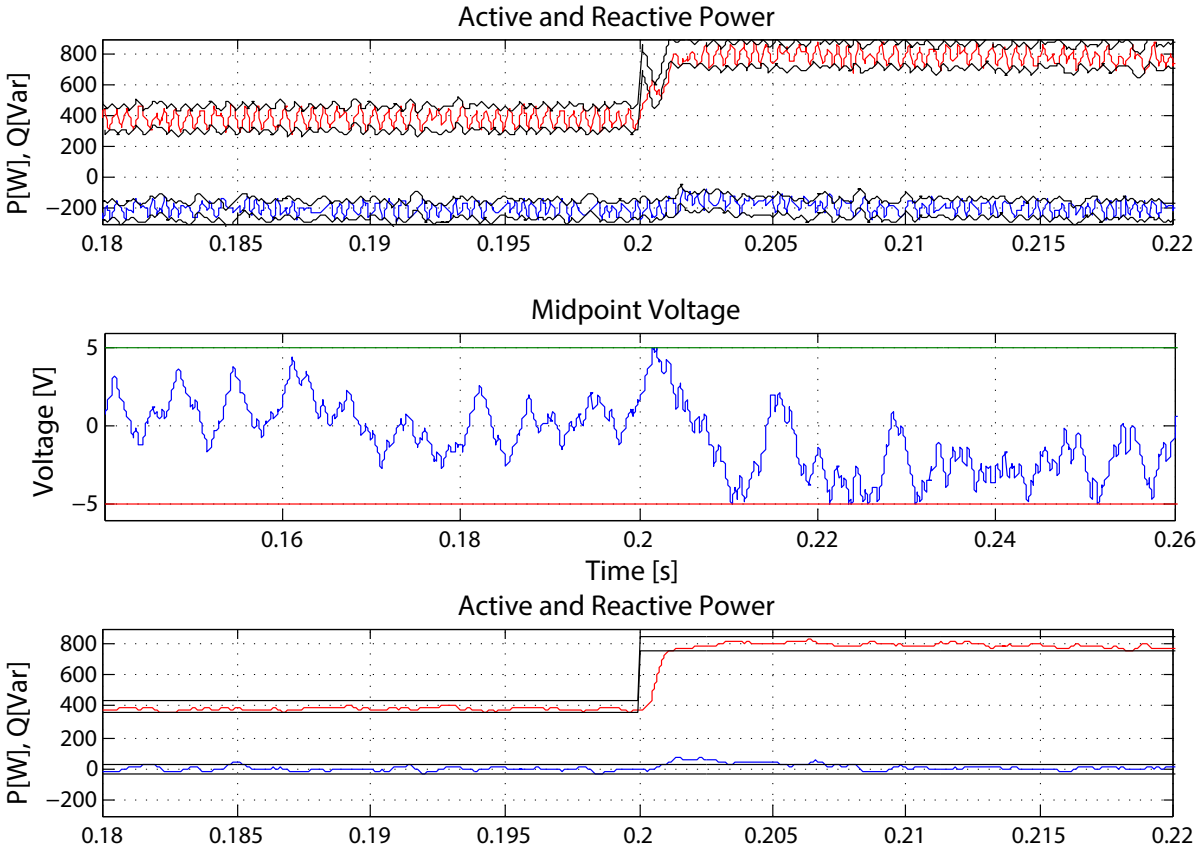


Figure 9.10: MPDPC LCL controlled variables active power step change

In an attempt to make solution algorithm more computationally efficient, and based on the assumption that change in damping signals is evolving slower than prediction horizon , utilized in this thesis, damping signals of LCL filter resonant power components are calculated once for present state, and are kept steady for all predicted candidate sequences. This technique relieves the controller of the greatest added part of the newly introduced solution algorithm, and allows for speed execution performance similar to MPDPC with just an inductor as output filter.

The same system utilized in simulations for MPDPC with LCL active damping throughout whole prediction horizon , is used to evaluate the proposed technique. The same two step reference changes are made and are depicted in the following figures.

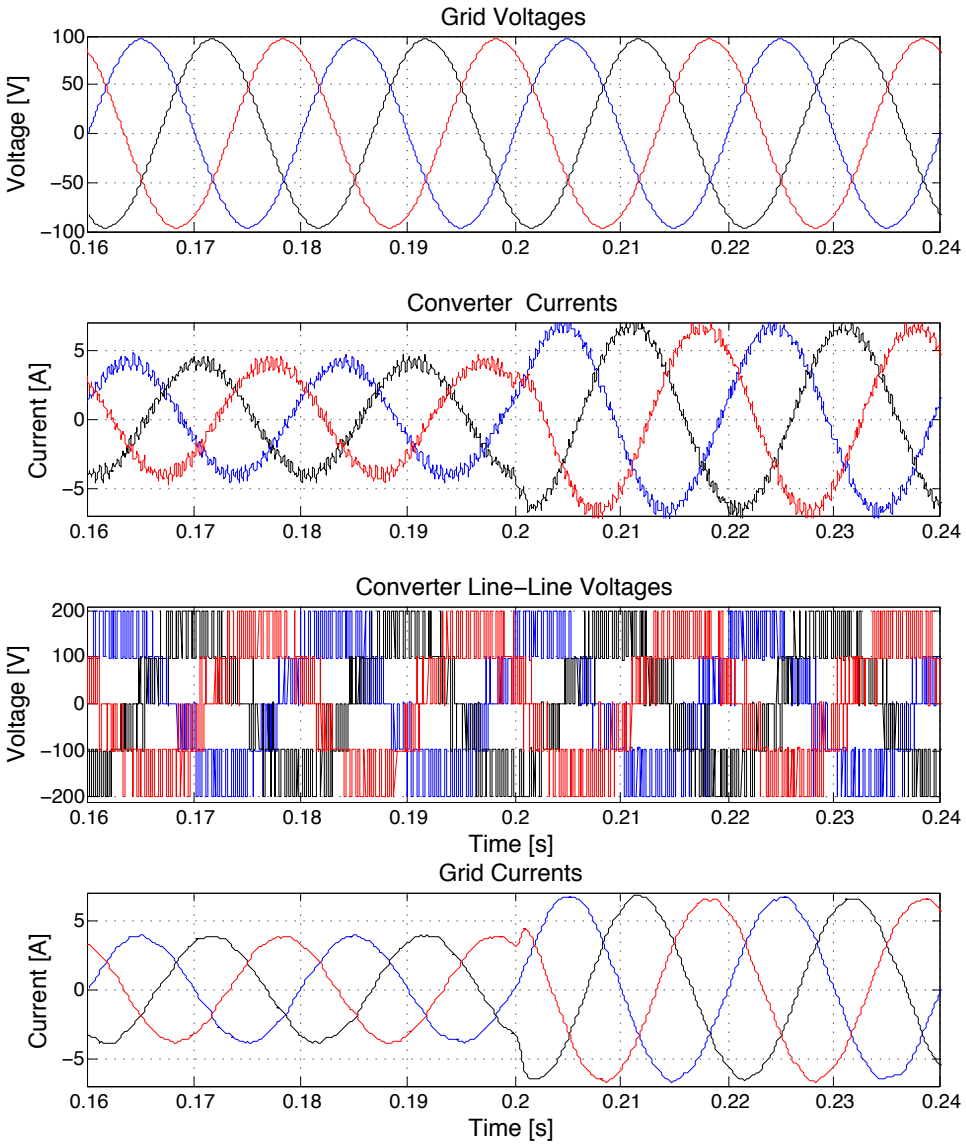


Figure 9.11: MPDPC LCL 3phase measurements - active power step change

As it gets obvious, for the presented simulated system, the proposed technique performs exceptionally, maintaining all controlled variables around specified reference values, with an output grid current presenting THD of 1.1% and a low average switching frequency measured around $790 - 830\,Hz$.

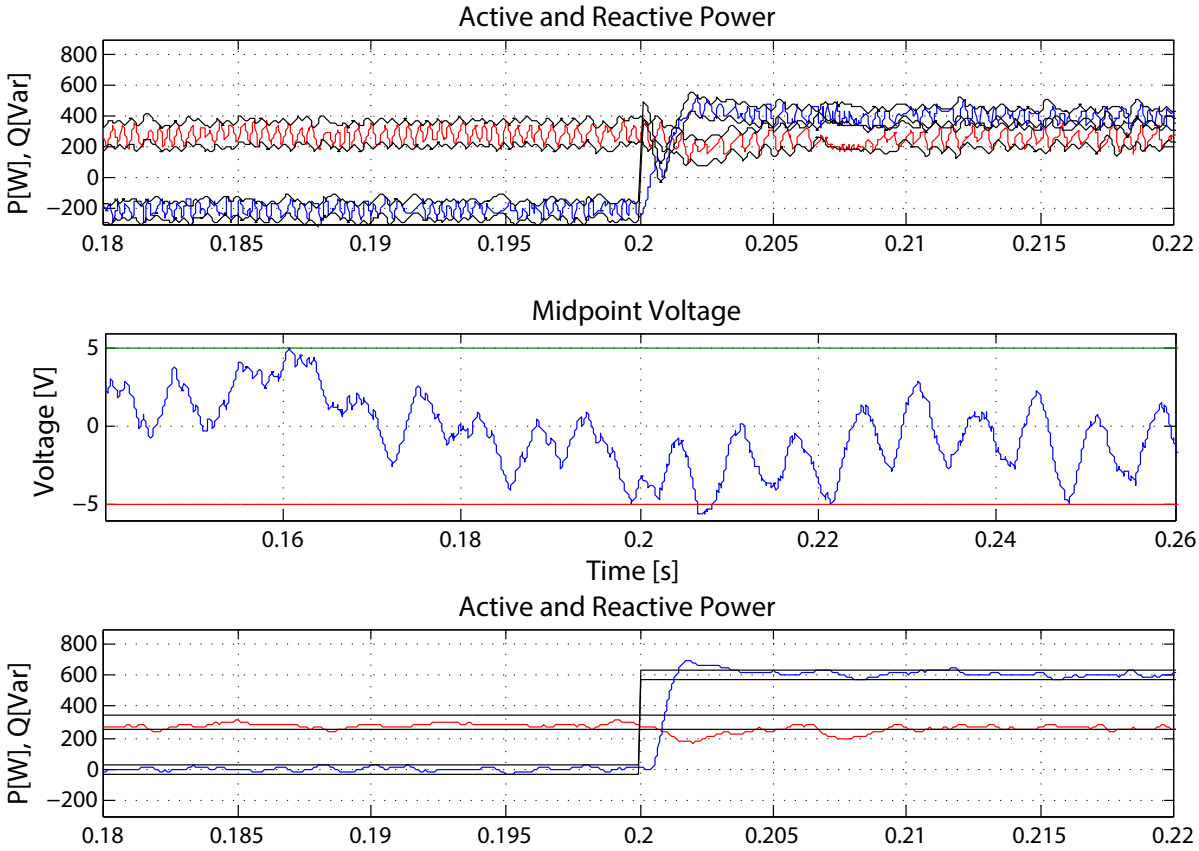


Figure 9.12: MPDPC LCL controlled variables reactive power step change

In general the simplified version of the proposed technique preserves the same performance, in the simulated system for the prediction horizon utilized, as in more complete MPDPC with LCL version where damping signals are calculated for the whole of the prediction horizon. Although by prolonging prediction horizon, or by decreasing total output inductance of the system,thus increasing rate of change in current waveforms, the simplified technique will undoubtedly deviate from the complete MPDPC with LCL solution algorithm. A proposal for this deviation compensation is instead of calculating damping signals for predicted states, calculate future damping signals by means of extrapolating present damping signals based on a computationally efficient analytical approach.

The same performane is maintained during Reactive Power reference step change. Controlled variables are properly driven delivering a smooth power and

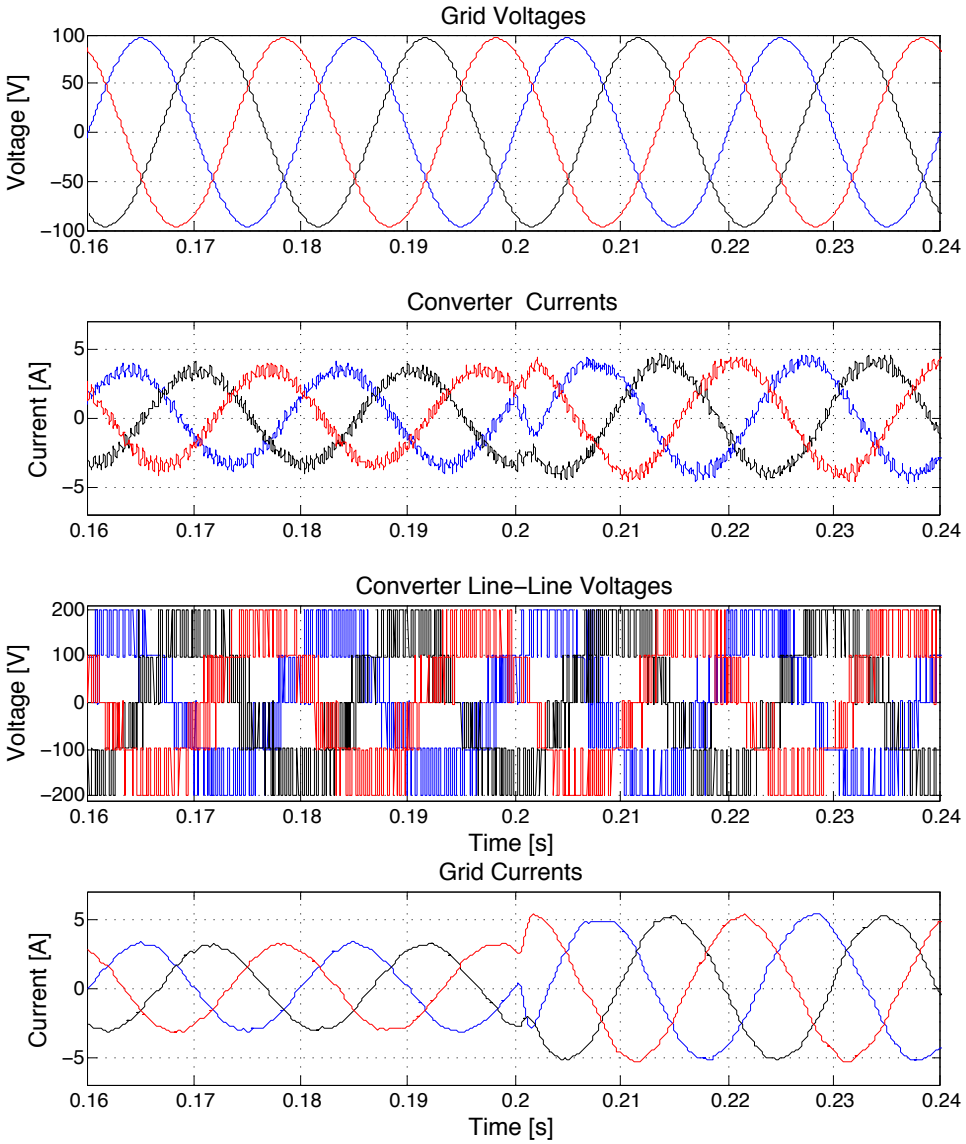


Figure 9.13: MPDPC LCL 3phase measurements - reactive power step change

current output in the grid side.

Resonance present in the simulated system is depicted in figure 9.14 where a simulation is run with a step change in damping ratio K_d from zero to 0.707. Active damping controller manages to compensate for the resonance present due to the LCL filter. As stated in the DPC with LCL filter section if increased low order harmonic distortion appear in the current output it can be selectively compensated by a harmonic controller in the external control loop.

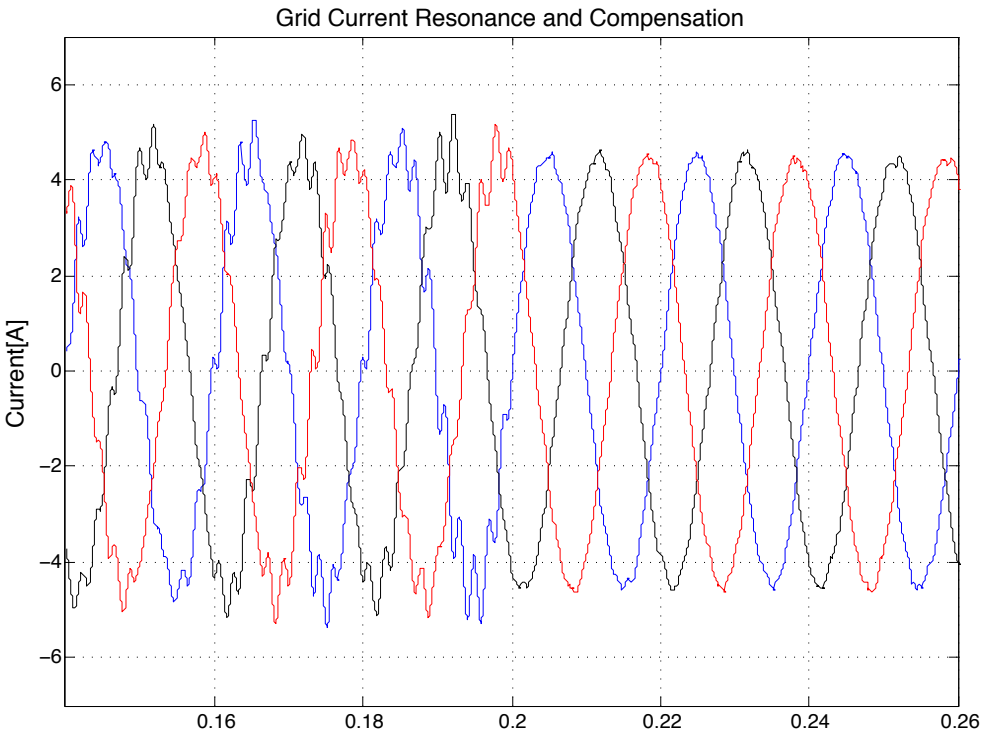


Figure 9.14: filter resonance

CHAPTER
TEN

COMPARATIVE STUDY RESULTS

In order to have a more broad overview of each control technique studied in previous chapters, their steady state performance is tested in a range of operating points, from 0 to 1KW of active power and from 0 to 1KVAr of reactive power references. The set of measurements made is presented in table 10.1 illustrating average characteristics of studied control schemes. An example of automating simulations through matlab scripting and the mex environment is given in the appendix. Average switching frequency reflects expected switching losses while average current Total Harmonic Distortion illustrates performance of employed control.

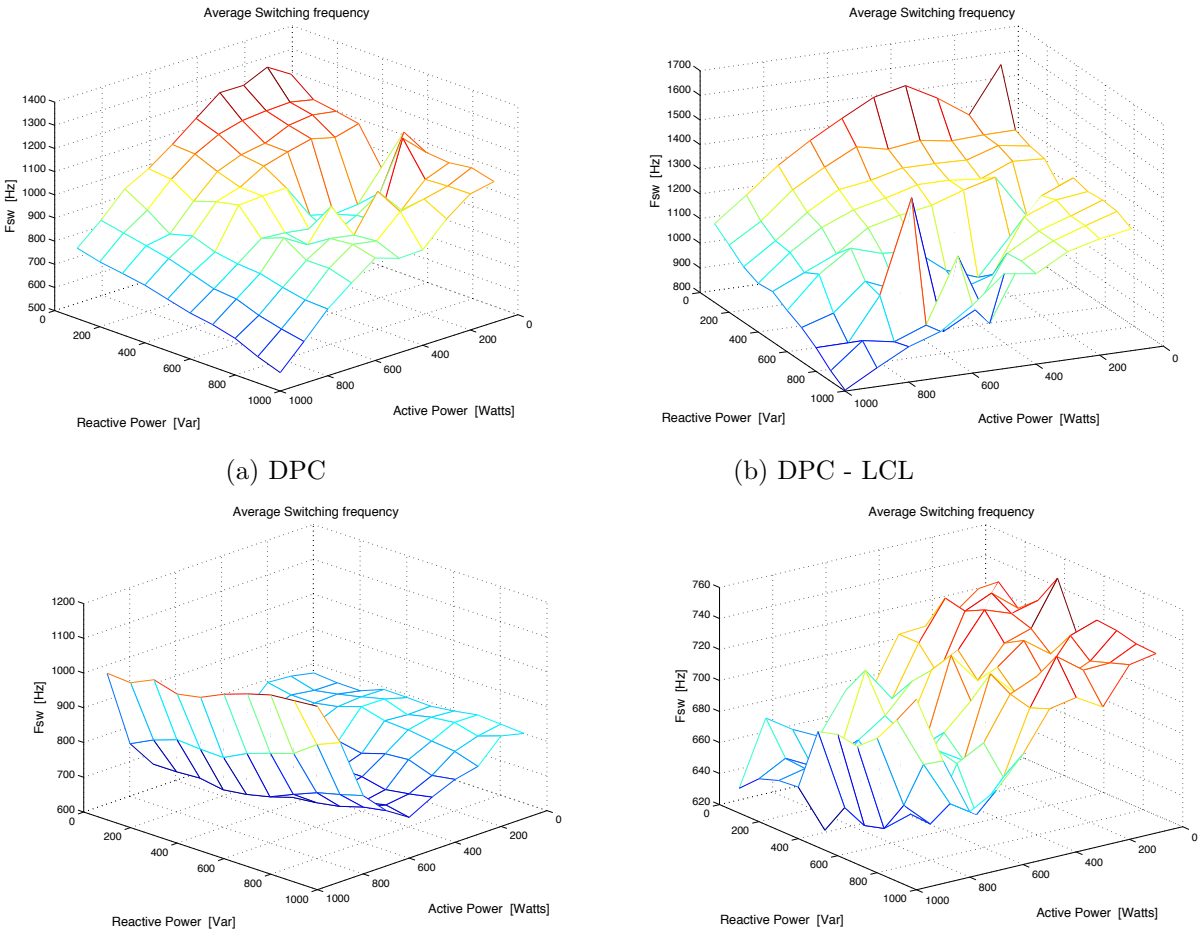
Control Scheme	Average Switching Frequency	Maximum Switching Frequency	Minimum Switching Frequency	Output Current Distortion
	$f_{sw}av$ [Hz]	$f_{sw}max$ [Hz]	$f_{sw}min$ [Hz]	T.H.D [%]
DPC	970	1006	931	2.24
DPC-LCL	1194	1234	1137	1.39
MPDPC	819	866	804	1.08
MPDPC-LCL	694	739	681	1.12

Control Scheme	Active Power Ripple Bounds	Reactive Power Ripple - Bounds	Midpoint Voltage Ripple	Filter Charachteristics		
	Δp [p.u]	Δq [p.u]	ΔU_{mp} [p.u]	L_{inv} [mH]	L_g [mH]	C_f [μF]
DPC	0.08	0.12	0.10	8.5	-	-
DPC-LCL	0.04	0.06	0.10	6.5	2.0	47
MPDPC	0.08	0.08	0.10	8.5	-	-
MPDPC-LCL	0.06	0.08	0.10	6.5	2.0	47

Table 10.1: Overall characteristics of evaluated control schemes.

Average switching frequency and total harmonic distortion data of studied control schemes are illustrated in figures 10.1 , 10.2 respectively. Analysis over various operating point provides more insight over each control strategy. In all

tests active and reactive power bounds were equally set, thus the sub-optimal operation in low power region. As a word of caution, both MPDPC strategies yielded better results in continuous time simulations, but in order to collect sufficient data for the study presented, discrete time simulations with slightly larger timestep have been adopted than the results presented in specific MPDPC chapters. Even so, both MPDPC techniques outperform their DPC counterparts.



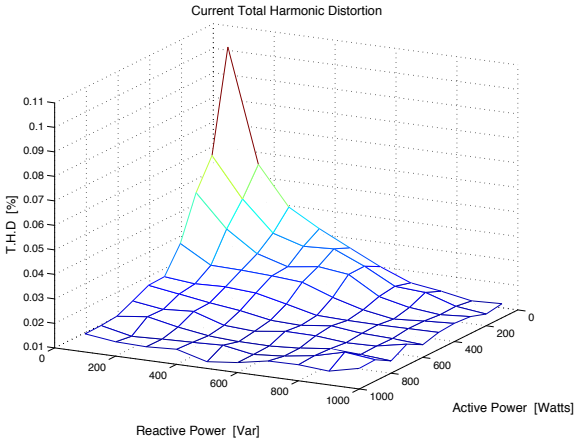
(a) DPC

(b) DPC - LCL

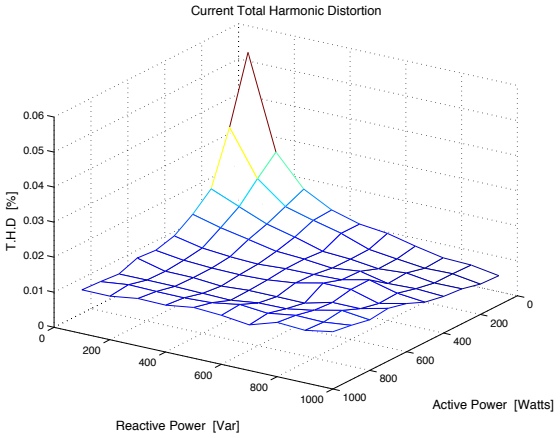
(c) MPDPC

(d) MPDPC - LCL

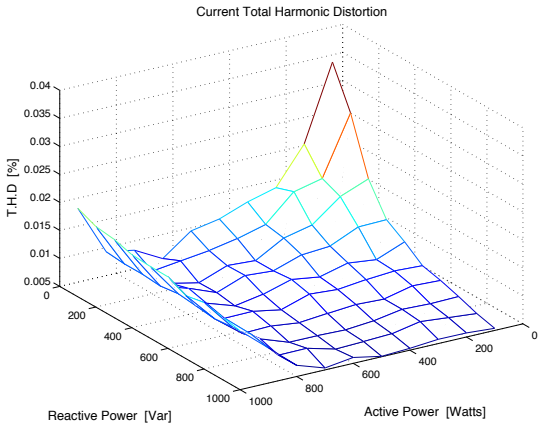
Figure 10.1: Average Switching frequency



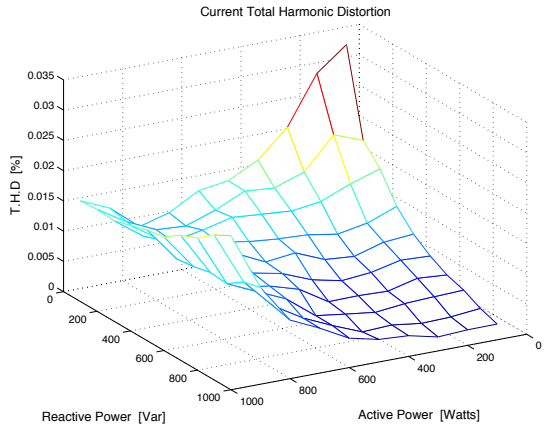
(a) DPC



(b) DPC - LCL



(c) MPDPC



(d) MPDPC - LCL

Figure 10.2: Total Harmonic Distortion

CHAPTER
ELEVEN

CONCLUSIONS AND FUTURE WORK

In this thesis several grid connected control systems were presented and studied focusing on predictive controller applications. Starting with Direct Power Control of a 3 level NPC converter setup interfaced to the grid with simple first order filter, and by expanding this system first to connection through third order LCL filter to the grid, and then by adapting the same setup to an MPDPC control scheme for both grid connection scenarios. All four systems were analysed and submitted to same tests in simulation environment, and proof of concept hardware has been developed. The case of MPDPC with LCL filter is a novel technique presented in this thesis, but for the rest cases several work has been developed.

11.1 Conclusions

For the Direct Power Control technique, an analytical way of constructing the Switching Look up table has been developed based on Virtual Flux quantities, and taking into account switching losses cost and NPC converter dynamics as in a pseudo explicit MPC scheme would be done. In order to keep switching losses at minimum, hysteresis controllers used in the simplest DPC form have been firstly adopted, but since spikes present in controlled reactive power have been observed, which is the case of simple DPC approach, a new 3 level hysteresis controller has been developed which successfully managed to stress out controlled reactive power spikes, with minor switching frequency augmentation.

By studying the DPC-LCL expansion, the idea of adding external cascaded control loops in an existing control scheme was understood and practised both in simulation and hardware. Also design of LCL output filters was analysed and a script for automatically generating real filter component values once design parameters set, has been developed. Also the concept of utilizing LCL filters in non constant switching frequency control scheme was confronted while concept and practice of active damping has been well studied.

After setting up the straightforward and well defined DPC technique, it was easier to start exploring the more complex MOdel-based Predictive Control approach. The MPDPC for grid connected NPC converter is thoroughly described, and through studying it, it gave a practitioners approach to Model Predictive Control, making clear the challenges and tradeoffs of such a complex and high end control topic. In literature, there is a lot of exceptional work, worth to be studied, but main obstacle met in hardware development was computational efficiency of existing algorithms given today's average computational resources. MPDPC is obviously favouring a parallel approach implementation, but a serial algorithm was examined adopting core concepts of the boombox platform. Of course boombox utilizes a competent FPGA able to implement peripherals for the DSP processor, but design of a parallel MPC peripheral specifically for the boombox was totally out of the thesis scope. In order to simplify the MPDPC algorithm, two new approaches have been suggested exploiting the nature of NPC converters and based on observations during simulations. More specifically the technique of controlling midpoint voltage balance of the NPC in an external control loop, not only simplifies optimization process from three to two variables but also reduces maximum possible states to be explored in the overall optimization process. The idea of coupling the controlled variables in one complex variable further reducing optimization process cost and allowing for positive integer optimization , while proved to be working, presents serious drawbacks, mainly the direct coupling of active and reactive output power which disallows for the fast response met in all previous control techniques. Moreover such a tricky implementation should also be further tested for stability issues.

With the introduction of MPDPC with LCL filter, knowledge structured in all previously studied control systems was combined in a new extension of existing MPDPC technique. By properly rearranging the model of new grid connection method and properly expressing the solution algorithm and cost function, the new MPC problem was fully described. The active damping control loop utilized in DPC with LCL filter was restructured in order to be computationally efficient, and properly incorporated into the MPC solution algorithm, illustrating a path of using extra control loops in existing MPC solutions. The final design is characterized by exceptional features, in terms of stability, fast response and robustness, while outperforming all other control techniques tested in this thesis in terms of switching losses and Total Harmonic Distortion of the output current. Also since the addition of active damping control loop adds sufficient computational burden to the already demanding MPDPC control scheme, a simpler heuristic approach was proposed and successfully tested, adding the smallest possible computational effort by employing the active damping section only to present state calculations and simplifying LCL filter transfer characteristics.

Concluding, each control scheme tested in this thesis presents features and drawbacks, which make selection largely dependent on intended application.

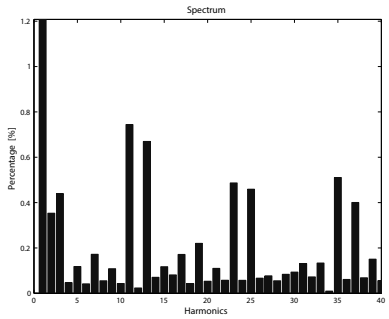
Since more than one proposal for grid connection topologies are made, application specific selection should investigate mainly two aspects. First if a Predictive controller can be employed given added hardware complexity and overall system reliability and second whether LCL filters can be utilized in the specific application. Proposed MPDPC with LCL filter yields top performance results for high power-high voltage grid connected applications, but utilization of such a complex and computationally demanding technique should justify use of LCL filters and cost of hardware development. While active damping is proved to efficiently compensate for higher order filters resonant characteristics, added complexity to a subsystem, may lead to hard to identify problems in larger systems such as power distribution networks. On the other hand, conventional DPC while outperformed by model predictive control solutions, is a proved in time control technique, easy to implement in most present hardware, with added reliability and less overall system complexity.

11.2 Future Work

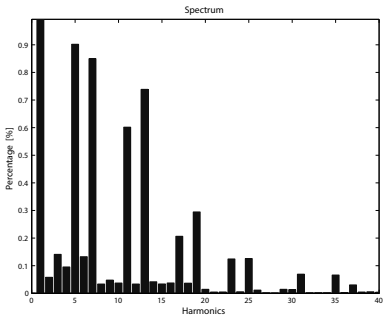
This work has studied and fully described several grid connection control methods for an NPC converter, and successfully proposed a new method to actively damp harmonics generated by utilization of LCL filters . Based on the results of aforementioned study, several investigation to be carried on addressed topics occur.

Of great interest would be to transpose described algorithms to different multilevel topologies and asses a comparative study. Also it would be preferable to perform all evaluations carried during this work, with real converter power losses as a benchmark. This would allow for a more clear overview of suggested techniques benefits.

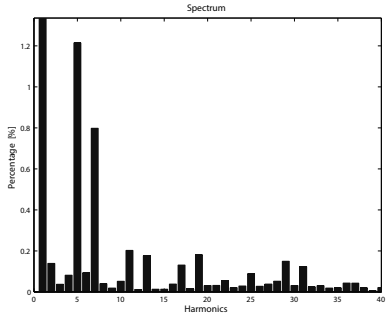
Since adoption of external control loops used in DPC, to existing MPC algorithms , proved to work, addition of a selective harmonic elimination control loop would probably prove beneficial for both MPDPC and MPDPC with LCL filter techniques. In fiqure 11.1 a frequency spectrum of current harmonics amplitude of four main techniques described is presented.



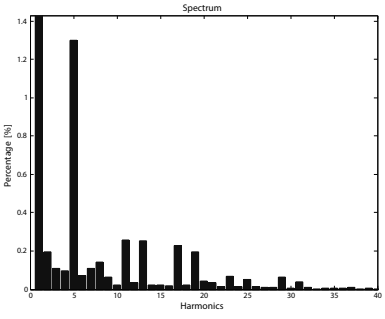
(a) DPC



(b) DPC - LCL



(c) MPDPC



(d) MPDPC - LCL

Figure 11.1: Current spectrum for 1KW Active Power reference and 1KVA Reactive Power reference

As it gets clear both MPDPC techniques present an augmented 5th har-

monic, which even if is the outcome of internal optimization, it might need to be properly controlled for specific applications.

Another point to consider is performance of more sophisticated explicit MPC control solutions than conventional DPC. MPDPC stems from MPDTC, but motor applications have a much broader speed range compared to the steady frequency of grid connected systems, thus an online optimization stage might be avoided by use of pre-calculated solutions over an expected range of operation.

Furthermore, a more analytical stability analysis both in theory and practice for the proposed Heuristic MPDPC algorithm variations would allow for a proven robust and computationally efficient MPDPC solution development. Moreover in area of computational efficiency, a parallel architecture implementation, modular enough to be adopted in several applications would drastically boost MPC hardware development. Such a feature in the form of an external module would naturally pair with native modular architecture of BoomBox platform.

Part III

Hardware Setup

CHAPTER
TWELVE

EXPERIMENTAL SETUP DESCRIPTION

In this chapter an overview of the hardware setup used for the experimental part is presented. All control routines have been realized utilizing BoomBox, a powerful modular control platform developed in LEI for power electronic experiments [39]. The Neutral Point Clamped converter utilized in the experimental part already existed in the LEI laboratory and an Interface card has been designed in order to make the NPC directly compatible to the BoomBox platform. First some basic information over BoomBox are presented, next information over the NPC and Interface card are presented and finally an overview of the whole setup is given.

12.1 BoomBox platform

Boombox,figure 12.1, is the new modular control platform for power electronic experiments developed in Laboratory of Industrial Electronics (LEI). A powerful processing unit is developed by utilizing a DSP(TMS320C28346) for main control routines and an FPGA(Actel ProAsic A3P1000) for low level custom peripherals implementation. Modular nature of Boombox is expressed by the fact that it can accept a number of custom daughterboards, which communicate with the central monolithic DSP-FPGA unit. Daughterboards might perform i/o tasks of specific nature, specified by the designer. Existing daughterboards include MultiA, which is a basic i/o unit with 6 shielded inputs with auxiliary power supply ready to use with LEM current and voltage sensors, and is also equipped with 8 outputs either optical, or electrical, ready to drive various semiconductor switches(MOSfet,IGBT etc). Output gates come in complementary pairs, as a part of the pwm modulator peripheral implemented on the FPGA, so as to be ready to use in complementary switching applications like normal H-bridges.

Apart from main control and basic i/o operations, there are plenty of features incorporated in BoomBox such as safety and data-logging mechanisms,

serial communication and programming interface. Moreover, on the firmware side a set of power electronics specific peripherals is developed such as various filters, coordinate transformations, pll etc. which are provided to the user in a library like interface. All these features combined together with developer's software framework accommodate for a complete, integrated control development solution.

Figure 12.1: BoomBox platform [39]

MultiA i/o Daughterboard card provides an extra front-end analogue interface for measurements manipulation. In the input section, a Programmable Gain Amplifier, Low Pass Filter and safety mechanism with high and low limits are set by the user through the multiA hardware controls, and are not controlled by the main control routine.

Working with BoomBox has been a great experience, and despite it was still in debugging stage, it proved a powerful tool, capable to implement most demanding tasks, in a user friendly manner.

12.2 NPC and Interface Card

Neutral Point Clamped converter utilized in the experimental part of the thesis already existed in Industrial Electronics Laboratory, and is a 4U rack mounted unit, consisting of Semikron SKH71 IGBT drivers, 30A 600V Semikron IGBT Modules and LEM current and Voltage sensors. NPC card also integrates a 3 phase bridge rectifier, but was not used in this part. Arrangement of the Semikron Modules is illustrated in figure 12.2

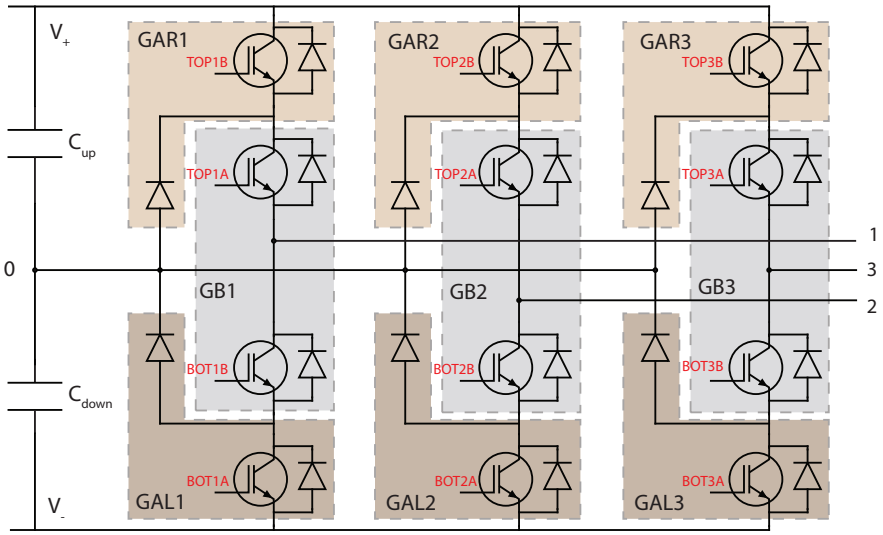


Figure 12.2: NPC Semikron IGBT arrangement

Semikron SKH71 IGBT drivers incorporate external control of deadtime between complementary outputs and fault detection mechanisms. If an error occurs, all driver outputs are deactivated, and this is managed by internal logic of Semikron drivers.

A digital front end, multiplexing input drive and enable signals, is implemented with logic gates, for each phase, as shown in figure 12.3. By using this multiplexing technique, only two signals ,*Ap-Am*, are needed for determining switching state of an NPC phase leg, and an extra signal for turning on and off the converter as well, *En*.

Since no schematic or pcb design files can be enclosed in this thesis, since NPC design is not author's work, a figure with most important debugging points of the pcb that proved useful when working with the NPC converter is illustrated in 12.4.

An interface card was designed in order to harness benefits of BoomBox i/o system, namely shielded Input cables and optical output drives, and make use of NPC converters easy to work with the BoomBox platform. Two sides of the

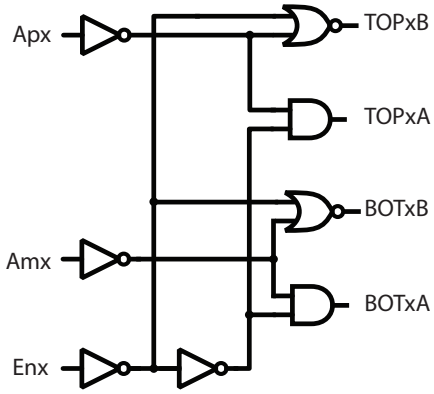


Figure 12.3: Logic Multiplexing of input and error signals

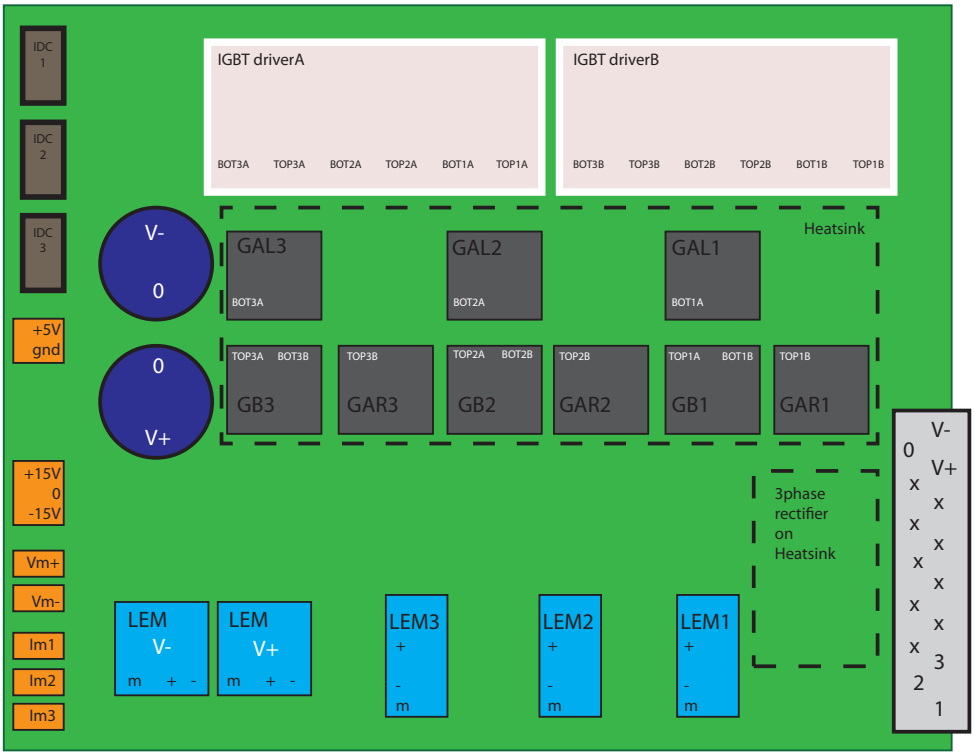


Figure 12.4: NPC pcb sketch with important debugging points

pcb are illustrated in figure 12.5, a model of the Interface card is illustrated in figure 12.6 and it snaps on and integrates with the NPC card is illustrated in figure 12.7

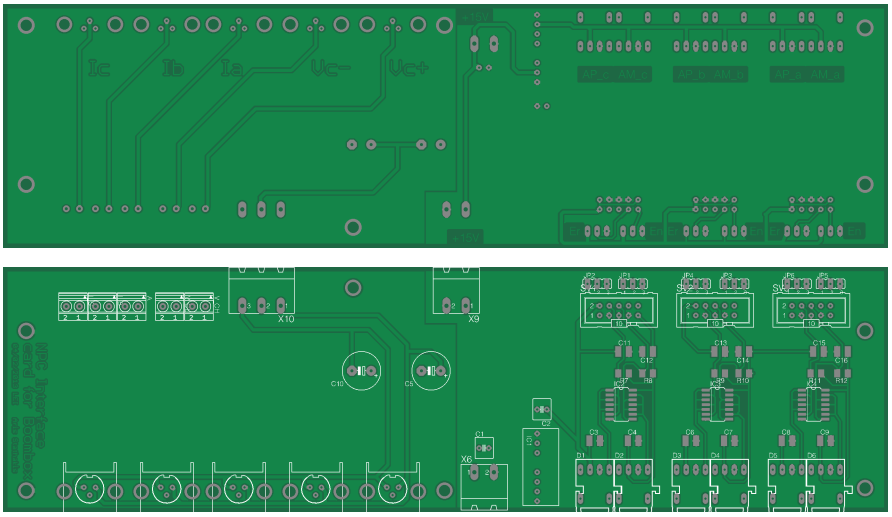


Figure 12.5: Top and Bottom Interface Card pcb

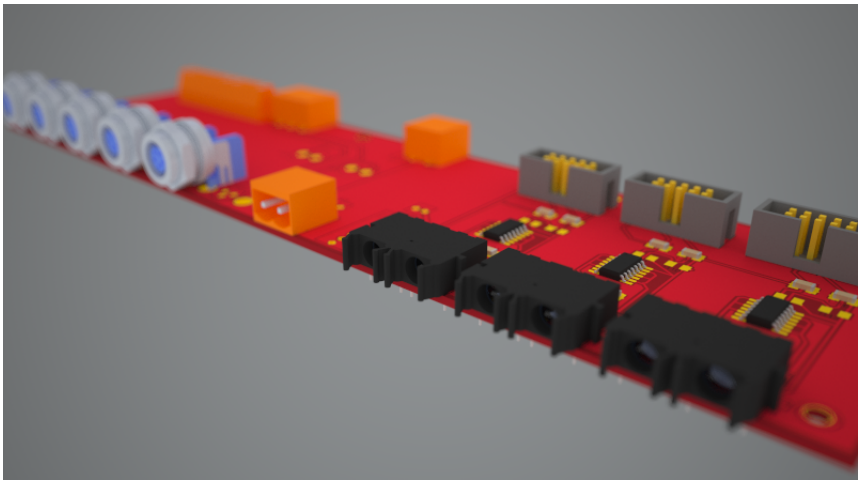


Figure 12.6: Interface Card 3d model

Also, for this thesis, where no modulator is used, a custom peripheral was implemented for BoomBox, which allows direct access to the FPGA registers from the main control routine, bypassing default modulator routing. In this way more processing power is available to the user program, and all outputs of a multiA board can be utilized in a non complementary way. This last feature is made possible due to the fact that integrated drivers on the NPC board ac-

commodate for deadtime protection. Moreover, as an extra safety mechanism, in any erroneous state, the enable signal is programmed to turn low, avoiding short circuits in the setup.

Figure 12.7: BBox ready - NPC with Interface Card installed model

Once the Interface card is connected to the NPC, connection with BoombBox is straightforward, since markings with signal names are printed on the pcb at connection points.

A matlab script is available at the appendix, where switching vectors of the converter are translated to an unsigned integer value corresponding to the FPGA output register. For the switching state nomenclature utilized in this setup, the following table is followed

FPGA output register:	bit 7	bit 6	bit 5	bit 4	bit 3	bit2	bit 1	bit 0
NPC logic gate signal:	x	Ap_A	Am_A	Ap_B	Am_B	Ap_C	Am_C	En

Table 12.1: FPGA register and NPC logic relation

NPC Switching Vector	FPGA register value
0	43
1	105
2	41
3	123
4	121
5	57
6	59
7	9
8	25
9	27
10	11
11	63
12	31
13	15
14	47
15	3
16	7
17	39
18	35
19	111
20	103
21	99
22	107
23	33
24	97
25	1
26	127

Table 12.2: FPGA register and NPC switching vector relation

12.3 Overview

An overview of the total hardware setup used to perform the experimental part of this thesis is given in figure 12.8

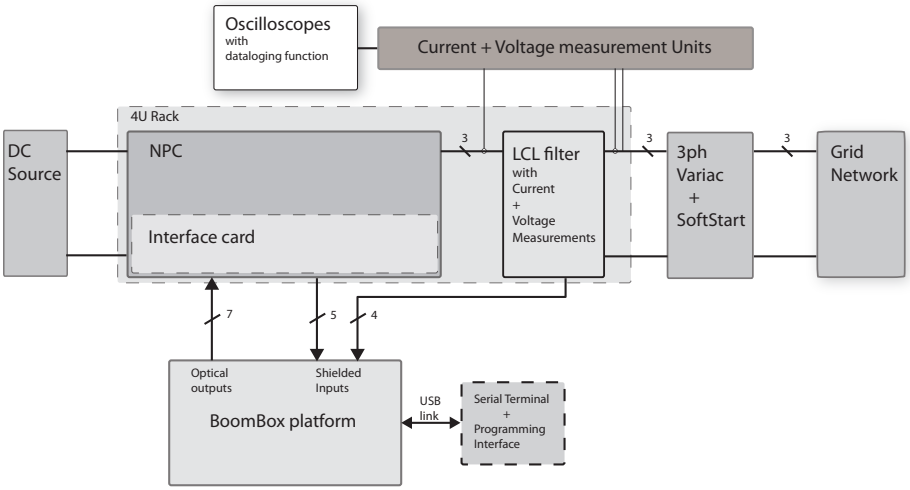


Figure 12.8: Block diagram of experimental setup

And a photographic illustration is given in picture 12.9

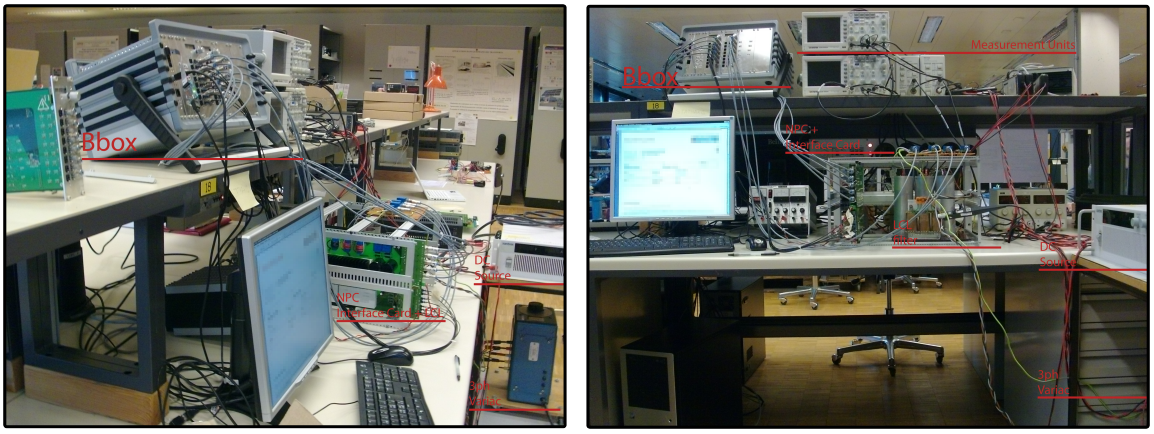


Figure 12.9: Photo of the Hardware setup

Part IV

Appendix

APPENDIX

A

MATLAB SCRIPTS

LCL filter design script

```
breaklines
clc
clear all

% This file designs a passive lcl filter given  quality requirements
% filter calculations are done as described in the following papers:

%[1]LCL Filter design for grid-connected NPC
%inverters in offshore wind turbines
%[2]Design and Control of an LCL-Filter-Based
%Three-Phase Active Rectifier
%[3]Output Filter Design for a
%Grid-interconnected Three-phase Inverter

%First define the power system characteristics

Vn=90;          %grid line voltage
Vph=Vn/sqrt(3); %grid phase voltage
Vdc=200;         %Dc link voltage
Pn=1000;        %nominal power
Fn=50;           %nominal frequency in hertz
Wn=2*pi*Fn;
Fsw=1200 ;       %expected switching frequency
Wsw=2*pi*Fsw;

%Then input the required quality characteristics

IinvRipple=0.2;  %percentage of current ripple in the converter side
Cpercentage=0.2; %percentage of reactive power in filter capacitor
Fres=578;         %desirable LCL filter resonance frequency in hertz
Fres=678;
Wres=2*pi*Fres;


%This is an array with the availiable capacitor values so as our
%design consists of real capacitor values


```

```
Capacitor=[0.000000001 , 0.00000001 , 0.0000001 , 0.000001 ...
          ,0.00000001 , 0.0000001 ,0.000001 , 0.00001 ...
          ,0.0001 , 0.001,0.0000000011 , 0.000000011 ...
          ,0.00000011 ,0.0000011 ,0.0000000012,0.000000012 ...
          ,0.00000012 , 0.0000012,0.0000000013,0.000000013 ...
          ,0.00000013 , 0.0000013,0.0000000015,0.000000015 ...
          ,0.00000015 ,0.0000015 ,0.000000015 , 0.00000015 ...
          ,0.0000015 ,0.000015,0.00015,0.0015,0.0000000016 ...
          ,0.000000016 ,0.00000016 ,0.0000016,0.0000000018 ...
          ,0.000000018 ,0.00000018 , 0.0000018,0.000000002 ...
          ,0.00000002 , 0.0000002 , 0.000002 ,0.0000000022 ...
          ,0.000000022 , 0.00000022 ,0.0000022,0.000000022 ...
          ,0.00000022,0.0000022 ,0.000022 ,0.00022 ,0.0022 ...
          ,0.0000000024 , 0.000000024,0.00000024,0.0000024 ...
          ,0.0000000027 , 0.000000027,0.00000027,0.0000027 ...
          ,0.000000003 , 0.00000003 , 0.0000003 , 0.000003 ...
          ,0.0000000033 , 0.000000033 , 0.00000033  ...
          ,0.0000033,0.000000033 ,  0.00000033 , 0.0000033 ...
          ,0.000033,0.00033,0.0033,0.0000000036,0.000000036...
          ,0.00000036 ,0.0000036,0.0000000039 ,0.000000039 ...
          ,0.00000039,0.0000039,0.0000000043 , 0.000000043 ...
          ,0.00000043,0.0000043,0.0000000047 , 0.000000047 ...
          ,0.00000047 , 0.0000047 ,0.000000047 ,0.00000047 ...
          ,0.0000047,0.000047 , 0.00047 , 0.0047 ...
          ,0.0000000051 , 0.000000051,0.00000051 ...
          ,0.0000051 , 0.0000000056,0.000000056,0.00000056 ...
          ,0.0000056,0.0000000062, 0.000000062, 0.00000062 ...
          ,0.0000062,0.0000000068 ,0.000000068 ,0.00000068 ...
          ,0.0000068 , 0.000000068 , 0.00000068 ,0.0000068 ...
          ,0.000068 ,0.00068,0.0068,0.0000000075 ...
          ,0.000000075,0.00000075,0.0000075 , 0.0000000082 ...
          ,0.000000082,0.00000082, 0.0000082, 0.0000000091 ...
          ,0.000000091 , 0.00000091 , 0.0000091];

dIlmax=IinvRipple*Pn*sqrt(2)/(3*Vph);
Linv=Vdc/(16*Fsw*dIlmax)
Zb=Vn^2 /Pn;
Cb=1/(Wn*Zb);
Cf=Cpercentage*Cb

%calculate Cfr which is the closest real capacitance

Cap=abs(Cf-Capacitor);
[Cdev,Cfrindex]=min(Cap);
Cfr=Capacitor(Cfrindex)
Cdev

r=1/(4*pi^2 *Fres^2 *Linv*Cfr-1)
Lg=r*Linv

%Here we calculate the grid current output ripple attenuation factor
OutputRippleFactor=1/abs(1+r*(1-Linv*Cfr*Wsw^2))

%bode plot of the final design
Linv=Linv;
Rinv=0;
Lg=Lg;
Rg=0;
Cf=Cfr;
Rc=0;

s1num=Rc*Cf;
```

```
100 s0num=1;%ti na po..
101 s3den=Lg*Linv*Cf;
102 s2den=Cf*(Lg*(Rc+Rinv));
103 s1den=Lg+Linv+Cf*(Rc*Rg+Rc*Rinv+Rg*Rinv);
104 s0den=Rg+Rinv+Linv*(Rc+Rg);
105 sys=tf([s1num,s0num],[s3den,s2den,s1den,s0den])
106
107 figure(1)
108 bode(sys);
```

DPC lookup table design based on virtual flux quantities

```
    breaklines
 1  clc
 2  clear all
 3
 4  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 5  %%%%    Switching vectors    %%%%%
 6  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 7
 8  VoltageVectorSwitch(1,:)=[1,80,80];
 9  VoltageVectorSwitch(2,:)=[1,1,80];
10  VoltageVectorSwitch(3,:)=[80,1,80];
11  VoltageVectorSwitch(4,:)=[80,1,1];
12  VoltageVectorSwitch(5,:)=[80,80,1];
13  VoltageVectorSwitch(6,:)=[1,80,1];
14  VoltageVectorSwitch(7,:)=[1,-1,-1];
15  VoltageVectorSwitch(8,:)=[1,80,-1];
16  VoltageVectorSwitch(9,:)=[1,1,-1];
17  VoltageVectorSwitch(10,:)=[80,1,-1];
18  VoltageVectorSwitch(11,:)=[-1,1,-1];
19  VoltageVectorSwitch(12,:)=[-1,1,80];
20  VoltageVectorSwitch(13,:)=[-1,1,1];
21  VoltageVectorSwitch(14,:)=[-1,80,1];
22  VoltageVectorSwitch(15,:)=[-1,-1,1];
23  VoltageVectorSwitch(16,:)=[80,-1,1];
24  VoltageVectorSwitch(17,:)=[1,-1,1];
25  VoltageVectorSwitch(18,:)=[1,-1,80];
26  %80 is used instead of 0 as a trick
27  for i=1:18
28      index=1;
29      for j=1:18
30          foo=VoltageVectorSwitch(i,:)+VoltageVectorSwitch(j,:);
31          flag=any( foo(:)==0 );
32          if (flag~=1)
33              candidate(i,index)=j;
34              index=index+1;
35          end
36      end
37      %CandidateNum(i)=nnz(candidate(i,:));
38      CandidateNum(i)=index-1;
39  end
40
41
42  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
43  %%%%%%   initialisation values   %%%%%%
44  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
45
46 Vdc=800;    %DC bus voltage
47 Vs=230*sqrt(2);     %AC grid Voltage
48 L=0.018;   %per phase inductance
49 f=50;       %grid frequency
50 W=2*pi*f;
51 NumSec=12;       %Number of sectors
52 Psimax=Vs/W;
53
54 %Table with Switch position of each phase for each voltage vector
55 VoltageVectorSwitch(1,:)=[1,0,0];
56 VoltageVectorSwitch(2,:)=[1,1,0];
57 VoltageVectorSwitch(3,:)=[0,1,0];
58 VoltageVectorSwitch(4,:)=[0,1,1];
59 VoltageVectorSwitch(5,:)=[0,0,1];
60 VoltageVectorSwitch(6,:)=[1,0,1];
61 VoltageVectorSwitch(7,:)=[1,-1,-1];
62 VoltageVectorSwitch(8,:)=[1,0,-1];
63 VoltageVectorSwitch(9,:)=[1,1,-1];
64 VoltageVectorSwitch(10,:)=[0,1,-1];
65 VoltageVectorSwitch(11,:)=[-1,1,-1];
66 VoltageVectorSwitch(12,:)=[-1,1,0];
67 VoltageVectorSwitch(13,:)=[-1,1,1];
68 VoltageVectorSwitch(14,:)=[-1,0,1];
69 VoltageVectorSwitch(15,:)=[-1,-1,1];
70 VoltageVectorSwitch(16,:)=[0,-1,1];
71 VoltageVectorSwitch(17,:)=[1,-1,1];
72 VoltageVectorSwitch(18,:)=[1,-1,0];
73
74 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
75 %%%%%%%%%%%%  Cost Evaluation  %%%%%%%%%%%%%%%%%%%%
76 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
77
78 for i=1:18
79     index=1;
80     for j=1:18
81         cost(i,j)=0;
82         flag=any( candidate(i,:)==j );
83         if flag
84
85         for k=1:3
86          if VoltageVectorSwitch(i,k)~=VoltageVectorSwitch(j,k)
87               cost(i,j)=cost(i,j)+1;
88          end
89         end
90
91         else
92             cost(i,j)=666;
93         end
94
95     end
96 end
97
98 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
99
100 [NumVec,col]= size(VoltageVectorSwitch); %Number of voltage vectors accounted
101
102 %voltage output in abc
103 Vabc=VoltageVectorSwitch*Vdc/2;
104
105 %voltage output in alpha beta plane
106 Vab(:,1)=(Vdc/3)*(2*VoltageVectorSwitch(:,1)-VoltageVectorSwitch(:,2)-VoltageVectorSwitch(:,3));
```

```
Vab(:,2)=(Vdc/(sqrt(3)))*(VoltageVectorSwitch(:,2)-VoltageVectorSwitch(:,3));

%flux output in alpha beta plane
Psinvab(:,1)=Vab(:,2)/W;  %Transformation of voltage to flux
                          %calculated in trigonometric graphical way
Psinvab(:,2)=-Vab(:,1)/W; %flux is lagging 90 degrees of voltage and
                          %is proportional by a factor of 1/Ws

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%     dP,dQ calculation     %%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


%Psiga,Psigb contain the grid flux calculated in the center of each
%sector.Here sector one is considered from 0-30 degrees
%for other sector numbering use circshift(Psiga,- number of sectors
% to shift.For example to shift back 120 degrees back in 12 sector
%defintion   back=120/(360/NumSec) =Numsec/3 =12/3 =4 )
for i = 1:NumSec

             Psiga(i)=Psimax*cosd((2*i-1)*180/NumSec);
             Psigb(i)=Psimax*sind((2*i-1)*180/NumSec);

end
%shifting flux 90 degrees backwards
back=NumSec/4    %360/4=90
Psiga=Psiga';
Psiga=circshift(Psiga,back);
Psiga=Psiga';
Psigb=Psigb';
Psigb=circshift(Psigb,back);
Psigb=Psigb';
i=0;
j=0;
         for i = 1:NumSec
             for j = 1:NumVec

              Iga(i,j) = (Psinvab(j,1)-Psiga(i))/L;
              Igb(i,j) = (Psinvab(j,2)-Psigb(i))/L;

              P(i,j)=(3*W/2)*(Psiga(i)*Igb(i,j)-Psigb(i)*Iga(i,j));
              Q(i,j)=(3*W/2)*(Psiga(i)*Iga(i,j)+Psigb(i)*Igb(i,j));

              dP(i,j)=(-3*(W^2)/(2*L))*(-Psiga(i)*Psinvab(j,1)-Psigb(i)*Psinvab(j,2)+(Psiga(i
              dQ(i,j)=(-3*(W^2)/(2*L))*(-Psigb(i)*Psinvab(j,1)+Psiga(i)*Psinvab(j,2)) +W*P(i,


             end
         end

         p=dP' ;
         q=dQ' ;
         a1=[abs(min(min(p))),abs(max(max(p)))];
         b1=max(a1);
         p_new=p/b1;
         a2=[abs(min(min(q))),abs(max(max(q)))];
         b2=max(a2);
         q_new=q/b2;
         p1=p(:,1:6);
         p2=p(:,7:12);
         q1=q(:,1:6);
         q2=q(:,7:12);
```

```
169
170 %Surf plots
171 %          N=linspace(1,NumSec,NumSec);
172 %          plot(N,Psiga,N,Psigb);
173 %          surf(p_new);
174 pr=p_new';
175 qr=q_new';
176
177          for i = 1:NumSec
178
179              Pipp=1;
180              Pip=1;
181              Pinn=1;
182              Pin=1;
183
184              Qipp=1;
185              Qip=1;
186              Qinn=1;
187              Qin=1;
188
189              for j = 1:NumVec
190
191
192                  if  (pr(i,j)>=0.1)&&(pr(i,j)<0.4)
193                      pr2(i,j)=1;
194                      Ptp(i,Pip)=j;
195                      Pip=Pip+1;
196                  elseif pr(i,j)>=0.4
197                          pr2(i,j)=2;
198                          Ptpp(i,Pipp)=j;
199                          Pipp=Pipp+1;
200                  elseif (pr(i,j)<=-0.1)&&(pr(i,j)>-0.4)
201                      pr2(i,j)=-1;
202                      Ptn(i,Pin)=j;
203                      Pin=Pin+1;
204                  elseif pr(i,j)<=-0.4
205                      pr2(i,j)=-2;
206                      Ptnn(i,Pinn)=j;
207                      Pinn=Pinn+1;
208                  else
209                       pr2(i,j)=0;
210                  end
211
212                  if  (qr(i,j)>=0.1)&&(qr(i,j)<0.4)
213                      qr2(i,j)=1;
214                      Qtp(i,Qip)=j;
215                      Qip=Qip+1;
216                  elseif qr(i,j)>=0.4
217                          qr2(i,j)=2;
218                          Qtpp(i,Qipp)=j;
219                          Qipp=Qipp+1;
220                  elseif (qr(i,j)<=-0.1)&&(qr(i,j)>-0.4)
221                      qr2(i,j)=-1;
222                      Qtn(i,Qin)=j;
223                      Qin=Qin+1;
224                  elseif qr(i,j)<=-0.4
225                      qr2(i,j)=-2;
226                      Qtnn(i,Qinn)=j;
227                      Qinn=Qinn+1;
228                  else
229                       qr2(i,j)=0;
230                  end
```

```
231
232                 end
233             end
234
235
236
237
238 %   %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
239 %   %%%%%%%%%%%%%%%       Final Evaluations          %%%%%%%%%%%%%%%%%%%
240 %   %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
241 %
242 % %++ on sector 1
243 % Q=nnz(Ptpp(1,:));
244 % if(Q>1)
245 %
246 %   for i=2:Q
247 %       if (CandidateNum(i)>CandidateNum(i-1))
248 %          Pfinal(1,1)=Ptpp(1,i);
249 %       end
250 %   end
251 %
252 % else
253 %       Pfinal(1,1)=Ptpp(1,1);
254 %
255 % end
256 %
257 %
258 % buffVector=intersect(Ptp(1,:),candidate(Pfinal(1,1),:));
259 %
260 % Q=nnz(buffVector);
261 % if(Q>1)
262 %
263 %   for i=2:Q
264 %       if (CandidateNum(i)>CandidateNum(i-1))
265 %          Pfinal(2,1)=buffVector(i);
266 %       end
267 %   end
268 %
269 % else
270 %       Pfinal(2,1)=buffVector(1);
271 %
272 % end
273 %
274 %
275 % buffVector=intersect(Ptnn(1,:),candidate(Pfinal(2,1),:));
276 %
277 % Q=nnz(buffVector);
278 % if(Q>1)
279 %
280 %   for i=2:Q
281 %       if (CandidateNum(i)>CandidateNum(i-1))
282 %          Pfinal(3,1)=buffVector(i);
283 %       end
284 %   end
285 %
286 % else
287 %       Pfinal(3,1)=buffVector;
288 %
289 % end
290 %
291 % buffVector=intersect(Ptn(1,:),candidate(Pfinal(3,1),:));
292 %
```

```
% Q=nnz(buffVector);
% if(Q>1)
%
%   for i=2:Q
%      if (CandidateNum(i)>CandidateNum(i-1))
%         Pfinal(4,1)=buffVector(i);
%      end
%   end
%
% else
%      Pfinal(4,1)=buffVector;
%
% end


   subplot(1,2,1), imagesc(p_new)
   title('Active Power Variation rates')
   subplot(1,2,2), imagesc(q_new)
   title('Reactive Power Variation rates')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


% vector sorting
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%         P+ P- Q+ Q-  creation        %%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


for i=1:NumSec
    s=1;
    for j=1:NumVec

        if p_new(j,i)>=0

            p_plus(s,i)=j; %contains all voltage vectors with
                    %positive dP for each sector in each column
            p_plusN(i)=s;  %number of positive voltage vectors
                           %for each sector in each column
            s=s+1;
        end
    end
end

for i=1:NumSec
    s=1;
    for j=1:NumVec

        if p_new(j,i)<0

            p_minus(s,i)=j; %contains all voltage vectors with
                            %negative dP for each sector in
                            %each column
            p_minusN(i)=s;  %number of negative voltage vectors
                            %for each sector in each column
            s=s+1;
        end
    end
end
```

```
for i=1:NumSec
    s=1;
    for j=1:NumVec

        if q_new(j,i)>0

            q_plus(s,i)=j;     %contains all voltage vectors with
                               %positive dQ for each sector in
                               %each column
            q_plusN(i)=s;      %number of positive voltage vectors
                               %for each sector in each column
            s=s+1;
        end
    end
end

for i=1:NumSec
    s=1;
    for j=1:NumVec

        if q_new(j,i)<0

            q_minus(s,i)=j;     %contains all voltage vectors with
                                %negative dQ for each sector in
                                %each column
            q_minusN(i)=s;      %number of negative voltage vectors
                                %for each sector in each column
            s=s+1;
        end
    end
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%         pq       %%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% PQ  P+ Q+
for i=1:NumSec

buffer=   intersect(p_plus(:,i),q_plus(:,i)) ;
[numa,trash]=size(buffer);


index=0;
for k=1:numa

    if (buffer(k)>0)
    index=index+1;
    PQ(index,i)=buffer(k);

    end
end
PQ_N(i)=index;
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Pq  P+ Q-
for i=1:NumSec

```

```
417 buffer=   intersect(p_plus(:,i),q_minus(:,i)) ;
418 [numa,trash]=size(buffer);
419
420
421 index=0;
422 for k=1:numa
423
424     if (buffer(k)>0)
425     index=index+1;
426     Pq(index,i)=buffer(k);
427
428     end
429 end
430 Pq_N(i)=index;
431 end
432
433 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
434
435 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% pQ  P- Q+
436 for i=1:NumSec
437
438 buffer=   intersect(p_minus(:,i),q_plus(:,i)) ;
439 [numa,trash]=size(buffer);
440
441
442 index=0;
443 for k=1:numa
444
445     if (buffer(k)>0)
446     index=index+1;
447     pQ(index,i)=buffer(k);
448
449     end
450 end
451 pQ_N(i)=index;
452 end
453
454 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
455
456 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% pq  P- Q-
457 for i=1:NumSec
458
459 buffer=   intersect(p_minus(:,i),q_minus(:,i)) ;
460 [numa,trash]=size(buffer);
461
462
463 index=0;
464 for k=1:numa
465
466     if (buffer(k)>0)
467     index=index+1;
468     pq(index,i)=buffer(k);
469
470     end
471 end
472 pq_N(i)=index;
473 end
474
475 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
476
477 for t=1:PQ_N(1)
478
```

```
479
480 PQf(1)=PQ(t,1); %to proto stoihio tou P+Q+ to orizoume emeis.
481                  %xnLUT oses kai oi pithanes protes liseis
482
483 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%Vrisko to Pqf(1)
484 Pqbuffer=intersect(Pq(:,1),candidate(PQf(1),:));
485 bufferLength=length(Pqbuffer);
486
487 if any(Pqbuffer)>0   %periptosi pou oproigoumenointersect ine keno
488
489     if Pqbuffer(1)>0 %an vgazei apo lathos to 0 san koino
490                      %stoiheio to vgazei stin proti thesi
491                      %epomenos edo lamvanoume ta metra mas
492                      %oste na min anazitisi se pinaka index 0
493
494      maxVector=Pqbuffer(1);       %arhikopio os veltisto to proto
495                           %vector tou intersection kai tin timi tou
496      maxC=p_new(Pqbuffer(1),1);
497      m=1;
498     else
499      maxVector=Pqbuffer(2); %an to proto stoihio ine to miden
500                             %arhikopio to 2o
501      maxC=p_new(Pqbuffer(2),1);
502      m=2;
503     end
504
505 %taksinomisi me vasi to to megalitero dP
506
507 for i=m:bufferLength                %to i to eho orisei parapano
508                                     %an tha ksekina apo 1 h 2
509     if  p_new(Pqbuffer(i),1)>maxC   % an to dP ine megalitero
510                                     %adikatestise
511         maxVector=Pqbuffer(i);
512         maxC=p_new(Pqbuffer(i),1);
513     end
514 end
515
516 maxC2=0;
517 maxVector2=0;
518 for i=m:bufferLength
519     if  p_new(Pqbuffer(i),1)>maxC2 && p_new(Pqbuffer(i),1)<=maxC
520         maxVector2=Pqbuffer(i);
521         maxC2=p_new(Pqbuffer(i),1);
522     end
523 end
524
525 maxC3=0;
526 maxVector3=0;
527 for i=m:bufferLength
528     if  p_new(Pqbuffer(i),1)>maxC3 && p_new(Pqbuffer(i),1)<=maxC3
529         maxVector3=Pqbuffer(i);
530         maxC3=p_new(Pqbuffer(i),1);
531     end
532 end
533
534 %%%%elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
535 buffmax=maxVector;
536
537 if maxVector2>0
538
539 if cost(PQf(1,1),maxVector)>cost(PQf(1,1),maxVector2)
540     buffmax=maxVector2;
```

```
541 else
542     buffmax=buffmax;
543 end
544
545 end
546
547 if maxVector3>0
548
549 if cost(PQf(1,1),buffmax)>cost(PQf(1,1),maxVector3)
550     buffmax=maxVector3;
551 else
552     buffmax=buffmax;
553 end
554
555 end
556
557
558 %Pqf(1)=maxVector;%dialego gia Pqf to proto apo ta
559                  %intersect me to megalytero dP
560 Pqf(1)=buffmax;
561
562 else
563
564 Pqbuffer=Pq(:,1);
565 bufferLength=length(Pqbuffer);
566
567
568
569     if Pqbuffer(1)>0 %an vgazei apo lathos to 0 san koino stoiheio
570                      %to vgazei stin proti thesi epomenos edo
571                      %lamvanoume ta metra mas oste na min anazitisi
572                      %se pinaka index 0
573
574      maxVector=Pqbuffer(1);   %arhikopio os veltisto to proto vector
575                               %tou intersection kai tin timi tou
576      maxC=p_new(Pqbuffer(1),1);
577      m=1;
578     else
579      maxVector=Pqbuffer(2);   %an to proto stoihio ine to miden
580                               %arhikopio to 2o
581      maxC=p_new(Pqbuffer(2),1);
582      m=2;
583     end
584
585
586 %taksinomisi me vasito to megalitero dP
587
588 for i=m:bufferLength
589    if Pqbuffer(i)>0
590     if  p_new(Pqbuffer(i),1)>maxC
591         maxVector=Pqbuffer(i);
592         maxC=p_new(Pqbuffer(i),1);
593     end
594    end
595 end
596
597 maxC2=0;
598 maxVector2=0;
599 for i=m:bufferLength
600    if Pqbuffer(i)>0
601     if  p_new(Pqbuffer(i),1)>maxC2 && p_new(Pqbuffer(i),1)<=maxC
602         maxVector2=Pqbuffer(i);
```

```
603          maxC2=p_new(Pqbuffer(i),1);
604      end
605     end
606  end
607
608  maxC3=0;
609  maxVector3=0;
610  for i=m:bufferLength
611     if Pqbuffer(i)>0
612      if  p_new(Pqbuffer(i),1)>maxC3 && p_new(Pqbuffer(i),1)<=maxC3
613          maxVector3=Pqbuffer(i);
614          maxC3=p_new(Pqbuffer(i),1);
615      end
616     end
617  end
618
619  %elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
620  buffmax=maxVector;
621
622  if maxVector2>0
623
624  if cost(PQf(1,1),maxVector)>cost(PQf(1,1),maxVector2)
625      buffmax=maxVector2;
626  else
627      buffmax=buffmax;
628  end
629
630  end
631
632  if maxVector3>0
633
634  if cost(PQf(1,1),buffmax)>cost(PQf(1,1),maxVector3)
635      buffmax=maxVector3;
636  else
637      buffmax=buffmax;
638  end
639
640  end
641
642
643  %Pqf(1)=maxVector;
644  Pqf(1)=buffmax;
645
646  end
647
648
649  %mehri na arhiso to apo 2 mehri NumSec ta idia sholia ektos to oti
650  %sta pq tha dialego afta me to pio arnitiko dP
651  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
652
653  %%%%%%%%%%%%%%%%Vrisko to pQf(1)
654
655  Pqbuffer=intersect(pQ(:,1),candidate(PQf(1),:));
656  bufferLength=length(Pqbuffer);
657
658  if any(Pqbuffer)>0
659
660      if Pqbuffer(1)>0
661
662       maxVector=Pqbuffer(1);
663       maxC=p_new(Pqbuffer(1),1);
664       m=1;
```

```
665     else
666      maxVector=Pqbuffer(2);
667      maxC=p_new(Pqbuffer(2),1);
668      m=2;
669     end
670 %taksinomisi me vasi to to mikrotero dP
671 for i=m:bufferLength
672     if  p_new(Pqbuffer(i),1)<maxC
673         maxVector=Pqbuffer(i);
674         maxC=p_new(Pqbuffer(i),1);
675     end
676 end
677 maxC2=0;
678 maxVector2=0;
679 for i=m:bufferLength
680     if  p_new(Pqbuffer(i),1)<maxC2 && p_new(Pqbuffer(i),1)>=maxC      %
681         maxVector2=Pqbuffer(i);
682         maxC2=p_new(Pqbuffer(i),1);
683     end
684 end
685
686 maxC3=0;
687 maxVector3=0;
688 for i=m:bufferLength
689     if  p_new(Pqbuffer(i),1)<maxC3 && p_new(Pqbuffer(i),1)>=maxC3
690         maxVector3=Pqbuffer(i);
691         maxC3=p_new(Pqbuffer(i),1);
692     end
693 end
694
695 %elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
696 buffmax=maxVector;
697
698 if maxVector2>0
699
700 if cost(PQf(1,1),maxVector)>cost(PQf(1,1),maxVector2)
701     buffmax=maxVector2;
702 else
703     buffmax=buffmax;
704 end
705
706 end
707
708 if maxVector3>0
709
710 if cost(PQf(1,1),buffmax)>cost(PQf(1,1),maxVector3)
711     buffmax=maxVector3;
712 else
713     buffmax=buffmax;
714 end
715
716 end
717
718
719 pQf(1)=buffmax;
720
721
722
723
724 %pQf(1)=maxVector;
725
726 else
```

```
727
728     Pqbuffer=pQ(:,1);
729 bufferLength=length(Pqbuffer);
730
731
732     if Pqbuffer(1)>0
733
734      maxVector=Pqbuffer(1);
735      maxC=p_new(Pqbuffer(1),1);
736      m=1;
737     else
738      maxVector=Pqbuffer(2);
739      maxC=p_new(Pqbuffer(2),1);
740      m=2;
741     end
742
743
744 %taksinomisi me vasi to to mikrotero dP
745
746
747 for i=m:bufferLength
748    if Pqbuffer(i)>0
749     if  p_new(Pqbuffer(i),1)<maxC
750         maxVector=Pqbuffer(i);
751         maxC=p_new(Pqbuffer(i),1);
752     end
753    end
754 end
755
756
757 maxC2=0;
758 maxVector2=0;
759 for i=m:bufferLength
760    if Pqbuffer(i)>0
761     if  p_new(Pqbuffer(i),1)<maxC2 && p_new(Pqbuffer(i),1)>=maxC
762         maxVector2=Pqbuffer(i);
763         maxC2=p_new(Pqbuffer(i),1);
764     end
765    end
766 end
767
768 maxC3=0;
769 maxVector3=0;
770 for i=m:bufferLength
771    if Pqbuffer(i)>0
772     if  p_new(Pqbuffer(i),1)<maxC3 && p_new(Pqbuffer(i),1)>=maxC3
773         maxVector3=Pqbuffer(i);
774         maxC3=p_new(Pqbuffer(i),1);
775     end
776    end
777 end
778
779 %elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
780 buffmax=maxVector;
781
782 if maxVector2>0
783
784 if cost(PQf(1,1),maxVector)>cost(PQf(1,1),maxVector2)
785     buffmax=maxVector2;
786 else
787     buffmax=buffmax;
788 end
```

```
789
790 end
791
792 if maxVector3>0
793
794 if cost(PQf(1,1),buffmax)>cost(PQf(1,1),maxVector3)
795     buffmax=maxVector3;
796 else
797     buffmax=buffmax;
798 end
799
800 end
801
802
803 pQf(1)=buffmax;
804
805 %      pQf(1)=PQf(1);
806       %pQf(1)=pQ(1,1);
807 end
808
809 %%%%%%%%%%%%%%%%%%%%%%Vrisko to pqf(1)
810 Pqbuffer=intersect(pq(:,1),candidate(pQf(1),:));
811 bufferLength=length(Pqbuffer);
812
813 if any(Pqbuffer)>0
814
815     if Pqbuffer(1)>0
816
817      maxVector=Pqbuffer(1);
818      maxC=p_new(Pqbuffer(1),1);
819      m=1;
820     else
821      maxVector=Pqbuffer(2);
822      maxC=p_new(Pqbuffer(2),1);
823      m=2;
824     end
825
826 %taksinomisi me vasi to mikrotero dP
827
828 for i=m:bufferLength
829     if  p_new(Pqbuffer(i),1)<maxC
830         maxVector=Pqbuffer(i);
831         maxC=p_new(Pqbuffer(i),1);
832     end
833 end
834
835 maxC2=0;
836 maxVector2=0;
837 for i=m:bufferLength
838     if  p_new(Pqbuffer(i),1)<maxC2 && p_new(Pqbuffer(i),1)>=maxC
839         maxVector2=Pqbuffer(i);
840         maxC2=p_new(Pqbuffer(i),1);
841     end
842 end
843
844 maxC3=0;
845 maxVector3=0;
846 for i=m:bufferLength
847     if  p_new(Pqbuffer(i),1)<maxC3 && p_new(Pqbuffer(i),1)>=maxC3
848         maxVector3=Pqbuffer(i);
849         maxC3=p_new(Pqbuffer(i),1);
850     end
```

```
851 end
852
853 %elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
854 buffmax=maxVector;
855
856 if maxVector2>0
857
858 if cost(Pqf(1,1),maxVector)>cost(Pqf(1,1),maxVector2)
859     buffmax=maxVector2;
860 else
861     buffmax=buffmax;
862 end
863
864 end
865
866 if maxVector3>0
867
868 if cost(Pqf(1,1),buffmax)>cost(Pqf(1,1),maxVector3)
869     buffmax=maxVector3;
870 else
871     buffmax=buffmax;
872 end
873
874 end
875 pqf(1)=buffmax;
876 %pqf(1)=maxVector;
877 else
878
879     Pqbuffer=pq(:,1);
880     bufferLength=length(Pqbuffer);
881     if Pqbuffer(1)>0
882      maxVector=Pqbuffer(1);
883      maxC=p_new(Pqbuffer(1),1);
884      m=1;
885     else
886      maxVector=Pqbuffer(2);
887      maxC=p_new(Pqbuffer(2),1);
888      m=2;
889     end
890 %taksinomisi me vasi to mikrotero dP
891
892 for i=m:bufferLength
893    if Pqbuffer(i)>0
894     if  p_new(Pqbuffer(i),1)<maxC
895         maxVector=Pqbuffer(i);
896         maxC=p_new(Pqbuffer(i),1);
897     end
898    end
899 end
900
901 maxC2=0;
902 maxVector2=0;
903 for i=m:bufferLength
904    if Pqbuffer(i)>0
905     if  p_new(Pqbuffer(i),1)<maxC2 && p_new(Pqbuffer(i),1)>=maxC
906         maxVector2=Pqbuffer(i);
907         maxC2=p_new(Pqbuffer(i),1);
908     end
909    end
910 end
911
912 maxC3=0;
```

```
maxVector3=0;
for i=m:bufferLength
   if Pqbuffer(i)>0
    if  p_new(Pqbuffer(i),1)<maxC3 && p_new(Pqbuffer(i),1)>=maxC3
        maxVector3=Pqbuffer(i);
        maxC3=p_new(Pqbuffer(i),1);
    end
   end
end

%elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
buffmax=maxVector;

if maxVector2>0

if cost(Pqf(1,1),maxVector)>cost(Pqf(1,1),maxVector2)
    buffmax=maxVector2;
else
    buffmax=buffmax;
end

end

if maxVector3>0

if cost(Pqf(1,1),buffmax)>cost(Pqf(1,1),maxVector3)
    buffmax=maxVector3;
else
    buffmax=buffmax;
end

end


pqf(1)=buffmax;


   % pqf(1)= pQf(1);
    %pqf(1)= pq(1,1);
end



%%%%%%%%%%%%%%%%%%%%%%%%%%%%ipologizo apo 2 mehi NumSec ta PQ Pq pQ pq
for j=2:NumSec
%%%%%%%%%%%%%%%%%%%%%%%%%%   PQ   P+ Q+

    Pqbuffer=intersect(PQ(:,j),candidate(PQf(j-1),:));
    bufferLength=length(Pqbuffer);

    if any(Pqbuffer)>0

%taksinomisi me vasi to to megalitero dP
if Pqbuffer(1)>0

     maxVector=Pqbuffer(1);
     maxC=p_new(Pqbuffer(1),j);
     m=1;
else
     maxVector=Pqbuffer(2);
     maxC=p_new(Pqbuffer(2),j);
     m=2;
```

```
975 end
976
977 for i=m:bufferLength
978     if p_new(Pqbuffer(i),j)>maxC
979         maxVector=Pqbuffer(i);
980         maxC=p_new(Pqbuffer(i),j);
981     end
982 end
983
984 maxC2=0;
985 maxVector2=0;
986 for i=m:bufferLength
987     if  p_new(Pqbuffer(i),j)>maxC2 && p_new(Pqbuffer(i),j)<=maxC
988         maxVector2=Pqbuffer(i);
989         maxC2=p_new(Pqbuffer(i),j);
990     end
991 end
992
993 maxC3=0;
994 maxVector3=0;
995 for i=m:bufferLength
996     if  p_new(Pqbuffer(i),j)>maxC3 && p_new(Pqbuffer(i),j)<=maxC3
997         maxVector3=Pqbuffer(i);
998         maxC3=p_new(Pqbuffer(i),j);
999     end
1000 end
1001
1002 %elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
1003 buffmax=maxVector;
1004
1005 if maxVector2>0
1006
1007 if cost(PQf(j-1),maxVector)>cost(PQf(j-1),maxVector2)
1008     buffmax=maxVector2;
1009 else
1010     buffmax=buffmax;
1011 end
1012
1013 end
1014
1015 if maxVector3>0
1016
1017 if cost(PQf(j-1),buffmax)>cost(PQf(j-1),maxVector3)
1018     buffmax=maxVector3;
1019 else
1020
1021     buffmax=buffmax;
1022 end
1023
1024 end
1025
1026
1027 PQf(j)=buffmax;
1028
1029
1030
1031
1032 %PQf(j)=maxVector;
1033
1034     else
1035
1036     Pqbuffer=PQ(:,j);
```

```
1037      bufferLength=length(Pqbuffer);
1038
1039
1040
1041
1042
1043  %taksinomisi me vasi to to megalitero dP
1044  if Pqbuffer(1)>0
1045
1046       maxVector=Pqbuffer(1);
1047       maxC=p_new(Pqbuffer(1),j);
1048       m=1;
1049  else
1050       maxVector=Pqbuffer(2);
1051       maxC=p_new(Pqbuffer(2),j);
1052       m=2;
1053  end
1054
1055  for i=m:bufferLength
1056     if Pqbuffer(i)>0
1057
1058      if p_new(Pqbuffer(i),j)>maxC
1059          maxVector=Pqbuffer(i);
1060          maxC=p_new(Pqbuffer(i),j);
1061      end
1062
1063     end
1064
1065
1066  end
1067
1068
1069
1070  maxC2=0;
1071  maxVector2=0;
1072  for i=m:bufferLength
1073     if Pqbuffer(i)>0
1074      if  p_new(Pqbuffer(i),j)>maxC2 && p_new(Pqbuffer(i),j)<=maxC
1075          maxVector2=Pqbuffer(i);
1076          maxC2=p_new(Pqbuffer(i),j);
1077      end
1078     end
1079  end
1080
1081  maxC3=0;
1082  maxVector3=0;
1083  for i=m:bufferLength
1084     if Pqbuffer(i)>0
1085      if  p_new(Pqbuffer(i),j)>maxC3 && p_new(Pqbuffer(i),j)<=maxC3
1086          maxVector3=Pqbuffer(i);
1087          maxC3=p_new(Pqbuffer(i),j);
1088      end
1089     end
1090  end
1091
1092  %%%%elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
1093  buffmax=maxVector;
1094
1095  if maxVector2>0
1096
1097  if cost(PQf(j-1),maxVector)>cost(PQf(j-1),maxVector2)
1098      buffmax=maxVector2;
```

```
else
    buffmax=buffmax;
end

end

if maxVector3>0

if cost(PQf(j-1),buffmax)>cost(PQf(j-1),maxVector3)
    buffmax=maxVector3;
else

    buffmax=buffmax;
end

end


PQf(j)=buffmax;




   % PQf(j)=PQf(j-1);
    % PQf(j)=PQ(1,j);
    end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Pq   P+ Q-
    Pqbuffer=intersect(intersect(Pq(:,j),candidate(Pqf(j-1),:)), candidate(PQf(j),:) );
    bufferLength=length(Pqbuffer);

    if any(Pqbuffer)>0



%taksinomisi me vasi to to megalitero dP
if Pqbuffer(1)>0

    maxVector=Pqbuffer(1);
    maxC=p_new(Pqbuffer(1),j);
    m=1;
else
    maxVector=Pqbuffer(2);
    maxC=p_new(Pqbuffer(2),j);
    m=2;
end

for i=m:bufferLength
    if p_new(Pqbuffer(i),j)>maxC
        maxVector=Pqbuffer(i);
        maxC=p_new(Pqbuffer(i),j);
    end
end


maxC2=0;
maxVector2=0;
for i=m:bufferLength
    if  p_new(Pqbuffer(i),j)>maxC2 && p_new(Pqbuffer(i),j)<=maxC
        maxVector2=Pqbuffer(i);
        maxC2=p_new(Pqbuffer(i),j);
    end
end
```

```
1161
1162 maxC3=0;
1163 maxVector3=0;
1164 for i=m:bufferLength
1165     if  p_new(Pqbuffer(i),j)>maxC3 && p_new(Pqbuffer(i),j)<=maxC3
1166         maxVector3=Pqbuffer(i);
1167         maxC3=p_new(Pqbuffer(i),j);
1168     end
1169 end
1170
1171 %%%%elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
1172 buffmax=maxVector;
1173
1174 if maxVector2>0
1175
1176 if cost(PQf(j),maxVector)>cost(PQf(j),maxVector2)
1177     buffmax=maxVector2;
1178 else
1179     buffmax=buffmax;
1180 end
1181
1182 end
1183
1184 if maxVector3>0
1185
1186 if cost(PQf(j),buffmax)>cost(PQf(j),maxVector3)
1187     buffmax=maxVector3;
1188 else
1189     buffmax=buffmax;
1190 end
1191
1192 end
1193
1194
1195 Pqf(j)=buffmax;
1196
1197
1198
1199
1200 %Pqf(j)=maxVector;
1201
1202     else
1203
1204     Pqbuffer=Pq(:,j);
1205     bufferLength=length(Pqbuffer);
1206
1207
1208
1209
1210
1211 %taksinomisi me vasi to to megalitero dP
1212 if Pqbuffer(1)>0
1213
1214     maxVector=Pqbuffer(1);
1215     maxC=p_new(Pqbuffer(1),j);
1216     m=1;
1217 else
1218     maxVector=Pqbuffer(2);
1219     maxC=p_new(Pqbuffer(2),j);
1220     m=2;
1221 end
1222
```

```
for i=m:bufferLength
   if Pqbuffer(i)>0
    if p_new(Pqbuffer(i),j)>maxC
        maxVector=Pqbuffer(i);
        maxC=p_new(Pqbuffer(i),j);
    end
   end
end


maxC2=0;
maxVector2=0;
for i=m:bufferLength
   if Pqbuffer(i)>0
    if  p_new(Pqbuffer(i),j)>maxC2 && p_new(Pqbuffer(i),j)<=maxC
        maxVector2=Pqbuffer(i);
        maxC2=p_new(Pqbuffer(i),j);
    end
   end
end

maxC3=0;
maxVector3=0;
for i=m:bufferLength
   if Pqbuffer(i)>0
    if  p_new(Pqbuffer(i),j)>maxC3 && p_new(Pqbuffer(i),j)<=maxC3
        maxVector3=Pqbuffer(i);
        maxC3=p_new(Pqbuffer(i),j);
    end
   end
end

%elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
buffmax=maxVector;

if maxVector2>0

if cost(PQf(j),maxVector)>cost(PQf(j),maxVector2)
    buffmax=maxVector2;
else
    buffmax=buffmax;
end

end

if maxVector3>0

if cost(PQf(j),buffmax)>cost(PQf(j),maxVector3)
    buffmax=maxVector3;
else
    buffmax=buffmax;
end

end


Pqf(j)=buffmax;



%     Pqf(j)=Pqf(j-1);
```

```
1285        %Pqf(j)=Pq(1,j);
1286      end
1287 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% pQ   P- Q+
1288      Pqbuffer=intersect(intersect(pQ(:,j),candidate(pQf(j-1),:)), candidate(Pqf(j),:) );
1289      bufferLength=length(Pqbuffer);
1290
1291  if any(Pqbuffer)>0
1292
1293
1294 %taksinomisi me vasi to mikrotero dP
1295 if Pqbuffer(1)>0
1296      maxVector=Pqbuffer(1);
1297      maxC=p_new(Pqbuffer(1),j);
1298      m=1;
1299 else
1300      maxVector=Pqbuffer(2);
1301      maxC=p_new(Pqbuffer(2),j);
1302      m=2;
1303 end
1304
1305 for i=m:bufferLength
1306      if p_new(Pqbuffer(i),j)<maxC
1307          maxVector=Pqbuffer(i);
1308          maxC=p_new(Pqbuffer(i),j);
1309      end
1310 end
1311
1312
1313 maxC2=0;
1314 maxVector2=0;
1315 for i=m:bufferLength
1316      if  p_new(Pqbuffer(i),j)<maxC2 && p_new(Pqbuffer(i),j)>=maxC
1317          maxVector2=Pqbuffer(i);
1318          maxC2=p_new(Pqbuffer(i),j);
1319      end
1320 end
1321
1322 maxC3=0;
1323 maxVector3=0;
1324 for i=m:bufferLength
1325      if  p_new(Pqbuffer(i),j)<maxC3 && p_new(Pqbuffer(i),j)>=maxC3
1326          maxVector3=Pqbuffer(i);
1327          maxC3=p_new(Pqbuffer(i),j);
1328      end
1329 end
1330
1331 %%%%elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
1332 buffmax=maxVector;
1333
1334 if maxVector2>0
1335
1336 if cost(PQf(j),maxVector)>cost(PQf(j),maxVector2)
1337      buffmax=maxVector2;
1338 else
1339      buffmax=buffmax;
1340 end
1341
1342 end
1343
1344 if maxVector3>0
1345
1346 if cost(PQf(j),buffmax)>cost(PQf(j),maxVector3)
```

```
1347      buffmax=maxVector3;
1348  else
1349      buffmax=buffmax;
1350  end
1351
1352  end
1353
1354
1355  pQf(j)=buffmax;
1356
1357
1358
1359  %pQf(j)=maxVector;
1360
1361   else
1362
1363      Pqbuffer=pQ(:,j);
1364      bufferLength=length(Pqbuffer);
1365
1366
1367
1368
1369  %taksinomisi me vasi to mikrotero dP
1370  if Pqbuffer(1)>0
1371      maxVector=Pqbuffer(1);
1372      maxC=p_new(Pqbuffer(1),j);
1373      m=1;
1374  else
1375      maxVector=Pqbuffer(2);
1376      maxC=p_new(Pqbuffer(2),j);
1377      m=2;
1378  end
1379
1380  for i=m:bufferLength
1381     if Pqbuffer(i) >0
1382      if p_new(Pqbuffer(i),j)<maxC
1383          maxVector=Pqbuffer(i);
1384          maxC=p_new(Pqbuffer(i),j);
1385      end
1386     end
1387  end
1388
1389
1390  maxC2=0;
1391  maxVector2=0;
1392  for i=m:bufferLength
1393     if Pqbuffer(i) >0
1394      if  p_new(Pqbuffer(i),j)<maxC2 && p_new(Pqbuffer(i),j)>=maxC
1395          maxVector2=Pqbuffer(i);
1396          maxC2=p_new(Pqbuffer(i),j);
1397      end
1398     end
1399  end
1400
1401  maxC3=0;
1402  maxVector3=0;
1403  for i=m:bufferLength
1404     if Pqbuffer(i) >0
1405      if  p_new(Pqbuffer(i),j)<maxC3 && p_new(Pqbuffer(i),j)>=maxC3
1406          maxVector3=Pqbuffer(i);
1407          maxC3=p_new(Pqbuffer(i),j);
1408      end
```

```
1409     end
1410 end
1411
1412 %%%%elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
1413 buffmax=maxVector;
1414
1415 if maxVector2>0
1416
1417 if cost(PQf(j),maxVector)>cost(PQf(j),maxVector2)
1418     buffmax=maxVector2;
1419 else
1420     buffmax=buffmax;
1421 end
1422
1423 end
1424
1425 if maxVector3>0
1426
1427 if cost(PQf(j),buffmax)>cost(PQf(j),maxVector3)
1428     buffmax=maxVector3;
1429 else
1430     buffmax=buffmax;
1431 end
1432
1433 end
1434
1435
1436 pQf(j)=buffmax;
1437
1438      % pQf(j)=pQf(j-1);
1439      % pQf(j)=pQ(1,j);
1440     end
1441 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% pq   P- Q-
1442     Pqbuffer=intersect(intersect(pq(:,j),candidate(pqf(j-1),:)), candidate(pQf(j),:) );
1443     bufferLength=length(Pqbuffer);
1444
1445     if any(Pqbuffer)>0
1446
1447
1448
1449 %taksinomisi me vasi to mikrotero dP
1450 if Pqbuffer(1)>0
1451
1452     maxVector=Pqbuffer(1);
1453     maxC=p_new(Pqbuffer(1),j);
1454     m=1;
1455 else
1456     maxVector=Pqbuffer(2);
1457     maxC=p_new(Pqbuffer(2),j);
1458     m=2;
1459 end
1460 for i=m:bufferLength
1461     if p_new(Pqbuffer(i),j)<maxC
1462         maxVector=Pqbuffer(i);
1463         maxC=p_new(Pqbuffer(i),j);
1464     end
1465 end
1466
1467
1468 maxC2=0;
1469 maxVector2=0;
1470 for i=m:bufferLength
```

```
1471      if  p_new(Pqbuffer(i),j)<maxC2 && p_new(Pqbuffer(i),j)>=maxC
1472          maxVector2=Pqbuffer(i);
1473          maxC2=p_new(Pqbuffer(i),j);
1474      end
1475  end
1476
1477  maxC3=0;
1478  maxVector3=0;
1479  for i=m:bufferLength
1480      if  p_new(Pqbuffer(i),j)<maxC3 && p_new(Pqbuffer(i),j)>=maxC3
1481          maxVector3=Pqbuffer(i);
1482          maxC3=p_new(Pqbuffer(i),j);
1483      end
1484  end
1485
1486  %%%%elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
1487  buffmax=maxVector;
1488
1489  if maxVector2>0
1490
1491  if cost(Pqf(j),maxVector)>cost(Pqf(j),maxVector2)
1492      buffmax=maxVector2;
1493  else
1494      buffmax=buffmax;
1495  end
1496
1497  end
1498
1499  if maxVector3>0
1500
1501  if cost(Pqf(j),buffmax)>cost(Pqf(j),maxVector3)
1502      buffmax=maxVector3;
1503  else
1504      buffmax=buffmax;
1505  end
1506
1507  end
1508
1509
1510  pqf(j)=buffmax;
1511
1512
1513
1514  %pqf(j)=maxVector;
1515
1516      else
1517        Pqbuffer=pq(:,j);
1518      bufferLength=length(Pqbuffer);
1519
1520
1521
1522
1523
1524  %taksinomisi me vasi to mikrotero dP
1525  if Pqbuffer(1)>0
1526
1527      maxVector=Pqbuffer(1);
1528      maxC=p_new(Pqbuffer(1),j);
1529      m=1;
1530  else
1531      maxVector=Pqbuffer(2);
1532      maxC=p_new(Pqbuffer(2),j);
```

```
    m=2;
end
for i=m:bufferLength
    if Pqbuffer(i) >0
    if p_new(Pqbuffer(i),j)<maxC
        maxVector=Pqbuffer(i);
        maxC=p_new(Pqbuffer(i),j);
    end
    end
end


maxC2=0;
maxVector2=0;
for i=m:bufferLength
   if Pqbuffer(i) >0
    if  p_new(Pqbuffer(i),j)<maxC2 && p_new(Pqbuffer(i),j)>=maxC
        maxVector2=Pqbuffer(i);
        maxC2=p_new(Pqbuffer(i),j);
    end
   end
end

maxC3=0;
maxVector3=0;
for i=m:bufferLength
   if Pqbuffer(i) >0
    if  p_new(Pqbuffer(i),j)<maxC3 && p_new(Pqbuffer(i),j)>=maxC3
        maxVector3=Pqbuffer(i);
        maxC3=p_new(Pqbuffer(i),j);
    end
   end
end

%%%elenho gia pio apo ta 3 megalytera dP ehei to mikrotero kostos
buffmax=maxVector;

if maxVector2>0

if cost(Pqf(j),maxVector)>cost(Pqf(j),maxVector2)
    buffmax=maxVector2;
else
    buffmax=buffmax;
end

end

if maxVector3>0

if cost(Pqf(j),buffmax)>cost(Pqf(j),maxVector3)
    buffmax=maxVector3;
else
    buffmax=buffmax;
end

end


pqf(j)=buffmax;
```

```

%      pqf(j)=pqf(j-1);
%      pqf(j)=pq(1,j);
    end
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
t
xnLUT=[PQf;Pqf;pQf;pqf]
end
```

Interface card gates and BBox FPGA output register relation

breaklines

```
% NPC switching vectors
dpcLUT=[
    0,0,0;
    1,0,-1;
    0,0,-1;
    1,1,0;
    1,1,-1;
    0,1,-1;
    0,1,0;
    -1,0,-1;
    -1,1,-1;
    -1,1,0;
    -1,0,0;
    0,1,1;
    -1,1,1;
    -1,0,1;
    0,0,1;
    -1,-1,0;
    -1,-1,1;
    0,-1,1;
    0,-1,0;
    1,0,1;
    1,-1,1;
    1,-1,0;
    1,0,0;
    0,-1,-1;
    1,-1,-1;
    -1,-1,-1;
    1,1,1;
]
dpcLUT=floor(dpcLUT);
% FPGAreg has values of output registers in binary vector form
% |bit6|bit5|bit4|bit3|bit2|bit1| bit0 |
% |Ap_a|Am_a|Ap_b|Am_b|Ap_c|Am_c|En_All|

FPGAreg=zeros(27,7);

for i=1:27

    if (dpcLUT(i,1)>0)%==1

        FPGAreg(i,1)=1;    %Ap_a
        FPGAreg(i,2)=1;    %Am_a

```

```
45      elseif (dpcLUT(i,1)==0)
46
47          FPGAreg(i,1)=0;      %Ap_a
48          FPGAreg(i,2)=1;      %Am_a
49
50      else% dpcLUT(i,1)<0%==-1
51
52          FPGAreg(i,1)=0;      %Ap_a
53          FPGAreg(i,2)=0;      %AM_a
54
55      end
56      %%%%%%%%%%%%%%%%%%%%%%%%%%
57
58
59      if (dpcLUT(i,2)>0)%==1
60
61          FPGAreg(i,3)=1;     %Ap_B
62          FPGAreg(i,4)=1;     %Am_B
63
64      elseif (dpcLUT(i,2)==0)
65
66          FPGAreg(i,3)=0;     %Ap_B
67          FPGAreg(i,4)=1;     %Am_B
68
69      else% dpcLUT(i,1)<0%==-1
70
71          FPGAreg(i,3)=0;      %Ap_B
72          FPGAreg(i,4)=0;      %Am_B
73
74      end
75      %%%%%%%%%%%%%%%%%%%%%%%%%%
76
77
78      if (dpcLUT(i,3)>0)%==1
79
80          FPGAreg(i,5)=1;      %Ap_C
81          FPGAreg(i,6)=1;      %Am_C
82
83      elseif (dpcLUT(i,3)==0)
84
85          FPGAreg(i,5)=0;      %Ap_C
86          FPGAreg(i,6)=1;      %Am_C
87
88      else% dpcLUT(i,1)<0%==-1
89
90          FPGAreg(i,5)=0;      %Ap_C
91          FPGAreg(i,6)=0;      %Am_C
92
93      end
94      %%%%%%%%%%%%%%%%%%%%%%%%%%
95
96        FPGAreg(i,7)=1;
97
98       i
99       dpcLUT(i,1:3)
100      FPGAreg(i,:)
101
102 end
103
104 reg=bi2de(FPGAreg,'left-msb');
```

An example of automated simulation profiles

```
breaklines
for j=1:100

    Qref= 10*j;
    Yaxis(j)=Qref;
    j


    for i=1:100
        i
        dInitMPCLCL;  % initialisation matlab script
                      % c sfunction compiled in this script
                      %with -mex environment
                      % all files must be in same folder
                      %and set as current workspace

        Pref= 10*i;
        Xaxis(i)=Pref;

        sim MPCLCLfullb  % run simulation model with saved parameters

        Q1maxC(i,j)=Q1max;
        Q1minC(i,j)=Q1min;
        Q1avgC(i,j)=Q1average;

        Q2maxC(i,j)=Q2max;
        Q2minC(i,j)=Q2min;
        Q2avgC(i,j)=Q2average;

        Q3maxC(i,j)=Q3max;
        Q3minC(i,j)=Q3min;
        Q3avgC(i,j)=Q3average;

        Q4maxC(i,j)=Q4max;
        Q4minC(i,j)=Q4min;
        Q4avgC(i,j)=Q4average;

        %Average of all four switche avg,min and max switching frequency
        Fsw_avg(i,j)= (Q1average+Q2average+Q3average+Q4average)/4;
        Fsw_max(i,j)= (Q1max+Q2max+Q3max+Q4max)/4;
        Fsw_min(i,j)= (Q1min+Q2min+Q3min+Q4min)/4;



        % THD calculation

        x=Igrid.signals.values(4001:end,1);
        Fs=1/Ts;
        N=length(x); %get the number of points
        k=0:N-1;     %create a vector from 0 to N-1
        T=N/Fs;      %get the frequency interval
        freq=k/T;    %create the frequency range
        X=fft(x)/N; % normalize the data
        % only want the first half of the FFT, since it is redundant
        cutOff = ceil(N/2);

        % take only the first half of the spectrum
        X = X(1:cutOff);
        freq = freq(1:cutOff);
```

```
59          datavec = X(51:50:10001); % 50 hz is the fundamental (bin 50+1) and every 50 hz there are
60
61          THD= sqrt(sum(abs(datavec(2:end).^2)))/abs(datavec(1))
62          thdC(i,j)=THD;
63
64      end
65  end
66
67
68  %thd surface plot
69  figure('Name','THD surf');
70  mesh(Xaxis,Yaxis,thdC)
71  zlabel('T.H.D  [%]','Fontsize',12);
72  ylabel('Reactive Power  [Var]','Fontsize',12);
73  xlabel('Active Power  [Watts]','Fontsize',12);
74  title('Current Total Harmonic Distortion','Fontsize',12);
75
76  %Fsw average surface plot
77  figure('Name','Fsw surf');
78  mesh(Xaxis,Yaxis,Fsw_avg)
79  zlabel('Fsw  [Hz]','Fontsize',12);
80  ylabel('Reactive Power  [Var]','Fontsize',12);
81  xlabel('Active Power  [Watts]','Fontsize',12);
82  title('Average Switching frequency','Fontsize',12);
83
84  % Results fon cocluding table
85
86  FswA = mean(mean(Fsw_avg));
87  str = sprintf('%f Hz Average average switching frequency', FswA);
88  disp(str);
89
90  FswM = mean(mean(Fsw_max));
91  str = sprintf('%f Hz Average MAX switching frequency', FswM);
92  disp(str);
93
94  Fswm = mean(mean(Fsw_min));
95  str = sprintf('%f Hz Average MIN switching frequency', Fswm);
96  disp(str);
97
98  THDavg = mean(mean(thdC))*100;
99  str = sprintf('%f  Average THD', THDavg);
100 disp(str);
```

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