ΕΘΝΙΚΟ ΜΕΤΣΟΒΙΟ ΠΟΛΥΤΕΧΝΕΙΟ

ΣΧΟΛΗ ΗΛΕΚΤΡΟΛΟΓΩΝ ΜΗΧΑΝΙΚΩΝ και ΜΗΧΑΝΙΚΩΝ ΥΠΟΛΟΓΙΣΤΩΝ

ΤΟΜΕΑΣ ΕΠΙΚΟΙΝΩΝΙΩΝ, ΗΛΕΚΤΡΟΝΙΚΗΣ και ΣΥΣΤΗΜΑΤΩΝ ΠΛΗΡΟΦΟΡΙΚΗΣ

Σχεδίαση mmWave Ενισχυτή Ισχύος Αρχιτεκτονικής Doherty σε Τεχνολογία SiGe BiCMOS

ΔΙΠΛΩΜΑΤΙΚΗ ΕΡΓΑΣΙΑ

του

ΙΩΑΝΝΗ ΠΕΠΠΑ

Επιβλέπων: Ιωάννης Παπανάνος
Καθηγητής Ε.Μ.Π.

ΕΡΓΑΣΤΗΡΙΟ ΗΛΕΚΤΡΟΝΙΚΗΣ

Αθήνα, Σεπτέμβριος 2018

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Εγκρίθηκε από την τριμελή εξεταστική επιτροπή την.....

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Ιωάννης Παπανάνος	Γεώργιος Στασινόπουλος	Ευστάθιος Συκάς
Καθηγητής Ε.Μ.Π.	Καθηγητής Ε.Μ.Π.	Καθηγητής Ε.Μ.Π.

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.....

Ιωάννης Πέππας Διπλωματούχος Ηλεκτρολόγος
Μηχανικός και Μηχανικός Υπολογιστών Ε.Μ.Π.

“Fall in love with some activity and do it!

Nobody ever figures out what life is all about, and it doesn't matter.”

Richard P. Feynman

Στους αξιαγάπητους γονείς μου,

Τάσο και Μαριάνθη

Ευχαριστίες

Γρήγορα που πέρασε ο καιρός! Σαν χτες μου φαίνεται ο Φλεβάρης, όταν πρωτοφτάσαμε στο Villach και βρήκαμε τα πάντα στολισμένα κατάλευκα από το χιόνι. Οι εμπειρίες που έζησα στα πλαίσια της εκπόνησης της διπλωματικής μου εργασίας θα μου μείνουν για πάντα αξέχαστες. Το να δουλέψω στην εταιρεία Infineon Technologies ήταν για μένα ένα όνειρο που τελικά βγήκε αληθινό.

Πρώτα από όλους είμαι υποχρεωμένος να ευχαριστήσω τον καθηγητή μου Ιωάννη Παπανάνο για την καθοδήγησή του σε όλο το διάστημα εκπόνησης της διπλωματικής μου εργασίας, καθώς και τη συνεχή ώθηση που μου δίνει. Εκτιμώ απίστευτα την ευκαιρία που μου έδωσε να εργαστώ στο περιβάλλον μιας τόσο μεγάλης και σημαντικής πολυεθνικής, σε ένα χώρο όπου επαγγελματίες μηχανικοί παράγουν ανταγωνιστικά προϊόντα, με κάποιες από τις πιο σύγχρονες και εντυπωσιακές τεχνολογίες.

Θέλω επίσης να ευχαριστήσω όλους τους συνεργάτες μηχανικούς που με βοήθησαν να λύσω τις απορίες μου, με τις συζητήσεις που κάναμε πάνω σε διάφορα τεχνικά ζητήματα. Είμαι ευγνώμων στον Franz Dielacher που μου έδωσε την ευκαιρία να εργαστώ στην ομάδα του. Και ακόμα περισσότερο στους φίλους και συναδέλφους μου Χρήστο Θώμο, Κωσταντίνο Γαλανόπουλο, Simone Scilabra και Μαρία Τζιτζιλάκη για τις όμορφες στιγμές που ζήσαμε μαζί τους τελευταίους μήνες.

Ιδιαίτερα πρέπει να ευχαριστήσω τον φίλο και συμφοιτητή μου Βασίλη Λιακώνη για τη συμπαράσταση και υπομονή που μου έδειξε στο διάστημα των τελευταίων μηνών. Επίσης όλους τους παιδικούς μου φίλους, τον Κώστα, τον Γιάννη, τη Μαρία, τη Θεοδώρα.

Τα ονόματα των ανθρώπων που πρέπει να ευχαριστήσω δεν έχουν τελειωμό, αλλά από όλους τους, πιο πολύ ξεχωρίζουν οι γονείς μου που με απίστευτη δύναμη με στηρίζουν για να στέκομαι εδώ που βρίσκομαι. Δεν υπάρχουν λόγια για να τους εκφράσω την ευγνωμοσύνη που νιώθω.

Σχεδιάγραμμα

Αντικείμενο της διπλωματικής μου εργασίας είναι η σχεδίαση ενός ενισχυτή ισχύος τύπου Doherty με κεντρική συχνότητα λειτουργίας στα 40GHz, χρησιμοποιώντας στάδια ισχύος συνδεσμολογίας κοινής βάσης. Οι εφαρμογές αφορούν τα μελλοντικά προϊόντα της ασύρματης τεχνολογίας 5G.

Στο κεφάλαιο 1 περιγράφεται ο σκοπό της εργασίας, καθώς και η θέση που βρίσκει στα επερχόμενα προϊόντα κινητών επικοινωνιών 5G.

Στο κεφάλαιο 2 γίνεται μια περιληπτική αναφορά στα στοιχεία της κλασικής θεωρίας των ενισχυτών ισχύος που είναι απαραίτητα για την υπόλοιπη εργασία. Γίνεται αναφορά στα βασικά μέρη ενός ενισχυτή ισχύος, στις βασικές παραμέτρους επίδοσης καθώς και στις συνήθεις κλάσεις λειτουργίας. Τέλος, γίνεται μια θεωρητική ανάλυση σχετικά με τη χρήση της συνδεσμολογίας κοινής βάσης ως ενισχυτή ισχύος.

Στο κεφάλαιο 3 γίνεται μια περιληπτική αναφορά στις τεχνικές επαύξησης απόδοσης. Δίνεται περισσότερη έμφαση στις δύο τεχνικές που χρησιμοποιούνται στη συγκεκριμένη εργασία. Όσον αφορά την αρχιτεκτονική Doherty, δίνεται έμφαση τόσο στη θεωρία, όσο και στις μεθόδους υλοποίησης. Η ανόρθωση ρεύματος στο στάδιο κοινής βάσης, που είναι η δεύτερη μέθοδος που χρησιμοποιείται σε αυτή την εργασία, είναι μια καινούργια μέθοδος που ανέκυψε αρκετά πρόσφατα.

Στο κεφάλαιο 4 γίνεται μια σύντομη συζήτηση σχετικά με τις επιδόσεις της τεχνολογίας που χρησιμοποιείται καθώς επίσης και τα μοντέλα που χρησιμοποιεί για τα στοιχεία ο προσομοιωτής.

Στο κεφάλαιο 5 εξηγείται η μέθοδος υλοποίησης του ενισχυτή ισχύος και εξηγούνται τα βήματα με επαρκή λεπτομέρεια.

Στο κεφάλαια 6 και 7 φαίνονται και συζητούνται αποτελέσματα προσομοιώσεων πάνω στην υλοποιημένη αρχιτεκτονική.

Outline

Object of this thesis is the design of a Doherty RF Power Amplifier operating at a center frequency of 40GHz, by utilizing a Common Base configuration for the power stages. The applications that this thesis targets are future products of the fifth generation (5G) of cellular mobile communications.

In chapter 1 the task of this thesis is described, as well as the position that it finds in the upcoming future 5G products.

In chapter 2 a brief reference is made on the elements of the classic RFPA theory that are important for this thesis. A reference is made on the basic building blocks of an RFPA, the basic performance parameters and the usual modes of operation. In the end of the chapter, a theoretical analysis is made on the use of a Common Base configuration as a power amplifier.

In chapter 3 a brief reference is made on back-off efficiency enhancement techniques. Emphasis is given on the two techniques used in this thesis. Concerning the Doherty architecture, the theory of operation, as well as implementation details are described with detail. The Current Clamping in a Common Base Stage is the second technique used and it is a new technique that emerged recently.

In chapter 4 a short discussion is made on the device parameters of the technology that directly affect the design, as well as the device models used by the simulator.

In chapter 5 the implementation method is explained, and the design steps are shown in detail.

In chapters 6&7 the simulation results of the designed architecture are shown and discussed.

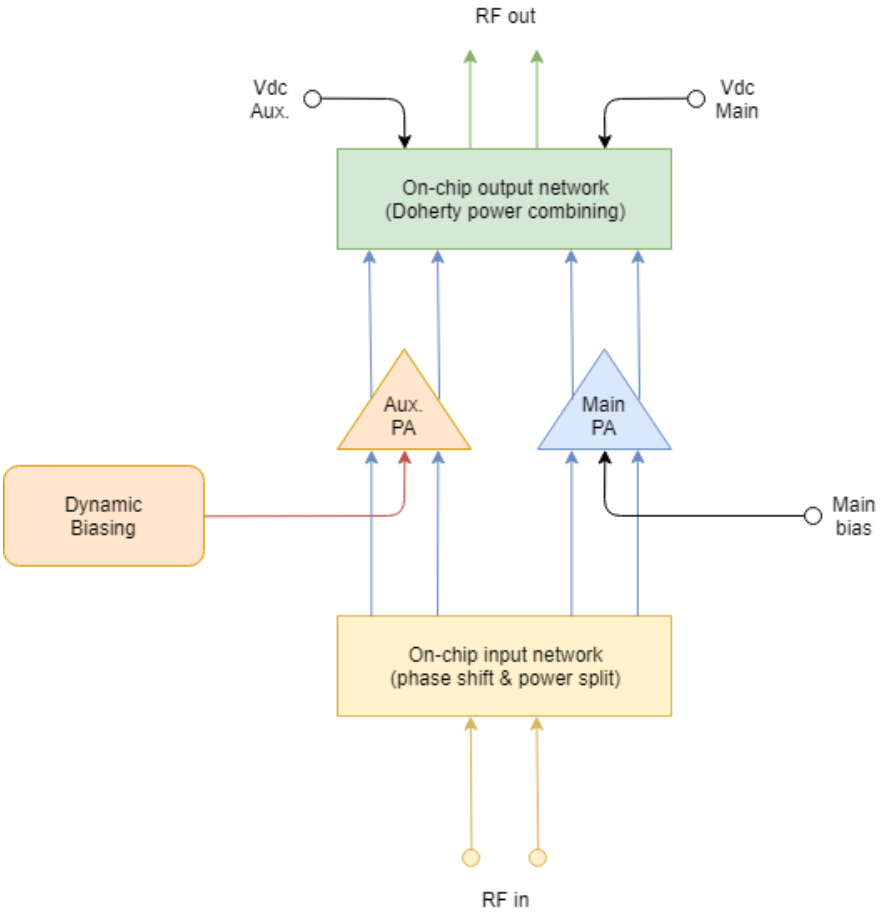
Key words: Power Amplifier, Doherty, Current Clamping, 40GHz, SiGe, BiCMOS

Εκτεταμένη Περίληψη

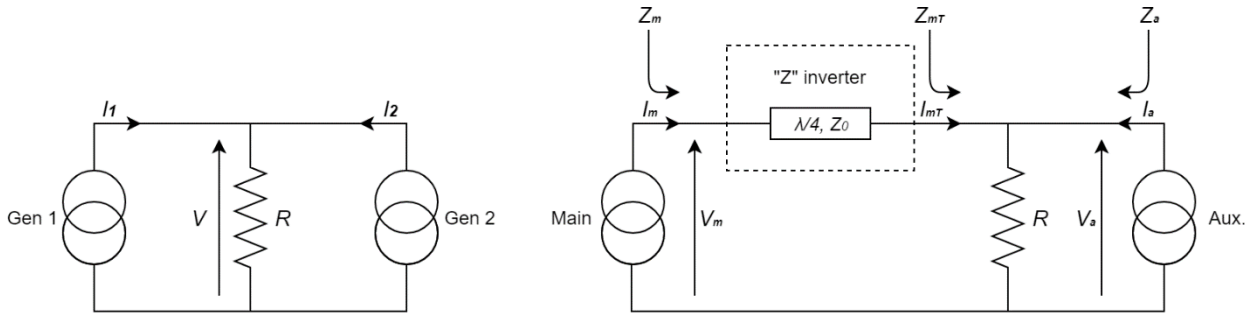
Το κυρίως κείμενο αυτής της διπλωματικής είναι γραμμένο στα αγγλικά. Αυτή η εκτεταμένη περίληψη συμπεριλαμβάνει με συνοπτικό τρόπο τα πιο σημαντικά σημεία της διπλωματικής. Αντικείμενο της διπλωματικής είναι η σχεδίαση ενός ενισχυτή ισχύος τύπου Doherty με κεντρική συχνότητα λειτουργίας τα 40GHz, που στοχεύει σε εφαρμογές κινητών επικοινωνιών πέμπτης γενιάς (5G).

Τα συστήματα mmWave πέμπτης γενιάς (5G) θα χρησιμοποιήσουν αρχιτεκτονικές massive MIMO για να βελτιώσουν τις επιδόσεις των ασυρμάτων ζεύξεών τους. Οι αρχιτεκτονικές αυτές χρησιμοποιούν πολλαπλούς ενισχυτές ισχύος (PAs) με τον κάθε ενισχυτή να λειτουργεί σε μετριάζουσα ισχύ εξόδου. Η ενεργειακή απόδοση των PA είναι αποφασιστικής σημασίας για τη θερμική διαχείριση και την διάρκεια ζωής συσκευών που λειτουργούν με μπαταρία. Εξαιτίας της χρήσης σχημάτων διαμόρφωσης με υψηλό PAPR, όπως υψηλής τάξης QAM και OFDM, τόσο η μέγιστη απόδοση όσο και η απόδοση σε PBO είναι κρίσιμες. Ωστόσο, για να επιτευχθούν Gb/s ρυθμοί μετάδοσης με σύνθετα σχήματα διαμόρφωσης, οι ενισχυτές τύπου EER και ET θα χρειάζονταν διαμόρφωση τροφοδοσίας υψηλής ταχύτητας και ακρίβειας. Από την άλλη, ενισχυτές τύπου LINC σε Gb/s εφαρμογές, απαιτούν για τη λειτουργία τους υπολογισμούς υψηλής ταχύτητας στη βασική ζώνη. Επειδή είναι δύσκολο να κατασκευαστούν αποδοτικοί μετατροπείς ισχύος για διαμόρφωση τροφοδοσίας, ενώ απαιτείται επιπλέον υλικό για υπολογισμούς στη βασική ζώνη, η παρούσα εργασία στρέφεται στην τεχνική Doherty για βελτίωση της ενεργειακής απόδοσης.

Η λειτουργία του DPA μοιράζεται σε δύο “μονοπάτια”, τον Main PA και τον Auxiliary PA. Ο Main PA είναι πολωμένος σαν ένα συνήθη γραμμικό ενισχυτή κλάσης B, ενώ ο Auxiliary PA έχει μια σχετικά πιο πολύπλοκη λειτουργία. Ένα στοιχείο-κλειδί για τη λειτουργία του DPA, είναι το παθητικό δίκτυο εξόδου το οποίο όχι απλώς προσθέτει την ισχύ εξόδου του κάθε μονοπατιού με τις ελάχιστες δυνατές απώλειες, αλλά ταυτόχρονα επιτελεί τη διαμόρφωση φορτίου τύπου Doherty.



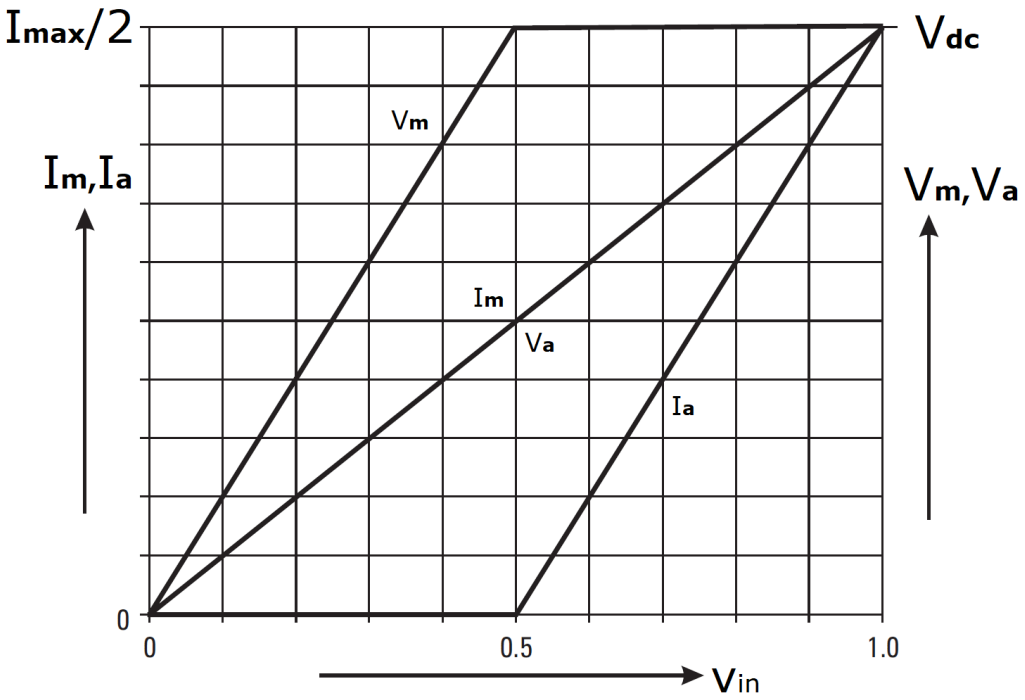
Εικόνα 1 Μπλοκ διάγραμμα της αρχιτεκτονικής Doherty



Εικόνα 2 Αριστερά: Δύο πηγές σήματος μοιράζονται το ίδιο φορτίο (active load-pull)
Δεξιά: δίκτυο εξόδου για διαμόρφωση φορτίου τύπου Doherty

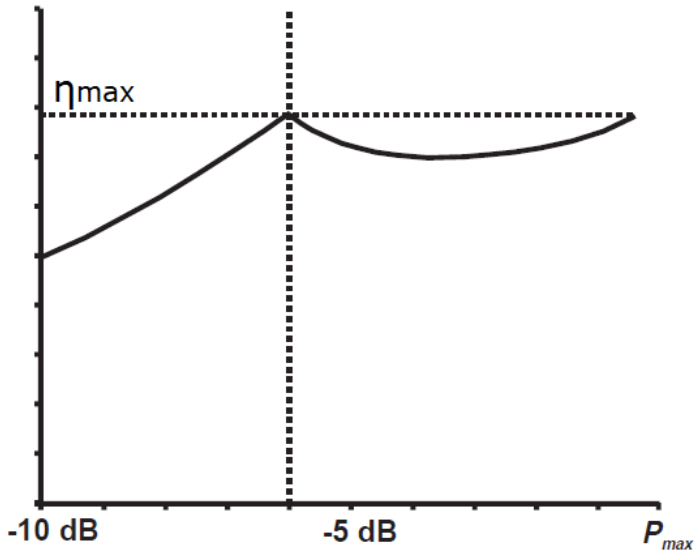
Γενικά, η διαμόρφωση φορτίου μπορεί να παρατηρηθεί όταν δύο (ή περισσότερες) πηγές σήματος μοιράζονται το ίδιο φορτίο R. Για παράδειγμα, αν δύο πηγές παράγουν

ρεύματα ίδιας συχνότητας και φάσης, και με ίδιο πλάτος I_{pk}, τότε το πλάτος της τάσης στα άκρα του φορτίου θα είναι $V_{pk} = 2I_{pk}R$, ώστε κάθε πηγή σήματος βλέπει στην έξοδό της φορτίο $V_{pk}/I_{pk} = 2R$, δηλαδή διπλάσιο φορτίο. Χρησιμοποιώντας επιπλέον έναν αντιστροφέα εμπέδησης στην έξοδο της μιας πηγής, ένας διπλασιασμός του φορτίου για τη μια πηγή μπορεί να φανεί σαν υποδιπλασιασμός φορτίου για την άλλη πηγή. Έτσι λειτουργεί και η διαμόρφωση φορτίου Doherty. Χρησιμοποιείται μία γραμμή μεταφοράς λ/4 σαν αντιστροφέας εμπέδησης και με τη λειτουργία του Auxiliary PA μπορεί να διαμορφώνεται το φορτίο στην έξοδο του Main PA. Έτσι, καθώς αυξάνεται η ισχύς εξόδου του Auxiliary PA, το φορτίο που βλέπει ο Main PA μειώνεται. Πρέπει τέλος να σημειωθεί οτι οι ισχύς από τους δύο ενισχυτές πρέπει να συνδυαστούν ενισχυτικά, οπότε πρέπει τα σήματα εξόδου τους να είναι συμφασικά πάνω στο φορτίο. Επειδή η γραμμή λ/4 προκαλεί διαφορά φάσης 90° στο σήμα του Main PA, χρησιμοποιείται ένα δίκτυο εισόδου το οποίο μοιράζει εξίσου μεταξύ των δύο ενισχυτών το σήμα εισόδου και ταυτόχρονα προκαλεί στην είσοδο του Auxiliary PA διαφορά φάσης 90°.



Εικόνα 3 Φαίνονται τα ρεύματα και οι τάσεις εξόδου των Main & Auxiliary PAs. Ο x-άξονας είναι το νορμαλισμένο σήμα εισόδου V_{in}. Για $V_{in} < 0.5$ φαίνεται η περιοχή χαμηλής ισχύος και για $V_{in} > 0.5$ η περιοχή υψηλής ισχύος. Το σημείο $V_{in} = 0.5$ είναι το σημείο 6dB PBO.

Η λειτουργία του DPA χωρίζεται σε δύο περιοχές ανάλογα με την ισχύ εξόδου, στην περιοχή χαμηλής ισχύος με PBO περισσότερο από 6dB και στην περιοχή υψηλής ισχύος με PBO από 6dB έως 0dB. Στην περιοχή χαμηλής ισχύος εξόδου, ο Main PA λειτουργεί σαν συνήθης γραμμικός ενισχυτής κλάσης B. Ο Auxiliary PA είναι πολωμένος με τέτοιο τρόπο ώστε να μην παράγει ισχύ, οπότε δεν λαμβάνει χώρα διαμόρφωση φορτίου του Main PA. Το φορτίο που βλέπει ο Main PA έχει σταθερή τιμή, τέτοια ώστε στο σημείο 6dB PBO το πλάτος της τάσης εξόδου να μεγιστοποιείται. Έτσι, στο σημείο 6dB PBO ο Main PA μεγιστοποιεί το πλάτος τάσης εξόδου του και κατά συνέπεια την απόδοσή του. Στην περιοχή υψηλής ισχύος, ο Auxiliary PA παράγει ισχύ, ενεργοποιώντας την διαμόρφωση φορτίου Doherty. Καθώς αυξάνεται το σήμα εισόδου, το ρεύμα εξόδου του Main PA αυξάνεται γραμμικά, ενώ το φορτίο μειώνεται με τέτοιο τρόπο ώστε σε όλη την περιοχή υψηλής ισχύος η τάση εξόδου του να μένει σταθερά στο μέγιστο πλάτος. Έτσι, ο Main PA παραμένει σε μέγιστη απόδοση, ενώ ο Auxiliary PA εξαιτίας της κλάσης λειτουργίας του έχει υψηλή απόδοση όταν συνεισφέρει σημαντικό μέρος ισχύος. Επειδή και τα δύο μονοπάτια διατηρούν βελτιωμένη απόδοση, η απόδοση εξόδου του ενισχυτή Doherty είναι σε όλη την περιοχή υψηλής ισχύος αυξημένη. Επιπλέον, καθώς το σήμα εξόδου καθορίζεται από το ρεύμα εξόδου του Main PA, το οποίο διατηρεί γραμμική σχέση με το σήμα εισόδου σε όλες τις περιοχές λειτουργίας, ο DPA είναι θεωρητικά γραμμικός.

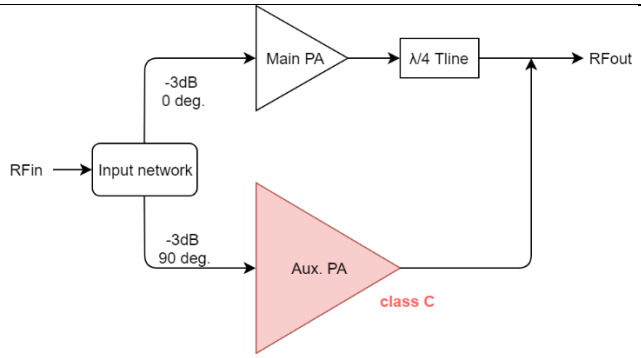
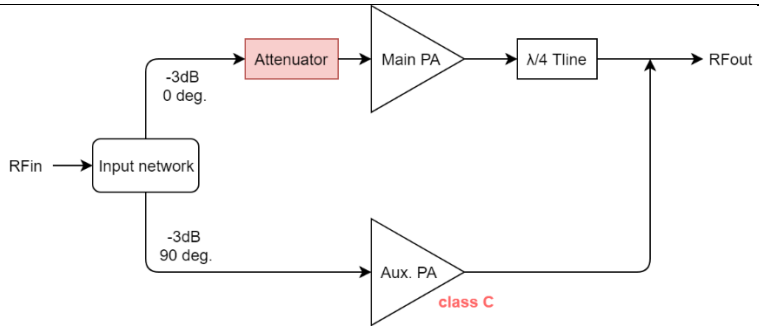
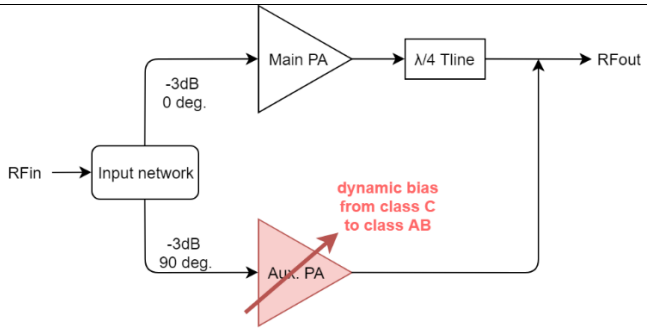


Εικόνα 4 Απόδοση εξόδου του ενισχυτή Doherty

Θεωρητικά, λοιπόν, ο DPA είναι ένας γραμμικός ενισχυτής, με βελτιωμένη απόδοση στην περιοχή από 6dB PBO έως 0dB PBO. Είναι δυνατόν, επίσης, ο DPA να χαρακτηριστεί ως τεχνική γραμμικοποίησης, καθώς η γραμμικότητα του καθορίζεται από τον Main PA που λειτουργεί σε γραμμική κλάση, ενώ ο Auxiliary PA μπορεί να είναι ένας ενισχυτής με σημαντικές μη-γραμμικότητες. Επίσης, ο DPA επιτυγχάνει όλα τα παραπάνω έχοντας μια εξαιρετικά απλή λειτουργία χωρίς εξωτερικό έλεγχο ή εξωτικά στοιχεία. Η πρακτική υλοποίηση του DPA επιφυλάσσει, ωστόσο, σημαντικά εμπόδια.

Το πρώτο σημείο δυσκολίας που συναντάται κατά τη σχεδίαση ενός DPA, είναι η υλοποίηση της συνάρτησης μεταφοράς του Auxiliary PA. Ο Auxiliary PA θα πρέπει να παράγει μηδενικό ρεύμα μέχρι το σημείο 6dB PBO και μετά το σημείο αυτό θα πρέπει να αυξήσει ταχύτατα το ρεύμα του, ώστε στο σημείο 0dB PBO να παράγει τόσο ρεύμα όσο ο Main PA. Στις πρώτες πολύ παλιές υλοποιήσεις με λυχνίες κενού, η διαγωγιμότητα και το μέγιστο ρεύμα εξόδου ήταν εύκολα ελέγξιμες παράμετροι. Η υλοποίηση με σύγχρονα RF transistor είναι μόνο προσεγγιστική και συνήθως επιτυγχάνεται πολώνοντας τις συσκευές του Auxiliary PA σε κλάση C. Ωστόσο, εξαιτίας του χαμηλού κέρδους που χαρακτηρίζει την κλάση C, εάν χρησιμοποιηθούν συσκευές ίδιου μεγέθους για τους Main και Auxiliary PAs, στο σημείο 0dB PBO το ρεύμα εξόδου του Auxiliary PA θα είναι σημαντικά χαμηλότερο από το ρεύμα εξόδου του Main PA. Ένας συνήθης τρόπος αντιμετώπισης είναι να χρησιμοποιηθούν μεγαλύτερες συσκευές για τον Auxiliary PA ώστε να αυξηθεί η διαγωγιμότητα και συνεπώς το κέρδος, ωστόσο αυτό θα έχει συνέπεια το PUF των συσκευών του Auxiliary PA να είναι αρκετά χαμηλό. Επίσης, εάν αυξηθεί το μέγεθος των συσκευών του Auxiliary PA, η εμπέδηση εισόδου του θα μειωθεί και αυτό μπορεί να οδηγήσει σε μείωση του κέρδους του προηγούμενου σταδίου ενίσχυσης. Ένας δεύτερος τρόπος αντιμετώπισης είναι να τοποθετηθεί ένας attenuator στην είσοδο του Main PA, μειώνοντας το κέρδος του και δίνοντας στον Auxiliary PA ένα περιθώριο για να προλάβει να φτάσει το μέγιστο ρεύμα εξόδου του. Ακόμα και αν ξεχαστεί το πρόβλημα του μειωμένου κέρδους που συνεπάγεται η πόλωση του Auxiliary PA σε κλάση C, υπάρχουν επιπλέον προβλήματα που συνδέονται με την τεχνολογία που χρησιμοποιείται σε αυτή τη διπλωματική. Επειδή κατά την πόλωση σε κλάση C η βάση των HBT πολώνεται σε πολύ χαμηλό δυναμικό, η ένωση συλλέκτη-βάσης θα αναγκαστεί να υποστεί τάσεις που

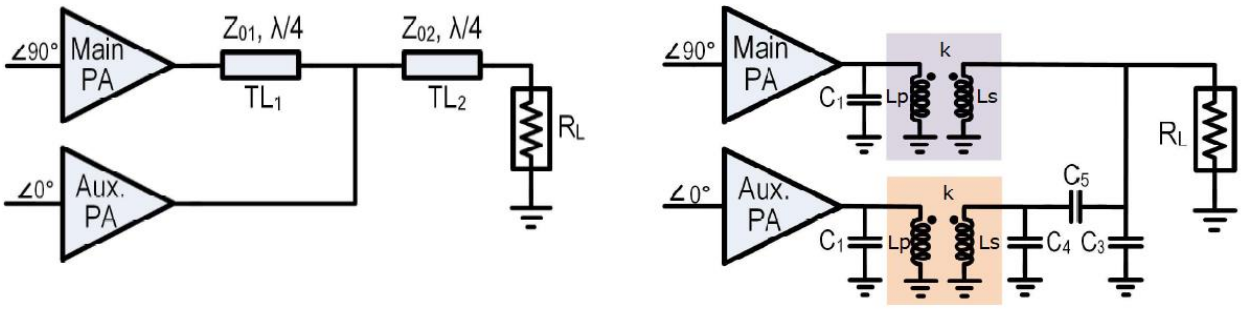
πλησιάζουν επικίνδυνα την τάση διάσπασής της, επομένως είναι ανάγκη να τοποθετηθεί επιπλέον προστασία στην έξοδο του Auxiliary PA, βάζοντας επιπλέον υλικό στο δίκτυο εξόδου και μειώνοντας την παθητική απόδοσή του. Εξαιτίας, της συσσώρευσης πρακτικών προβλημάτων που συνεπάγεται η κλάση C, σε αυτή την εργασία χρησιμοποιήθηκε μια τρίτη εναλλακτική λύση, ο δυναμικός έλεγχος της τάσης πόλωσης, που θα παρουσιαστεί σε λίγο.

Μεθοδολογία	Μπλοκ διάγραμμα	Κέρδος ισχύος	Αξιοπιστία Συσκευών του Auxiliary PA
Αύξηση μεγέθους συσκευών		Χαμηλό (<κλάση AB)	Απαιτείται εξωτερική προστασία
Εισαγωγή Attenuator		Χαμηλό (<κλάση AB)	Απαιτείται εξωτερική προστασία
Δυναμικός έλεγχος της τάσης πόλωσης		Υψηλό (≈κλάση AB)	Δεν απαιτείται εξωτερική προστασία

Πίνακας 1 Μεθοδολογίες υλοποίησης του Auxiliary PA

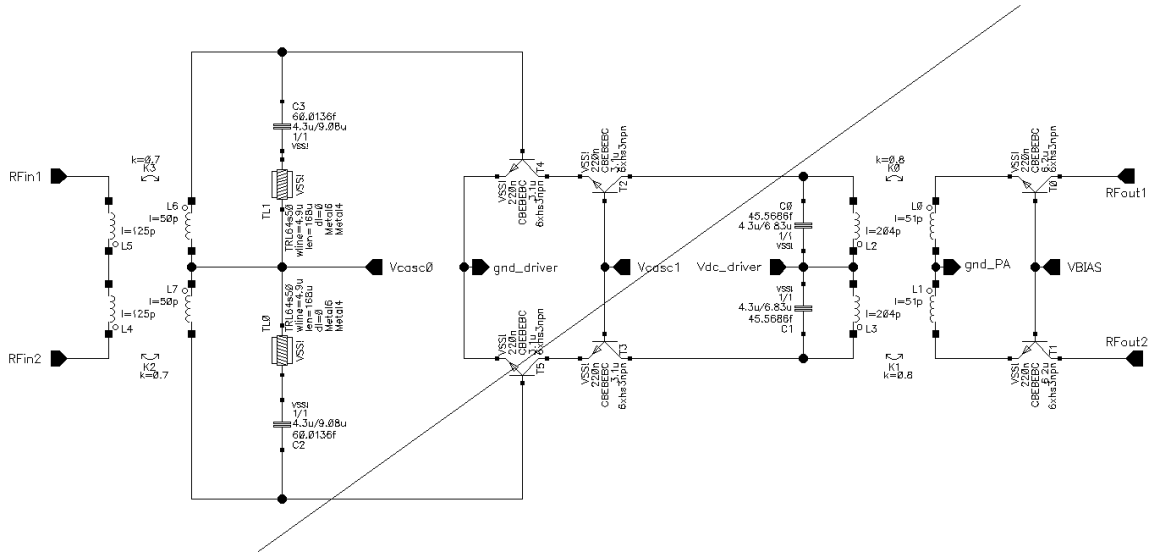
Το δεύτερο σημείο δυσκολίας που συναντάται κατά τη σχεδίαση ενός DPA είναι η κατασκευή του παθητικού δικτύου εξόδου. Το κλασικό δίκτυο εξόδου, όπως συζητήθηκε προηγουμένως, περιλαμβάνει τη γραμμή μεταφοράς λ/4 που επιτελεί το ρόλο του αντιστροφέα εμπέδησης, προσθέτοντας τις ισχύς εξόδου των Main και Auxiliary Pas επάνω σε ένα φορτίο. Το φορτίο αυτό θα έχει μια βέλτιστη τιμή, η οποία καθορίζεται από τους περιορισμούς μέγιστης τάσης και ρεύματος των δύο PAs. Προκειμένου να μετασχηματιστεί το εξωτερικό περιβάλλον των 50Ω στο βέλτιστο φορτίο του DPA, χρησιμοποιείται μια δεύτερη γραμμή μεταφοράς λ/4 με κατάλληλη εμπέδηση.

Το κλασικό δίκτυο εξόδου έχει δύο μειονεκτήματα. Το πρώτο είναι οτι η πρώτη γραμμή μεταφοράς επιτελεί μεγάλους μετασχηματισμούς εμπέδησης (ITRs). Για παράδειγμα, σε όλη την περιοχή χαμηλής ισχύος, το $ITR = 4$. Αποδεικνύεται οτι εξαιτίας του μεγάλου ITR η αρχιτεκτονική Doherty αποκτά το στενό εύρος ζώνης για το οποίο είναι γνωστή. Το δεύτερο μειονέκτημα είναι η χαμηλή απόδοση του παθητικού δικτύου στην περιοχή χαμηλής ισχύος, όπου δουλεύει μόνο ο Main PA. Επειδή η ισχύς του Main PA έχει στο μονοπάτι της και τις δύο γραμμές μεταφοράς, έχει παθητικές απώλειες και από τις δύο, με αποτέλεσμα η συνολική βελτίωση της απόδοσης στο 6dB PBO να είναι περιορισμένη. Προκειμένου να αποφευχθούν τα μειονεκτήματα του κλασικού δικτύου εξόδου, χρησιμοποιήθηκε μια διαφορετική τοπολογία. Στην εργασία [10] εισήχθη μια τροποποιημένη τοπολογία DPA, που μπορεί να λειτουργεί σε δύο κοντινές μπάντες. Με βάση αυτή την εργασία, δημοσιεύτηκε πρόσφατα [6] μια ολοκληρωμένη τοπολογία του τροποποιημένου DPA, βασισμένη στη χρήση δύο μετασχηματιστών και ελάχιστων άλλων παθητικών στοιχείων για το δίκτυο εξόδου. Ο τροποποιημένος DPA πετυχαίνει σημαντική βελτίωση απόδοσης σε σύγκριση με την κλασική υλοποίηση, σε όλες τις περιοχές λειτουργίας. Επιπλέον, πετυχαίνει ένα εντυπωσιακό εύρος ζώνης λειτουργίας. Τέλος, εξαιτίας της χρήσης λίγων παθητικών στοιχείων, το τροποποιημένο δίκτυο εξόδου μπορεί να ολοκληρωθεί σε πολύ μικρό εμβαδόν.



Εικόνα 5 Αριστερά: κλασικό δίκτυο εξόδου Doherty
Δεξιά: υλοποίηση του τροποποιημένου δικτύου εξόδου Doherty με χρήση μετασχηματιστών

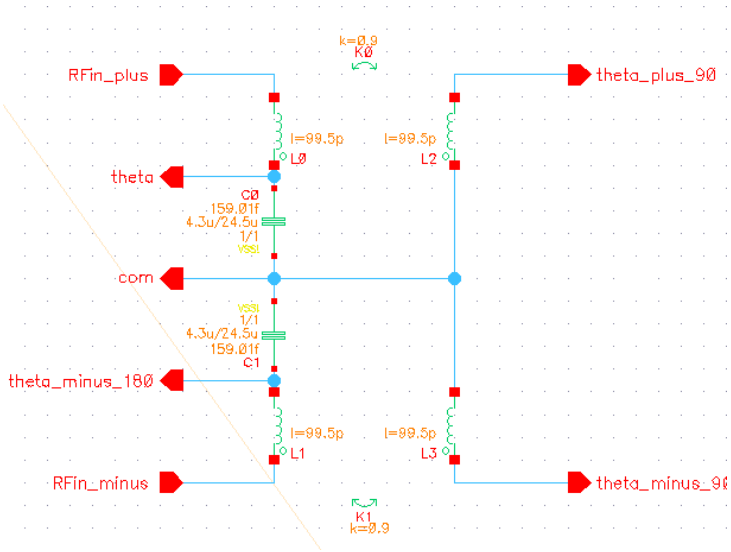
Έχοντας υπόψιν τον τρόπο λειτουργίας του DPA, καθώς και τις δυσκολίες που συναντήθηκαν κατά τη υλοποίησή του, μπορούν να εξηγηθούν τα βήματα που ακολουθήθηκαν κατά τη σχεδίασή του. Πρώτο βήμα αποτελεί η σχεδίαση του Main PA. Συνήθως, για το στάδιο ισχύος χρησιμοποιείται τοπολογία κοινού εκπομπού, αλλά σε αυτή την εργασία χρησιμοποιήθηκε τοπολογία κοινής βάσης, προκειμένου να ερευνηθούν τα πλεονεκτήματά του. Αποδεικνύεται, οτι το στάδιο κοινής βάσης μπορεί να παράγει περισσότερη ισχύ από το στάδιο κοινού εκπομπού και το σημείο συμπίεσης 1dB του κέρδους είναι πολύ κοντά στην ισχύ κορεσμού, παρέχοντας μια πολύ πιο εκτενή γραμμική περιοχή. Επίσης, ένα φαινόμενο που είναι μοναδικό στη συνδεσμολογία κοινής βάσης, γνωστό ως Current Clamping είναι δυνατόν να χρησιμοποιηθεί για βελτίωση της απόδοσης του Main PA [7]. Το μειονέκτημα του σταδίου κοινής βάσης είναι το μικρό κέρδος ισχύος του. Χρησιμοποιήθηκε επίσης push-pull συνδεσμολογία, προκειμένου να εξαλειφθούν οι ζυγές αρμονικές και ταυτόχρονα να αποφευχθούν προβλήματα τύπου common-lead. Το στάδιο ισχύος του Main PA σχεδιάστηκε κατά τα άλλα με συνήθεις τεχνικές σχεδίασης ενισχυτών ισχύος. Το βέλτιστο φορτίο του βρέθηκε χρησιμοποιώντας loadline match αντί για conjugate match. Για την οδήγηση του σταδίου ισχύος χρησιμοποιήθηκε driver με συνδεσμολογία cascode, προκειμένου να ισοφαριστεί το χαμηλό κέρδος του σταδίου κοινής βάσης. Επιπλέον, η υψηλή απομόνωση του σταδίου cascode επέτρεψε να σχεδιαστούν ξεχωριστά το στάδιο ισχύος και το δίκτυο εισόδου του DPA. Για την προσαρμογή του driver και του σταδίου ισχύος χρησιμοποιήθηκε ένας μετασχηματιστής interstage. Ένας ακόμα μετασχηματιστής χρησιμοποιήθηκε για προσαρμογή της εμπέδησης εισόδου του Driver στο περιβάλλον των 50Ω του δικτύου εισόδου.



Εικόνα 6 Σχηματικό του Main PA. Από τα αριστερά προς τα δεξιά φαίνονται, ο μετασχηματιστής για προσαρμογή της εμπέδισης εισόδου στα 50Ω, δύο harmonic traps συντονισμένα στη δεύτερη αρμονική, το κασκοδικό στάδιο του Driver, ο μετασχηματιστής interstage μαζί με δύο πυκνωτές συντονισμού MIM, και το στάδιο ισχύος κοινής βάσης

Για τη σχεδίαση του Auxiliary PA χρησιμοποιήθηκε η τεχνική του Dynamic Biasing. Ανακυκλώθηκε η τοπολογία που σχεδιάστηκε προηγουμένως για τον Main PA και χρησιμοποιήθηκε μια προσαρμοστική μεταβολή της τάσης πόλωσης του σταδίου ισχύος. Με λίγα λόγια, η τάση πόλωσης του σταδίου ισχύος του Auxiliary PA εξαρτάται από το σήμα εισόδου, με τέτοιο τρόπο ώστε να υλοποιείται η συνάρτηση μεταφοράς που πρέπει να έχει ιδανικά ο Auxiliary PA. Στην περιοχή χαμηλής ισχύος, το στάδιο ισχύος του Auxiliary PA έχει μια σταθερή-χαμηλή τάση πόλωσης ώστε να μην παράγει ισχύ. Από το σημείο 6dB PBO και καθώς αυξάνεται το σήμα εισόδου, η τάση πόλωσης αυξάνεται. Στο σημείο 0dB PBO η τάση πόλωσης του Auxiliary PA γίνεται ίση με την τάση πόλωσης του Main PA, οπότε και παράγουν το ίδιο ρεύμα εξόδου. Έτσι, χρησιμοποιώντας την τεχνική του Dynamic Biasing το πρόβλημα υλοποίησης του Auxiliary PA σχεδόν λύνεται αρκετά εύκολα. Φυσικά, η μέθοδος αυτή αφαιρεί από την απλότητα του κλασικού DPA, καθώς απαιτεί ένα εξωτερικό σήμα ελέγχου. Ωστόσο, δεν είναι δύσκολο ένας σύγχρονος πομπός να παράγει ένα σήμα ανάλογο της περιβάλλουσας του σήματος που ”θέλει” να εκπέμψει, το οποίο μπορεί άμεσα να χρησιμοποιηθεί σαν σήμα για τη δυναμική πόλωση για του Auxiliary PA.

Μένουν οι σχεδιάσεις των δικτύων εισόδου και εξόδου. Για το παθητικό δίκτυο εισόδου, σχεδιάστηκε ένα differential quadrature hybrid. Το δίκτυο αυτό ανήκει στη γενικότερη κατηγορία των δικτύων quadrature hybrid, τα οποία λαμβάνουν μια ισχύ εισόδου από ένα port και την ισομοιράζουν μεταξύ δύο ports με διαφορά φάσης 90˚ (μπορούν να χρησιμοποιηθούν και για την αντίστροφη λειτουργία). Το quadrature hybrid που σχεδιάστηκε σε αυτή την εργασία χρειάζεται να είναι διαφορικό, δηλαδή να παράγει όχι δύο αλλά τέσσερις φάσεις, επειδή η τοπολογία των ενισχυτών είναι επίσης διαφορική (push-pull). Η σχεδίαση του δικτύου βρίσκεται συνοπτικά στην παράγραφο 5.2 και βασίζεται στην εργασία [8]. Τέλος, για το δίκτυο εξόδου χρησιμοποιήθηκε η τροποποιημένη τοπολογία δικτύου εξόδου Doherty που φαίνεται στην Εικόνα 5. Οι υπολογισμοί για τη σχεδίαση του δικτύου εξόδου βρίσκονται αναλυτικά στην παράγραφο 5.3.2 αυτής της εργασίας.



Εικόνα 7 Το διαφορικό υβριδικό δίκτυο εισόδου

Λεξιλόγιο Περίληψης

Auxiliary PA	Ο βοηθητικός ενισχυτής ισχύος που αποτελεί ένα από τα δύο "μονοπάτια" του DPA.
Current Clamping	Μέθοδος ανόρθωσης ρεύματος, παρόμοια με τη γνωστή μέθοδο ανόρθωσης τάσης, χρησιμοποιώντας μια δίοδο και έναν πυκνωτή. Χρησιμοποιείται σε στάδια ισχύος κοινής βάσης για τη βελτίωση της απόδοσης σε PBO [7].
Common lead effects	Φαινόμενα εξαιτίας της σύνδεσης των τρανζίστορ σε πηγές τροφοδοσίας, πόλωσης ή τη γείωση, μέσω κάποιου σύρματος το οποίο χαρακτηρίζεται από κάποια παρασιτική αυτεπαγωγή. Η συνδεσμολογία push-pull, εξαιτίας της διαφορικής λειτουργίας της, είναι απαλλαγμένη από τέτοιου είδους προβλήματα.
Conjugate match	Από απλή θεωρία κυκλωμάτων προκύπτει ότι για βέλτιστη μεταφορά ισχύος από μια πηγή πεπερασμένης εμπέδησης σε ένα φορτίο, το φορτίο θα πρέπει να έχει εμπέδηση ίση με τη συζυγή τιμή της εμπέδησης πηγής.
Cascode	Κασκοδική συνδεσμολογία δύο τρανζίστορ
DPA	Συντομογραφία για Doherty Power Amplifier
Driver	Το κύκλωμα ενισχυτή που παράγει την ισχύ εισόδου για να οδηγηθεί ένα στάδιο ισχύος.
Dynamic biasing	Μέθοδος δυναμικής πόλωσης των τρανζίστορ. Μπορεί να χρησιμοποιηθεί για διαφορετικούς σκοπούς, αλλά σε αυτή την εργασία χρησιμοποιήθηκε για την υλοποίηση του Auxiliary PA.
EER	Συντομογραφία για Envelope Elimination and Restoration που είναι μια από τις πολύ γνωστές μεθόδους βελτίωσης της απόδοσης σε PBO αλλά και γραμμικοποίησης.
ET	Συντομογραφία για Envelope Tracking. Βασίζεται στην ιδέα του EER, αλλά είναι μια τελείως διαφορετική τεχνική βελτίωσης της απόδοσης σε PBO.
HBT	Συντομογραφία για Heterojunction Bipolar Transistor, η κατηγορία ενεργών συσκευών που χρησιμοποιούνται σε αυτή την εργασία.
ITR	Συντομογραφία για Impedance Transformation Ratio. Οι γραμμές μεταφοράς λ/4 συχνά χρησιμοποιούνται για το μετασχηματισμό εμπέδησης. Ο λόγος των εμπεδήσεων που βλέπουν στα άκρα τους είναι το ITR.
Interstage	Σημαίνει "ενδιάμεσα σε στάδια" και χαρακτηρίζει το μετασχηματιστή μεταξύ των σταδίων driver και ισχύος, που χρησιμοποιείται για την προσαρμογή τους.
Loadline match	Η προσαρμογή αυτή λαμβάνει υπόψιν τους περιορισμούς ενός τρανζίστορ για την τάση και το ρεύμα εξόδου, ώστε να παραχθεί η μέγιστη δυνατή ισχύς εξόδου.
LINC	Συντομογραφία για Linear amplification by Non-linear Components. Είναι μια από τις πολύ γνωστές μεθόδους βελτίωσης της απόδοσης σε PBO αλλά και γραμμικοποίησης.

mmWave	Κατηγορία εφαρμογών με συχνότητες λειτουργίας μεταξύ 30GHz και 300GHz.
massive MIMO	Ο όρος MIMO αναφέρεται στη χρήση πολλαπλών κεραιών εκπομπής και λήψης για την αύξηση της χωρητικότητας μιας ασύρματης ζεύξης. Η τεχνολογία massive MIMO στηρίζεται σε αυτή την ιδέα, χρησιμοποιώντας μεγάλες συστοιχίες από κεραίες για την ταυτόχρονη εξυπηρέτηση πολλαπλών αυτόνομων τερματικών.
Main PA	Ο κύριος ενισχυτής ισχύος, ένα από τα δύο “μονοπάτια” του DPA.
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier, ενισχυτής ισχύος
PAPR	Peak to Average Power Ratio λόγος της μέγιστης προς τη μέση ισχύ
PBO	Power Back-Off υποχώρηση από την ισχύ κορεσμού της στιγμιαίας τιμής της ισχύος εξόδου.
Push-pull	Συνδεσμολογία που χρησιμοποιεί ένα ζευγάρι από τρανζίστορ, τα οποία εναλλάξ παρέχουν ρεύμα, ή απορροφούν ρεύμα από ένα φορτίο.
QAM	Quadrature Amplitude Modulation γνωστή μέθοδος ψηφιακής διαμόρφωσης.

Table of Contents

1 Introduction

The design and measurements of a Power Amplifier with a Common Base power stage is presented in order to investigate the advantages and drawbacks of that configuration. The designed Power Amplifier is then used as a building block for the design of a Doherty architecture to demonstrate the effectiveness of the Doherty technique in mmWave applications.

1.1 Motivation

Worldwide commercial launch of 5G is on the horizon and the first phase of 5G specifications has already started, with the ITU IMT-2020 standard and the more recent 3GPP Release 15 standard. Early roll-outs of 5G in Europe and Asia will likely use sub-6GHz bands, while in the USA operators will mainly start with high bands (above 24GHz) for 5G and reuse some 4G low bands. In the IMT-2020 the peak & user experienced data rate, area traffic capacity, latency, spectrum efficiency and network energy efficiency are specified as key capabilities of high importance. For the first three, the use of the high bands is a necessity, however due to spectrum efficient modulations, with high peak-to average power ratios, both PA (power amplifier) peak efficiency and power back-off efficiency are critical. To achieve Gb/s data rates, Envelope Tracking requires high speed supply modulators and Outphasing requires high-speed baseband overhead for computation, both of which are difficult to implement in practice. Until recently DPAs (Doherty power amplifiers) suffered from limited PBO (power back-off) efficiency enhancement and narrow bandwidths of operation. However recent work [6] has resolved both issues, achieving a very impressive -1dB bandwidth of operation covering the entire 28-to-42 GHz (40%) band.

1.2 Task Description

The objective of this project is to design a DPA and demonstrate back-off efficiency enhancement due to the Doherty operation. Given the increasing interest for 5G applications in the 40GHz band, it was decided that the operation of the DPA must be centered at 40GHz. There are no specific design goals concerning the bandwidth or the linearity of the DPA, however care was taken during the design, so that the operation stays within reasonable limits for the target application. Given that 5G applications will extensively exploit MIMO structures, using multiple PAs with moderate power capabilities for each element, the power capabilities of each individual PA can be moderate. In this thesis the saturation power was chosen to be over 20dBm.

There were no readily available PAs to use for the main and auxiliary PAs, centered at or close to the intended frequency of operation. As a result, a major part of this project is dedicated to the development of those two PAs using a SiGe BiCMOS technology which was made available thanks to Infineon Technologies. A stumbling block during the design was the implementation of the auxiliary amplifier. It was decided to develop the power stages of both PAs using a Common-Base configuration, since it offers certain advantages in back-off efficiency according to recent work [7].

Finally, due to the work needed in order to develop the two PAs, as well as develop and demonstrate the operation of the full Doherty architecture there was no time to develop and simulate the inductors and transformers using an EM simulator. Models with realistic parameters (inductance, quality factor and coupling factor), in relation to the operating frequency, are used instead.

2 Power Amplifier in Theory

This chapter is intended to be an introduction into the theory of RF power amplifier design. It discusses a linear RF amplifier in theory, a conceptual structure of a generic power amplifier, definitions of the key figures, usual modes of power amplifier operation and a short investigation on the advantages and drawbacks of a Common Base power stage.

2.1 Linear RF amplifiers in theory

In RF design, it is difficult to employ traditional methods for network parameters such as Y-, Z-, H- and G-parameters, because they require open-circuit or short-circuit conditions for their measurement, which are difficult to realize in RF and mmWave frequencies. To face these challenges, RF designers use S-parameters, which are measured under controlled finite impedance conditions. Using S-parameters, the basic results of matched two-port linear RF amplifiers were first derived over 50 years ago. The key results can be illustrated by examining the schematic in Figure 2.1.

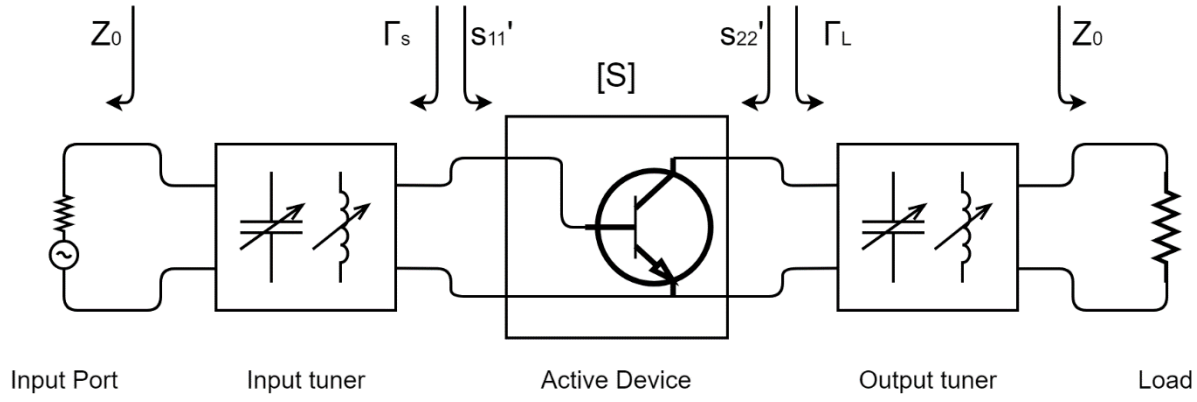


Figure 2.1 Schematic for 2-port gain and stability analysis

An active device is represented as a two-port S-parameter matrix. The input and output impedances (or equivalently reflection coefficients) presented to the transistor can be adjusted using conceptual tuning devices. Since these tuners are realized using passive

circuitry, the reflection coefficients Γ_S and Γ_L at the input and output device reference planes are restricted to the range of $0<|\Gamma_{S,L}|<1$ in magnitude.

Much of the complexity of the behavior of the system in Figure 2.1 is due to the relative magnitude of the product $s_{12}.s_{21}$. The key equations are quite straightforward and represent the change in the input reflection from s_{11} to s_{11}', due to the output plane being presented with the output load reflection Γ_L:

Input Match:

$$s_{11}' = s_{11} + \frac{s_{21}.s_{12}.\Gamma_L}{1 - s_{22}.\Gamma_L} \tag{2.1}$$

Output Match:

$$s_{22}' = s_{22} + \frac{s_{21}.s_{12}.\Gamma_s}{1 - s_{11}.\Gamma_s} \tag{2.2}$$

And for a conjugate match:

$$s_{11}' = \Gamma_s^*, \qquad s_{22}' = \Gamma_L^* \tag{2.3}$$

Inserting (2.3) in (2.1), (2.2) gives two equations which can be solved for Γ_s and Γ_L. And in general, this solution exists, however an additional constraint must be put for the magnitudes of Γ_s and Γ_L in order to ensure the stability of the two-port amplifier and this constraint is Rollett's Stability Factor or k-factor. The k-factor is calculated as follows:

$$k = \frac{1 + |s_{11}.s_{22} - s_{21}.s_{12}|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{11}||s_{22}|} \tag{2.4}$$

The simple k>1 rule is undoubtedly a good guideline to follow, since it is a necessary condition for stability at a given frequency for a two-port device. There are also other measures for the stability of a two-port amplifier such as the B1-factor, stability circles and others.

2.2 Diagram of a single stage power amplifier

A very simplified diagram of a single stage PA can be seen in Figure 2.2. It is very similar to Figure 2.1. An active device is used as the amplifying element with two ports, input and output. A passive network is connected to each port, a passive input network and a passive output network.

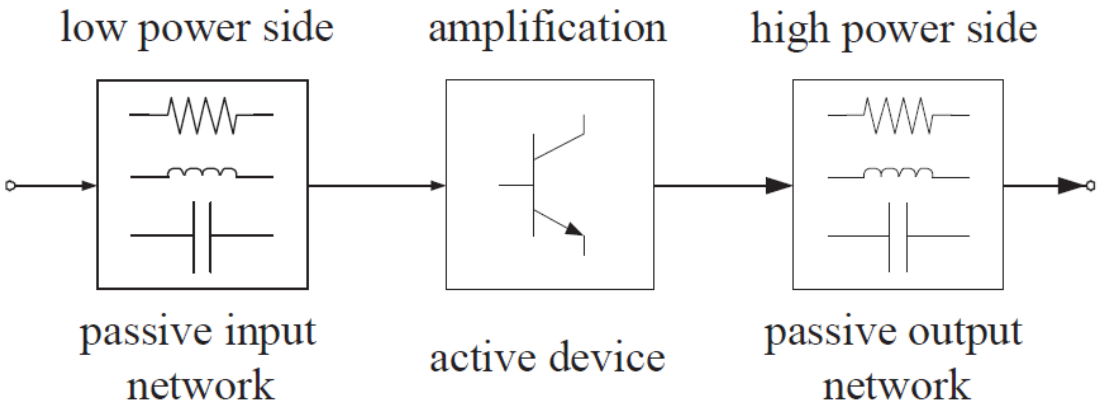


Figure 2.2 Very simplified diagram of a single-stage power amplifier

2.2.1 Active device

The active device is the workhorse of a power amplifier, being the component that performs the amplification of the input signal. In a general sense, it converts power provided by a DC source into RF power, so that the output signal is essentially a higher power version of the input signal. Typical examples of active devices used in RF power amplifiers are BJTs, MOSFETs, HEMTs and HBTs. The choice of device for an application is based on criteria such as operating frequency, maximum output power and cost.

The active devices used for the design in this thesis consist of arrays of HBTs connected in parallel. In particular, the HBTs used are devices of the B11HFC 130nm SiGe BiCMOS technology. Although the active devices are the heart of the power amplifier, they are not the main concern of this thesis, as the designer is given freedom to affect only few of their parameters.

2.2.2 Passive network

The engineering of the input and output passive networks is the essential part of the PA design. Their function includes:

Matching: The impedance levels at the ports of the active device, must be transformed to a desired interface level, e.g. 50 Ω.

Filtering: The out-of-band spectrum components must be filtered in both directions.

Waveform shaping: The impedances the passive networks present to the active device, partake in the shaping of the current and voltage waveforms, allowing a particular mode of operation.

Biasing: The biasing of the active device determines together with the wave shaping the class of operation and therefore figures as linearity, efficiency and gain.

Stability: The passive network must ensure and maintain stability of the amplifier, usually for defined load and source impedances. For a single-stage two-port power amplifier, potential instability is caused when the terminating impedance on one side of the device, can be transformed through the device so that the device presents negative impedance at the other port. This can often happen on either or both ports. Typically, the situation does not happen across all frequencies and often it does not happen in the design band of interest.

2.3 Definitions of the figures of interest

2.3.1 Gain, Power and Efficiency

The illustration in Figure 2.3 shows a PA connected to a signal source, a power supply, a bias supply and an RF load. The Gain of the amplifier is simply defined as the amplification of the available power P_{avs} at the input port to the power P_{del} delivered to the load resistance R_{load}. P_{del} is calculated by the fundamental components of the load current I_{load} and load voltage V_{load} as shown below.

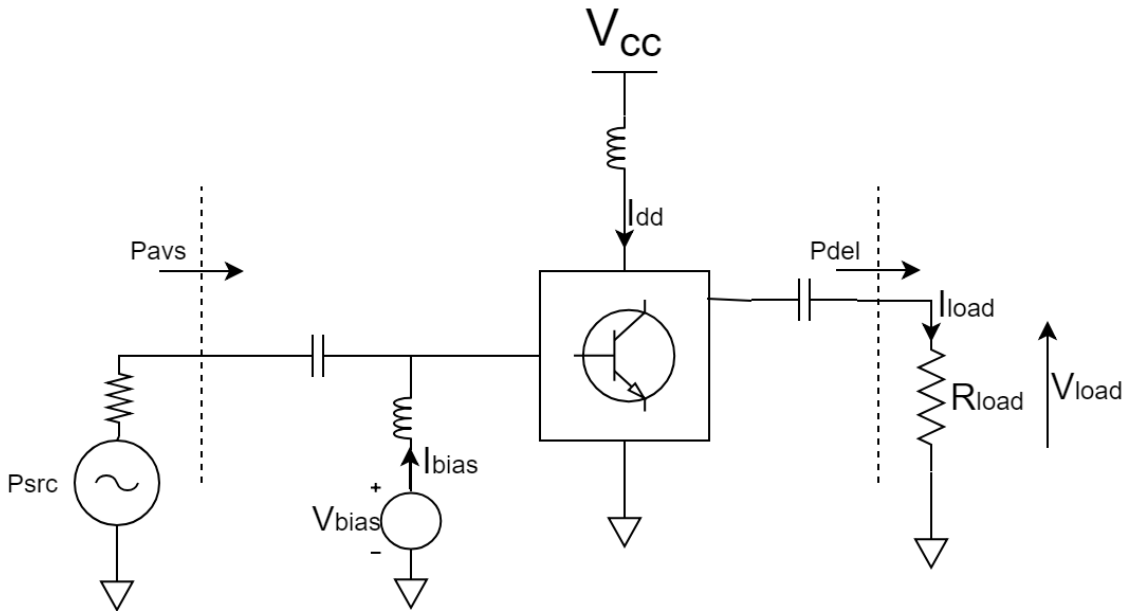


Figure 2.3 PA schematic

$$G = \frac{P_{del}}{P_{avs}} \tag{2.5}$$

$$P_{del} = \frac{1}{2} real(V_{load}.I_{load}^{*})|_{f=f_0} \tag{2.6}$$

The dissipated dc power consists of two contributions, one being the power supply (V_{dd} times I_{dd}), and the other being the (less significant) bias voltage source (V_{bias} times I_{bias}).

$$P_{dc} = V_{bias}.I_{bias} + V_{cc}.I_{cc} \tag{2.7}$$

An important thing to spend time on in a power amplifier design, is achieving a good efficiency η, i.e. the ratio between the delivered power at the fundamental frequency and the dissipated dc power. Furthermore, taking into account the amplification capability of the amplifier, the power added efficiency (PAE) can be defined:

$$\eta = \frac{P_{del}}{P_{dc}} \tag{2.8}$$

$$PAE = 100\% \frac{P_{del} - P_{avs}}{P_{dc}} = 100\%.\eta.\left(1 - \frac{1}{G}\right) \tag{2.9}$$

2.3.2 Linearity

A first way to describe linearity is defined in a straight forward manner, as the derivative G'' of the gain G where perfect linearity stands for zero. If G' at higher power levels starts to deviate from zero, compression ($G'<0$) or expansion ($G'>0$) occurs. However, this definition is a pure amplitude to amplitude analysis at the design frequency and does not take into account anything like bandwidth or phase shift. Later in this thesis, the bias point that creates a maximally flat gain is found.

$$G' = \frac{dG}{dP_{in}} \tag{2.10}$$

Another, widely prevalent definition is based on a two-tone signal analysis. Two sine signals (f_1 and f_2) separated by a very small frequency offset ($f_2 - f_1 \ll f_{1,2}$) and amplified by a nonlinear amplifier produce frequency components lying very close to the signal frequencies. These components are caused by third and fifth order term of the (nonlinear) transfer function and are called *third* and *fifth order intermodulation products* (IM3 resp. IM5). The telecom industry is highly interested in keeping them as low as possible since for a modulation incorporating frequency multiplexing, the intermodulation products fall into the neighboring channels. The IM3 suppression (IM3S) is now the ratio between the two-tone powers and the power of the intermodulation products. All powers in the equation below are referred to the output:

$$IM3S = \frac{P_{f_1} + P_{f_2}}{P_{2f_1-f_2} + P_{2f_2-f_1}} \tag{2.11}$$

2.4 Different modes of operation

A short summary of the classic modes of amplifier operation are presented and the important tradeoffs are pointed out. Detailed treatment of the topic can be found in [1]. In general, a distinction is made between two major types of power amplifiers: transconductor type amplifiers (Classes A, AB, B and C) and switching type amplifiers (Classes D, E and F).

2.4.1 Class A

The Class-A amplifier is often described as "Linear" or as the bias point at which the amplifier works linearly. However, a Class-A power amplifier does not always have to work linearly, and highly linear amplifiers can also be designed using other modes of operation. In a classical manner, the Class-A operation point is defined as the bias condition at which the quiescent current of the device is half of its maximum current.

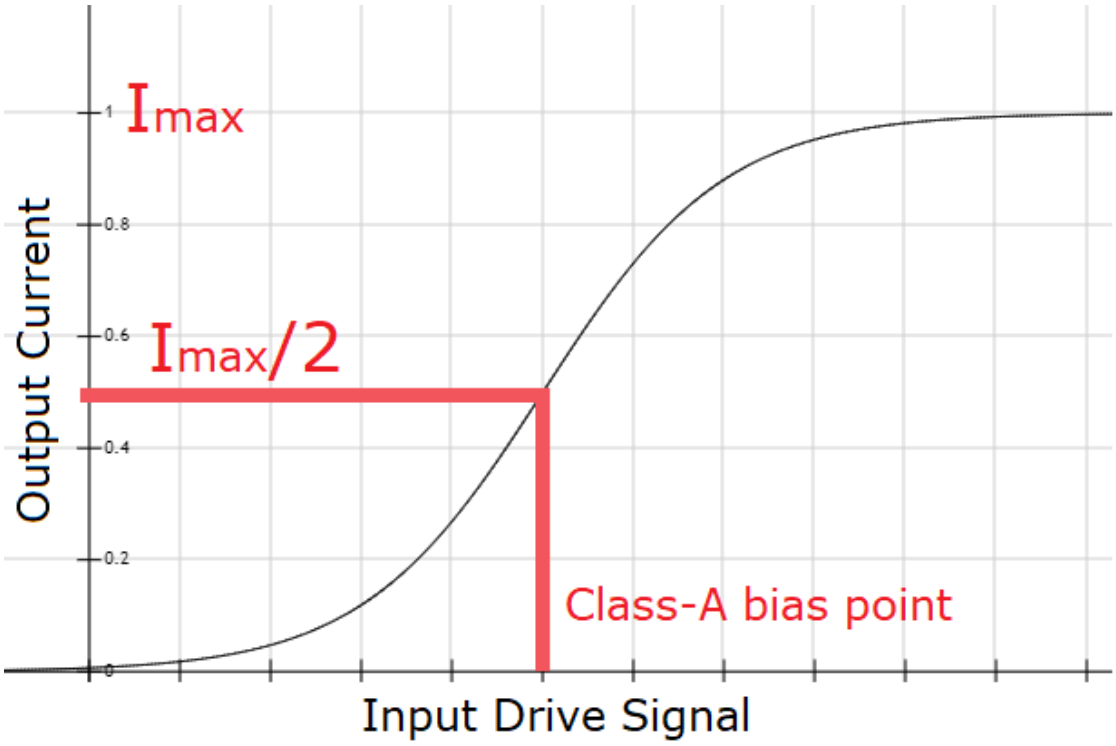


Figure 2.4 The class A bias point on the transfer characteristic of an active device

If the RF input drive signal is sinusoidal and small enough, then the output current will also be sinusoidal with insignificant harmonic content, while as the input signal increases, weak nonlinearities will appear at the output current. It is however necessary to swing the device through the increasingly nonlinear parts of the transfer characteristic in

order to reach the hard-clipping limits. In this case, the output current will have significant harmonic content. The signal level must not exceed these two limits in order to avoid clipping. In general, however, one can expect greater linearity from a Class-A than a Class-AB amplifier.

The act of setting an amplifier at a Class-A bias point has the advantage that the design can be reduced to a linear design problem. The input matching network can be simply designed using s-parameter methods and the output matching network can be designed using loadline techniques. However, the major drawbacks of the Class-A amplifier cannot be ignored. First of all, by setting the bias point exactly in the middle of the linear region, the theoretical maximum efficiency is limited to 50%. What is more, even at standby the amplifier dissipates the same dc power. As a result, at back off powers the efficiency of the Class-A will drop very fast:

$$\eta = \frac{I_1^2}{I_{1\,max}^2} * 50\% \qquad (2.12)$$

where I_1 is the amplitude of the sinusoidal output current.

This means that at the 6dB power back-off point the theoretical maximum efficiency will be an alarming 12.5%. Power wasted in such a manner causes two problems. First, in battery-operated equipment, it has a severe impact on the battery life time and should therefore be avoided. Second, the power wasted in the circuit will be dissipated in the active devices, increasing their operating temperature and increasing their failure rate. The modes of operation presented later on will sacrifice the linearity of the Class-A mode in favor of efficiency.

2.4.2 Reduced conduction angle modes

The conduction angle is defined as the part of a period during which current is flowing through the transistor. For Class A, the conduction angle is 2π since the transistor is switched on during the whole period of a sine wave. By lowering the bias point, the swing of the input signal brings the input voltage temporarily below the cut off voltage, the transistor switches off for a part of the period and the conduction angle is reduced consequently. It is also necessary to increase the input drive level and to provide suitable impedance terminations

at the harmonics of the signal frequency. Increasing the input level by maintaining the output level signifies lower gain.

The dc current component will of course decrease as the conduction angle is reduced, resulting in higher efficiency. However, it is less obvious what happens to the fundamental component; furthermore, harmonics will be generated. A Fourier analysis of the current waveforms is done in [1]. The magnitude of the nth harmonic is

$$I_n = \frac{1}{\pi}\int_{-\frac{a}{2}}^{\frac{a}{2}} \frac{I_{max}}{1-\cos\left(\frac{a}{2}\right)}\left[\cos(\theta)-\cos\left(\frac{\alpha}{2}\right)\right]\cos(n\theta)\,d\theta \tag{2.13}$$

The fundamental term is given for $n = 1$.

The mean current, or DC component, is given by:

$$I_{dc} = \frac{1}{2\pi}\int_{-\frac{a}{2}}^{\frac{a}{2}} \frac{I_{max}}{1-\cos\left(\frac{a}{2}\right)}\left[\cos(\theta)-\cos\left(\frac{\alpha}{2}\right)\right]d\theta \tag{2.14}$$

The Fourier components of the emitter versus a sweep over the conduction angle is plotted in [1].

$$I_{dc} = \frac{I_{max}}{2\pi}\frac{2\sin\left(\frac{a}{2}\right)-a\cos\left(\frac{a}{2}\right)}{1-\cos\left(\frac{a}{2}\right)} \tag{2.15}$$

$$I_1 = \frac{I_{max}}{2\pi}\frac{a-\sin(a)}{1-\cos\left(\frac{a}{2}\right)} \tag{2.16}$$

$$I_{n\geq 2} = \frac{2I_{max}}{\pi}\frac{\frac{\left[\cos\left(\frac{a}{2}\right)\sin\left(\frac{na}{2}\right)\right]}{n}-\left[\cos\left(\frac{na}{2}\right)\sin\left(\frac{a}{2}\right)\right]}{(n-1)(n+1)\left(1-\cos\left(\frac{a}{2}\right)\right)} \tag{2.17}$$

All harmonics of the output current are assumed to be shorted and generate no voltage, so the collector emitter voltage is a pure sine wave whose magnitude will be set by the load resistor value to generate the maximum permissible voltage swing, in a fashion similar to the previous consideration of a Class A amplifier. The output signal power and the

dissipated dc power are therefore calculated by the following equations, the efficiency η and the PAE are given by equations (2.8) and (2.9). The RF output power and the efficiency versus a sweep over the conduction angle are shown in [1].

$$P_1 = \frac{V_{dc}}{\sqrt{2}} \frac{I_1}{\sqrt{2}} \tag{2.18}$$

$$P_{dc} = V_{dc} I_{dc} \tag{2.19}$$

2.4.2.1 Class B and AB

For class B, the bias voltage is set close to the cut off voltage, resulting in a conduction angle of half the period and an output current waveform that resembles a half-way rectified sinusoid. An exact 50% conduction angle is a mathematical point, of course, so true class B amplifiers do not actually exist. Class B amplifiers are usually built in a push-pull (differential) configuration of two transistors, since by using that configuration, the even harmonics cancel out from the output current. In contrast to the class-A mode, much less current flows at zero input signal. The maximum theoretical efficiency is 78.5%. A very important advantage of the Class B amplifier is the much improved efficiency at back off powers:

$$\eta = 78.5\% \frac{I_1}{I_{1\,max}} \tag{2.20}$$

This means that at the 6dB power back off point the output efficiency will be 39.3%. For the ideal case, all odd current harmonics are zero, so shorts have to be provided only for the even harmonics. A small bias adjustment around the Class B point can be considered to be a viable method of controlling the precise level of the third harmonic component. This results in a good linearity as no odd order intermodulation products appear (IM3 and IM5). Notice that the fundamental current has the same magnitude as the Class A.

A conduction angle somewhere between 50% and 100% is typical for class AB being the mode for most practical power amplifier implementations with high linearity requirement.

2.4.2.2 Class C

If the bias is arranged to cause the transistor to conduct for even less than half the period, Class C operation is obtained. For a conduction angle shrinking towards zero, the efficiency can approach 100%. An easy and hence popular way is to connect the base to ground resulting in zero bias current. Large efficiency can be achieved at the cost of reduced power-handling capability, gain and linearity.

2.5 Conjugate match vs loadline match

Conjugate match is often used in RF design to obtain maximum power transfer from a source with finite impedance to a load. However, the conjugate match does not take into consideration the factors that limit the power performance of a device. In order to achieve maximum output power, it is necessary to reach maximum voltage and current amplitude at the same time. This is why in RF power amplifier design, the output network does not perform a conjugate match but a power match. This means that the output of the amplifier is presented with the optimal impedance R_{opt} at which it produces its maximum power.

A usual tactic to find the optimal impedance is by performing a load-pull measurement at several points of compression. However, it is possible to predict the optimal impedance. For this, it is important to consider the point at which the device produces its maximum power. At the point of maximum power, both the voltage and the current will swing over their full range. Then the fundamental voltage will have an amplitude of $V_{1,max}$ and the fundamental current, an amplitude of $I_{1,max}$. For this to happen the optimal impedance must obviously be:

$$R_{opt} = \frac{V_{1,max}}{I_{1,max}} \tag{2.21}$$

For example, in a Class A or Class B the maximum voltage amplitude will be V_{dc} (equal to the supply voltage) and the fundamental current amplitude will be $\frac{I_{max}}{2}$. As a result, the optimal load will be:

$$R_{opt} = \frac{2V_{dc}}{I_{max}} \tag{2.22}$$

A small correction can be made in the above equation in order to compensate for the knee voltage V_{knee} of the device:

$$R_{opt} = \frac{2(V_{dc} - V_{knee})}{I_{max}} \tag{2.23}$$

As a final note, at the output of the device there might exist parasitic capacitance, extra capacitance placed on purpose, or both. This extra capacitive reactance exists in parallel with the optimal impedance and will transform it. For this purpose, some added inductive reactance will be needed to cancel out the capacitive reactance, so that the device will see on its output only the optimal impedance calculated above. However, this enters the discussion about output network design and is beyond the scope of this paragraph. An extended analysis can be found in [1].

2.6 A power stage with a Common Base configuration

Usually RF engineers prefer the common-emitter configuration when designing power amplifiers. However, the common-base configuration has some significant advantages to offer in comparison. For example, devices of a specific size can, from a theoretical perspective, produce more power in a C.B. (common-base) configuration rather than in a C.E. (common-emitter). This and other advantages of the C.B. stage in a power amplifier are investigated below.

2.6.1 Increased output power and efficiency

By simply connecting the same device in a C.E. and then a C.B. configuration, and the running some DC simulations an important advantage of the C.B. stage can be revealed.

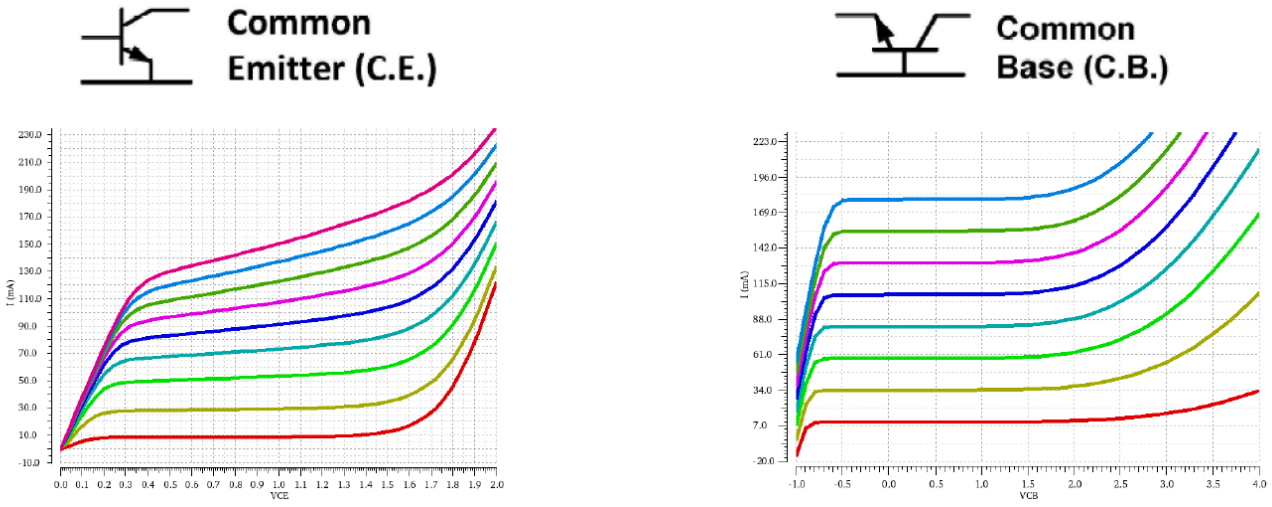


Figure 2.5 I-V curves for the same device in a C.E. and a C.B. configuration

The C.B. seems to have a significantly larger usable collector voltage range. The I-V curves are much flatter due to a less pronounced Early effect and the breakdown seems to happen at a higher voltage.

The breakdown of the J_{CB} happens due to avalanche. A short investigation in a good undergraduate book [3] will reveal some empirical formulation about the reverse current I_{RA} during an avalanche breakdown process:

$$I_{RA} = MI_R$$

Where the multiplication factor is defined as:

$$M = \frac{1}{1 - \left(\frac{V_R}{BV}\right)^n} \tag{2.24}$$

V_R is the reverse voltage that theoretically never reaches the BV. At the breakdown voltage reverse current will become infinite, which practically means "very large". In a C.B. configuration, at $I_E = 0$, the collector-base junction undergoes breakdown for a reverse voltage BV_{CBO}. The effects of the breakdown on the collector current can be modeled using the avalanche multiplication factor:

$$I_C = -aI_E M = -aI_E \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n} \tag{2.25}$$

The effects due to avalanche breakdown are slightly more complicated in the case of a C.E. configuration. The current due to avalanche is *amplified* in a sense, by the transistor. By the Kirchhoff current law, the base current can still be calculated as:

$$I_B = -(I_C + I_E) \tag{2.26}$$

The equation (2.25) from the C.B. case still holds. By replacing it in (2.26) we get:

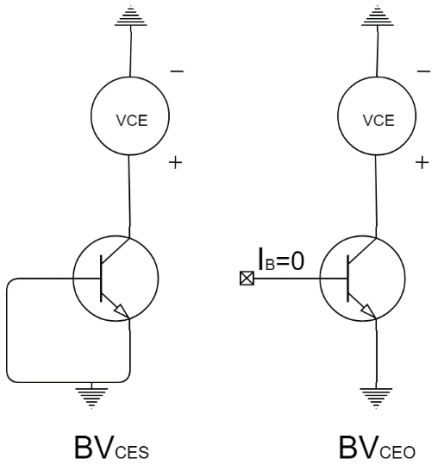
$$I_C = \frac{Ma}{1 - Ma} I_B \tag{2.27}$$

The breakdown voltage happens when $I_C \to \infty$ so we can get BV_{CEO} by solving:

$$Ma = 1 \xrightarrow{V_{CB} \approx V_{CE}} \frac{a}{1 - \left(\frac{BV_{CEO}}{BV_{CBO}}\right)^n} = 1 \tag{2.28}$$

$$\frac{BV_{CEO}}{BV_{CBO}} = \sqrt[n]{1 - a} \xrightarrow{a = \frac{\beta}{\beta + 1}} BV_{CEO} \cong \frac{BV_{CBO}}{\sqrt[n]{\beta}} \tag{2.29}$$

Equation (2.29) proves that the BV_{CEO} will be significantly lesser than BV_{CBO}. In the target technology, a slightly different measure is used for the base-collector breakdown. Instead, the shorted-base breakdown voltage BV_{CES} is measured, when the base is shorted to the emitter.



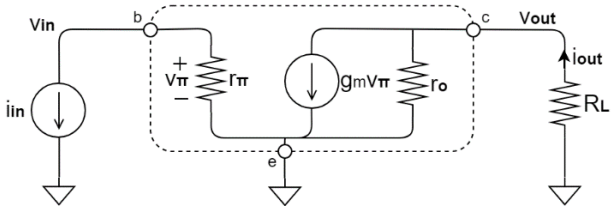
2.30 Setups for the measurement of the collector-base and collector-emitter breakdown voltages

However, $BV_{CBO} \cong BV_{CES}$ so it is expected that the above conclusions should still hold true. Indeed, in the target technology $BV_{CES} = 5.3\ V$ at the worst case, which is significantly larger than the $BV_{CEO} = 1.5\ V$.

The above results have important implications about the maximum deliverable power by a C.B. stage. The output voltage swing of a C.E. is restricted by the BV_{CEO} and the C.B. by the BV_{CES}, which in the worst case is 3.5 times larger, meaning 3.5 times more deliverable power for the same device size. What is more, the increased output voltage swing of the C.B. will reduce the effects of the knee voltage, possibly improving the output efficiency.

2.6.2 Small signal analysis

The C.B. configuration will in practice have a decreased power gain compared to the C.E. The reason for the reduced power gain can be evident after a small-signal analysis of the two stages:



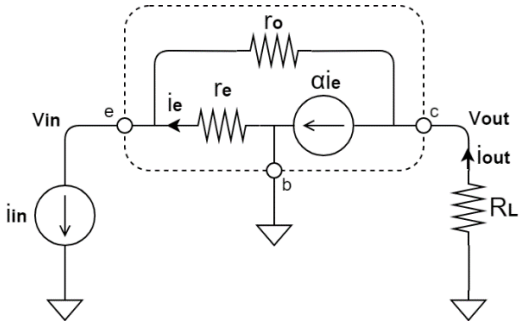
2.31 Small signal equivalent of a C.E. stage

Current sources are used to supply the input signals, modeling in a simplified manner the output of a previous transistor stage. The analysis of the small-signal equivalent of the C.E. can be done in a straightforward manner, resulting in a voltage gain A_v of:

$$A_v = \frac{v_{out}}{v_{in}} = -g_m(r_o||R_L) \approx -g_m R_L \tag{2.32}$$

And a current gain of:

$$A_i = \frac{i_{out}}{i_{in}} = -\beta \frac{r_o}{r_o + R_L} \approx -\beta \tag{2.33}$$



2.34Small signal equivalent of a C.B. stage

Due to the topic of this thesis, the C.B. configuration will be investigated in a bit more detail. First of all, the input resistance is calculated:

$$R_{in} = r_e||\left(-\frac{r_o + R_L}{g_m R_L}\right) \cong r_e \tag{2.35}$$

Since r_e has usually a value between a few Ohms and a few tens of Ohms, the input impedance of the C.B. stage will be relatively small. An interesting note is that due to a positive feedback that the Early resistor r_o causes, R_{in} is slightly increased.

The output resistance of the C.B. is calculated:

$$R_{out} = \frac{r_o + r_e}{a + 1} \approx \frac{r_o}{2} \tag{2.36}$$

which is very large, similarly to the output resistance of the C.E. stage. The voltage gain and the current gain of the C.B. is calculated as follows:

$$A_v = \frac{(r_o g_m + 1)R_L}{r_o + R_L} \approx g_m R_L \tag{2.37}$$

$$A_i = \frac{(aR_L)||r_o}{R_L} \approx a \tag{2.38}$$

The last equation shows that indeed the C.B. has an almost unity current gain. This results in an inferior power gain compared to the C.E.:

$$\frac{G_{C.E.}}{G_{C.B.}} = \frac{g_m R_L \beta}{g_m R_L a} \approx \frac{\beta}{a} \tag{2.39}$$

The reduced gain of the C.B. is not an immediate problem. A driver stage can be used in order to compensate for the low gain of the C.B. power stage. The problem with the low gain is that the extra power provided by the driver stage will result in a reduction of the PAE of the C.B. stage. So the advantage in output efficiency due to the increased output voltage range that was found out in the previous section, is effectively canceled out by the reduced gain.

On the other side, β is not a constant but varies with current. Under high currents, the value of β gradually drops due to the Kirk effect. The result is that mmWave PAs based on C.E. stages will suffer from "soft saturation" meaning that the output power at 1dB gain compression (OP1dB) will be remarkably lower than the saturation power (Psat) where efficiency peaks. On the contrary, the current gain of the C.B. is very linear, because $a = \frac{\beta}{\beta+1}$ is close to unity relying on the fact that β is large, and as a result α will not change much, even

as β starts to drop. This means that in a C.B. stage the OP1dB will be very close to Psat, allowing operation very close to the point of maximum efficiency.

Finally, in recent work [7] a new technique has emerged, that can be used to significantly improve the efficiency of the C.B. stage at back-off powers. This new technique is called Current Clamping and will be overviewed in another section. The fact that the C.B. stage can produce more output power than the C.E. stage, in combination with the current clamping technique that improves back-off efficiency, where in the end the decisive factors in choosing the C.B. configuration for this application.

3 Efficiency Enhancement Techniques

A central goal of this thesis is to maintain efficiency over a wide signal dynamic range. This chapter is intended for the analysis of some of the most popular techniques currently used for back-off efficiency enhancement. Special care is given on the two techniques used in this thesis, the DPA and the Current Clamping.

3.1 The Doherty Power Amplifier

3.1.1 Active load pull using two signal generators

Before introducing the classic Doherty Architecture, it is important to understand the concept of load modulation, by introducing the technique of active load-pull. Referring to Figure 3.1 generator 1 "sees" a load resistance of R_L if generator 2 is to give zero current.

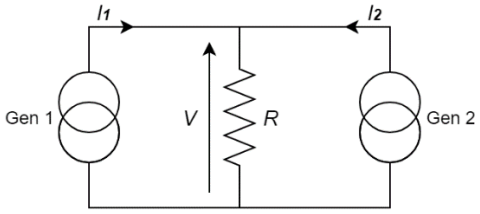


Figure 3.1 Active load-pull using two signal generators

Using Kirchhoff's current law, if generator 1 produces a current I_1 and generator 2 produces a current I_2 then the voltage across the load resistance will be:

$$V_L = R_L(I_1 + I_2) \tag{3.1}$$

So, the effect at the terminals of generator 1 is the same as if there were a simple passive resistor connected across it that has a value of:

$$R_1 = R_L \frac{(I_1 + I_2)}{I_1} = R_L \left(1 + \frac{I_2}{I_1}\right) \tag{3.2}$$

Simultaneously, the effect at generator 2 would be the equivalent to a resistor having a value:

$$R_2 = R_L \frac{I_1 + I_2}{I_2} \tag{3.3}$$

In this form, the equations show the possibility of changing, or "pulling" the load seen by generator 2, by simply setting a constant $\frac{I_2}{I_1}$ ratio. What is more, the above equations can be extended to AC circuits by simply using complex notation. So, for example instead of R_1 we have:

$$Z_1 = R_L\left(1 + \frac{I_2}{I_1}\right) \tag{3.4}$$

By controlling the magnitude and phase of the current I_2 it is possible to transform the impedance Z_1 to a higher resistive value if I_2 is in phase with I_1, or to a lower resistive value if I_2 is out of phase with I_1. Consequently, if the two generators are now considered to model the output transconductance generators of two separate RF transistors, having co-phased input signals, the effective output impedance seen by one device can be modified by the other.

3.1.2 Quick overview of the Doherty operation

The conceptually important parts of the Doherty operation can easily be "lost" in the formulation. A brief overview will be made here as a guide, before the formulation is introduced. The "classical" Doherty PA architecture can be seen in Figure 3.2. The operation is divided between two "paths" the Main PA and the Auxiliary PA. A key part for the operation is the output network that performs the combination of the output powers of the two "paths" with minimum losses, as well as the Doherty load modulation which is unique to the architecture and is similar to the active load-pull that was introduced in the previous paragraph. In the Doherty load modulation scheme, as the output power of the Aux. PA increases, the load "seen" by the Main PA decreases.

The operation goes as follows:

- At deep power back-off the Aux. PA is turned off and does not produce any power. Only the Main PA is in operation and produces power, with a resistive load two times larger than the optimal.
- At 6dB power back-off the Main PA is reaches its maximum collector voltage swing, since its load is double the optimal. As a result, at that point the Main PA is performing

at maximum collector efficiency. However, if left as is, the Main PA will start compressing when the input power increases further.

- To relieve the Main PA from its high resistive load, the Aux. PA starts producing power after the 6dB power back-off point. As a result, the Doherty load modulation is activated, and the load of the Main PA is reduced, keeping its collector voltage-swing, as well as the collector efficiency at maximum.
- At maximum output power, both the Main and the Aux. Pas "see" at their outputs their optimal load and as a result they operate at maximum power and efficiency.

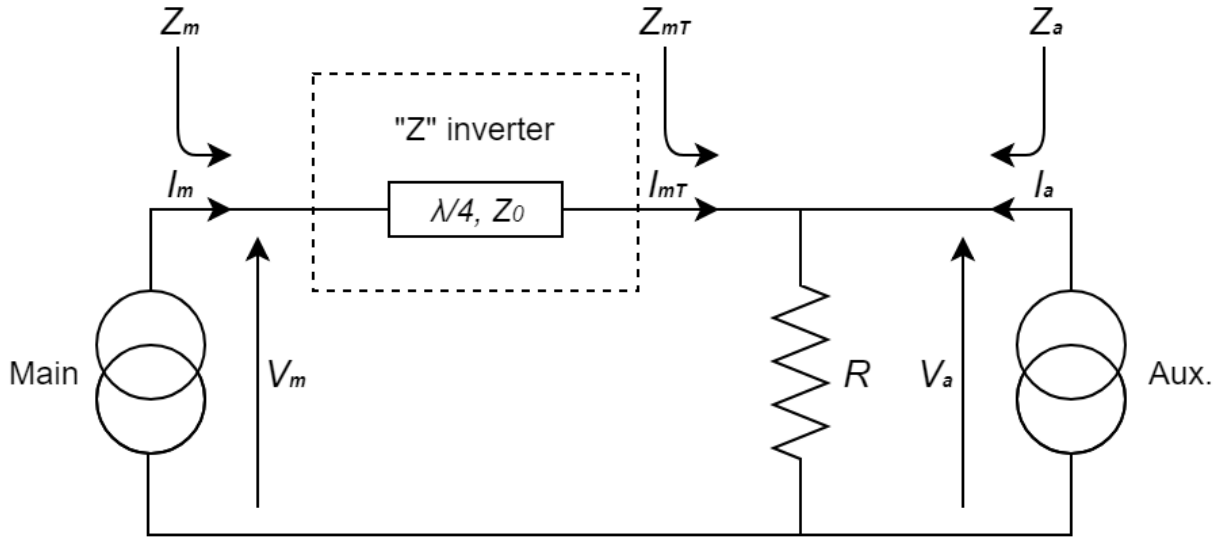


Figure 3.2 Schematic for the analysis of the Doherty amplifier

As seen from the operation overview the Main and Aux. PAs behave quite differently, despite the fact that the input signal is equally split between them. The Main PA may be simply a transistor biased for a linear gain, like an AB or B class amplifier. However, the Aux. PA has a very non-linear behavior: at deep PBO it produces zero power, however at the 6dB point it abruptly turns on, starts producing power and with 6dB more input power, it produces just as much power as the main device. The design of a PA that fits this model may be challenging and will be discussed in a following paragraph. As a final note, despite the non-linear gain of the Aux. PA, the overall gain of the Doherty architecture is exclusively determined by the Main PA and as a result it is linear.

3.1.3 Formulation

The simplified schematic of the "classical" Doherty PA in Figure 3.2 models two active devices as the Main and Aux. Pas that have a DC supply V_{dc} and a maximum collector current I_{max}, an impedance inverter and a load resistor R. The impedance inverter can be considered conceptually to be a simple quarter-wave transmission line, whose terminal characteristics have the form:

$$\begin{bmatrix} jV_a \\ -jI_0 \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ \frac{1}{jZ_0} & 0 \end{bmatrix} \begin{bmatrix} V_m \\ I_m \end{bmatrix} \tag{3.5}$$

The active devices are assumed to produce current amplitudes I_m and I_a, at any given signal amplitude v_{in}, where:

$$I_m = f_m(v_{in}), \qquad I_a = f_a(v_{in}) \tag{3.6}$$

As a result we have:

$$V_a = Z_0 I_m \tag{3.7}$$

$$I_0 = \frac{1}{Z_0} V_m \tag{3.8}$$

and from Kirchhoff's current law the remaining circuit relation is:

$$-jI_0 = jI_a - \frac{jV_a}{R} \tag{3.9}$$

by replacing (3.7) and (3.8) in (3.9):

$$V_m = Z_0 \left(\frac{Z_0}{R} I_m - I_a \right) \tag{3.10}$$

Now, v_{in} is normalized between 0 and 1. For a "classical" Doherty configuration:

$$f_m(v_{in}) = I_M . v_{in}, \quad 0 < v_{in} < 1 \tag{3.11}$$

$$f_a(v_{in}) = \begin{cases} 0 & ,0 < v_{in} < 0.5 \\ 2(v_{in} - 0.5) I_M & ,0.5 < v_{in} < 1 \end{cases} \tag{3.12}$$

where $I_M = \frac{I_{max}}{2}$ is the maximum current amplitude for each device.

And from (3.7, 3.11) and (3.10, 3.11, 3.12) we get respectively:

$$V_a = Z_0 I_M . v_{in} \tag{3.13}$$

$$V_m = \begin{cases} Z_0 \frac{Z_0}{R} I_M v_{in}, 0 < v_{in} < 0.5 \\ Z_0 \left(\frac{Z_0}{R} I_M v_{in} - 2(v_{in} - 0.5) I_M \right), 0.5 < v_{in} < 1 \end{cases} \tag{3.14}$$

At $v_{in} = 0.5$ the Main device reaches its maximum voltage swing $V_m = V_{dc}$. Thus:

$$V_{dc} = Z_0 \frac{Z_0}{R} \frac{I_M}{2} \tag{3.15}$$

At $v_{in} = 1$ the Main device has remained at its maximum voltage swing. Thus:

$$V_{dc} = Z_0 \left(\frac{Z_0}{R} I_M - I_M \right) = 2V_{dc} - Z_0 I_M \Rightarrow Z_0 = \frac{V_{dc}}{I_M} = \frac{V_{dc}}{0.5 I_{max}} = R_{opt} \tag{3.16}$$

$$(3.15, 3.16) \Rightarrow R = \frac{R_{opt}}{2} \tag{3.17}$$

From (3.16) and (3.17) the impedance of the quarter-wave line and the RF load can be calculated.

Finally, from (3.13,3.16) and (3.14,3.15):

$$V_a = V_{dc} . v_{in} \tag{3.18}$$

$$V_m = \begin{cases} 2V_{dc} . v_{in}, & 0 < v_{in} < 0.5 \\ V_{dc}, & 0.5 < v_{in} < 1 \end{cases} \tag{3.19}$$

The fundamental current and voltage amplitudes against input voltage amplitude, as defined by (3.11), (3.12), (3.18), (3.19) can be seen in Figure 3.3. The key feature is the Main PA voltage amplitude V_m, that is kept at a constant maximum in the upper 6dB region. This will result in high efficiency for the Main device over the entire extent of the upper 6dB region and a much better efficiency/backoff characteristic than would be obtained from a

conventional design. Also, from (3.13) the voltage V_a across the load is proportional the input voltage v_{in} and as a result the gain of the Doherty power amplifier is linear.

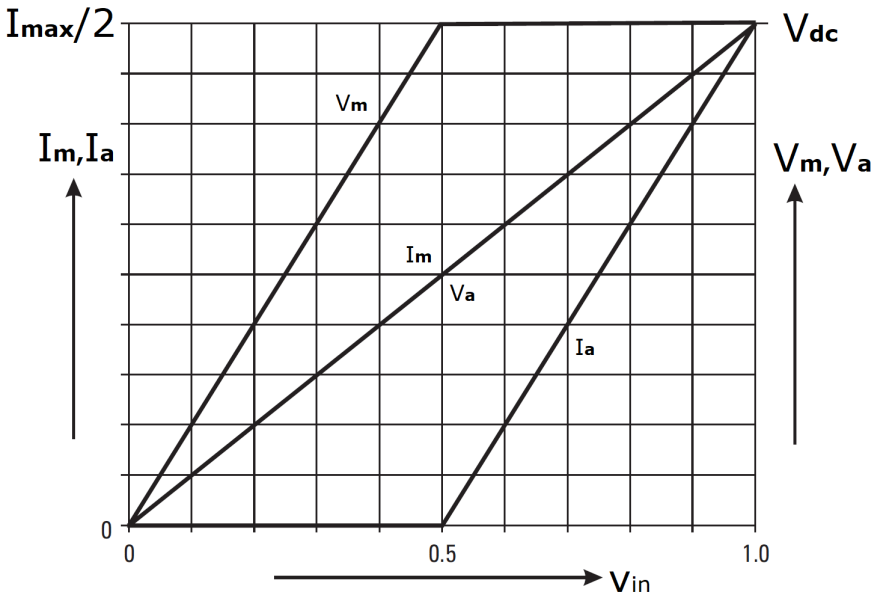


Figure 3.3 Classical Doherty PA; current and voltage (fundamental amplitudes) characteristics for main and peaking devices plotted against input drive signal amplitude.

In order to determine an expression for overall efficiency an assumption must be made for the output efficiency of each path. Assuming that both Main and Aux. PAs have an output efficiency similar to a normalized Class-B (a common assumption to make when analyzing the "classical" Doherty PA) the efficiency of each amplifier will drop proportionately with the output RF voltage amplitude:

$$\eta_{out,m} = \eta_{max}\frac{V_m}{V_{dc}}, \quad \eta_{out,a} = \eta_{max}\frac{V_a}{V_{dc}} \tag{3.20}$$

Ignoring the passive losses of the Doherty combining network, it is now possible to determine the output efficiency of the Doherty PA.

- For the low power region, only the Main PA is on:

$$\eta_{out} = \eta_{max}.v_{in}, \quad 0 < v_{in} < 0.5 \tag{3.21}$$

- In the upper 6dB region, both amplifiers are active.

The composite RF power is:

$$P_{COMP} = \frac{V_a^2}{2R} = \frac{V_{dc}^2}{R_{opt}} v_{in}^2 = \frac{V_{dc} I_{max}}{2} v_{in}^2 \tag{3.22}$$

The DC power consumed by the main device is:

$$P_{DC,M} = \frac{P_{RF,M}}{\eta_{out,M}} = \frac{\frac{V_m I_m}{2}}{\eta_{max} \frac{V_m}{V_{dc}}} = \frac{V_{dc} I_{max}}{4\eta_{max}} v_{in} \tag{3.23}$$

The DC power consumed by the aux device is:

$$P_{DC,A} = \frac{P_{RF,A}}{\eta_{out,A}} = \frac{\frac{V_a I_a}{2}}{\eta_{max} \frac{V_a}{V_{dc}}} = \frac{\frac{V_{dc} v_{in} . I_{max}(v_{in} - 0.5)}{2}}{\eta_{max} v_{in}} = \frac{V_{dc} I_{max}(v_{in} - 0.5)}{2\eta_{max}} \tag{3.24}$$

The total DC power consumption is:

$$P_{DC,total} = P_{DC,M} + P_{DC,A} = \frac{V_{dc} I_{max}}{4\eta_{max}} (3v_{in} - 1) \tag{3.25}$$

As a result the output efficiency in the upper 6dB region is:

$$\eta_{out} = \frac{P_{COMP}}{P_{DC,total}} = \eta_{max} \frac{2v_{in}^2}{(3v_{in} - 1)}, \quad 0.5 < v_{in} < 1 \tag{3.26}$$

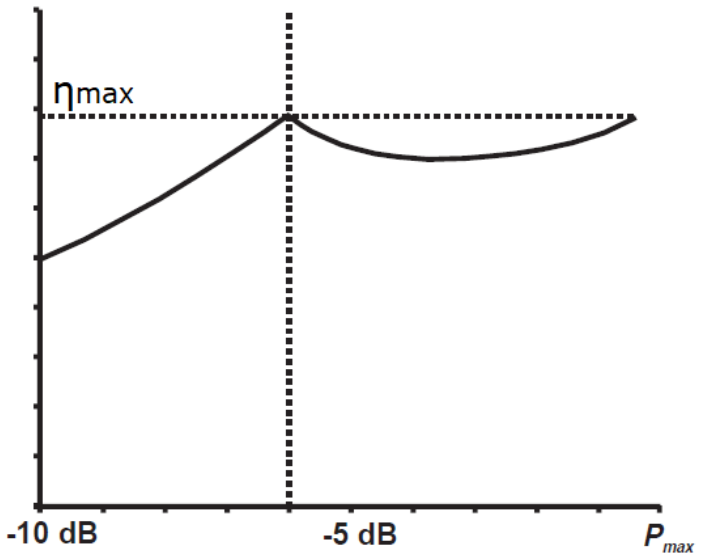


Figure 3.4 Efficiency versus input power back-off

From (3.21) and (3.26) the overall efficiency can now be plotted as a function of power back-off in dB Figure 3.4. The efficiency rolls off at the low power region similarly to a conventional Class-B PA. The efficiency reaches its maximum value η_{max} at the 6dB and 0dB power back-off. The small dip in the middle of the upper 6dB region is due to the lower efficiency of the Aux. PA, where it does not display a full rail-to-rail RF voltage swing.

3.1.4 Auxiliary amplifier configurations

As discussed previously, the design of an amplifier that fits the model of the Aux. PA can be challenging. The usual approach is to follow the original implementation and use a Class-C bias. The gain expansion of the Class-C PA creates a useful approximation of the Aux. PA characteristic; however the peak output current will be lower than that of the Class-B or AB biased Main PA. An obvious solution would be to scale-up the periphery of the Aux. device, however this would result in a reduced power-utilization factor of the Aux. device. Another solution would be to reduce the gain of the Main PA using an attenuator, however this would result in a reduction of the overall gain of the Doherty PA and gain is an important resource at the target frequency. This is not the last of the problems that come with the Class-C bias. The voltage stress of the Aux. PA can also be an important issue, because of the low bias voltage of the base and external protection is required in order to protect the Aux. device, creating additional overhead at the output of the Doherty PA.

Fortunately, it is possible to avoid the cascade of practical difficulties that come with the simple Class-C bias. Given the growing use of DSP to linearize RFPAs in modern telecommunication systems, it is reasonable to assume that accurate control signals and adaptive bias voltages can be provided with relative ease. Clearly, at the system level the transmitter “knows” everything about the signal it inputs to the RFPA, so it is fair to assume that it will not be much of an extra burden for the system processor to generate, for example, a signal proportional to the RF envelope. Such a signal can be put to immediate use in a Dynamic Biasing scheme of the Aux. Device ant the Aux. PA problem almost solves itself.

It is also possible to create a standalone PA solution, using some form of envelope detector circuit to provide the dynamic bias. However, the envelope detector will probably need several cycles to perform a measurement, reducing the RF bandwidth. Fortunately, the

precision needed in this kind of application is very forgiving and a small number of cycles will probably be needed for each measurement. Finally, the control of the Aux. PA could be implemented using RF control elements such attenuators and switches.

3.2 Current Clamping in Common-Base

Conventional efficiency enhancement techniques adopted at RF, such as supply modulation for envelope tracking and linearization of switching PAs, are difficult to implement in mm-Wave applications. The current clamping technique was introduced in recent work as a method of back-off efficiency enhancement for E-band RFPAs (80GHz center frequency) [7]. A Common-Base power stage is used that implements a current-mode version of the well-known diode voltage clamper. The DC current of the active devices tracks the envelope of the input signal current, achieving reduced current consumption and improved efficiency at power back-off.

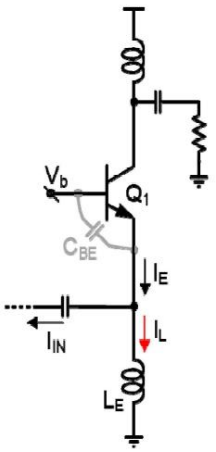


Figure 3.5 Circuit for the analysis of current clamping

By observing Figure 3.5, the basic operation of current-clamping in a common-base configuration can be illustrated. Firstly, the parasitic capacitance of the base-emitter junction is assumed to be zero ($C_{BE} = 0$). At the same time, L_E is assumed to be a relatively big inductor at the frequency of operation. The bias voltage V_b at the base of Q_1 is set for a small quiescent current (ideally zero, in practice a $I_q \approx 0.1\, I_{max}$ is used). A sinusoidal input signal current is assumed:

$$I_{IN} = I_{pk} \cos(\omega_0 t + \varphi) \tag{3.27}$$

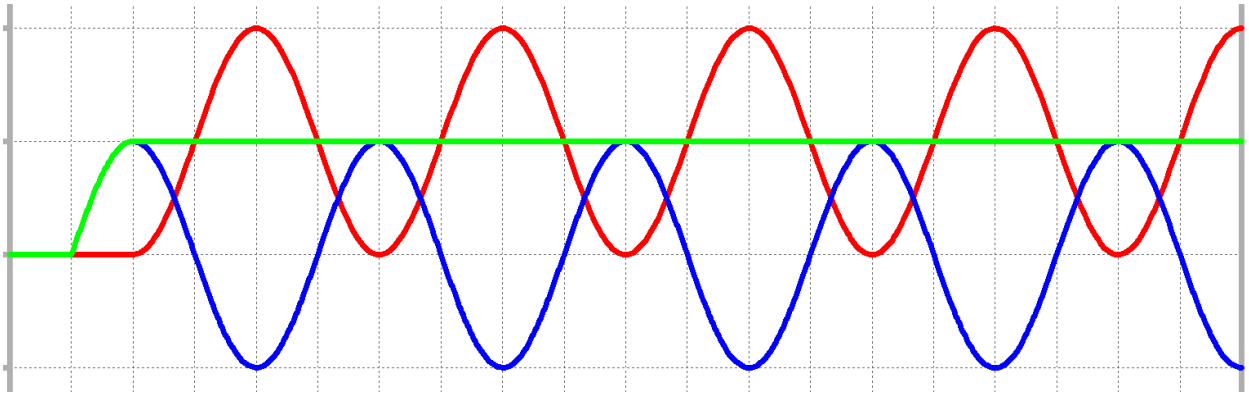


Figure 3.6 Current waveforms for $C_{BE} = 0$; blue is I_{IN}; green is I_{L_E}; red is I_E

Initially, the input source is off. During the first quarter-cycle, the input drive signal is trying to "push" $I_{IN}(t)$ current through L_E, as well as the base emitter junction (J_{BE}) of Q_1 but in a reverse fashion. The reverse current of course cannot flow through the reverse biased J_{BE}; as a result, Q_1 remains in cut-off. All of I_{IN} flows through L_E until I_{L_E} charges up to a maximum value of I_{pk}.

During the second quarter-cycle, the input current starts decreasing form its maximum value of I_{pk}. However, L_E is very big and it is difficult to change its current; I_{L_E} stays approximately constant. Instead the input current has found another path; a forward current with a value $I_{L_E} - I_{IN}$ starts passing through J_{BE} biasing it forward. As a result, Q_1 turns on.

From that point on, Q_1 does not have to turn off any time. The current of L_E has ensured that $I_{L_E} - I_{IN} \geq 0$, always, so the J_{BE} is always forward biased. Even if the amplitude of I_{IN} varies slowly over time, I_{L_E} will track its envelope. Thanks to the inductor L_E, the power amplifier can control its bias current adaptively, tracking the envelope of the input signal without any external help.

From the above discussion, it is clear that the collector current of Q_1 will be in the steady state:

$$I_C \approx I_E = I_1 + I_1 \cos(\omega_0 t + \varphi) \qquad (3.28)$$

The collector current swings from 0 to $2I_1$. At its maximum value the amplitude of the collector current will be $I_{1max} = I_{max}/2$.

The collector voltage will be:

$$V_C = V_{dc} + V_1 \cos(\omega_0 t + \varphi) \tag{3.29}$$

The collector voltage swings from $V_{dc} - V_1$ to $V_{dc} + V_1$. At its maximum value the amplitude of the collector voltage will be $V_{1max} = V_{dc}$.

The optimal impedance is:

$$R_{opt} = \frac{V_{1max}}{I_{1max}} = \frac{2V_{dc}}{I_{max}} \tag{3.30}$$

The DC power dissipated is:

$$P_{dc} = V_{dc} I_1 \tag{3.31}$$

The RF power produced is:

$$P_1 = \frac{V_1 I_1}{2} = \frac{I_1^2}{2} R_{opt} = \frac{I_1^2 V_{dc}}{I_{max}} \tag{3.32}$$

Resulting in an output efficiency of:

$$\eta = \frac{P_1}{P_{dc}} = \frac{I_1}{I_{max}} \xrightarrow{I_{1max} = \frac{I_{max}}{2}} \eta = 50\% \frac{I_1}{I_{1max}} \tag{3.33}$$

The output efficiency is limited to a theoretical maximum of 50% similarly to a class A. This does not come as a surprise, since the Current Clamping C.B. is many ways similar to a class A. The collector current is completely sinusoidal and does not contain any harmonics. However, at power back-off the PA behaves in a completely different way from the class A. The current consumption tracks the envelope of the input signal and backs-off as well, with positive effects to the efficiency. As a result, the efficiency rolls-off at the back-off proportionally to the current amplitude. This is very similar to a class B PA.

However, the parasitic capacitance of J_{BE} has still not been taken into consideration. At high frequencies C_{BE} plays a key role and a number of problems arise if L_E is kept at a large value in a practical application. To solve these problems, the L_E is simply chosen to resonate with C_{BE} at the fundamental. The basic operation can be seen in Figure 3.7.

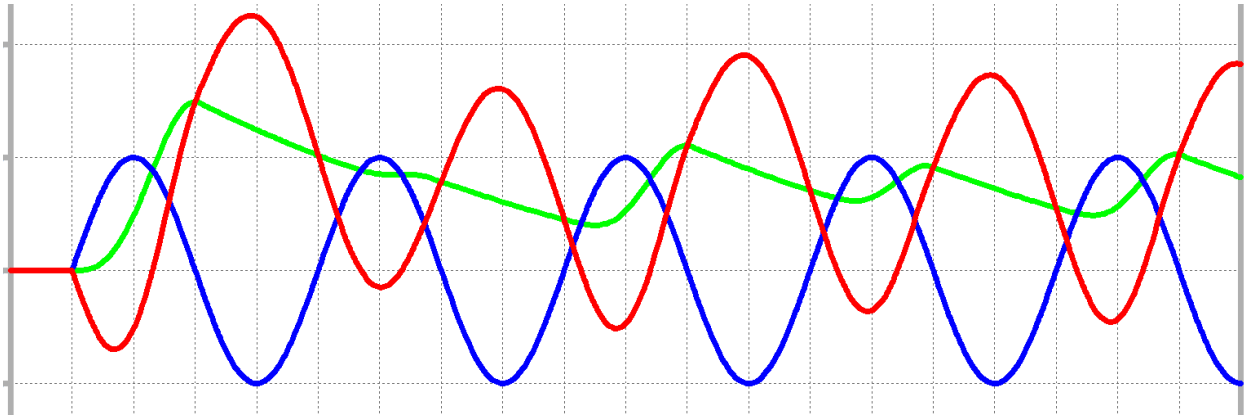


Figure 3.7 Current waveforms for finite C_{BE}; blue is I_{IN}; green is I_{L_E}; red is I_E

For the purpose of realistic results, the inductor was assumed to have a finite $Q = 15$. The waveforms seen are very similar to the case where $C_{BE} = 0$ was assumed. The inductor current rises quickly and after a small overshoot it reaches steady state in two cycles only, tracking in approximation the input current envelope. The high impedance of the tuned pair $C_{BE} - L_E$ forces the ac component of the emitter current to be equal to the input current thus achieving a constant current gain up to amplifier saturation. C_{BE} also sets low impedance at the emitter, thus allowing input harmonics to appear at the collector current, but the latter may be simply filtered out by the output matching network of the amplifier.

In conclusion, one could say that the Current Clamping C.B. PA adopts the positive characteristics of both conventional classes A and B. The output current is very sinusoidal and ideally does not contain harmonics, yet the efficiency rolls off slowly at back-off powers. An efficiency roll-off, this similar to a conventional class B, is very difficult to achieve at mm-Wave applications in any other way. In practical design, one can expect very similar results to the ones calculated above with the ideal model of $C_{BE} = 0$.

3.3 Chireix's outphasing

The outphasing technique is also known as LINC (linear amplification by nonlinear components. It was invented in 1935 by Chireix. The main idea of this technique is to decompose a non-constant envelope signal into two constant envelope signals.

$$x(t) = A(t)\cos\big(\omega_0 t + \varphi(t)\big)$$

$$= \cos\big(cos^{-1}\big(A(t)\big)\big)\cos(\,\omega_0 t + \varphi(t))$$

$$= x_1(t) + x_2(t)$$

Where $x_1(t) = \cos\big(\omega_0 t + \varphi(t) + cos^{-1}\big(A(t)\big)\big)$

$x_2(t) = \cos\big(\omega_0 t + \varphi(t) - cos^{-1}\big(A(t)\big)\big)$

Note that in the above decomposition, $A(t)$ is always assumed to be less than one, otherwise a normalizing factor has to be used. This decomposition can be depicted as in Figure 3.8. It can be seen that by phasing the two unit vectors $x_1(t)$ and $x_2(t)$ properly, the resultant vector can be of any phase with an amplitude between zero and two.

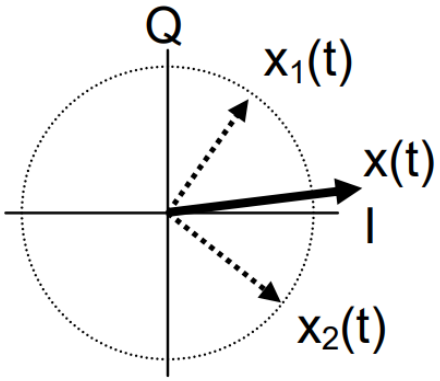


Figure 3.8 Outphasing decomposition

Since $x_1(t)$ and $x_2(t)$ both have constant envelope, two nonlinear amplifiers can be used. A block diagram is given in Figure 3.9. Even though this technique seems very attractive, there are practical difficulties in combining the output powers of the two amplifiers. What is more, the generation of the drive signals and inevitable DSP corrections,

require extra overhead and have been something of a detraction from the Chireix outphasing system, in comparison with the other techniques described in this chapter. Nevertheless, useful performance can be obtained using a basic uncompensated combining structure.

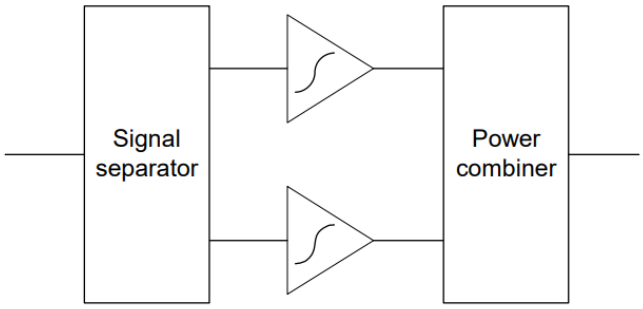


Figure 3.9 Block diagram of the outphasing technique

3.4 Envelope Elimination and Restoration (EER)

The EER technique, also known as the polar modulator, has been of much interest in recent years. Figure 3.10 shows a block diagram of an EER. EER separates the input signal into two paths, the amplitude path and the phase path. The phase portion of the signal can be obtained by using a limiter. It is then amplified a nonlinear PA. The amplitude portion of the signal can be obtained by using an envelope detector. This envelope detector is then used to modulate the power supply of the PA via a DC-to-DC converter, thereby getting the amplitude information back at the output of the PA.

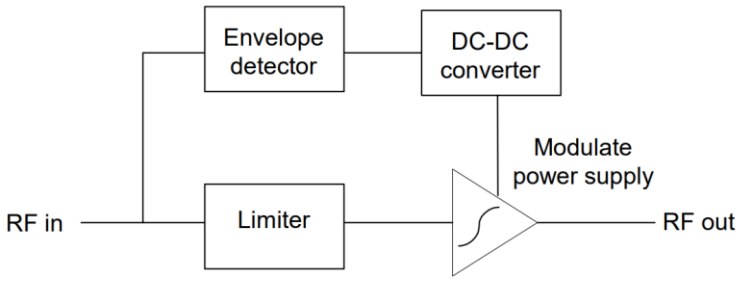


Figure 3.10 Block diagram of an EER power amplifier

The output voltage of the DC-to-DC converter must be able to change quickly enough to track the envelope of the signal. Since it is very difficult to design an efficient DC-DC converter with large bandwidth, this technique is generally limited to applications with

relatively small bandwidth. Another important characteristic that makes this technique unfit for applications with large bandwidth is that the phase delay of the two dissimilar signal paths cannot be easily matched.

3.5 Envelope tracking (ET)

This technique is similar to EER, in that the supply voltage is varied to conserve power. The block diagram of an ET RF PA system is shown in Figure 3.11. An envelope-derived modulation is applied to the supply voltage of the conventional linear RF PA. The supply voltage is increased in proportion to the increasing drive voltage envelope. As a result a result, maximum efficiency is maintained since the output voltage always swings at its full range (from 0 to $2V_{dc}$) and the output power increases linearly with input drive power.

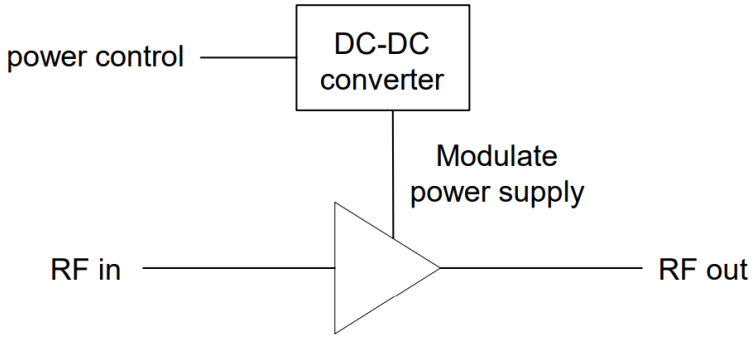


Figure 3.11 Block diagram of an ET power amplifier

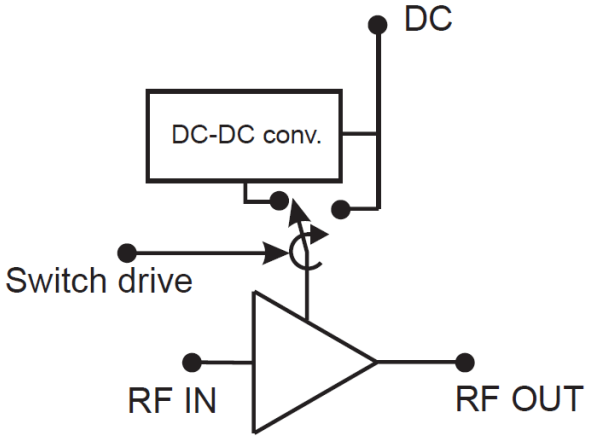


Figure 3.12 ET system using a two-level switched supply

The supply voltage does not have to track the input signal envelope with great accuracy, which makes ET much more appealing than the EER technique. Even better, the

efficiency enhancement process is not dependent on the RF matching in contrast to the Doherty and Chireix techniques. In a simple case, only two supply voltages are used, and a supply switch selects between the two as in Figure 3.12.

4 Target Technology

4.1 General Information

The technology used in this thesis, is provided by Infineon Technologies. It is a 400GHz/130nm SiGe BiCMOS process with copper metallization for analog mixed signal mmWave applications which provides high performance at low power consumption. The intended applications include Automotive Radar MMICs, RF ASICs and high bit rate wireless datalinks. In brief, the technology includes three types of HBT NPN devices in several sizes and contact configurations, metal film resistors, MIM capacitors, several types of varactor devices, PIN diodes and different types of RF transmission lines.

4.2 NPN SiGe Heterojunction Bipolar Transistors

4.2.1 High speed npn

High speed npn devices are available for:

- Minimum emitter mask widths of 0.22um
- Maximum emitter mask lengths of 10um
- Several contact configurations such as single-base, double-base etc.

The technology library also offers devices with two or more npn transistors in parallel. The highest transit frequency f_T is obtained for a current density of about 11.5 $\frac{mA}{\mu m^2}$. However, the current density must not exceed an average root mean square value of 13 $\frac{mA}{\mu m^2}$ for time scales longer than $1\mu s$ for long term reliability and parameter drift reasons.

The following table contains some important parameters for a high speed npn device of specific size are, at a temperature of $T = 25°C$.

Parameter	Unit	Min.	Typical	Max
$A_{E,mask}$	μm^2		0.22x2.80	
$A_{E,eff}$	μm^2		0.13x2.71	
BV_{CEO}	V	1.2	1.5	
BV_{CES}	V	4.7	5.3	

BV_{EBO}	V	0.8	2	
V_{Early}	V		100	
Maximum f_T	GHz		$250@j_C = 11.5\frac{mA}{\mu m^2}$	
Maximum f_{max}	GHz	345	370	400

4.2.2 Medium speed npn

Medium speed npn devices are available for the same sizes and contact configurations as the high-speed devices. The following table contains some important parameters for a medium speed npn device of specific size , at a temperature of $T = 25℃$.

Parameter	Unit	Min.	Typical	Max
$A_{E,mask}$	μm^2		0.22x2.80	
$A_{E,eff}$	μm^2		0.13x2.71	
BV_{CEO}	V	1.9	2.5	
BV_{CES}	V	9.5	14	
BV_{EBO}	V	0.8	2	
V_{Early}	V		100	
Maximum f_T	GHz		$80@j_C = 1.8\frac{mA}{\mu m^2}$	
Maximum f_{max}	GHz		-	

4.2.3 High voltage npn

High Voltage npn devices are available for the same sizes and contact configurations as the high speed devices. The following table contains some important parameters for a high voltage npn device of specific size , at a temperature of $T = 25℃$.

Parameter	Unit	Min.	Typical	Max
$A_{E,mask}$	μm^2		0.22x2.80	
$A_{E,eff}$	μm^2		0.13x2.71	
BV_{CEO}	V	2.5	4	

BV_{CES}	V	10	14.5
BV_{EBO}	V	0.8	2
V_{Early}	V		100
Maximum f_T	GHz		$55@j_C = 0.9\frac{mA}{\mu m^2}$
Maximum f_{max}	GHz		-

4.2.4 Simulation models

4.2.4.1 Default model

The default model for the high speed, medium speed and high voltage npn transistors is currently Spice Gummel Poon. However, this model does not currently simulate some effects which are important for the design of RFPAs such as high current effects and saturation effects. Since these effects are not modeled, the simulation results may diverge significantly from the measurements. In order to test the extent of this, the transit frequency f_T with relation to the current density of the collector j_C was simulated.

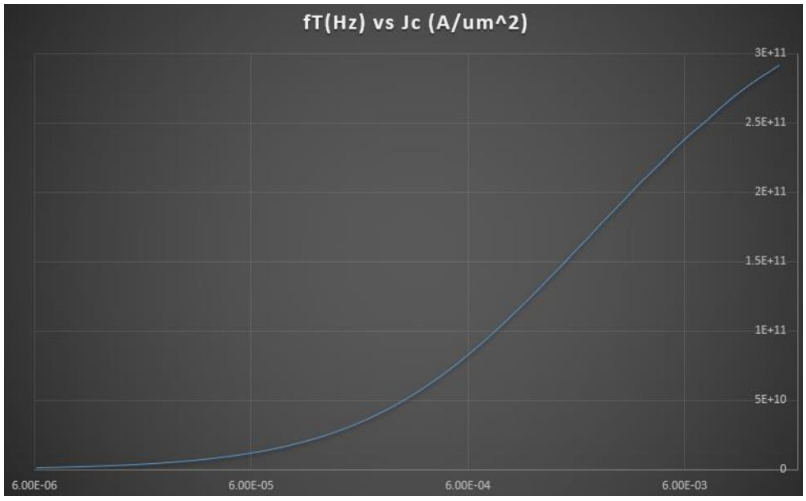


Figure 4.1 Transit frequency vs collector current density using the default model

According to the measurements, as j_C increases the f_T also increases. At some point however, the f_T reaches a plateau, a maximum and then starts decreasing. However, in the simulated results the f_T continuously increases without reaching a maximum. Further simulations revealed that the default model also does not simulate breakdown, making it unsuitable for the simulations in this thesis.

4.2.4.2 HICUM

A preliminary HICUM model is also available for the high speed transistors. After discussions with experts it seems that the HICUM model is well fitted with the measured data and does model high current effects, saturation effects, self-heating and breakdown. Running the same simulation for f_T yields results that agree with the measurements.

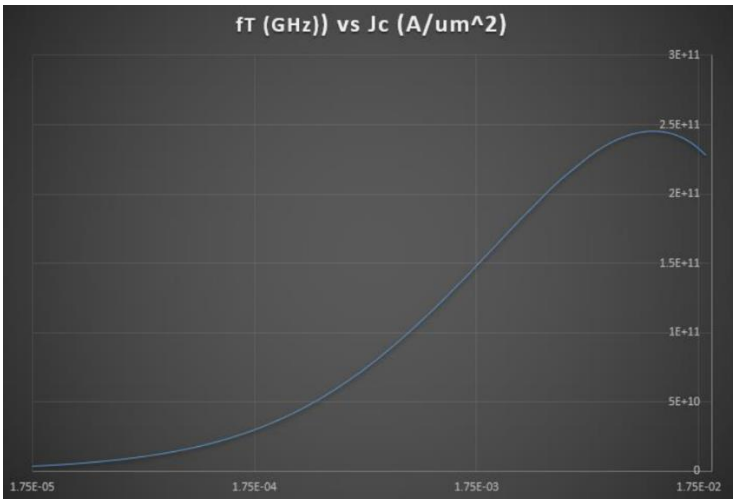


Figure 4.2 Transit frequency vs collector current density using the HICUM model

The simulations for the breakdown voltages were also in agreement with the measured data. As a result, the HICUM model seemed much more reliable and was used for the simulations in this thesis.

4.3 MIM capacitors

The MIM capacitor model takes into account their frequency dependency. The quality factor seems from simulations to be inversely proportional to frequency and capacitance. In Figure 4.3 and Figure 4.4 a frequency sweep of the quality factor for two characteristic capacitance values can be seen.

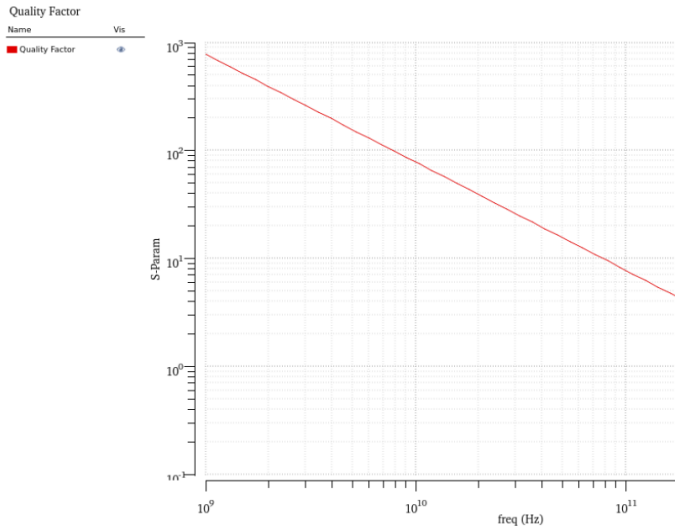


Figure 4.3 Quality factor of an 100fF MIM cap versus frequency

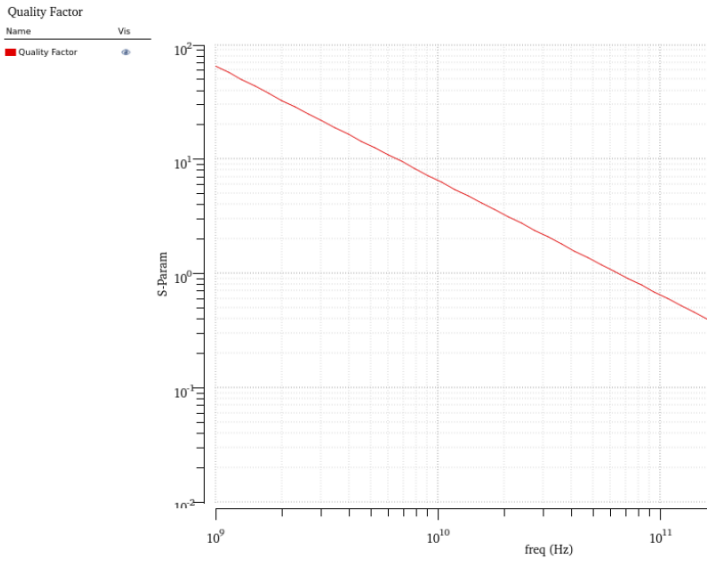


Figure 4.4 Quality factor of an 1.99pF MIM cap versus frequency

However the frequency performance seems to be independent of the dimensions used to implement one particular capacitance value.

4.4 TaN resistors

The TaN resistor models also take into account frequency dependence. Their value over frequency seems to change as if a simple parasitic capacitance is connected in parallel. What is more, the performance seems to be dependent on the dimensions used; larger resistors seem to have greater parasitic capacitance. In Figure 4.5 and Figure 4.6 a frequency sweep of the real and imaginary parts is performed on a TaN resistor of characteristic value.

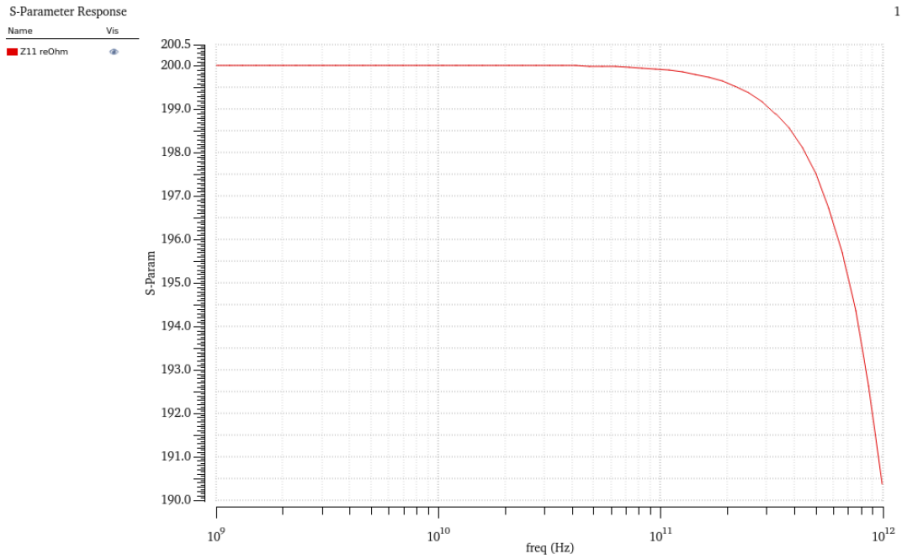


Figure 4.5 Real part of a 200 Ohm TaN resistor vs frequency

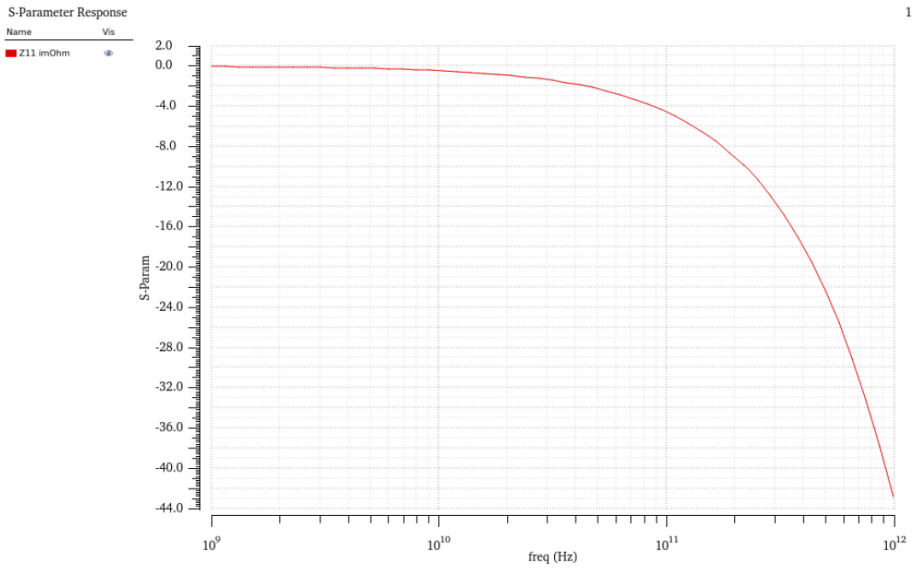


Figure 4.6 Imaginary part of a 200 Ohm TaN resistor vs frequency

4.5 Inductors and transformers

Inductors and transformers are designed using electromagnetic simulation software. However, for the simulations in this thesis realistic models were used for the inductors instead. The inductors used have realistic values for the fundamental frequency and a quality factor of $Q = 17$ was used. Finally, for the transformers, realistic coupling factors were chosen. As a result, despite the use of models for the inductors and transformers, the simulation results are expected to not be far from reality.

5 Implementation

Usually, designs of commercial products are based on preceding versions built in the same technology, meaning that the process and the design flow become more mature with every iteration. As an inexperienced designer, it is a difficult task to acquire all the needed information concerning the technology and its specialties in order to end up “first time right”. Hence, to establish a design flow is like putting pieces of a puzzle together. Some traps are specifically related to this particular process and can be avoided by learning from experience of other designers. Subsequently, the design strategy is listed point for point. Obviously, there was a lot of back and forth in this flow to improve, correct or change parts of the architecture.

The following steps will extensively use simulations performed in the Virtuoso Analog Design Environment by Cadence, using the technology libraries provided by Infineon Technologies. It is important to note the conditions under which the simulations where performed. First, a temperature rise from the ambient was assumed, as a result the temperature for the simulations was set at 65˚C. Second, the HICUM model was used for the active devices.

5.1 The Main power amplifier

As discussed before, the design of the main PA is a major part of this thesis. The main PA will consist of two stages, a driver stage and a power stage. The power stage will of course have a common base configuration and will leverage current clamping for back-off efficiency enhancement. A push-pull (differential) architecture will be employed to reject even harmonics, avoid common lead effects and double the optimal impedance of the PA.

For the driver stage, a cascode configuration was chosen, since the high gain will compensate for the limited gain of the power stage. Also, the high isolation will allow to independently design the power stage and the Doherty input network. For the matching of the two stages, an interstage transformer was used. Finally, to match the input of the cascode stage to the 50 Ohm environment of the Doherty input network an input transformer was used.

5.1.1 Design of the power stage

5.1.1.1 The active devices

As mentioned earlier, the HBT devices leave only few degrees of freedom in the design, namely the number of devices used in parallel, the contact configuration of each device, as well as the emitter mask width and length. The transistors used for the power stage are formed by 6 high-speed npn devices in parallel. The contact configuration is CBEBEBC, meaning that there are two emitters in each device. The emitter mask area is 0.22×6.2 μm^2 giving an effective emitter area of 0.13×6.11 μm^2.

The size of the transistors sets the high current limit. Current densities greater than the high current limit will degrade the transistor's cutoff frequencies. As a result, the high current limit restricts the maximum possible current amplitude. According to the technology parameters the current density must not exceed an average root mean square value of 13 $\frac{mA}{\mu m^2}$ for time scales longer than 1μs. As a result, the only current restriction used is:

$$\text{limit}\left(I_{C,rms}\right) = 6 \times 2 \times 0.13 \times 6.11 \times 13 \cong 124\, mA$$

The maximum possible voltage amplitude is restricted by the avalanche breakdown. The usable voltage at the collector would be reduced to the collector-base breakdown voltage which has a minimum value of $BV_{CES} = 5.3V$. However, it is not needed to bring the devices very close to their breakdown voltages. A collector voltage swing of about 4V will be more than sufficient to obtain the required power performance. As a result, the used power supply voltage, will be half of the collector voltage swing (ignoring the knee voltage):

$$V_{dc} = 2V$$

5.1.1.2 Bias voltage

The decision for the bias voltage of the power stage is of great importance, since it is one of the two design parameters that defines the mode of operation of the PA, the other being the passive network, as discussed previously. There are a number of methods that can be used to choose a bias voltage. In this thesis the method used is by the trade-off of gain linearity versus quiescent current consumption.

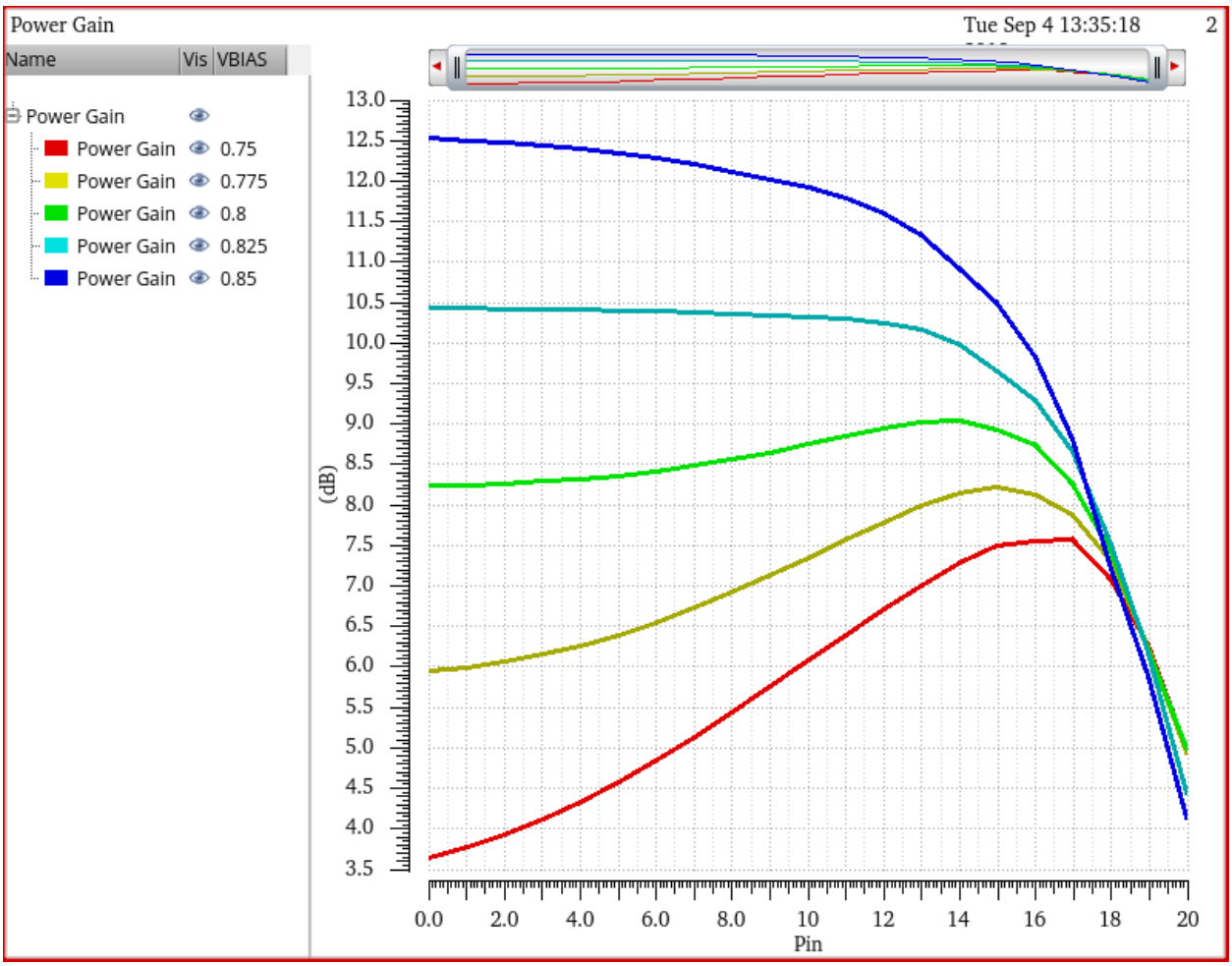


Figure 5.1 Simulated power gain for different bias voltages

In Figure 5.1 the gain of the power amplifier is simulated over a range of input power levels for different bias voltages. Depending on the bias voltage, the linearity of the gain varies. For a low bias (e.g. 750mV), initially the gain is small and shows a gradual expansion with rising power levels, until a maximum point is reached and before the region of compression. For a high bias (e.g. 850mV) the gain is significantly increased, however compression starts at much lower power levels. However, using a bias point between 810mv and 820mV a highly linear gain is achieved.

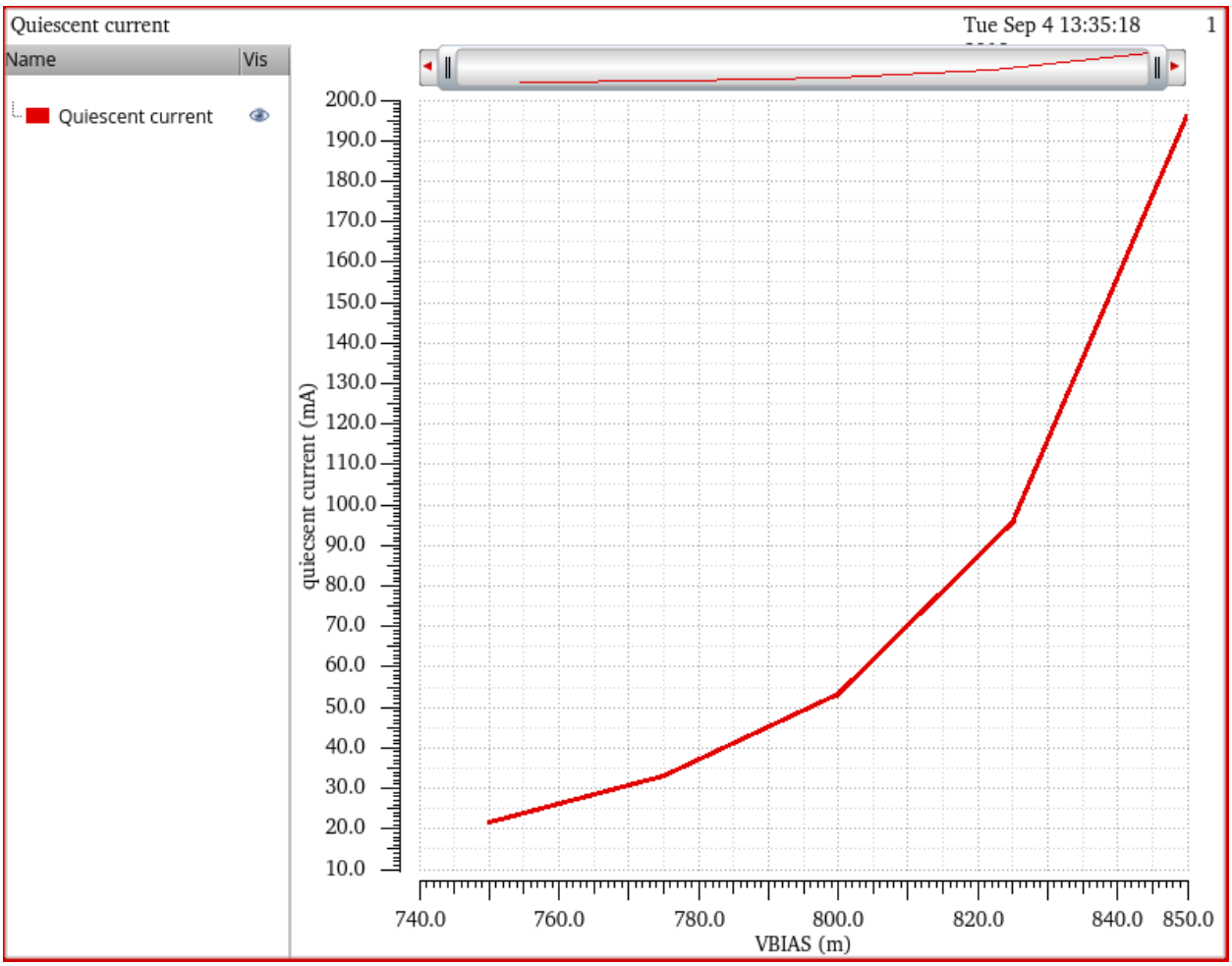


Figure 5.2 Quiescent current consumption versus bias voltage

Since however, the main goal of this design is back-off efficiency, the quiescent current consumption must be considered as well. In Figure 5.2 the quiescent current (current consumption at zero input signal) is measured for different bias voltages. If maximum gain linearity was a design goal, a bias point between 810mV and 820mV would be sought after. However, such a bias point would result in a rather high quiescent current and degraded back-off efficiency.

As discussed before, in order to implement the current clamping technique in the common base stage the quiescent current must be around $I_q = 0.1 \times I_{max}$. This means that a low bias voltage of $750mV$ will be used. The power amplifier will have to live with the gain expansion shown in Figure 5.1. The issue will be partially dealt with, using the driver stage in a following paragraph, however, it is not the end of the world. According to literature gain expansion can easily be treated using DPD.

5.1.1.3 Measurement of C_{BE}

In the discussion about current clamping in paragraph 3.2, the parasitic capacitance C_{BE} was assumed to be a constant. In reality, the C_{BE} varies with bias and signal level due to varactor-type effects. The non-linear nature of the varactor type effects in the emitter-base junction complicate not only the analysis of the circuit, but also the actual measurement of C_{BE}. In this subsection, the method of measurement of the large-signal value of C_{BE} is explained.

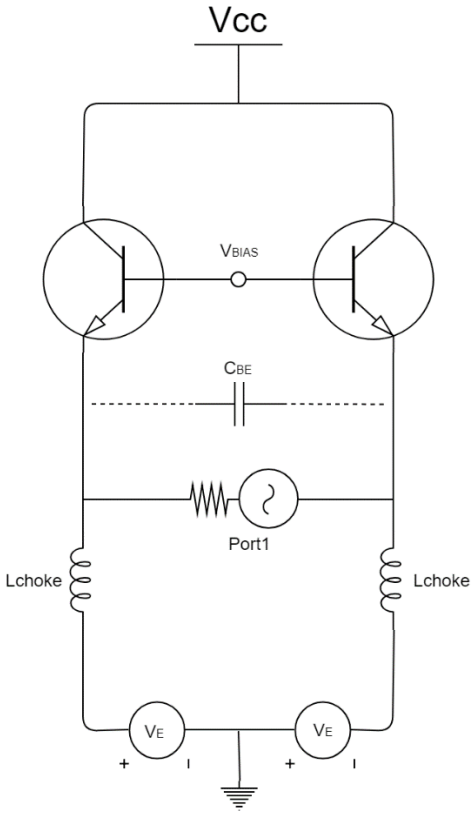


Figure 5.3 Setup for the measurement of C_{BE}

The setup used to measure C_{BE} is illustrated in Figure 5.3. Port 1 is used to directly measure the input capacitance of the push-pull stage by the input admittance Y_{11}. The small signal capacitance at 40GHz is measured as follows:

$$C_{be} = \frac{Imag(Y_{11})}{2 \times 3.1416 \times 40 \times 10^9}$$

Then a dc sweep is performed for V_E within the linear region of the transfer characteristic of the devices (in this case from -200mV to +200mV) and the average value of C_{be} is measured.

$$C_{BE} = avg(C_{be}) = 155.1fF$$

This method has been very useful for the accurate measurement of C_{BE}. Also, sing this method instead of a simple small-signal measurement, the insertion losses at large input signal levels are successfully minimized. A similar method can be used for the collector-base C_{CB} parasitic capacitance, although the variation of that capacitance is much smaller, and this complicated method is not needed in that case. As a result:

$$C_{CB} = 76{,}5fF$$

5.1.1.4 Output matching

Due to the non-linear relationship of V_{be} and I_{ce} it is inevitable that the collector current will have significant harmonic content. This harmonic content must be filtered out of the collector voltage waveform, so that the output power of the amplifier is not wasted on harmonics.

In order to achieve this, the output network will ideally have two functions:

- At the base frequency f0, it will present at the output of the amplifier its optimal load.
- At all the harmonics of f0 the output of the amplifier is shorted to the ground

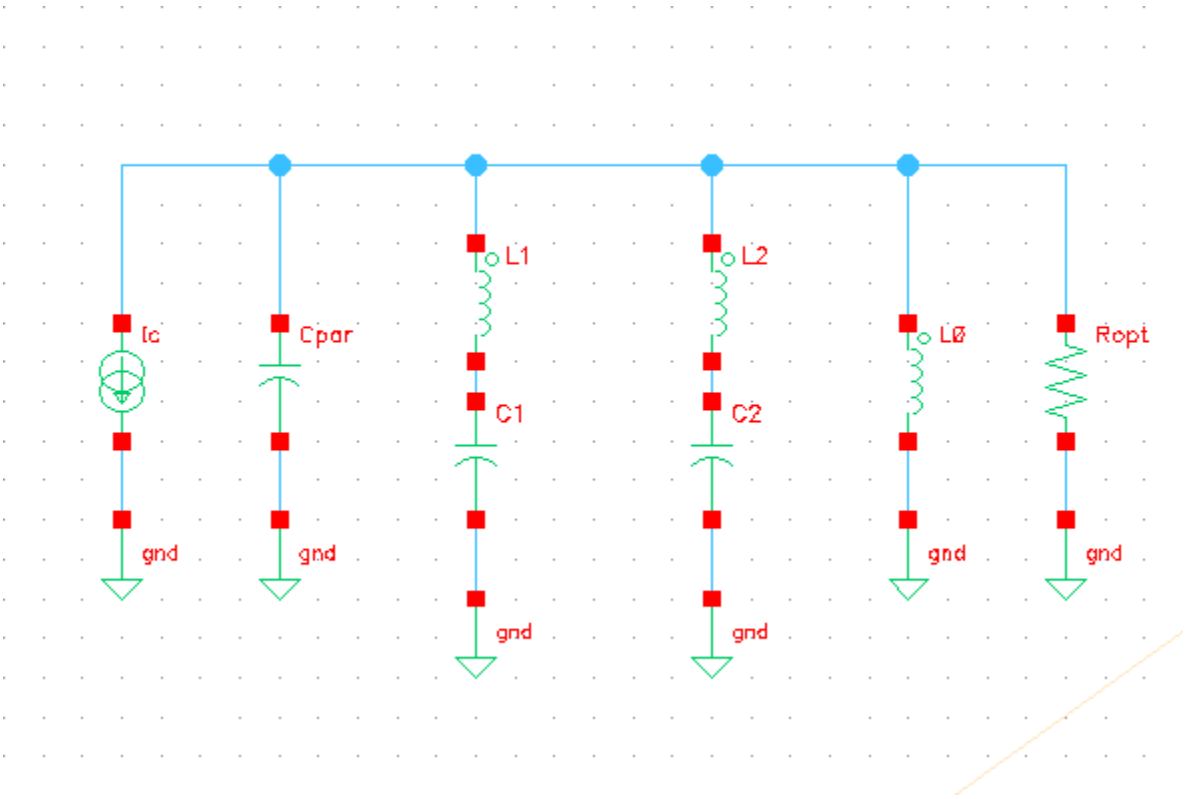


Figure 5.4 Equivalent circuit of commonly used output networks;I_C and C_{par} model the output of the active device.

Many designs of RF power amplifiers use a network that approximates these two functions, similar to what is shown on Figure 5.4. In this network:

- Ic and Cpar model the output of the active device
- C1, L1 and C2, L2 pairs form harmonic shorts. Each pair is tuned to one significant harmonic and shorts that harmonic to ground.
- Finally, the inductance L0 is used to tune the network at the base frequency f0, so that the impedance that Ic sees at f0 is equal to Ropt.

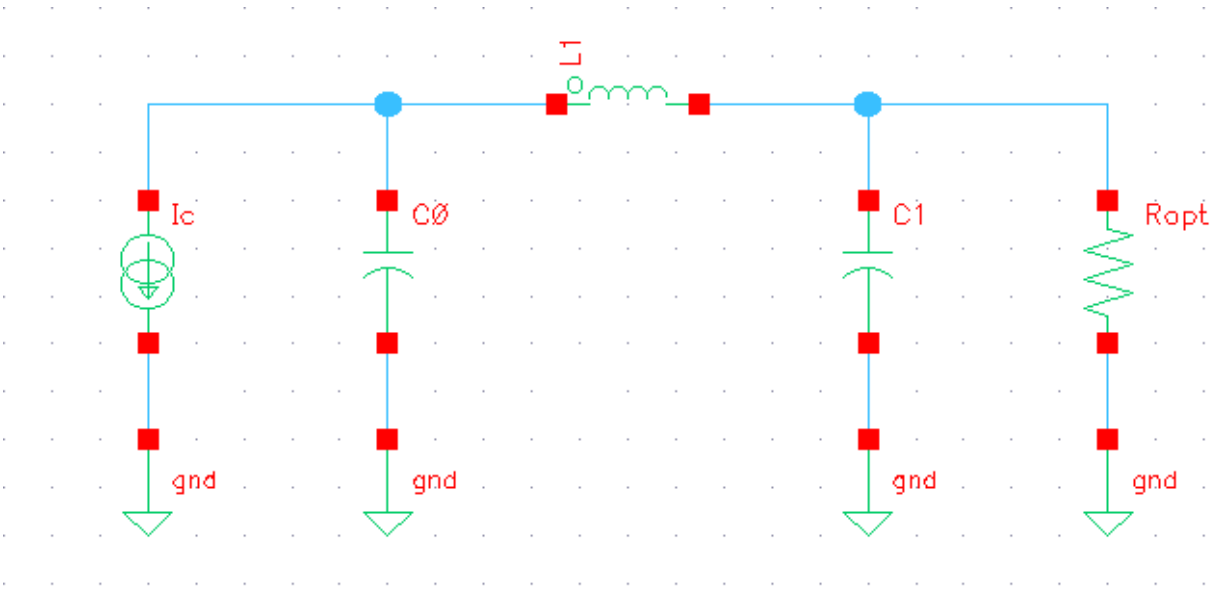


Figure 5.5 Equivalent circuit of output network used in this thesis; C_0 absorbs C_{par}

By using harmonic shorts, it is possible to eliminate the most significant harmonics, however they will also introduce losses reducing the output efficiency. Since the passive components used often have Q=17 or less at the target frequency, the use of harmonic shorts will be avoided and instead a simpler network will be used. In the network illustrated in Figure 5.5, C0 absorbs Cpar.

$$\frac{X_{C_0}}{Ropt} \geq 1 \tag{5.1}$$

In [1] extended analysis and simulations are performed on this type of output network. As long as equation (5.1) holds, it is possible to achieve power performance similar to the ideal.

5.1.1.5 Fundamental load impedance

It has been discussed previously, that it is possible in usual PA modes to predict and calculate the exact value of the optimal load impedance. The two parameters needed are the maximum collector voltage swing and current swing.

In this design it was difficult to exactly predict the value of the optimal load, since it is difficult to know before simulations the maximum current swing. The design parameters only define the maximum root mean square value for the collector current and in order to use that, the dc and fundamental components would have to be calculated, which is difficult to do by hand.

In order to overcome this obstacle, the load impedance was defined using simulations. A simple setup was used, as in Figure 5.6 with just the power stage and no driver stage. The ideal transformers at the input and output are simply used for matching and to convert single-ended to differential. At the collectors, two MIM capacitors were added in order to satisfy equation (5.1). A sweep of the input power was performed from the 10dB back-off point and until the saturation power is reached. The same simulation was performed for five loads with values between 20 Ohm and 50 Ohm. The performance figures used were the saturation power P_{sat}, the power gain and the total harmonic distortion of the collector voltage waveform.

The three figures form a tradeoff triangle. The maximum P_{sat} is reached at one load impedance only and slowly degrades as the load impedance deviates from that point. The power gain increases for higher load impedances, however the THD% will also increase.

In the end, the load impedance was decided to be around 35 Ohms. This was decided so that at the power level where the rms collector current meets the previously calculated constraint of 124mA, at that same level the voltage reaches its maximum output swing of about 3,6V. As a result:

$$R_{opt} \cong 35\ Ohm$$

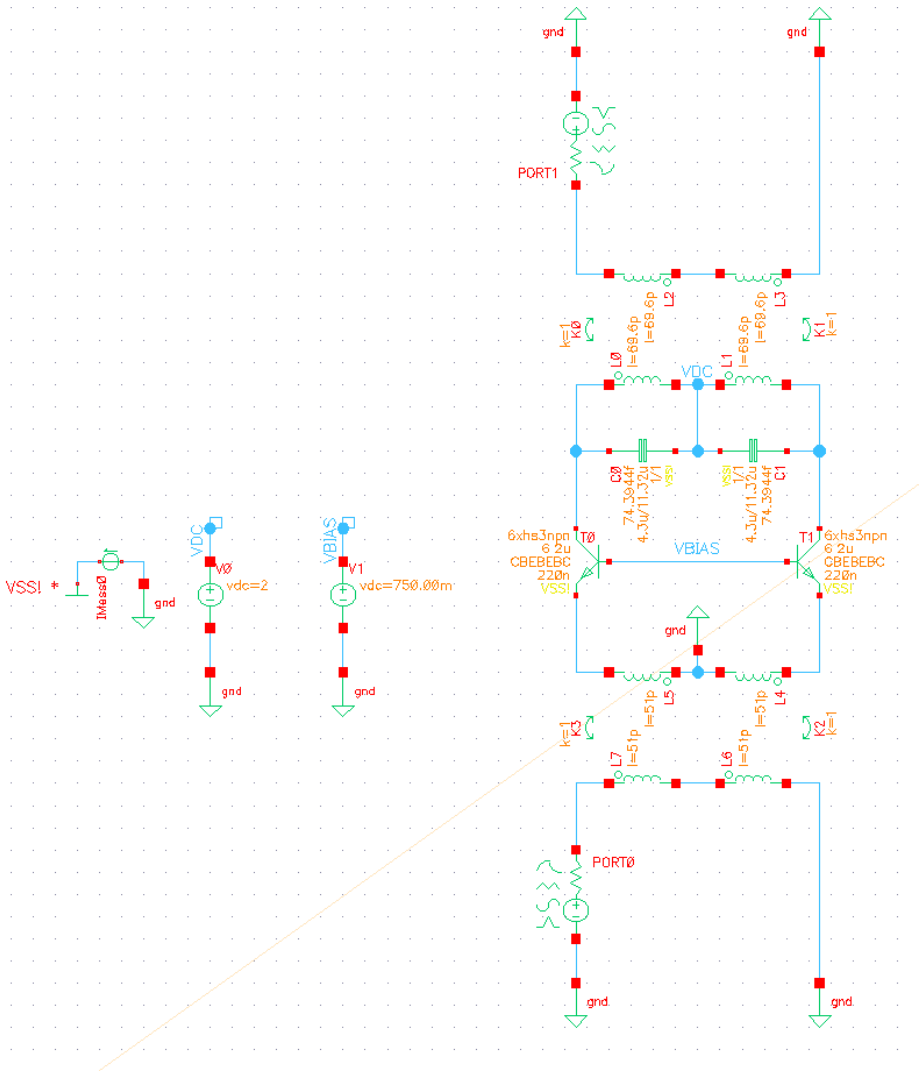


Figure 5.6 Test setup for power stage

Using that load impedance, the $P_{sat} = 24.8dBm$, close to its maximum value. The start of the compression region is at $22.25dBm$ so indeed the OP1dB point will be very close to the saturation. However due to the current restriction of 124mA, output powers greater than $22.25dBm$ should be avoided for timescales longer than $1\mu s$. Concerning the power gain, as expected it shows an expansion. At the start of compression, the maximum value of 7.6dB is reached, however at the 10dB back-off point the gain is reduced to 4.6dB. Finally, the THD% stays under 10% before the start of the compression region and then, as expected, it rises quickly as compression increases. However, the distortion is mainly due to even harmonics and is rejected in the output transformer. As result, the THD% at the load reaches a maximum of 10.5% at P_{sat}.

5.1.2 Interstage transformer

The driver stage of the power amplifier will be a cascode stage for reasons. However, the input impedance of the power stage is much smaller than the optimal impedance of the driver stage. In order to achieve a power match at the output of the driver stage, a 2:1 center-tapped transformer will be used.

Since the parasitic capacitance at the input of the power stage is approximately Cpar=155.1fF the secondary of the transformer will be:

$$L_s = \frac{1}{(2 * \pi * f)^2 * C_{par}} = 102pH$$

Also, for a 2:1 transformer the primary will be:

$$Lp = 2^2 * L_s = 408pH$$

Finally, in order to make the model of the c.t. transformer more realistic, the coupling factor will be set to k=0.8 and the Q=17.

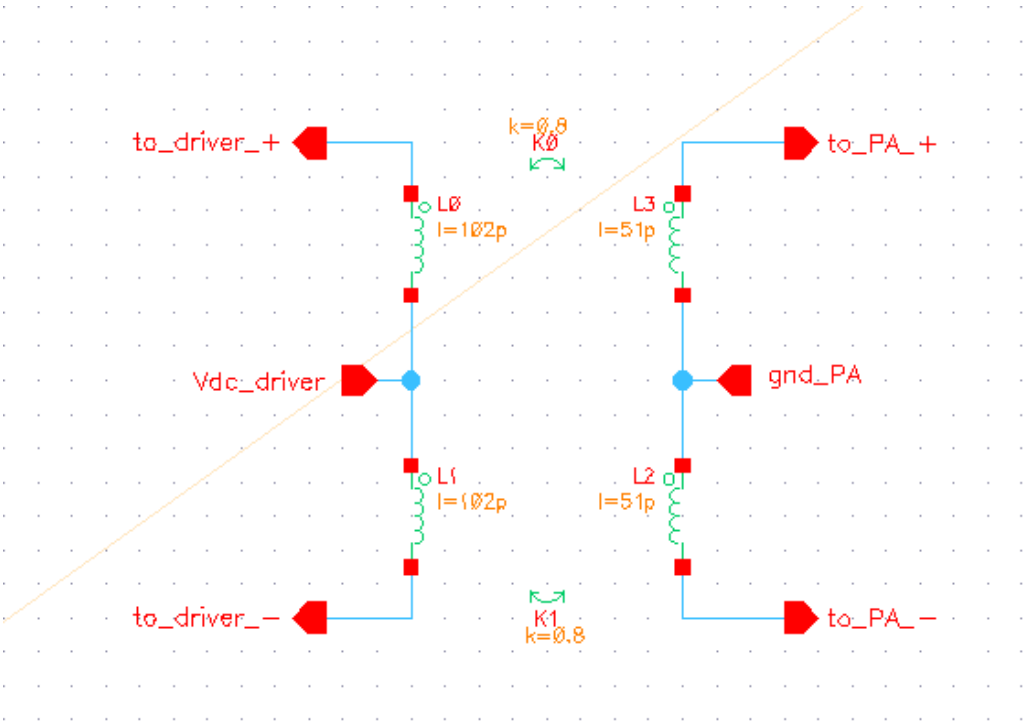


Figure 5.7 Interstage transformer model

5.1.3 Cascode driver stage

A cascode stage is selected to drive the power amplifier, due to its large gain and isolation. A simpler solution, for example a common emitter stage, would lack in both of these traits. As discussed in the previous section, the 2:1 interstage transformer is used in order to achieve a power match between the small input impedance of the power stage and the output of the driver stage. Moreover, two extra MIM capacitors will be used, in order to tune the transformer at the target frequency.

5.1.3.1 Device size

The size of the devices for the driver stage is decided, based on the current needed to drive the power amplifier. Since the common base stage is effectively a current buffer ($I_C \approx I_E$), normally devices of the same size would be needed in order to drive it. However, due to the 2:1 transformer the driving current demands are halved. Consequently, the size of the driver devices must be half that of the power amplifier devices.

The transistors of the driver are formed by 6 high-speed npn devices in parallel. The contact configuration is CBEBEBC (two emitters in each device). The emitter mask area is 0.22×3.1 μm^2 giving an effective emitter area of 0.13×3.01 μm^2.

5.1.3.2 Bias point

In paragraph 5.1.1.2 it was shown that for a higher bias voltage, the compression region starts earlier. Therefore, by setting the driver to a high bias, it is possible that the gain compression will partially cancel the gain expansion of the power stage, leading to an overall more linear gain.

In Figure 5.8 the gain of the power amplifier with its driver is simulated over a range of input power levels. By setting the bias point of the driver closer to class A, the gain linearity can be improved, and the overall gain is increased. As a result, the bias point is set at Vcasc0=800mV, close to class A, compromising some of the driver back-off efficiency.

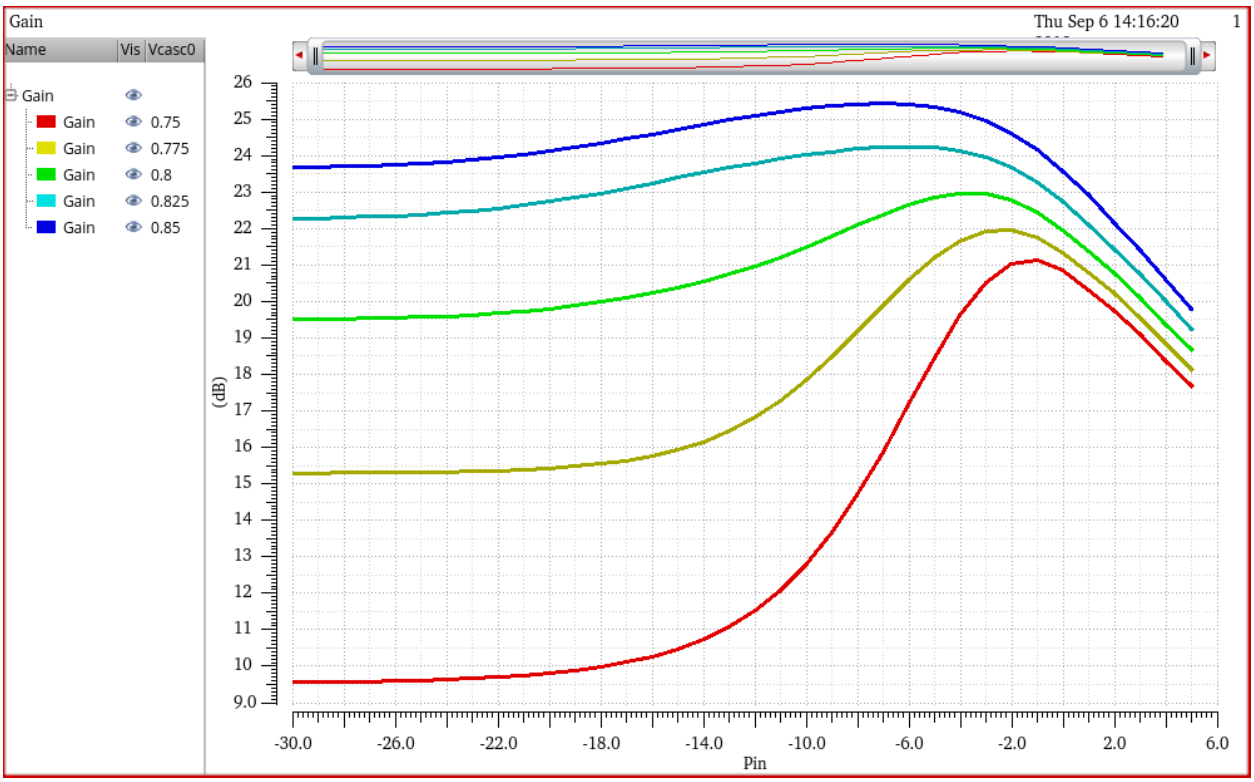


Figure 5.8 Gain of the power amplifier with its driver for different driver bias voltages versus input power

5.1.3.3 Driver input matching and filtering

The base-emitter junction of HBTs functions more like a varactor diode, rather than a fixed linear impedance. The consequence of simply tuning-out the average input capacitance of the driver, can be seen at the simulated base voltage waveform of the bottom driver transistors, in Figure 5.9. The voltage waveform looks half-way rectified, which hints the introduction of second harmonic content.

Using that observation, it may be possible to restore the sinusoidal waveform by placing a second-harmonic trap as close as possible to the base. The resulting voltage waveform at the base can be seen in Figure 5.10. The waveform looks slightly more sinusoidal than before, however the success of the harmonic trap is limited. This happens due to the low Q of the elements that form the trap, but more importantly, the trap does not filter higher order harmonics.

Input varactor effects are discussed in [1]. According to this discussion, the act of tuning the fundamental will automatically change the harmonic environment as well, which will in turn affect power, efficiency and linearity. However, by using the harmonic short, the harmonic environment gains some independence (at least for the second, most significant harmonic) from the tuning of the fundamental. This independence will in the next section simplify the design of the input quadrature hybrid, by allowing the input of the driver to be treated as a simple fixed linear impedance.

As a final addition, a center tapped transformer is used to convert the input impedance of the driver to 50Ω. The full circuit of the power amplifier with its driver can be seen in Figure 5.11.

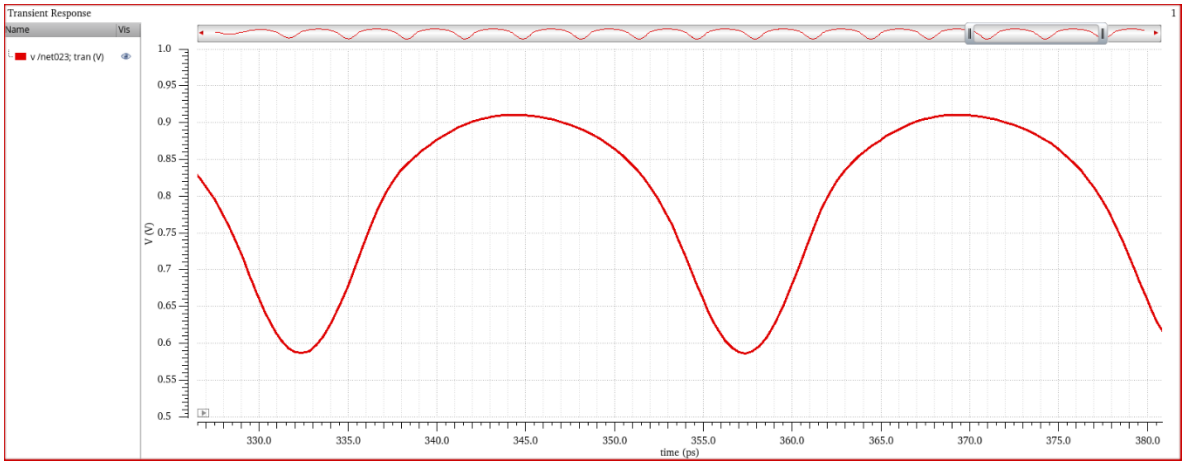


Figure 5.9 Voltage waveform at the input of the Driver, without harmonic traps

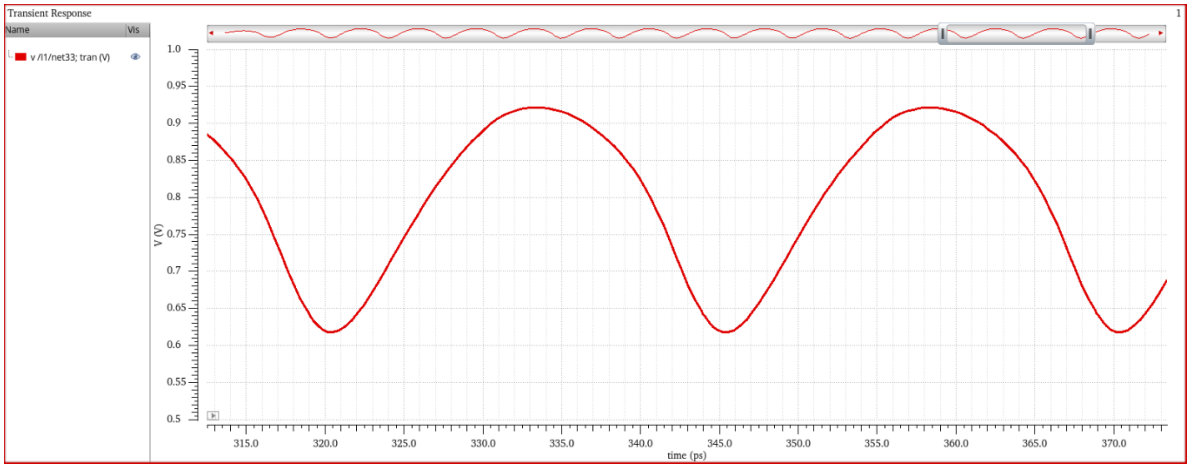


Figure 5.10 Voltage waveform at the input of the Driver, with harmonic traps

Common Base power stage

Interstage transformer with tuning MIM caps

Cascode driver stage

Input 2nd harmonic traps

Input matching transformer

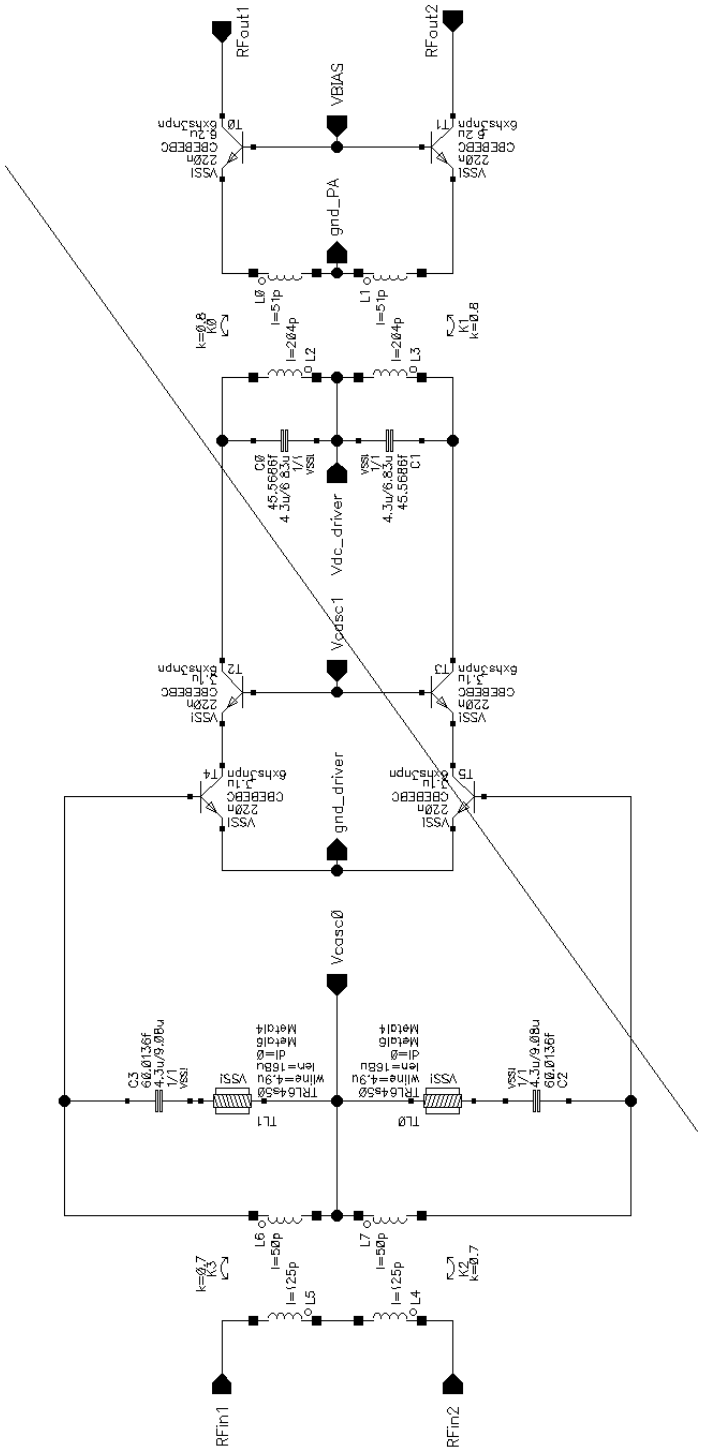


Figure 5.11 Full schematic of Main power amplifier

5.2 On-chip Doherty input network

The input network of a Doherty amplifier is usually a power splitting quadrature hybrid. It is used to perform equal power splitting and phasing between the main and auxiliary path. Since the power amplifier designed in the previous section has a differential (push-pull) architecture, a differential quadrature hybrid [8] is used that creates four phases, 0˚, -180˚, 90˚ and -90˚.

5.2.1 Single ended transformer-based quadrature generation

The simplified circuit of a single-ended quadrature generator can be seen in Figure 5.12. The input signal from port0m is split into Z_1 and Z_2 where:

$$Z_1 = j\omega L_1 || R_1,\ Z_2 = \frac{1}{j\omega C_2} || R_2$$

As a result the voltage across R1

$$V_1 = V_0 * \frac{Z_1}{R_0 + Z_1 + Z_2}$$

And across R2

$$V_2 = V_0 * \frac{Z_2}{R_0 + Z_1 + Z_2}$$

For equal power dividing and 90˚ phase between the two output ports (R1 and R2) :

$$\frac{V_1}{V_2} = 1 < 90^\circ = j \rightarrow \frac{Z_1}{Z_2} = j \qquad (5.2)$$

Moreover, to ensure that port0 is matched to 50Ω

$$Z_1 + Z_2 = 50\Omega \qquad (5.3)$$

For $R_0 = R_1 = R_2 = 50\Omega$ equations (5.2) & (5.3) are satisfied if $X_{L_1} = -X_{C_2} = 50\Omega$. The inductor L1 can be replaced by a transformer, achieving separation between the two output ports, as in Figure 5.13. According to [8] a high coupling coefficient (k≥0.9) transformer with a 1:1 turn ratio can be used for that purpose.

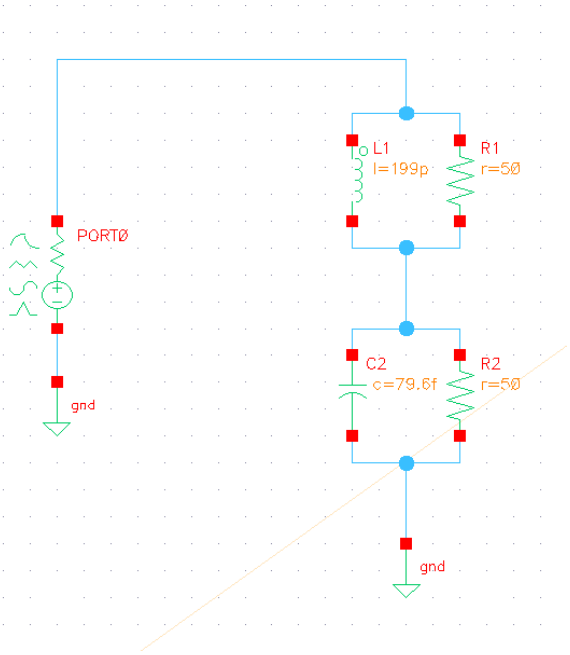


Figure 5.12 Transformer-less single ended quadrature generator

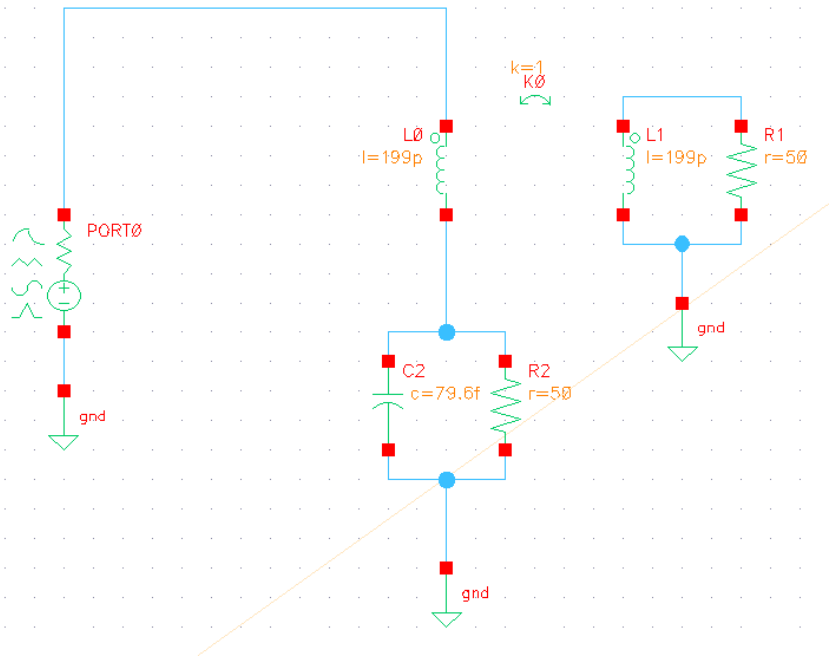


Figure 5.13 Transformer-based single ended quadrature generator

5.2.2 Fully differential transformer-based quadrature generation

Differential operation can be achieved by simply placing two identical single-ended quadrature generation blocks side-by-side and then the shunt capacitors can be combined into one. Moreover, the constructive magnetic coupling of the two transformers can be utilized, in order to implement them in only one inductor footprint, significantly increasing the compactness of the design. For the performance simulations in the next chapter, the equivalent circuit in Figure 2.1 is used.

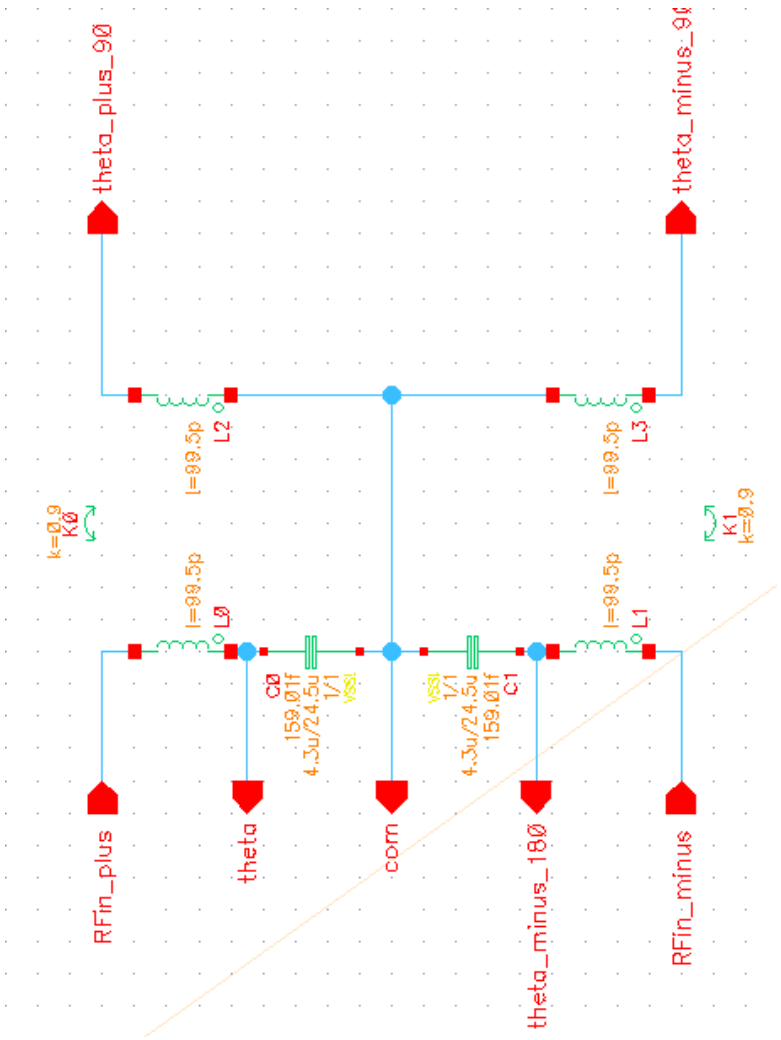


Figure 5.14 Equivalent circuit of differential quadrature generator

5.3 On-chip Doherty output network

At first implementations of the Doherty architecture in this thesis, a conventional approach was used to the Doherty output network. However, a disadvantage of the conventional approach quickly emerged: the high impedance transformation ratio (ITR), in power back-off (PBO):

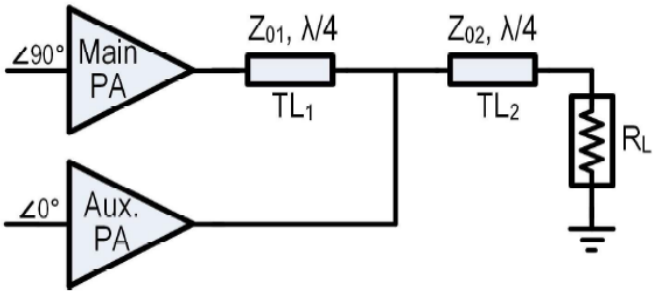


Figure 5.15 Conventional Doherty output network. TL1 is the impedance inverter that performs the load modulation. TL2 is simply used to transform the R_L into half the optimal impedance.

The characteristic impedances of TL1 and TL2 are

$$Z_{01} = R_{opt}, Z_{02} = \sqrt{\frac{R_{opt}R_L}{2}}$$

In PBO TL2 transforms R_L into $\frac{R_{opt}}{2}$ and TL1 transforms that into $2R_{opt}$ (since in PBO the aux. PA is off, and its output impedance is much larger than $\frac{R_{opt}}{2}$). As a result, the ITR of TL1 at PBO is

$$\frac{2R_{opt}}{\frac{R_{opt}}{2}} = 4$$

The repercussion of the high ITR is the compromised bandwidth that the DPA architecture is well known for. Also, due to TL1 the main PA output will experience more passive losses than the aux. PA, which means that at PBO the passive efficiency is degraded.

In [10] a modified design is introduced Figure 5.16 that enhances the passive efficiency in PBO and enlarges the bandwidth. What is more, a previous work has already managed to integrate the modified design, in a broadband and low-loss on-chip Doherty output network.

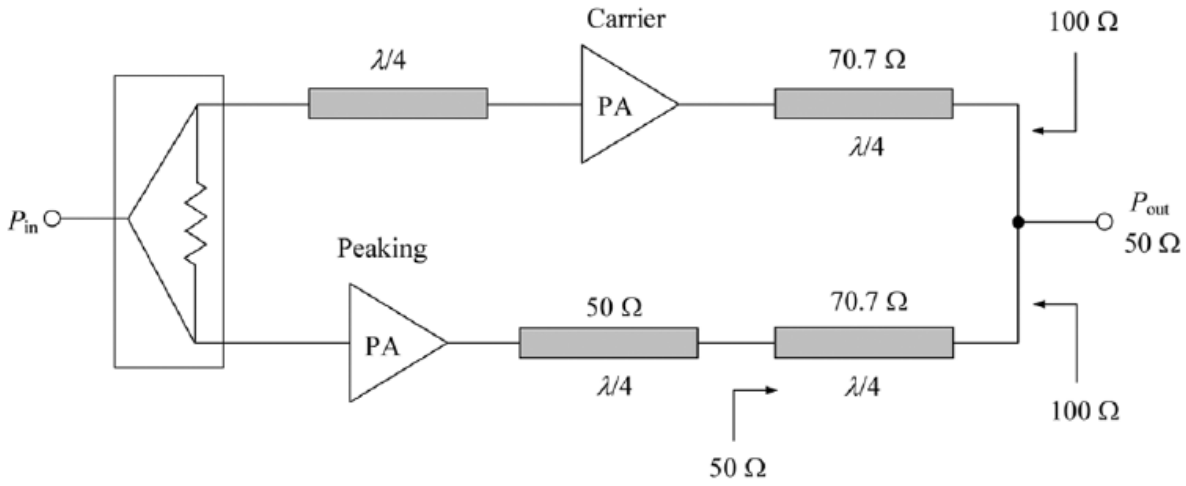


Figure 5.16 Grebennikov's dual band Doherty PA

5.3.1 Transformer-based modified-Doherty output network

The introduced design in [6] uses a transformer-based modified Doherty output network to implement the modified DPA from [10], in order to reduce ITRs in PBO, improving PBO passive efficiency and broadening the Doherty PA carrier bandwidth. Basically, the transmission lines are first approximated by lumped elements and then absorbed into two on-chip transformers to achieve compactness.

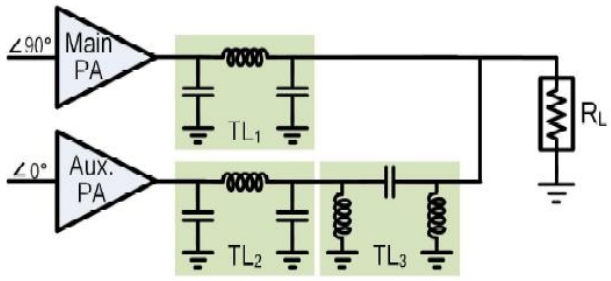


Figure 5.17 Approximation of quarter wave TLs with lumped elements

5.3.2 Calculations

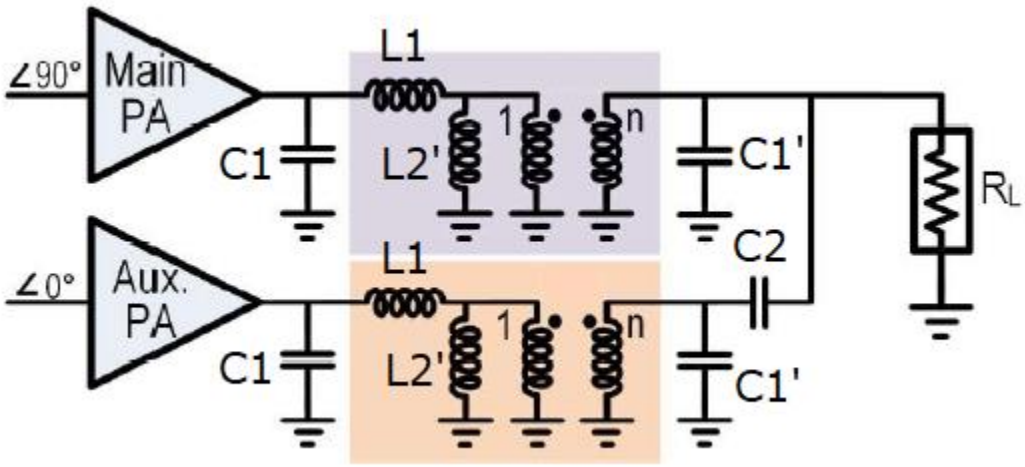


Figure 5.18 Equivalent circuit used for calculations

- Transmission lines 1&2

TLs 1&2 are formed by C1, L1 and C1'. It has already been calculated in paragraph 5.1.1.4 that C1 must have a capacitive reactance of 35Ω. As a result:

$$Z_{T1,2} = 35\ Ohms$$

$$C_1 = \frac{1}{\omega \times Z_{T1,2}} = 114fF$$

$$L_1 = \frac{Z_{T1,2}}{\omega} = 139pH$$

- Transmission line 3

TL 3 is formed by C2, L2 and L2'. It is known that $Z_{T3} = 2R_L = 100\Omega$. As a result:

$$C_2 = \frac{1}{\omega \times Z_{T3}} = 39.8fF$$

$$L_2 = \frac{Z_{T3}}{\omega} = 398pH$$

- Ideal transformer

  TL 1&2 will transform R_{opt} to $R'_{opt} = \frac{Z_{T1,2}^2}{R_{opt}} = R_{opt}$

  TL 3 will transform $2R_L$ to $\frac{Z_{T3}^2}{2R_L} = 2R_L$

  And the ideal transformer will have $n^2 = \frac{2R_L}{R'_{opt}} = 2.86$

  As a result:

$$L'_2 = \frac{L_2}{n^2} = 139pH$$

$$C'_1 = \frac{C_1}{n^2} = 39.9fF$$

- Output Doherty network

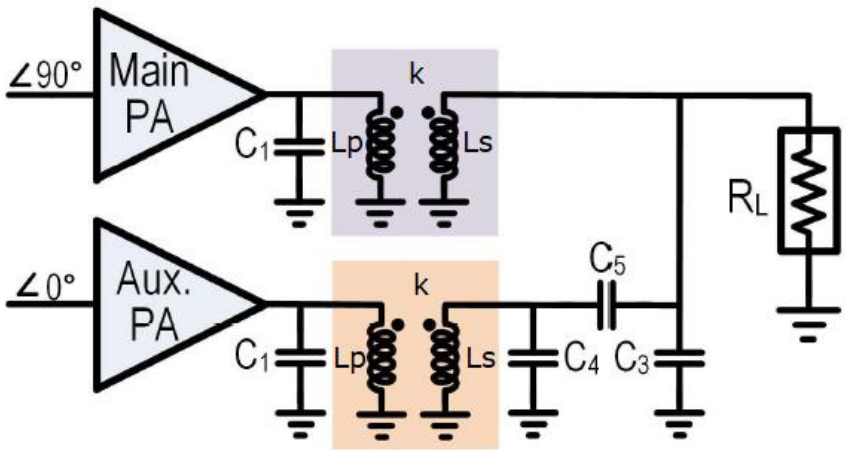


Figure 5.19 Output Doherty network

The values for the components are:

$$C_1 = 114fF, C_3 = C_4 = C'_1 = 39.9fF$$

$$L_p = L_1 + L'_2 = 278pH, k = \sqrt{\frac{L'_2}{L_1 + L'_2}} = 0.707, L_s = (n \times k)^2 L_p = 397pH$$

5.4 Auxiliary power amplifier

As discussed in 3.1.4 designing the auxiliary PA is not as simple as biasing the auxiliary devices in Class C. A simple method to implement the auxiliary PA function is to assume an external signal that will dynamically bias the auxiliary devices.

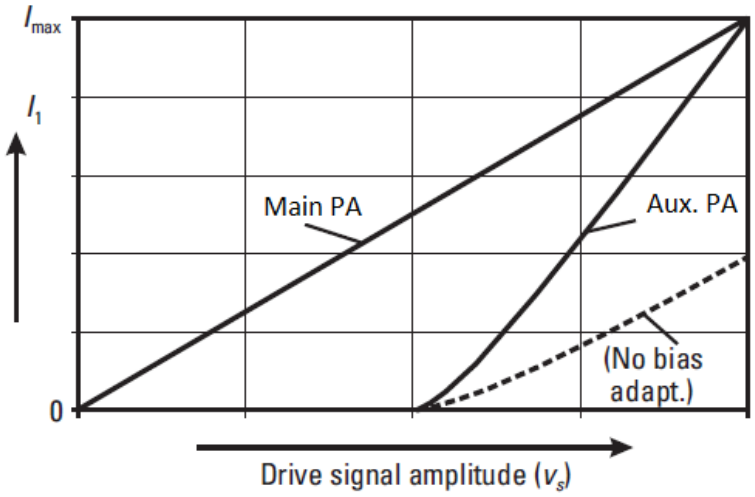


Figure 5.20 The main and auxiliary transfer functions; the dashed line is the transfer function of the auxiliary PA when simply biased in class C

The bias voltage of the auxiliary PA is varied as follows:

- At back off powers the auxiliary PA is simply biased in class C.
- After the 6dB point, the bias is gradually increased as input power increases.
- At maximum input drive the auxiliary and main PAs are biased at the same point and as a result they output the same current

In this thesis the dynamic bias is simply provided by a dc voltage source, dependent on the input power. Apart from the dynamic bias, the schematic of the auxiliary amplifier is exactly the same as the main PA.

6 Performance Simulation Results

6.1 Main power amplifier performance

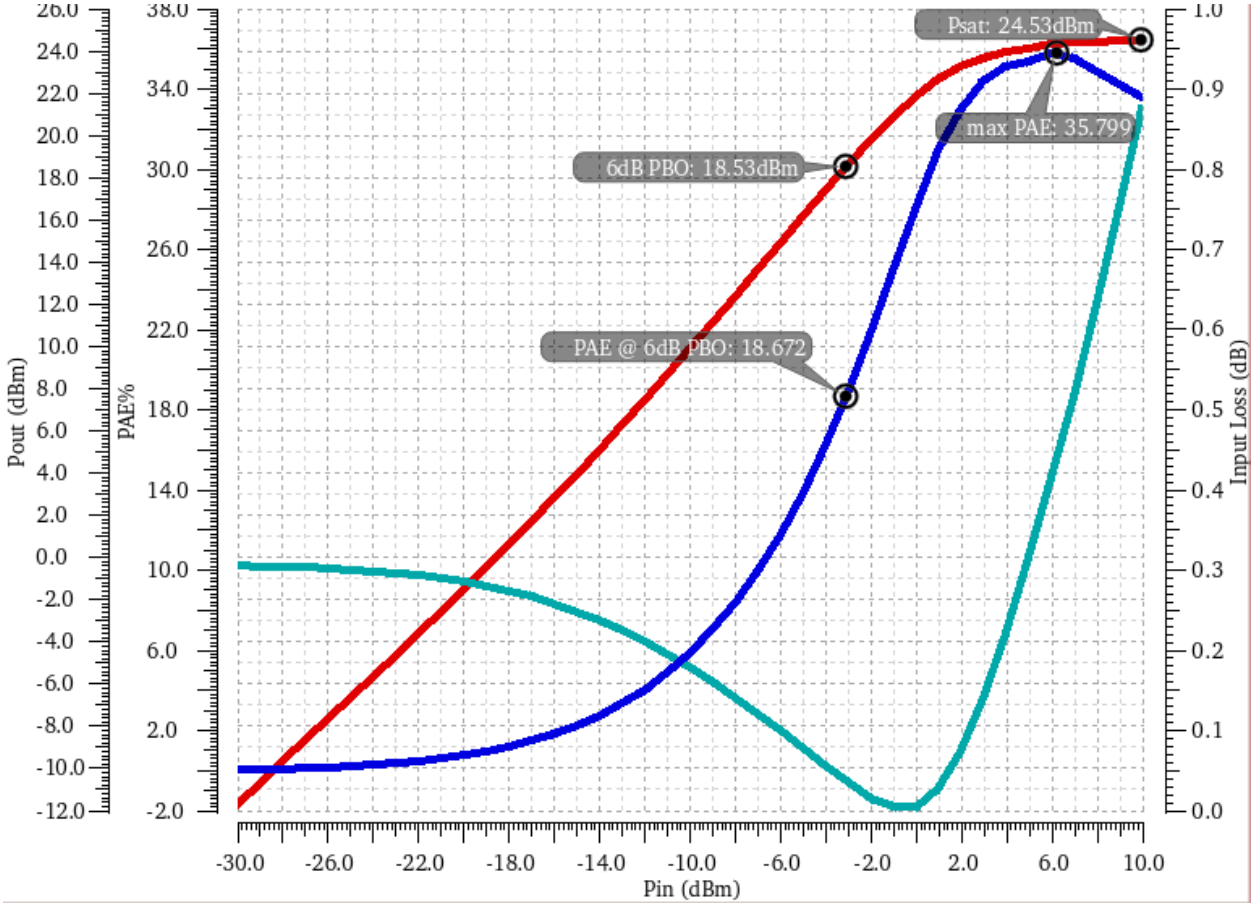


Figure 6.1Power performance of main PA

The power performance of the main PA is illustrated in Figure 6.1. The x-axis is the input power P_{in} (dBm). The red line is the output power P_{out} (dBm). The main PA reaches a saturation power of 24.5dBm, easily satisfying the output-power requirements. An impressive point is the hard transition, between the linear region and the saturation region happening at about $P_{in} = 0dBm$ and $P_{out} = 22dBm$. This means that the main amplifier can utilize more of its output power without getting into compression. In comparison common-emitter stages suffer from soft saturation, meaning that compression starts much earlier. This advantage of the common-base was predicted theoretically in paragraph 2.6.2 and is due to the linear current gain.

The light-blue line depicts the insertion losses to the power amplifier. It can be seen that the losses are very low (approx. 0.3dB) at back-off powers. The input loss reduces as the amplifier approaches the high-power region and becomes zero at the end of the linear region, at $P_{in} = 0dBm$. Then as the PA gets into deep compression, the input loss starts to increase again. The input losses are minimized at the high-power region, rather than at the small signal region, thanks to the method used to calculate the input parasitic capacitance, as explained in paragraph 5.1.1.3.

Finally, the blue line is the PAE% of the main PA, taking into account all dc power consumption from power supplies and bias sources, as well as the input RF power. The maximum PAE is about 35.8%. The PAE% was also measured at the output referred 6dB back-off point, OP=18.53dBm. At that point the PAE%=18.7. This means that the PAE has only halved at the 6dB PBO, demonstrating the back-off efficiency enhancement that the current clamping achieves. The efficiency halving at the 6dB PBO point is indeed very similar to the behavior of a class B amplifier and agrees with the theoretical results derived in paragraph 3.2.

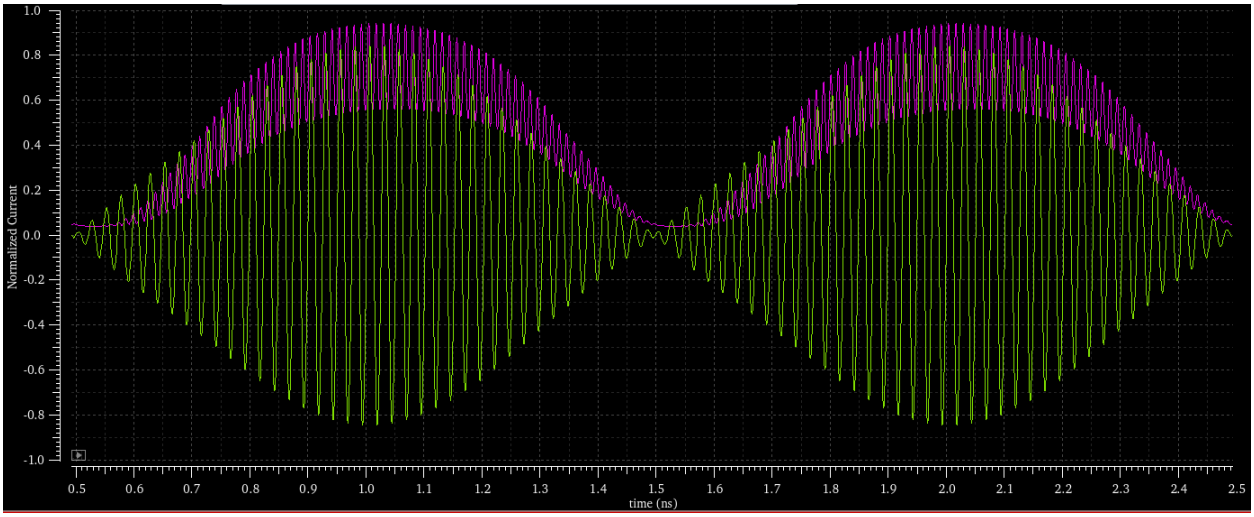


Figure 6.2Normalized input current and current consumption

A great way to see the current-clamping action of the power stage is to create an input signal of varying power and then look at the current consumption of the power stage. This experiment is performed in Figure 6.2. The yellow waveform is the input signal, created by two tones of equal power, one at 39GHz and one at 40GHz. The result is a periodic waveform with varying envelope. The purple waveform is the current consumption of the power stage, measured at its power supply. It can be seen how the average value of the current consumption quickly tracks the envelope of the input signal. At low input power, the current consumption is significantly reduced and when the input power rises, the current consumption rises to cover the demand for higher output power.

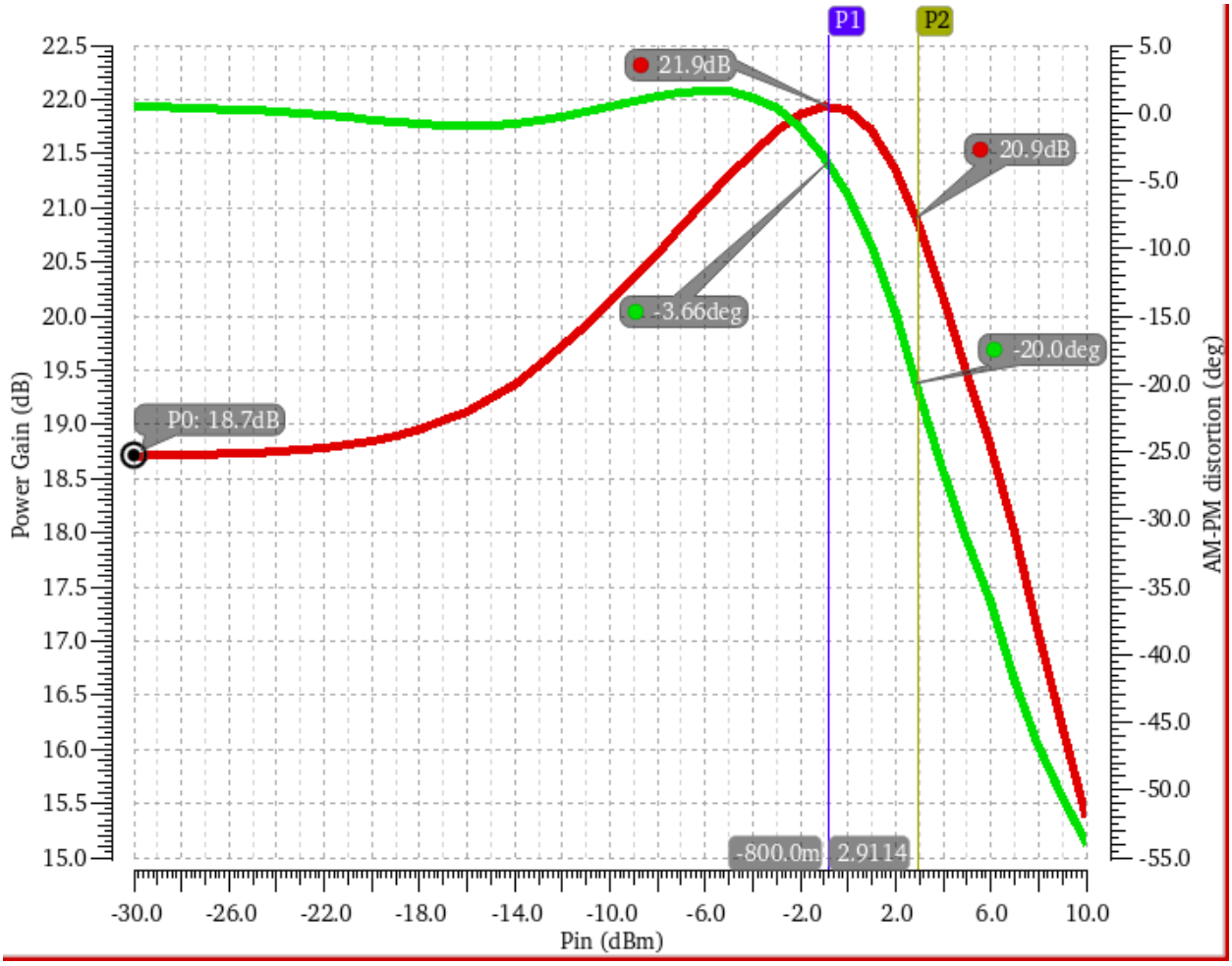


Figure 6.3 Gain and AM-PM distortion

In Figure 6.3 the red line is the gain of the main PA over a sweep of input power. At back-off powers the gain is 18.7dB and as the input power rises, the gain starts expanding. The start of the compression region can be found at the point where the gain maximizes, and the maximum gain is 21.9dB. The total gain expansion is 3.2 dB.

The green waveform is the phase of the fundamental at the output load and can be used to measure the AM-PM distortion. Until the start of the compression region the phase is fairly flat and as the amplifier enters the compression region the phase starts decreasing. At the OP1dB compression point, at $P_{in} = 3dBm$, the AM-PM distortion is 20 degrees.

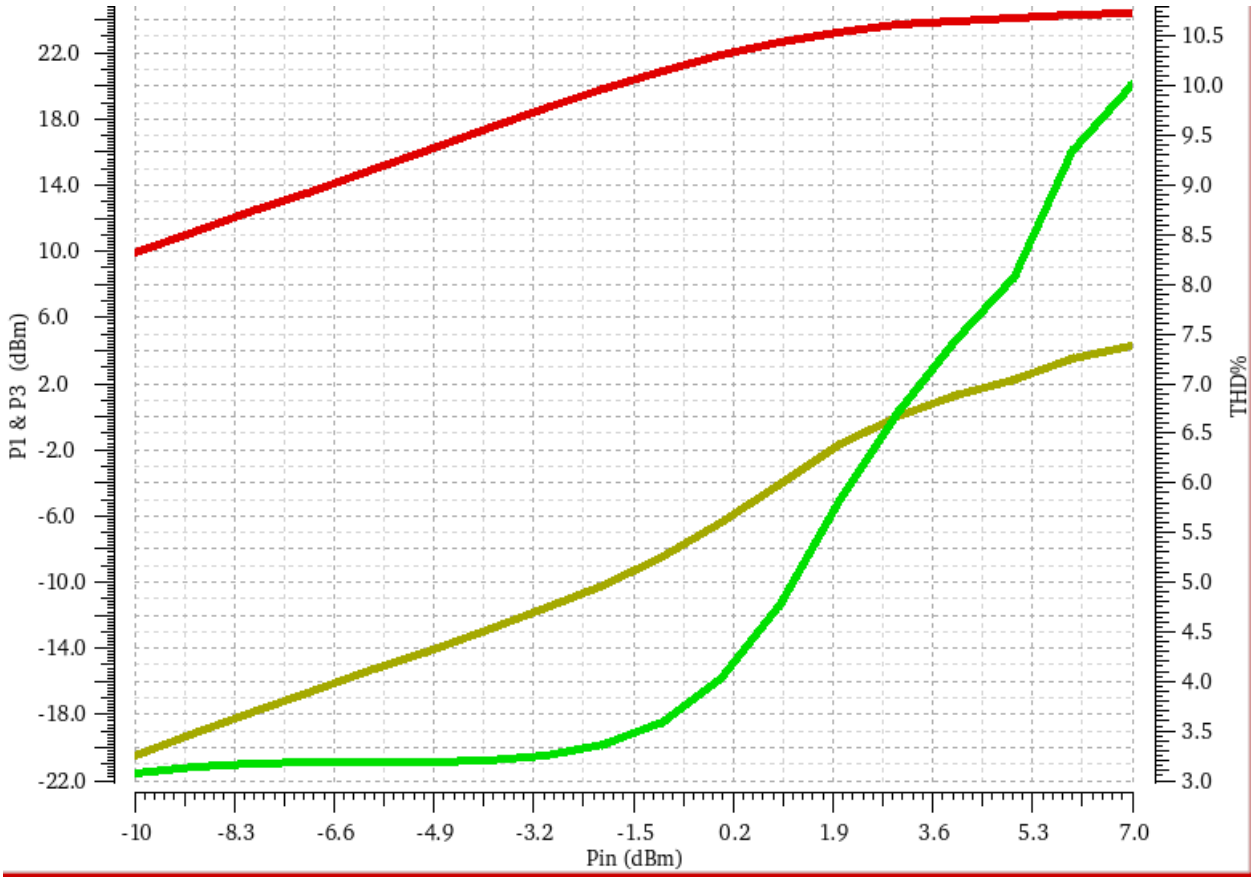


Figure 6.4 Harmonic distortion

In Figure 6.4 the harmonic distortion of the output power over a sweep of input power is measured. The red waveform is the power at the fundamental. Due to the differential architecture all even harmonics are rejected, and the most significant harmonic is the third, illustrated in the yellow waveform. The difference between the fundamental and third harmonic powers is 30dB before the compression region. In the compression region the third harmonic increases rapidly and at the saturation power the difference between the fundamental and the third harmonic is 20dB. Finally, in the green waveform, the total harmonic distortion of the voltage waveform at the load is measured. It is low before the compression region and then starts increasing rapidly.

6.2 Doherty power amplifier performance

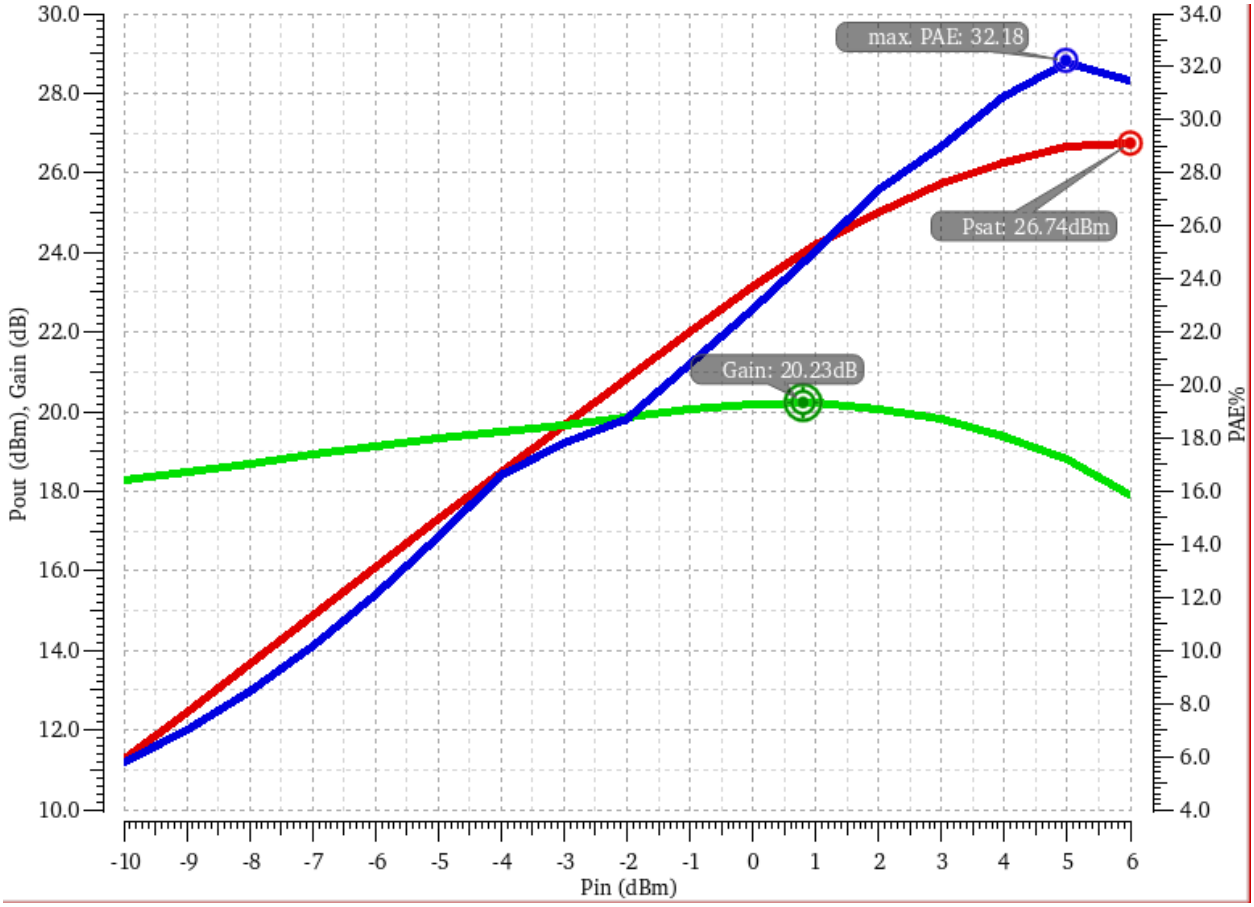


Figure 6.5 Power performance of the DPA

The performance of the full DPA is illustrated in Figure 6.5 over a sweep of the input power. The red waveform is the output power at the fundamental. The DPA reaches a saturation power of 26.74dBm, well over the 20dBm requirements for this thesis. The PAE% is in the blue waveform, showing a maximum value of 32.2%. This is very close to the maximum PAE of the main PA showing that the maximum PAE was not compromised in this design. At the point of 7dB output-referred PBO, at about $P_{in} = -3dBm$, the output efficiency shows its second maximum, however that is not too visible in the PAE%, due to the power consumption of the drivers. Finally, the green waveform illustrates the gain of the DPA. Again the gain shows an expansion, similarly to the main PA, and shows a maximum of 20.2dB at $P_{in} = 1dBm$. The OP1dB compression point is reached at $P_{in} = 4.5dBm$, very close to the point of saturation.

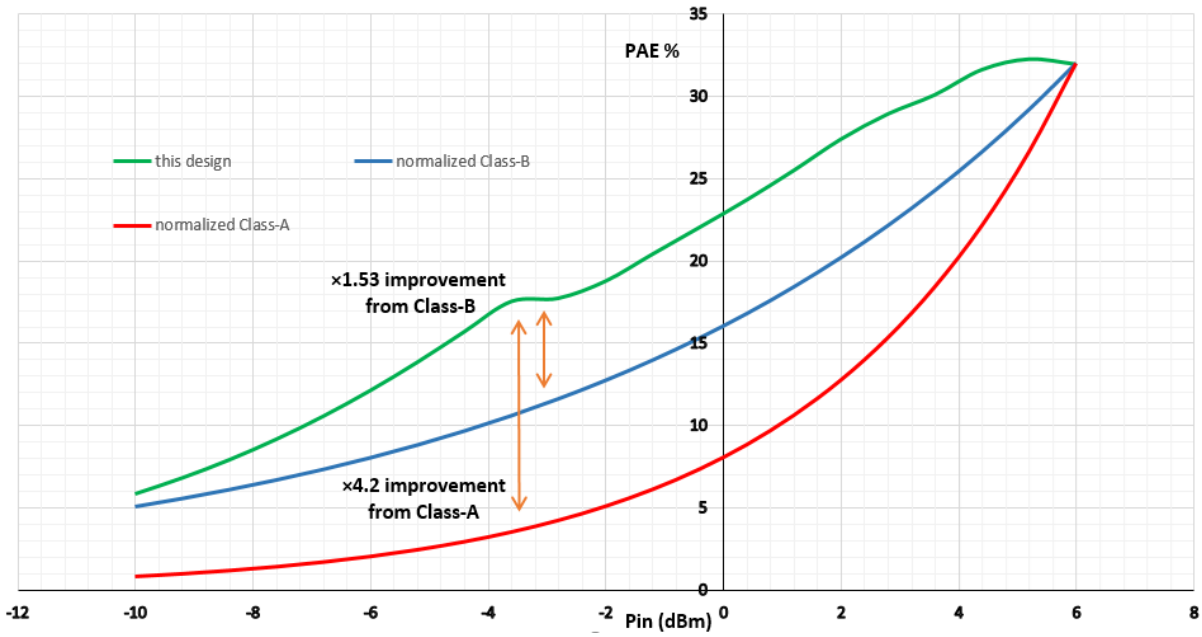


Figure 6.6 Power added efficiency improvement

The improvement in PAE% can be seen in Figure 6.6. The green waveform is the PAE% of the designed DPA. The blue waveform is the normalized output efficiency of an ideal class B PA. The green waveform is the normalized output efficiency of an ideal class A. The improvement in PAE is compromised by the power consumption of the drivers which are biased close to class A. Still at the output referred 6dB PBO point, at $P_{in} = -3dB$ the PAE is improved by factor of 1.53 from the class B and by a factor of 4.2 from the class A.

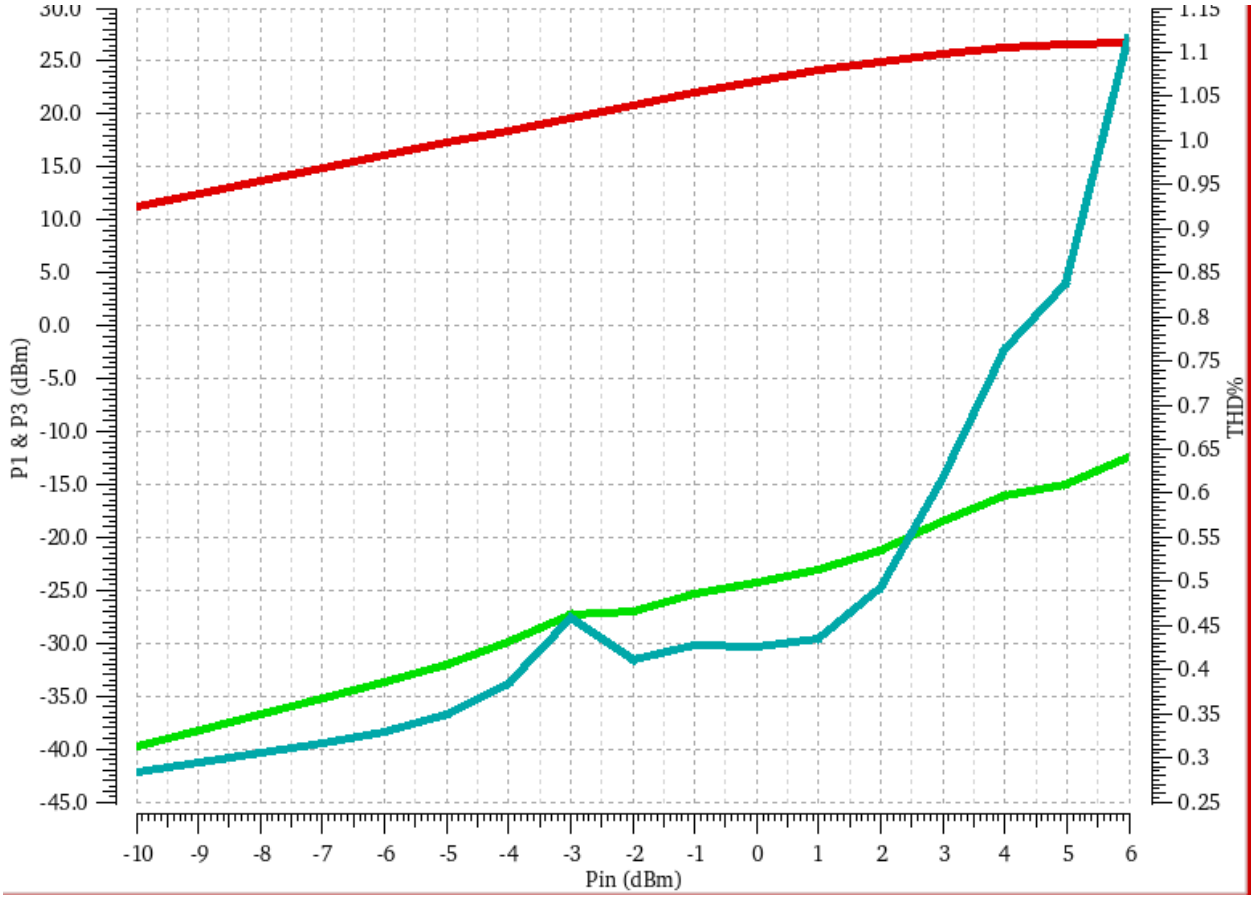


Figure 6.7 Harmonic distortion in the DPA

The harmonic distortion of the DPA over a sweep of the input power is illustrated in Figure 6.7. The red waveform is the power at the fundamental. The most significant harmonic is again the third, illustrated in the green waveform. The difference between the fundamental and third harmonic powers is more than 45dB before the compression region. At the saturation power the difference between the fundamental and the third harmonic is 40dB. Finally, in the light-blue waveform, the total harmonic distortion of the voltage waveform at the load is measured. It stays below 1% for almost the entire range.

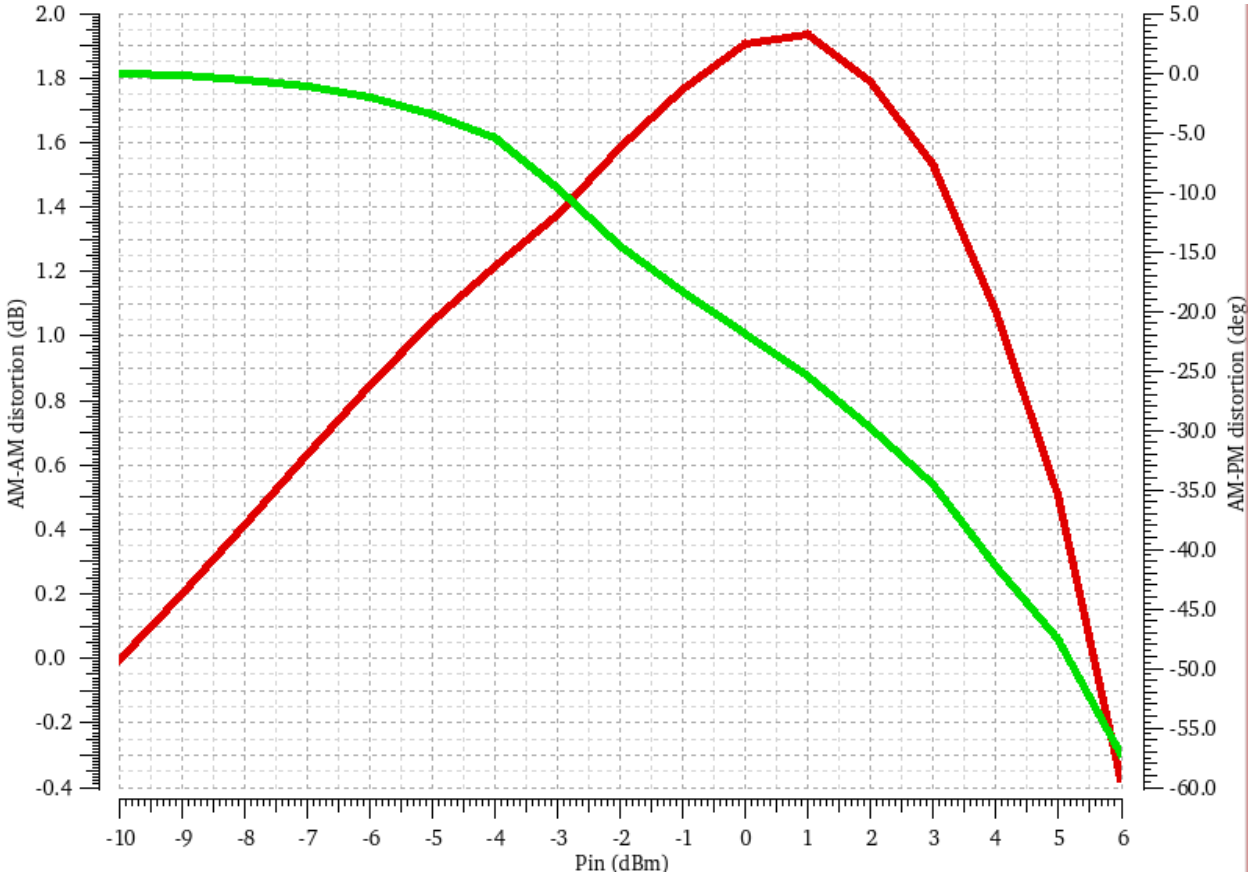


Figure 6.8 AM-AM and AM-PM distortion

The AM-AM and AM-PM distortion is shown in Figure 6.8. The gain expansion of about 2dB creates the AM-AM distortion shown in the red waveform. The green waveform shows the AM-PM distortion and is very large. The AM-PM distortion should not be that large given the fact that the main PA has very low AM-PM distortion. It is suspected that the reason for this result is the input termination of the main and auxiliary PAs by the quadrature generator and more investigation is needed in order to improve it.

7 Conclusions

In this thesis the design of a 40GHz Doherty power amplifier is presented. For the design of the Doherty power amplifier, it was necessary to first design a main power amplifier. Due to the common-base configuration used, the main PA was able to deliver satisfactory output power and by using the current-clamping technique the PAE efficiency rolls off slowly at the back-off. Consequently, it must be said that the common-base PA designed here is a very good trade-off between design complexity and back-off efficiency enhancement.

The DPA designed did successfully improve further the back-off efficiency and is an overall promising solution for energy efficient 5G applications in the 40GHz band. Next steps in this design will include implementation of the transformers and the dynamic-biasing circuitry with components available by the technology. Further research must be made in order to reduce the AM-AM and AM-PM distortion in the final design.

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