

# Εθνικο Μετσοβιο Πολυτεχνειο

ΤΜΗΜΑ ΗΛΕΚΤΡΟΛΟΓΩΝ ΜΗΧΑΝΙΚΩΝ ΚΑΙ ΜΗΧΑΝΙΚΩΝ ΥΠΟΛΟΓΙΣΤΩΝ

Τομέας Επικοινωνιών, Ηλεκτρονικής και Συστημάτων Πληροφορικής
Εργαστήριο Ηλεκτρονικής


# Σχεδίαση και Υλοποίηση Ενισχυτή Ισχύος στη Μπάντα FR3 για Μελλοντικές Εφαρμογές 5G/6G σε Τεχνολογία 22nm CMOS FD-SOI

ΔΙΠΛΩΜΑΤΙΚΗ ΕΡΓΑΣΙΑ

του


**Απόστολου Ε. Χρήστου**

**Επιβλέπων**: Γεώργιος Δ. Παναγόπουλος
Επίκουρος Καθηγητής Ε.Μ.Π.


Αθήνα, Ιούλιος 2025

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Εγκρίθηκε από την τριμελή εξεταστική επιτροπή την 3η Ιουλίου 2025

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**Απόστολος Ε. Χρήστου**
Διπλωματούχος Ηλεκτρολόγος Μηχανικός και Μηχανικός Υπολογιστών Ε.Μ.Π.

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Οι απόψεις και τα συμπεράσματα που περιέχονται σε αυτό το έγγραφο εκφράζουν τον συγγραφέα και δεν πρέπει να ερμηνευθεί ότι αντιπροσωπεύουν τις επίσημες θέσεις του Εθνικού Μετσόβιου Πολυτεχνείου.

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# Περίληψη

Στην παρούσα διπλωματική εργασία πραγματοποιείται η ανάλυση, η σχεδίαση και η υλοποίηση ενός δισταδιακού ενισχυτή ισχύος τάξης B, ο οποίος λειτουργεί στη ζώνη FR3 και είναι υλοποιημένος σε τεχνολογία 22nm CMOS FD-SOI. Η κεντρική συχνότητα λειτουργίας είναι 7.76 GHz, ενώ το εύρος ζώνης κυμαίνεται από 7.125 GHz έως 8.4 GHz.

Η δομή της εργασίας έχει ως εξής: Αρχικά, παρουσιάζεται η αρχιτεκτονική των σύγχρονων ψηφιακών πομποδεκτών, επισημαίνοντας και το ρόλο του ενισχυτή ισχύος. Στη συνέχεια, παρατίθενται οι βασικοί ορισμοί μεγεθών που χρησιμοποιούνται στις τηλεπικοινωνίες για τον χαρακτηρισμό της επίδοσης ενός ενισχυτή ισχύος, όπως η γραμμικότητα, το κέρδος, η ισχύς εξόδου και η απόδοση.

Έπειτα, εισάγονται οι παράμετροι σκέδασης (S-parameters), οι μέθοδοι ελέγχου της ευστάθειας και το μοντέλο υψηλών συχνοτήτων του MOS τρανζίστορ. Ακολουθεί η παρουσίαση των βασικών αρχών σχεδίασης ενισχυτών ισχύος καθώς και των βασικών τάξεων λειτουργίας. Οι τάξεις αυτές υλοποιούνται και συγκρίνονται στην τεχνολογία 22nm CMOS FD-SOI.

Στη συνέχεια, συγκρίνεται η single-ended τοπολογία με τη διαφορική, ενώ παρουσιάζεται αναλυτικά ο τρόπος με τον οποίο αντιμετωπίζεται το πρόβλημα της χαμηλής ονομαστικής τάσης $V_{\mathrm{DS}}$ στις σύγχρονες τεχνολογίες πυριτίου, μέσω της στοίβαξης τρανζίστορ.

Ακολούθως, παρουσιάζεται η τοπολογία του δισταδιακού ενισχυτή ισχύος. Αφού έχει προηγηθεί η παρουσίαση όλης της απαιτούμενης θεωρίας, αναλύονται λεπτομερώς όλα τα βήματα της σχεδίασης, τόσο του ενισχυτικού σταδίου ισχύος όσο και του driver, τόσο σε επίπεδο σχηματικού όσο και σε επίπεδο layout.

Στα τελευταία κεφάλαια παρατίθενται τα τελικά αποτελέσματα της υλοποίησης και προτείνονται κατευθύνσεις για μελλοντική έρευνα και βελτιώσεις.

Η παρούσα διπλωματική εργασία αποτελεί μια χρήσιμη εισαγωγή στη θεωρία των ενισχυτών ισχύος και μπορεί να λειτουργήσει ως πολύτιμο βοήθημα για όσους πρόκειται να σχεδιάσουν για πρώτη φορά έναν ενισχυτή ισχύος, ιδιαίτερα σε σύγχρονες τεχνολογίες πυριτίου. Παρουσιάζονται αναλυτικά τρόποι επίτευξης όσο το δυνατόν μεγαλύτερης ισχύος εξόδου, υπερβαίνοντας τους περιορισμούς των σύγχρονων τεχνολογιών πυριτίου που χαρακτηρίζονται από χαμηλή ονομαστική τάση $V_{\mathrm{DS}}$.

**Λέξεις-κλειδιά:** Ενισχυτής ισχύος, CMOS FD-SOI, Ζώνη FR3, RF, Τάξη B, Διαφορική τοπολογία, Στοίβαξη τρανζίστορ

# Abstract

In this thesis, the analysis, design, and implementation of a two-stage class-B power amplifier operating in the FR3 band is presented. The amplifier is implemented in 22nm CMOS FD-SOI technology. The central frequency is 7.76 GHz, while the bandwidth ranges from 7.125 GHz to 8.4 GHz.

The structure of the thesis is as follows: Initially, the architecture of modern digital transceivers is presented, highlighting the role of the power amplifier. Then, the fundamental definitions of key performance metrics used in telecommunications to evaluate power amplifiers—such as linearity, gain, output power, and efficiency—are discussed.

Subsequently, the S-parameters, stability analysis techniques, and the high-frequency model of the MOS transistor are introduced. This is followed by an overview of basic design principles for power amplifiers and a comparison of the basic amplifier operation classes, which are also implemented and compared using the 22nm CMOS FD-SOI process.

Next, a comparison is made between single-ended and differential topologies. Particular attention is given to addressing the challenge posed by the low nominal $V_{\mathrm{DS}}$ of modern silicon technologies, which is mitigated through transistor stacking.

Following that, the topology of the two-stage power amplifier is presented. After the theoretical background has been established, all the design steps for both the power amplifier stage and the driver are thoroughly analyzed, both at the schematic and layout levels.

In the final chapters, the implementation results are presented and directions for future work are proposed.

This thesis serves as a useful introduction to the theory of power amplifiers and can be a valuable guide for those designing a power amplifier for the first time, especially in modern silicon technologies. Detailed design techniques are presented to achieve maximum output power while overcoming the limitations imposed by the low nominal $V_{\mathrm{DS}}$ in advanced CMOS processes.

**Keywords:** Power amplifier, CMOS FD-SOI, FR3 band, RF, Class-B, Differential Topology, Transistor Stacking

# Ευχαριστίες

Αφιερώνεται στα μέλη του εργαστηρίου, με τα οποία καταφέραμε να δημιουργήσουμε ένα όμορφο κλίμα συνεργασίας και αλληλοβοήθειας. Παρά την πίεση της δουλειάς, βρήκαμε στιγμές χαλάρωσης και απολαύσαμε ευχάριστες συζητήσεις. Μη ξεχνάμε: η ευτυχία είναι στιγμές· κι αξίζει να προσπαθούμε να μεγιστοποιούμε την πυκνότητά τους.

Στο εργαστήριο είχα την τεράστια τύχη να γνωρίσω τον εξαιρετικό Βασίλειο Μανουρά, υποψήφιο διδάκτορα – και σύντομα διδάκτορα. Έναν άνθρωπο με αγνή καρδιά και καλή ψυχή. Τον ευχαριστώ που έδωσε ζωντάνια στο εργαστήριο και συνέβαλε στη διαμόρφωση ενός γνήσιου ομαδικού πνεύματος. Τον ευχαριστώ για την αμέριστη βοήθεια που προσέφερε σε όλα τα μέλη. Η εργατικότητα και το πείσμα του αποτέλεσαν για μένα έμπνευση να κυνηγήσω ένα δικό μου διδακτορικό στο μέλλον. Εύχομαι να είναι πάντα ευτυχισμένος. Δεν θα τον ξεχάσω ποτέ και ελπίζω να κρατήσουμε επαφή μέχρι τα βαθιά γεράματα.

Ένα μεγάλο ευχαριστώ στους καθηγητές Γεώργιο Παναγόπουλο και Ιωάννη Παπανάνο, που με την εμπειρία και τις εύστοχες συμβουλές τους με καθοδήγησαν στο σωστό δρόμο.

Ευχαριστώ θερμά την οικογένειά μου για τη διαρκή ηθική και υλική τους υποστήριξη. Ιδιαίτερη μνεία στη μαμά μου, Βενετία Διακογιάννη, που είναι πάντα εκεί για να με ακούσει και να με στηρίξει.

Τέλος, ένα τεράστιο ευχαριστώ στους πολυαγαπημένους μου φίλους: το Νικόλα Πετρόπουλο, τον Αντώνη Δημάκη, το Μάνο Μαρκουλάκη και τη Σοφία Κουράκου. Ένα "ευχαριστώ" είναι το ελάχιστο που μπορώ να πω για την ανεκτίμητη ηθική τους υποστήριξη. Μου στάθηκαν πραγματικά στις πιο δύσκολες στιγμές μου και γι' αυτό τους οφείλω πολλά. Ήταν πάντα δίπλα μου στα ευχάριστα και στα δυσάρεστα, στα εύκολα και στα δύσκολα. Μη ξεχνάμε ότι οι άνθρωποι στα δύσκολα φαίνονται. Με στήριξαν με αγάπη, κατανόηση και σταθερότητα, και μοιραστήκαμε στιγμές αληθινής χαράς. Χάρη σε αυτούς ξαναβρήκα την εμπιστοσύνη μου στους ανθρώπους. Οι καλοί άνθρωποι υπάρχουν – απλώς είναι σπάνιοι. Θα κρατήσουμε επαφή για πάντα, ακόμα κι όταν φύγω από την Ελλάδα. Μας φαντάζομαι γερασμένους πια, να θυμόμαστε με νοσταλγία τα νεανικά μας χρόνια.

# Acknowledgements

This is dedicated to the members of the lab, with whom we managed to create a wonderful atmosphere of collaboration and mutual support. Despite the pressure of work, we found moments to relax and enjoy meaningful conversations. Let us not forget: happiness is found in fleeting moments—and we should strive to maximize their density.

At the lab, I had the great fortune to meet the exceptional Vasileios Manouras, a PhD candidate—and soon to be a doctor. A person with a pure heart and a kind soul. I sincerely thank him for bringing life to the lab and for contributing to the development of a true team spirit. I am especially grateful for the immense help he offered to all members. His work ethic and perseverance inspired me to consider pursuing a PhD myself. I wish him all the happiness in the world. I will never forget him, and I hope we stay in touch well into old age.

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I deeply thank my family for their unwavering moral and financial support. A special mention goes to my mother, Venetia Diakogianni, who is always there to listen and support me.

Finally, a huge thank you to my dearest friends: Nikolas Petropoulos, Antonis Dimakis, Manos Markoulakis, and Sofia Kourakou. Saying "thank you" feels like the bare minimum I can offer for their priceless moral support. They truly stood by me during my most difficult moments, and for that, I owe them everything. They were there for me through the highs and the lows, the easy and the hard times. People reveal their true selves in difficult times—and they showed me nothing but love and understanding. We shared moments of genuine joy and relief from the pressures of daily life. Thanks to them, I regained my trust in people. Good people do exist—but they are exceptionally rare. I will keep in touch with them always, even when I leave Greece. I can picture us as old folks someday, fondly reminiscing about our youth.

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# Κεφάλαιο 1

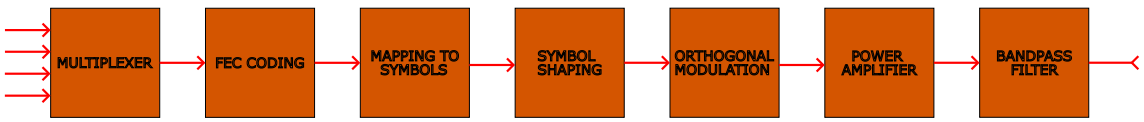
# Εκτεταμένη Περίληψη στα Ελληνικά

## 1.1 Εισαγωγή

Η παρούσα εργασία έχει ως στόχο την ανάλυση, σχεδίαση και υλοποίηση ενός δισταδιακού ενισχυτή ισχύος τάξης B, ο οποίος λειτουργεί στη ζώνη FR3 (7.125–8.4 GHz) και είναι κατάλληλος για μελλοντικές εφαρμογές 5G/6G. Ο ενισχυτής υλοποιείται με την τεχνολογία 22 nm CMOS FD-SOI και εφαρμόζονται μέθοδοι για να μεγιστοποιηθεί η ισχύς εξόδου του, ξεπερνώντας τους περιορισμούς που επιβάλλει η χαμηλή ονομαστική τάση $V_{DS}$.

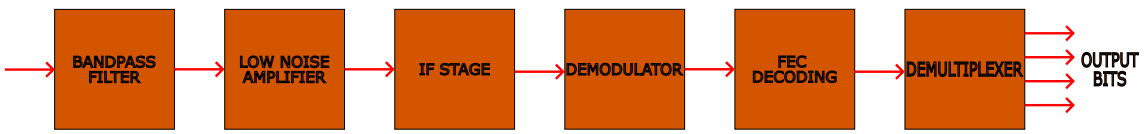
## 1.2 Σύγχρονα Τηλεπικοινωνιακά Συστήματα

Τα σύγχρονα τηλεπικοινωνιακά συστήματα είναι ψηφιακά. Οι δομικές μονάδες του πομπού και του υπερετερόδυνου δέκτη παρουσιάζονται στα Σχήματα 1.1 και 1.2.




Σχήμα 1.1: Πομπός

Αρχικά, στον πομπό, οι διάφορες ροές ψηφιακής πληροφορίας πολυπλέκονται σε μία ενιαία μορφή. Στη συνέχεια προστίθενται επιπλέον ψηφία, ώστε το σύστημα να αποκτήσει δυνατότητα αυτοδιόρθωσης σφαλμάτων. Η διαδικασία αυτή βελτιώνει την αξιοπιστία της επικοινωνίας, αν και μειώνει τον ωφέλιμο ρυθμό μετάδοσης. Έπειτα, τα ψηφία αντιστοιχίζονται σε σύμβολα, τα οποία περνούν από παλμο μορφοποίησης και στη συνέχεια από ορθογώνιο διαμορφωτή. Τέλος, εντοπίζεται η κρίσιμη βαθμίδα του ενισχυτή ισχύος, ο οποίος παρέχει στο σήμα την απαιτούμενη ισχύ για να τροφοδοτήσει την κεραία και να μεταδοθεί το σήμα.




Σχήμα 1.2: Υπερετερόδυνος δέκτης

Η λειτουργία του δέκτη είναι αντίστροφη αυτής του πομπού. Αρχικά, ένα ζωνοπερατό φίλτρο επιλέγει το επιθυμητό σήμα και απορρίπτει τα εκτός ζώνης σήματα. Στη συνέχεια, το σήμα ενισχύεται από έναν ενισχυτή χαμηλού θορύβου (LNA), ο οποίος χαρακτηρίζεται από υψηλό κέρδος και χαμηλό συντελεστή θορύβου, ώστε να ελαχιστοποιηθεί ο συνολικός συντελεστής θορύβου του συστήματος. Έπειτα, το σήμα οδηγείται στη βαθμίδα ενδιάμεσης συχνότητας (IF), η οποία έχει σταθερή τιμή ανεξαρτήτως του επιθυμητού σήματος. Ακολουθούν ο αποδιαμορφωτής, η βαθμίδα αποκωδικοποίησης και τέλος ο αποπολυπλέκτης, ο οποίος ανακτά τις επιμέρους ροές πληροφορίας.

## 1.3 Θεμελιώδεις Έννοιες και Ορισμοί στις Τηλεπικοινωνίες

Η πιο συνηθισμένη μονάδα μέτρησης στις τηλεπικοινωνίες είναι τα dB, τα οποία χρησιμοποιούνται για την ποσοτικοποίηση των περισσότερων μεγεθών, όπως η ισχύς, το κέρδος τάσης και το κέρδος ισχύος.

Ο θόρυβος αποτελεί ανεπιθύμητη οντότητα με στοχαστικό χαρακτήρα, η οποία υποβαθμίζει την ποιότητα της τηλεπικοινωνιακής ζεύξης. Οι περισσότερες πηγές θορύβου είναι ασυσχέτιστες και παράγουν λευκό θόρυβο, δηλαδή θόρυβο με σταθερή φασματική πυκνότητα ισχύος σε όλο το φάσμα. Επιπλέον, ο θόρυβος είναι αθροιστικός.

Η ποιότητα του σήματος στο δέκτη εκφράζεται μέσω του λόγου σήματος προς θόρυβο (SNR), ενώ η υποβάθμιση αυτού του λόγου λόγω της παρουσίας μιας βαθμίδας εκφράζεται από το συντελεστή θορύβου (NF).

Η ηλεκτρική συμπεριφορά αρκετών κυκλωμάτων δεν είναι ακριβώς γραμμική. Ένας τρόπος να ποσοτικοποιηθεί ο μη γραμμικός χαρακτήρας ενός κυκλώματος είναι μέσω της πολυωνυμικής προσέγγισης, όπου η τάση εξόδου εκφράζεται ως πολυώνυμο της ισχύος εισόδου.

Λόγω των μη γραμμικοτήτων, το σήμα εξόδου μπορεί να περάσει από φάση συμπίεσης (compression) ή επέκτασης (expansion) για αρκετά υψηλές τιμές της εισόδου. Έτσι, ορίζεται το σημείο συμπίεσης 1 dB, το οποίο είναι το σημείο όπου το κέρδος του κυκλώματος μειώνεται κατά 1 dB σε σχέση με το κέρδος στη γραμμική περιοχή.

Επίσης, λόγω των μη γραμμικοτήτων εμφανίζεται το φαινόμενο της ενδοδιαμόρφωσης. Όταν δύο ανεπιθύμητα σήματα με συχνότητες $\omega_1$ και $\omega_2$ εφαρμόζονται σε ένα μη γραμμικό κύκλωμα, στην έξοδο εμφανίζονται συνιστώσες που δεν είναι αρμονικές αυτών των συχνοτήτων. Κάποιες από αυτές μπορεί να βρεθούν πολύ κοντά στη συχνότητα του επιθυμητού σήματος και να προκαλέσουν άμεση παρεμβολή. Οι συχνότητες αυτές είναι, για παράδειγμα, οι $2\omega_1 - \omega_2$ και $2\omega_2 - \omega_1$. Για να ελεγχθεί η γραμμικότητα ενός κυκλώματος ορίζεται το σημείο τομής τρίτης τάξης (IP3), το οποίο είναι ένα θεωρητικό σημείο στο οποίο τα προϊόντα ενδοδιαμόρφωσης έχουν το ίδιο πλάτος με τη θεμελιώδη συχνότητα.

Τέλος, παρουσιάζονται τα μεγέθη που χρησιμοποιούνται για το χαρακτηρισμό της επίδοσης ενός ενισχυτή ισχύος. Για το χαρακτηρισμό της γραμμικότητας αξιοποιούνται τα δύο μεγέθη που ορίστηκαν προηγουμένως. Επίσης, χρησιμοποιείται το κέρδος ισχύος, που είναι ο λόγος της ισχύος εξόδου προς την ισχύ εισόδου και εκφράζεται συνήθως σε dB. Ορίζεται επίσης η ισχύς κορεσμού, που είναι η μέγιστη ισχύς εξόδου που μπορεί να παρέχει ο ενισχυτής. Τέλος, ορίζεται η απόδοση, η οποία λαμβάνει υπόψη το κέρδος του ενισχυτή, δηλαδή την ισχύ που απαιτείται για να τροφοδοτήσει τον ενισχυτή, ως εξής:

$$\mathrm{PAE} = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{DC}}} \times 100\%$$

όπου

- $P_{\text{out}}$: η ισχύς εξόδου
- $P_{\text{in}}$: η ισχύς εισόδου
- $P_{\text{DC}}$: η ισχύς τροφοδοσίας DC που καταναλώνει ο ενισχυτής.

Από την άλλη, η απλή απόδοση ορίζεται ως ο λόγος της ισχύος εξόδου προς την ισχύ τροφοδοσίας.

## 1.4 Τα RF Κυκλώματα ως Μικροκυματικά Δίκτυα

Η ανάλυση, προσομοίωση και μέτρηση των RF κυκλωμάτων γίνεται κατά κανόνα χρησιμοποιώντας τις παραμέτρους σκέδασης (S-παράμετροι). Οι παράμετροι σκέδασης περιγράφουν πώς συνδέονται τα ανακλώμενα κύματα $b_i$ κάθε θύρας ενός n-port με τα κύματα που εισέρχονται σε αυτή, $a_i$, μέσω της μήτρας σκέδασης:

$$\begin{pmatrix} b_1 \\ \vdots \\ b_n \end{pmatrix} = \begin{pmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{nn} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ \vdots \\ a_n \end{pmatrix}$$

όπου

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k=0,\, \forall k \neq j}$$

Η παραπάνω εξίσωση εκφράζει τον συντελεστή μετάδοσης από τη θύρα $j$ στη θύρα $i$ και υπολογίζεται διεγείροντας τη θύρα $j$ με το εισερχόμενο κύμα $a_j$ και μετρώντας το ανακλώμενο κύμα $b_i$ στη θύρα $i$, ενώ όλες οι υπόλοιπες θύρες τερματίζονται στην χαρακτηριστική αντίσταση $Z_0$ (δηλαδή, $a_k = 0$ για κάθε $k \neq j$) ώστε να αποφεύγονται ανακλάσεις.

Επιπλέον, αναλύεται πώς μπορεί να ελεγχθεί η ευστάθεια ενός δίθυρου μέσω των κύκλων ευστάθειας. Παρουσιάζονται τα μαθηματικά κριτήρια που προσδιορίζουν αν ένα κύκλωμα είναι ευσταθές άνευ όρων όπως το κριτήριο $\mu$ και το κριτήριο Κ-Δ. Εάν κάποιο από αυτά τα κριτήρια δεν ικανοποιείται, τότε το κύκλωμα θεωρείται ευσταθές με όρους και πρέπει να χρησιμοποιηθούν οι κύκλοι ευστάθειας για περαιτέρω ανάλυση.

Τέλος, παρουσιάζεται το ισοδύναμο κυκλωματικό μοντέλο του MOS τρανζίστορ στις υψηλές συχνότητες. Στο μοντέλο αυτό, πέρα από την πηγή ρεύματος ελεγχόμενη από τάση και την αντίσταση $r_{ds}$, περιλαμβάνονται επίσης η αντίσταση στο gate και οι παρασιτικές χωρητικότητες μεταξύ gate-drain, gate-source, drain-body και source-body.

## 1.5 Ενισχυτές Ισχύος

Ο ενισχυτής ισχύος είναι ένα μη γραμμικό κύκλωμα και η πλήρης μαθηματική του ανάλυση είναι δύσκολη. Η ανάλυση αυτή μπορεί να γίνει προσεγγιστικά σε έναν ενισχυτή ενός τρανζίστορ, όπου η τροφοδοσία παρέχεται από RF choke, δηλαδή ιδανικό πηνίο άπειρης αυτεπαγωγής, και η έξοδος του τρανζίστορ συνδέεται με το ωμικό φορτίο μέσω ιδανικού άπειρου πυκνωτή. Σε αυτήν την περίπτωση, ένας τρόπος να εκτιμηθεί η συμπεριφορά αυτού του ενισχυτή ισχύος είναι να γίνει φασματική ανάλυση και η χαρακτηριστική ρεύματος-τάσης του τρανζίστορ να αντικατασταθεί από την τμηματικά γραμμική προσέγγιση. Με αυτόν τον

τρόπο μπορούν να προσδιορισθούν αναλυτικά όλες οι αρμονικές του ρεύματος στην έξοδο. Η τάση στην έξοδο είναι καθαρό ημίτονο λόγω του παράλληλου κυκλώματος συντονισμού που εισάγεται.

Έπειτα, παρουσιάζονται οι τέσσερις βασικές τάξεις λειτουργίας: A, AB, B, C. Η μόνη τάξη η οποία λειτουργεί στη γραμμική περιοχή του τρανζίστορ είναι η τάξη A. Η συμπεριφορά του ρεύματος σε κάθε τάξη είναι η εξής:

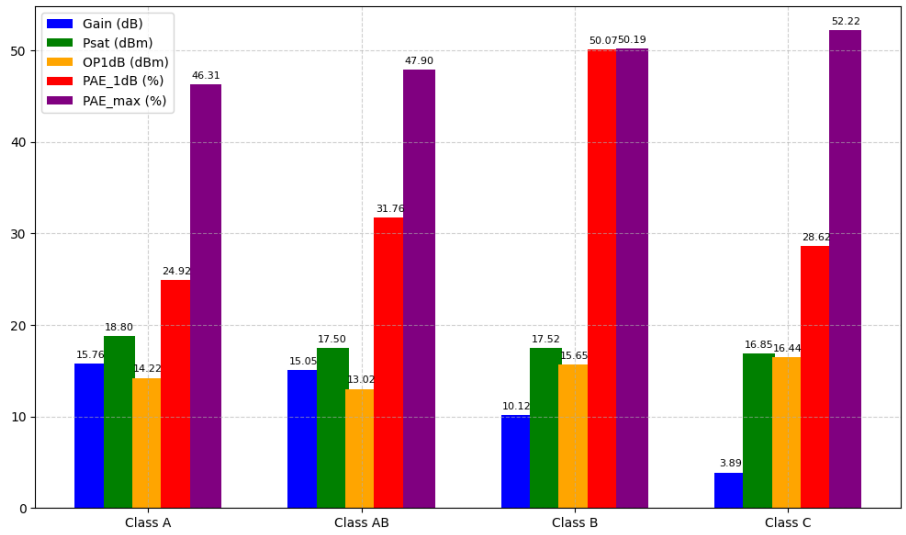
- Τάξη A: Το τρανζίστορ άγει σε όλη τη διάρκεια της περιόδου
- Τάξη AB: Το τρανζίστορ άγει για διάρκεια μεγαλύτερη από τη μισή περίοδο
- Τάξη B: Το τρανζίστορ άγει για διάρκεια ακριβώς ίση με τη μισή περίοδο
- Τάξη C: Το τρανζίστορ άγει για διάρκεια μικρότερη της μισής περιόδου

Ρυθμίζοντας κατάλληλα την πόλωση στην πύλη του τρανζίστορ μπορεί να καθοριστεί η τάξη λειτουργίας του.

Καθώς μετακινούμαστε από την τάξη A στη C, οι αρμονικές γίνονται όλο και πιο έντονες, συντελώντας στην αύξηση της απόδοσης.

Για να λειτουργεί ο ενισχυτής ισχύος βέλτιστα, πρέπει το ωμικό φορτίο να έχει τη βέλτιστη τιμή. Ένας τρόπος να προσδιοριστεί αυτή η τιμή στην τάξη A είναι μέσω της ευθείας φορτίου.

Στη συνέχεια, υλοποιήθηκε ένας ενισχυτής ισχύος ενός τρανζίστορ σε τεχνολογία 22 nm CMOS FD-SOI σε όλες τις τέσσερις βασικές τάξεις λειτουργίας. Τα αποτελέσματα είναι συγκεντρωμένα στο σχήμα 1.3.




Σχήμα 1.3: Σύγκριση των επιδόσεων του ενισχυτή ισχύος στις τάξεις λειτουργίας A, AB, B και C

Είναι εμφανές ότι το καλύτερο trade-off μεταξύ όλων των παραμέτρων επίδοσης το πετυχαίνει η τάξη B.

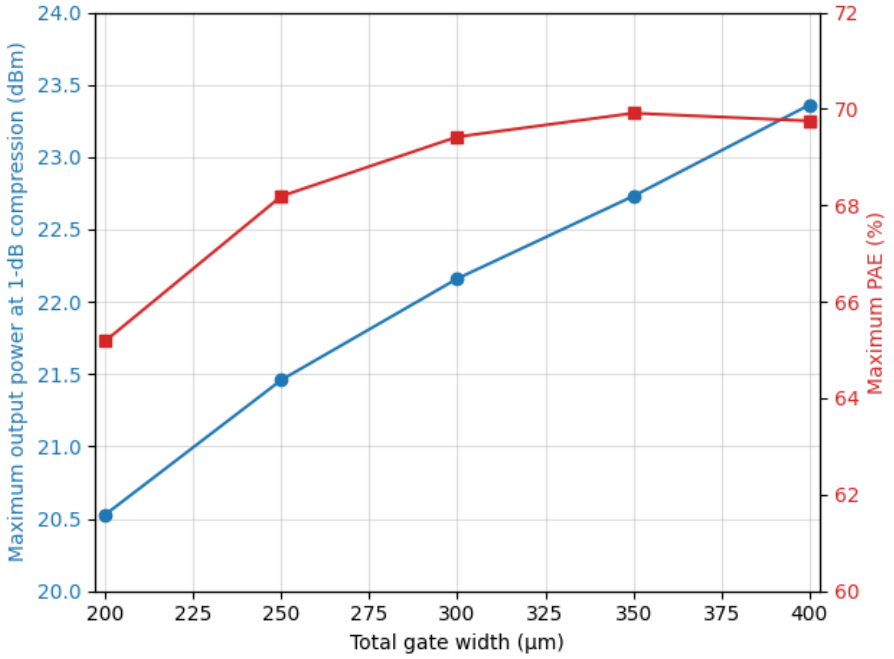
Αφού έγινε η σύγκριση των τεσσάρων βασικών τάξεων, εισάγεται η διαφορική τοπολογία, η οποία διπλασιάζει την ισχύ εξόδου. Ταυτόχρονα, οι neutralization πυκνωτές επιτρέπουν να επιτευχθεί εύκολα ευστάθεια ανευ όρων, επιτρέποντας πιθανόν αύξηση του κέρδους. Οι παρατηρήσεις αυτές επιβεβαιώνονται από πειραματικά αποτελέσματα.

Επίσης, οι σύγχρονες τεχνολογίες πυριτίου παρουσιάζουν το μειονέκτημα της χαμηλής ονομαστικής τάσης $V_{\mathrm{DS}}$, με συνέπεια να είναι περιορισμένη η τιμή της τροφοδοσίας και άρα και της ισχύος εξόδου. Ένας τρόπος να αυξηθεί η ισχύς εξόδου είναι η στοίβαξη τρανζίστορ, αφού επιτρέπει την αύξηση της τροφοδοσίας. Όμως, η σχεδίαση πρέπει να γίνει προσεκτικά ώστε να έχουμε βέλτιστη επίδοση, αλλά και να είναι αξιόπιστος (reliable) ο ενισχυτής. Απαιτείται η εισαγωγή RC δικτύων στις πύλες των τρανζίστορ της δεύτερης σειράς και των ανώτερων σειρών, ώστε να ισομοιράζεται η τάση $V_{\mathrm{DS}}$ στη στοίβα και να βελτιστοποιηθεί η επίδοση. Επιβεβαιώθηκε πειραματικά ότι ένας διαφορικός cascode ενισχυτής ισχύος παρουσιάζει σχεδόν διπλάσια ισχύ εξόδου σε σχέση με ένα απλό διαφορικό ζευγάρι, αλλά με λίγο χειρότερη απόδοση λόγω περισσότερων παρασιτικών.

Τέλος, παρουσιάζεται και ο δισταδιακός ενισχυτής, ο οποίος αυξάνει το κέρδος και χρησιμοποιείται σε περιπτώσεις όπου η ισχύς που παρέχουν τα στάδια πίσω από τον ενισχυτή ισχύος δεν επαρκεί για να τον οδηγήσει στο 1 dB σημείο συμπίεσής του. Αυτό βέβαια γίνεται με το κόστος χειρότερης απόδοσης και χειρότερης γραμμικότητας.

## 1.6 Σχεδίαση του Σταδίου Ενισχυτή Ισχύος

Η τοπολογία του σταδίου ενισχυτή ισχύος είναι διαφορική με στοίβαξη τριών τρανζίστορ, προκειμένου να μεγιστοποιηθεί η ισχύς εξόδου. Τα τρανζίστορ επιλέχτηκαν πολύ παχιά ώστε να μεγιστοποιηθεί η ισχύς εξόδου, όπως φαίνεται στο σχήμα 1.4.

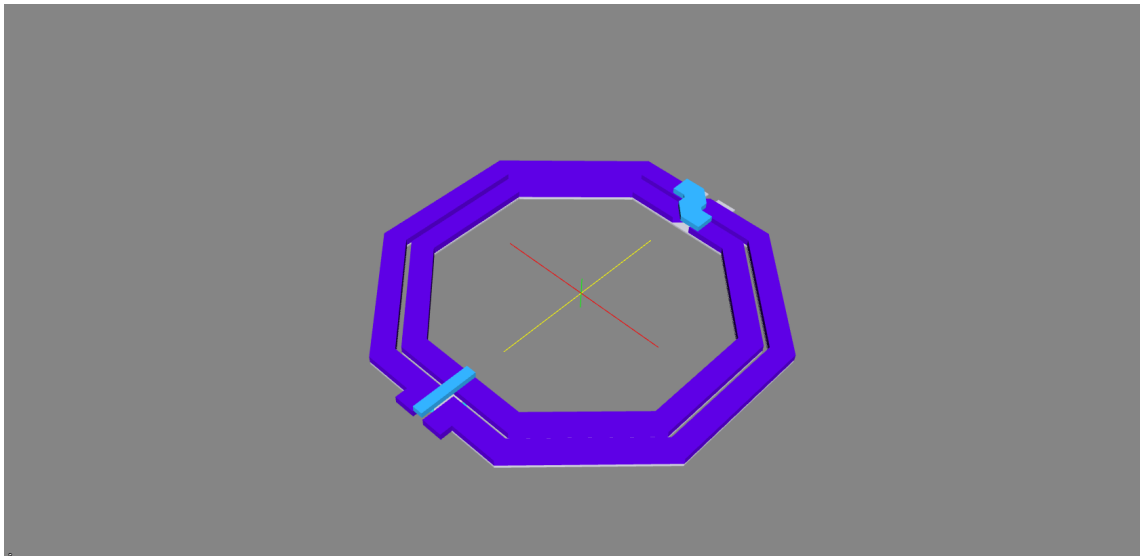



Σχήμα 1.4: Μέγιστη ισχύς εξόδου στο σημείο συμπίεσης 1 dB και μέγιστη απόδοση ισχύος (PAE) σε συνάρτηση με το συνολικό πλάτος πύλης

Οι τιμές των neutralization πυκνωτών επιλέχτηκαν με τέτοιο τρόπο ώστε να μεγιστοποιούν το μ-Factor. Η βέλτιστη τιμή της αντίστασης που έπρεπε να βλέπει ο ενισχυτής ισχύος στην έξοδό του προσδιορίστηκε με load pull προσομοιώσεις.

Επίσης, το balun στην έξοδο επιλέχτηκε να χαρακτηρίζεται από υψηλό συντελεστή σύζευξης, ώστε να ελαχιστοποιηθούν οι απώλειες, ενώ χρησιμοποιήθηκε και ένας πυκνωτής στα

άκρα της εισόδου του ώστε να εξασφαλιστεί το απαιτούμενο matching. Το balun στην έξοδο φαίνεται στο σχήμα 1.5. Το ισοδύναμο κυκλωματικό μοντέλο των μετασχηματιστών, αλλά και τα χαρακτηριστικά των baluns και του μετασχηματιστή που χρησιμοποιήθηκε στον τελικό δισταδιακό ενισχυτή ισχύος, παρουσιάζονται στο παράρτημα.



Σχήμα 1.5: Balun στην έξοδο

Ακόμη, μεταξύ των πυλών των κάτω τρανζίστορ τοποθετήθηκε αντίσταση, προκειμένου να μειωθεί το φανταστικό μέρος στην αντίσταση εισόδου του σταδίου ενισχυτή ισχύος αλλά και να αυξηθεί το ωμικό μέρος. Με το κόστος βέβαια χειρότερου κέρδους. Η αντίσταση αυτή ήταν όμως απαραίτητη για να επιτευχθεί καλό εύρος ζώνης και ευκολότερο matching μεταξύ του σταδίου οδήγησης και του σταδίου ενισχυτή ισχύος. Χωρίς αυτήν την αντίσταση το ωμικό μέρος είναι πολύ μικρό ενώ το φανταστικό πολύ μεγάλο.

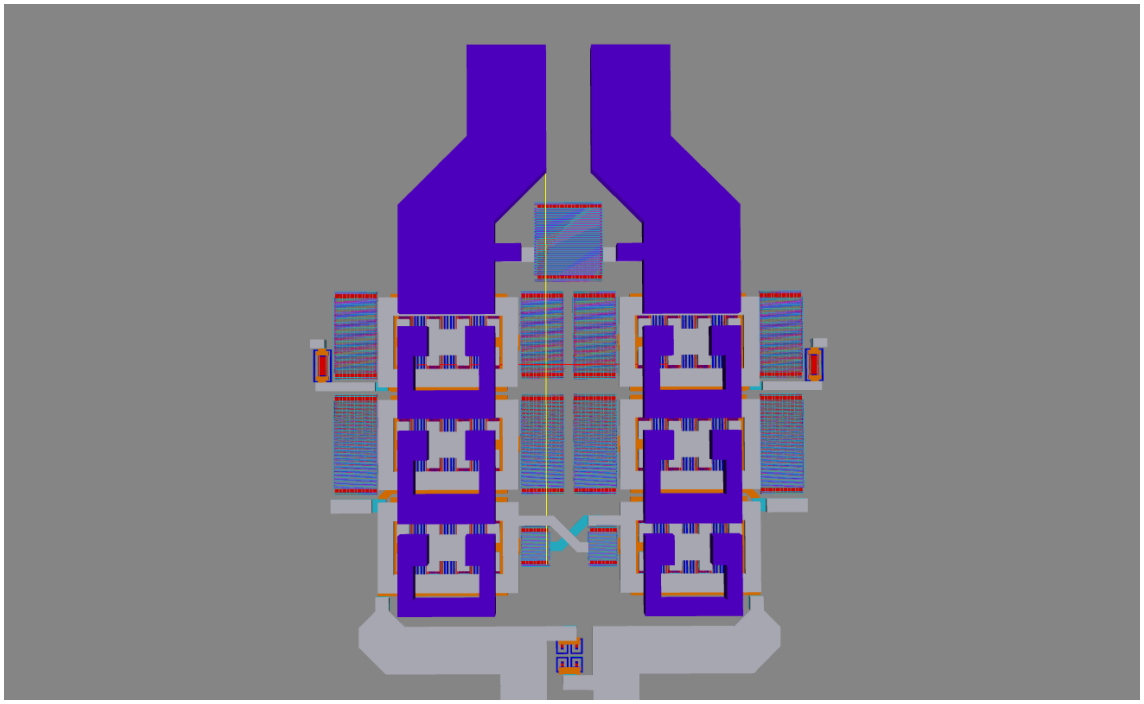
Τα αποτελέσματα στο nominal φαίνονται στον πίνακα 1.1.

Πίνακας 1.1: Σύνοψη επιδόσεων του σταδίου ενισχυτή ισχύος

| | |
|---|---|
| Supply Voltage ($V_{\mathrm{DD}}$) | 2.4 V |
| Gain | 16.62 dB |
| Saturated Output Power ($P_{\mathrm{sat}}$) | 23.31 dBm |
| 1 dB Compression Point ($OP_{\mathrm{1dB}}$) | 22.04 dBm |
| PAE at 1 dB Compression Point ($PAE_{\mathrm{1dB}}$) | 51.34% |
| Maximum PAE ($PAE_{\mathrm{max}}$) | 51.51% |
| Difference Between $IIP_3$ and $IP_{\mathrm{1dB}}$ | 6 dB |

Επιπρόσθετα, εξετάστηκε η λειτουργία του ενισχυτή ισχύος στα corners. Σε κάποια corners παρατηρήθηκε αύξηση στο κέρδος και μείωση στο σημείο συμπίεσης 1 dB, ενώ σε κάποια άλλα παρατηρήθηκε το αντίστροφο. Στην πρώτη περίπτωση η τάση κατωφλίου μειώθηκε, ενώ στη δεύτερη περίπτωση αυξήθηκε. Η επίδοση στα corners της πρώτης περίπτωσης βελτιώθηκε μειώνοντας τη DC τάση στις πύλες των τρανζίστορ, ώστε να οδηγηθεί ο ενισχυτης πάλι στην

τάξη B. Στη δεύτερη περίπτωση πρέπει να εφαρμοστεί θετική DC τάση στο back gate των κάτω κάτω τρανζίστορ, ώστε να μειωθεί η τάση κατωφλίου.



Σχήμα 1.6: Layout του σταδίου ενισχυτή ισχύος

Στο σχήμα 1.6 παρουσιάζεται το layout του σταδίου ενισχυτή ισχύος. Η τεχνολογία παρέχει οκτώ στρώματα μετάλλου, εκ των οποίων τα τρία ανώτερα είναι παχιά. Από αυτά, το Μέταλλο 7 παρουσιάζει την υψηλότερη αγωγιμότητα. Για να ελαχιστοποιηθούν οι απώλειες κατά μήκος της στοίβας τρανζίστορ — από την υποδοχή του κατώτερου τρανζίστορ έως την υποδοχή του ανώτερου — και να μεγιστοποιηθεί η ισχύς που αποδίδεται στην έξοδο, χρησιμοποιήθηκε ένας συνδυασμός των στρωμάτων Μέταλλο 6 και Μέταλλο 7 για τις διασυνδέσεις υποδοχής και πηγής.

Τα πρώτα τέσσερα στρώματα μετάλλου χρησιμοποιήθηκαν για τη δρομολόγηση των σημάτων των πυλών. Παρόλο που αυτή η επιλογή ήταν αναγκαία, εισήγαγε αυξημένες απώλειες, με αποτέλεσμα μια ελαφρά υποβάθμιση του κέρδους.

Οι πυκνωτές στις πύλες των τρανζίστορ της δεύτερης και τρίτης στοίβας χωρίστηκαν σε δύο ίσα μέρη, προκειμένου να επιτευχθεί πιο συμπαγές layout.

Επιπλέον, λόγω των τροποποιήσεων που εισήχθησαν από τις διασυνδέσεις, οι χωρητικότητες των πυκνωτών στη δεύτερη και τρίτη στοίβα έπρεπε να αυξηθούν για να βελτιωθεί η επίδοση και να επιτευχθεί πιο ομοιόμορφη κατανομή των τάσεων υποδοχής-πηγής ($V_{\mathrm{DS}}$) κατά μήκος της στοίβας. Επιπλέον, ήταν απαραίτητη η μείωση της αντίστασης στις πύλες των τρανζίστορ της δεύτερης στοίβας, ώστε να βελτιωθεί η επίδοση και να γίνει περισσότερο ομοιόμοφη η κατανομή των τάσεων.

Τα αποτελέσματα παρουσιάζονται συγκεντρωτικά στον Πίνακα 1.2 και συγκρίνονται με εκείνα σε επίπεδο σχηματικού. Είναι εμφανές ότι η απόδοση υποβαθμίστηκε ελαφρώς, με εξαίρεση τη γραμμικότητα, η οποία βελτιώθηκε.

Πίνακας 1.2: Σύγκριση της επίδοσης του σταδίου ενισχυτή ισχύος μεταξύ schematic και post-layout αποτελεσμάτων

| **Parameter** | **Schematic** | **Post-Layout** |
|---|---|---|
| Supply Voltage ($V_{\mathrm{DD}}$) | 2.4 V | 2.4 V |
| Gain | 16.62 dB | 15.66 dB |
| Saturated Output Power ($P_{\mathrm{sat}}$) | 23.31 dBm | 22.45 dBm |
| PAE at 1 dB Compression Point ($PAE_{\mathrm{1dB}}$) | 51.34% | 43.93% |
| Maximum PAE ($PAE_{\mathrm{max}}$) | 51.51% | 44.10% |
| Difference Between $IIP_3$ and $IP_{\mathrm{1dB}}$ | 6 dB | 10.18 dB |

## 1.7 Σχεδίαση του Σταδίου Οδήγησης

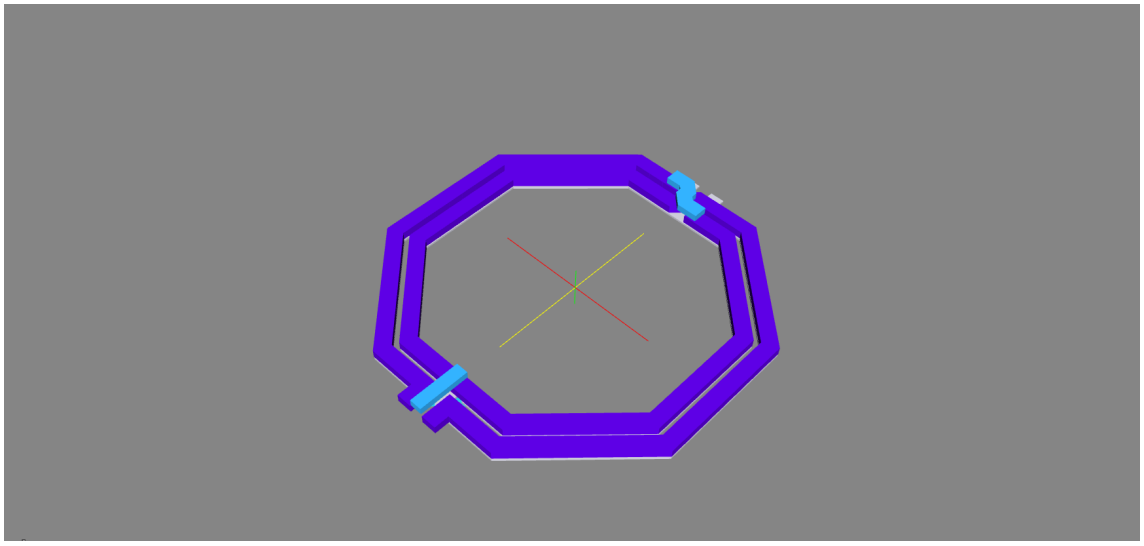
Η σχεδίαση του σταδίου οδήγησης (driver), αν και όχι τόσο κρίσιμη, απαιτεί και αυτή προσοχή. Για τον σχεδιασμό του σταδίου οδήγησης, πρέπει να ληφθεί υπόψη ότι το κέρδος του driver θα πρέπει να παραμένει γραμμικό στο σημείο συμπίεσης 1 dB του σταδίου ενισχυτή ισχύος, όταν αυτό αναφέρεται στην είσοδο. Κατά συνέπεια, το σημείο συμπίεσης 1 dB του driver στην έξοδο θα πρέπει να είναι τουλάχιστον 3 dB υψηλότερο από το αντίστοιχο σημείο συμπίεσης 1 dB του σταδίου ενισχυτή ισχύος στην είσοδο. Επιπλέον, το σημείο συμπίεσης 1 dB στην έξοδο του driver δεν θα πρέπει να είναι υπερβολικά υψηλό, προκειμένου να περιοριστεί η υποβάθμιση της απόδοσης του συνολικού ενισχυτή ισχύος. Έτσι, για να γίνει ευκολότερος ο σχεδιασμός, μειώθηκε η πόλωση των πυλών του σταδίου ενισχυτή ισχύος κατά 0.01 V. Αυτό είχε ως αποτέλεσμα αύξηση της απόδοσης και του σημείου συμπίεσης 1 dB τόσο στην έξοδο όσο και στην είσοδο κάπως περισσότερο, αλλά μειώθηκε το κέρδος.

Ο driver που υλοποιήθηκε αποτελείται από δύο διαφορικά ζευγάρια συνδεδεμένα παράλληλα μεταξύ τους. Και τα δύο διαφορικά ζευγάρια αξιοποιούν τους neutralization πυκνωτές και μεταξύ των πυλών κάθε ζευγαριού τοποθετήθηκε μία αντίσταση. Συνδέσαμε δύο διαφορικά ζευγάρια, ώστε να είναι πιο εύκολο το matching μεταξύ των δύο σταδίων, μιας και κάθε ζευγάρι βλέπει αντίσταση διπλάσια από αυτήν στην είσοδο του μετασχηματιστή και απαιτείται, επίσης, σχετικά μεγάλη βέλτιστη αντίσταση να βλέπει το κάθε ζευγάρι.

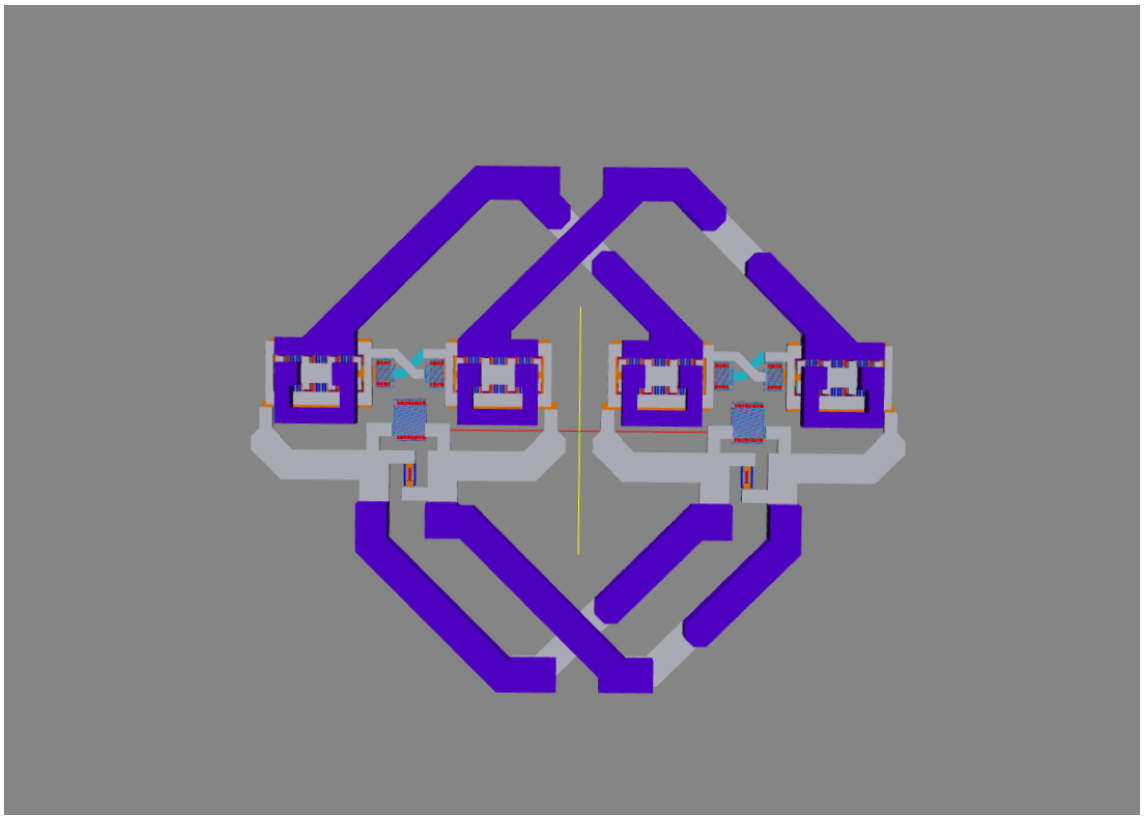
Το πάχος των τρανζίστορ επιλέχτηκε 200 $\mu$m ώστε να εξασφαλιστεί ικανοποιητικό κέρδος. Επίσης, επειδή το σημείο συμπίεσης 1 dB στην είσοδο του σταδίου ενισχυτή ισχύος είναι περίπου 7 dBm τόσο σε σχηματικό όσο και σε layout επίπεδο, κάθε ζευγάρι θα πρέπει να έχει σημείο συμπίεσης στην έξοδο του τουλάχιστον 8 dBm, λαμβάνοντας υπόψη τις απώλειες που θα προκαλέσουν το layout και η εισαγωγή πραγματικών στοιχείων. Παίρνοντας τα 1 dB compression point contours στην έξοδο κάθε διαφορικού ζευγαριού, καταφέραμε να εντοπίσουμε την αντίσταση που πρέπει να βλέπει κάθε ζευγάρι.

Ο μετασχηματιστής μεταξύ των δύο σταδίων είναι ακριβώς ίδιος με το balun στην έξοδο. Το balun στην είσοδο επιλέχτηκε και αυτό να χαρακτηρίζεται από μεγάλο συντελεστή σύζευξης και έχει ίδια δομή με το balun στην έξοδο, αλλά με μικρότερη εσωτερική διάμετρο και μικρότερο πάχος μετάλλων. Το balun φαίνεται στο σχήμα 1.7. Επίσης, στην είσοδο τόσο του balun όσο και του μετασχηματιστή τοποθετήθηκε ένας matching πυκνωτής.

Το layout του driver σταδίου παρουσιάζεται στο σχήμα 1.8.



Σχήμα 1.7: Balun στην είσοδο

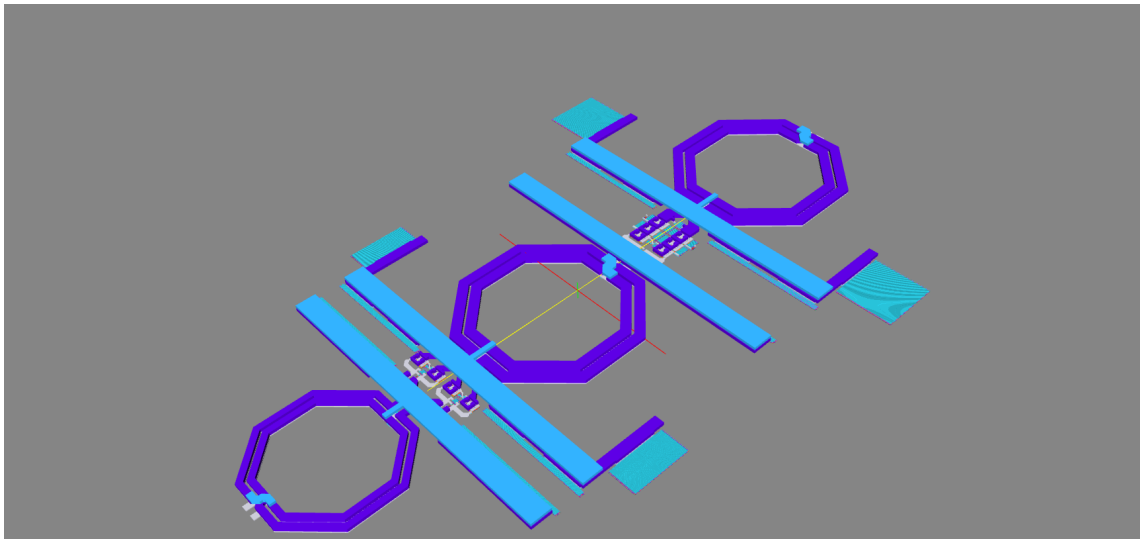


Σχήμα 1.8: Layout του Driver σταδίου

## 1.8 Δισταδιακός Ενισχυτής Ισχύος

Το layout του τελικού δισταδιακού ενισχυτή ισχύος φαίνεται στο σχήμα 1.9.

Στον πίνακα 1.3 παρουσιάζεται η σύγκριση των παραμέτρων επίδοσης μεταξύ των προσομοιώσεων σε επίπεδο σχηματικού και σε επίπεδο layout. Όπως φαίνεται, το layout επιφέρει μικρή μείωση στις επιδόσεις του ενισχυτή, ενώ παρατηρείται βελτίωση στη γραμμικότητα.



Σχήμα 1.9: Layout δισταδιακού ενισχυτή ισχύος

Πίνακας 1.3: Σύγκριση της επίδοσης του δισταδιακού ενισχυτή ισχύος μεταξύ schematic και post-layout αποτελεσμάτων

| **Parameter** | **Schematic** | **Layout** |
|---|---|---|
| Supply Voltage | 2.4 V | 2.4 V |
| Gain | 29.1 dB | 27.74 dB |
| Saturated Output Power ($P_{sat}$) | 23.22 dBm | 22.66 dBm |
| 1 dB Compression Point ($OP_{1\text{dB}}$) | 22.19 dBm | 21.26 dBm |
| PAE at 1 dB Compression Point ($PAE_{1\text{dB}}$) | 47.57% | 41.38% |
| Maximum PAE ($PAE_{\max}$) | 47.81% | 41.76% |
| Difference Between $IIP_3$ and $OP_{1\text{dB}}$ | 4 dB | 7.55 dB |

## 1.9 Συμπεράσματα και Μελλοντική Εργασία

Ο ενισχυτής ισχύος αποτελεί ένα από τα πιο κρίσιμα στάδια στον πομπό ενός τηλεπικοινωνιακού συστήματος. Είναι το μπλοκ με τη μεγαλύτερη κατανάλωση ισχύος σε ολόκληρο το σύστημα και πρέπει να παρέχει επαρκώς υψηλή ισχύ εξόδου με υψηλή απόδοση, ώστε να διασφαλίζεται η αποδοτική διαχείριση της ισχύος. Ταυτόχρονα, ο ενισχυτής ισχύος πρέπει να παρουσιάζει υψηλό κέρδος, ώστε τα προηγούμενα στάδια να μπορούν να τον οδηγήσουν αποτελεσματικά στο σημείο συμπίεσης 1 dB. Επιπλέον, απαιτείται καλή γραμμικότητα, για να διατηρείται υψηλή η ποιότητα της ζεύξης και να υποστηρίζονται σύγχρονα πολύπλοκα σχήματα διαμόρφωσης υψηλής τάξης με μεταβαλλόμενο φάσμα σήματος, που χρησιμοποιούνται ευρέως στα σύγχρονα ψηφιακά συστήματα επικοινωνίας.

Στην παρούσα εργασία, ο ενισχυτής ισχύος υλοποιήθηκε σε λειτουργία τάξης B, μία από τις τέσσερις κλασικές τάξεις ενισχυτών, που προσφέρει ισορροπία μεταξύ ισχύος εξόδου, κέρδους, αποδοτικότητας και γραμμικότητας. Για την αντιμετώπιση των περιορισμών των σύγχρονων τεχνολογιών πυριτίου — δηλαδή της χαμηλής ονομαστικής τάσης μεταξύ υποδοχής

και πηγής $V_{DS}$ — επιλέχθηκε η τοπολογία διαφορικού ενισχυτή ισχύος με διαδοχικά στοιβαγμένα τρανζίστορ. Η προσέγγιση αυτή επιτρέπει την επίτευξη ικανοποιητικά υψηλής ισχύος εξόδου, ενώ προσεκτικές επιλογές σχεδιασμού διασφαλίζουν ότι τόσο η τάση $V_{DS}$ όσο και η τάση $V_{GD}$ παραμένουν κάτω από τις τάσεις κατάρευσης, διατηρώντας την αξιοπιστία της συσκευής. Επιπλέον, προστέθηκε στάδιο οδήγησης για αύξηση του κέρδους.

Τα πολύπλοκα σχήματα διαμόρφωσης υψηλής τάξης με μεταβαλλόμενο φάσμα σήματος απαιτούν εξαιρετική γραμμικότητα. Ως εκ τούτου, ο ενισχυτής ισχύος συχνά καλείται να λειτουργεί σε συνθήκες Power Back-Off (PBO) — τυπικά 3, 6 ή ακόμα και 9 dB κάτω από το σημείο συμπίεσης 1 dB. Ωστόσο, η απόδοση μειώνεται σημαντικά. Συνεπώς, το επόμενο βήμα της έρευνας είναι η ανάπτυξη αρχιτεκτονικής ενισχυτή ισχύος που βελτιώνει την απόδοση στο PBO. Η πλέον διαδεδομένη τεχνική για αυτόν τον σκοπό είναι η αρχιτεκτονική Doherty. Παρόλα αυτά, η διερεύνηση μιας ευρύτερης γκάμας ιδεών και η πειραματική εξέταση εναλλακτικών τάξεων ενισχυτών πέρα από τις συμβατικές — όπως η τάξη J και η τάξη F [4] — μπορεί να οδηγήσει σε καινοτόμες λύσεις στο σχεδιασμό ενισχυτών ισχύος.

# Chapter 2

# Modern Telecommunication Systems

## 2.1 Digital Telecommunication Systems

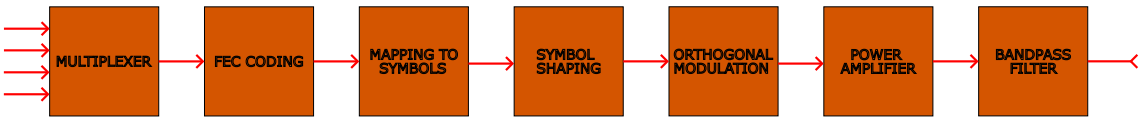



Figure 2.1: Transmitter

Modern telecommunication transmitters follow the architecture shown in Figure 2.1 [5]. Initially, multiple streams of digital information are multiplexed into a single stream. This is followed by the Forward Error Correction (FEC) stage, which adds redundant bits to enable error detection and correction to the receiver. While this process decreases Bit Error Ratio (BER), it also reduces the effective data rate by a factor $R_c$. This factor, called Code Rate, is given by the following equation:

$$R_c = \frac{k}{n} \tag{1}$$

- $k$ is the number of information bits
- n is the total number of transmitted bits

After that, the bits are mapped to symbols through a modulation scheme. Then, the symbols are shaped using a shaping pulse. The most common shaping pulses are square pulses and raised cosine pulses. The shaped symbols pass through an orthogonal modulator, as shown in Figure 2.2.

Next, a Power Amplifier (PA) is used to provide the signal with sufficient power, and the signal is transmitted through the antenna. Sometimes, a bandpass filter is inserted directly after the PA in order to limit the transmitted bandwidth within its allocated region. This is necessary because the nonlinear behavior of the PA causes spectral expansion of the signal. As a result, the bandpass filter reduces Adjacent Channel Interference (ACI).

The receiver follows the same architecture as the transmitter, but in reverse. Subsequently, the operation of the superheterodyne receiver is analyzed.

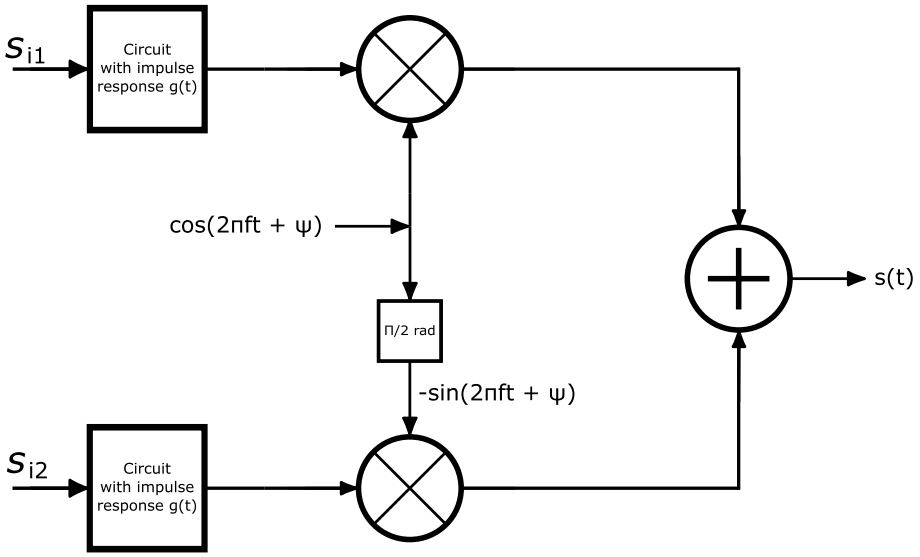



Figure 2.2: The orthogonal modulator along with the pulse shaping circuit

## 2.2 Superheterodyne Receiver

The block diagram of the superheterodyne receiver is presented in Figure 2.3. Special attention must be given to the first four stages. Initially, a bandpass filter is used to remove signals that fall outside the frequency band of interest. The following stage is a Low Noise Amplifier (LNA), which provides sufficient gain while maintaining a low Noise Figure (see Chapter 3.2.6). This design approach minimizes the overall Noise Figure of the system up to the input of the decision circuit (Figure 2.5). This can be demonstrated using Friis' equation for noise (see Chapter 3.2.7), which describes how the total Noise Figure of a cascaded system is influenced primarily by the first few stages.

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdots \tag{2}$$

- $NF_i$ is the Noise Figure of stage i
- $G_i$ is the gain of stage i

The LNA is followed by the Intermediate Frequency (IF) stage (Figure 2.4). In this stage, the signal frequency is down-converted to the intermediate frequency using a mixer and a bandpass filter centered at the IF frequency. The resulting IF signal is then amplified. The intermediate frequency is fixed and independent of the desired signal frequency, $f_c$. Therefore, the frequency of the Local Oscillator (LO) should be set to $f_{LO} = f_c - f_{IF}$ or $f_{LO} = f_c + f_{IF}$. Additionally, the intermediate frequency is small compared to $f_c$.

The superheterodyne receiver faces a problem when unwanted out-of-band signals exist at the image frequencies [6]. When an interfering signal with frequency $f_{IM}$ enters the input

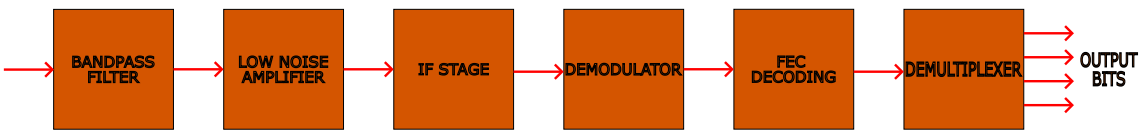



Figure 2.3: Superheterodyne Receiver

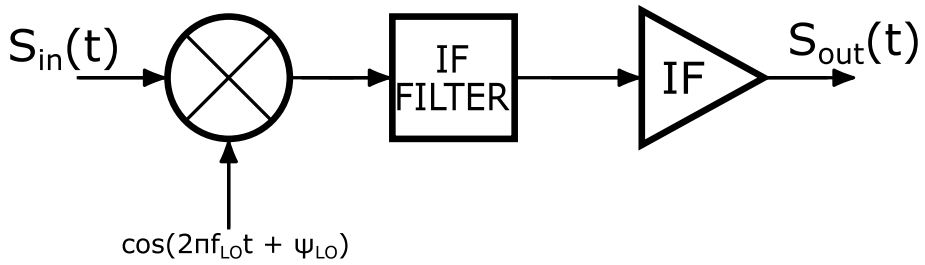



Figure 2.4: Intermediate Frequency stage

of the IF stage mixer, the output contains both the sum and difference frequencies of the inputs with the frequency of the LO:

- $f_{LO} + f_c$
- $f_{LO} + f_{IM}$
- $f_{LO} - f_c$
- $f_{LO} - f_{IM}$

Interference occurs when $f_{LO} - f_c = f_{IM} - f_{LO} = f_{IF}$. Thus, the image frequencies are $f_{IM} = f_c + 2f_{IF}$ or $f_{IM} = f_c - 2f_{IF}$. Because the intermediate frequency is small compared to $f_c$, the image frequencies are located very close to the desired signal frequency. It is obvious that the image frequency problem is serious and should be countered.

This problem can be alleviated by adding a bandpass filter centered around $f_c$ directly after the LNA. This design approach is hard to implement, as the bandpass filter's response should be very steep. There are other architectures that counter the Image frequency problem more efficiently [1].

After the IF stage the signal is demodulated by the circuit shown in Figure 2.5. The quality of the overall system can be quantified by the Bit Error Ratio (BER). The BER depends on the Signal-to-Noise Ratio (see Chapter 3.2.5) at the input of the decision circuit, the modulation scheme and the code rate $R_c$.

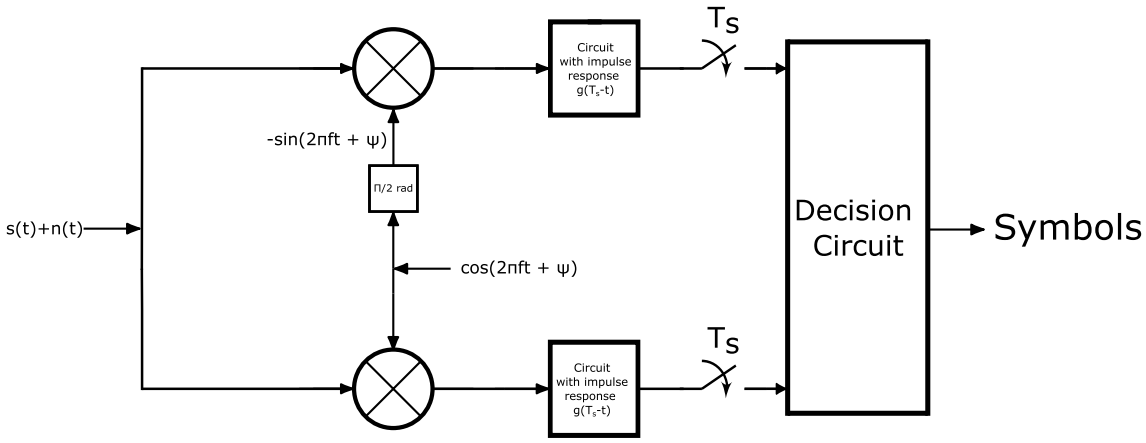



Figure 2.5: Demodulator

# Chapter 3

# Basic Telecommunication Terms and Definitions

## 3.1 High-Frequency Measurement Units

In telecommunications, specific units are used to express gain and signal levels. Voltage gain and power gain are typically expressed in decibels (dB) as:

$$A_V = 20 \log \left( \frac{V_{\text{out}}}{V_{\text{in}}} \right) \tag{1}$$

$$A_P = 10 \log \left( \frac{P_{\text{out}}}{P_{\text{in}}} \right) \tag{2}$$

The power of a signal is usually expressed in dBm, which represents the power level in decibels relative to a reference of 1 milliwatt:

$$P_{\text{dBm}} = 10 \log \left( \frac{P_s}{1\,\text{mW}} \right) \tag{3}$$

Other commonly used measurement units include:

- dBW: A unit frequently used in power amplifiers, where the reference power is 1 Watt.
- dBuV: Used in receiver measurements, with a reference voltage of 1 μV.
- dBi: Describes the gain of an antenna relative to the gain of an ideal isotropic radiator.
- dB/Hz: Represents noise power within a 1 Hz bandwidth. It is commonly used to characterize spectral noise density.

## 3.2 Noise

Noise is an unwanted entity of the same nature as the signals, which interferes with them and degrades the reliability of telecommunication systems. Noise is mathematically described as a random process and usually consists of uncorrelated noise sources of different origins, which combine in a random manner [5].

### 3.2.1 Parameters Describing Noise

- Mean value of the noise signal $n(t)$:

$$\mathbb{E}[n(t)] = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} n(t)\, dt \tag{4}$$

- Mean square value of the noise signal:

$$\mathbb{E}[n^2(t)] = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} n^2(t)\, dt \tag{5}$$

- Power spectral density (PSD) of the noise signal, which describes how the noise power is distributed over the frequency domain. When the PSD refers only to positive frequencies, it is called one-sided; when it refers to both positive and negative frequencies, it is called two-sided.

### 3.2.2 White Noise

In telecommunications, the most common type of noise is white noise, whose power is uniformly distributed across the frequency domain. As a result, the power spectral density of white noise is constant. More specifically, the one-sided power spectral density is given by:

$$S_n(f) = n_0 \quad \text{for } f \geq 0 \tag{6}$$

Additionally, in telecommunications systems, white noise is typically assumed to be additive, hence referred to as Additive White Gaussian Noise (AWGN).

### 3.2.3 Thermal Noise

The random movement of electrons in a resistor produces a noise voltage at its terminals, characterized by the following two-sided power spectral density:

$$S_n(f) = 2\frac{h|f|}{\exp\left(\frac{h|f|}{kT_s}\right) - 1} \tag{7}$$

- $h$ is the Planck constant,
- $k$ is the Boltzmann constant,
- $T_s$ is the physical temperature of the resistor.

For temperatures up to 300 K and frequencies up to approximately 6 THz, this relation can be accurately approximated as:

$$S_n(f) \approx 2kT_s \tag{8}$$

The available thermal noise power produced by a resistor over a bandwidth $B$ is given by:

$$N = kT_sB \tag{9}$$

### 3.2.4 Equivalent Noise Temperature

A noise source produces white noise and transfers it to a load. Its one-sided power spectral density can be expressed by the following relation:

$$n_0 = kT_e \tag{10}$$

- $k$ is the Boltzmann constant
- $T_e$ is the equivalent noise temperature

Equivalent noise temperature of a noisy source is the physical temperature of a resistor that produces, over the same frequency bandwidth, the same available noise power as the noisy source. The available noise power of this source is given by:

$$N = kT_eB \tag{11}$$

- $B$ is the operating bandwidth

Equivalent noise temperature can be used to quantify the noise of a component or a circuit of a telecommunication system. A characteristic example is the equivalent noise temperature of an antenna.

### 3.2.5 Signal-to-Noise Ratio (SNR)

The quality of the signal at the receiver is expressed by the Signal-to-Noise Ratio (SNR), defined as:

$$\text{SNR} = \frac{P_{\text{signal}}}{P_{\text{noise}}} \tag{12}$$

This quantity plays a decisive role in the receiver sensitivity and the overall quality of the communication link.

### 3.2.6 Noise Figure (NF)

The degradation of the signal-to-noise ratio caused by a stage is expressed by the Noise Figure (NF), defined as:

$$NF = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \tag{13}$$

- $\text{SNR}_{\text{in}}$ is the Signal-to-Noise Ratio at the input of the stage
- $\text{SNR}_{\text{out}}$ is the Signal-to-Noise Ratio at the output of the stage

### 3.2.7 Noise in Multiple cascaded stages

If the gain of a stage is $G$, then the Noise Figure (NF) can be written as:

$$NF = \frac{S_i/N_i}{S_o/N_o} = \frac{S_i/N_i}{(GS_i)/N_o} = \frac{N_o}{GN_i} \tag{14}$$

The total noise at the output is given by $N_o = GN_i + N_n$, where $N_n$ is the additional noise contributed by the stage. Thus, the Noise Figure becomes:

$$NF = \frac{GN_i + N_n}{GN_i} = 1 + \frac{N_n}{GN_i} \tag{15}$$

Next, the Noise Figure of two cascaded stages will be calculated. The gain of the first and second stage is $G_1$ and $G_2$, respectively. The noise at the output of the first stage is:

$$N_{o1} = G_1N_i + N_{n1}$$

The total noise at the output of the second stage is:

$$N_o = G_2N_{o1} + N_{n2} = G_1G_2N_i + G_2N_{n1} + N_{n2}$$

Using equation (14), the overall Noise Figure of the system is:

$$NF = \frac{N_o}{G_1G_2N_i} = 1 + \frac{N_{n1}}{G_1N_i} + \frac{N_{n2}}{G_1G_2N_i} \tag{16}$$

From equation (15) we obtain:

$$NF_1 - 1 = \frac{N_{n1}}{G_1N_i} \quad \text{and} \quad NF_2 - 1 = \frac{N_{n2}}{G_2N_i}$$

Therefore, the total Noise Figure becomes:

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} \tag{17}$$

If we have $n$ cascaded stages, the expression generalizes to:

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1G_2} + \cdots + \frac{NF_n - 1}{G_1G_2\cdots G_{n-1}} \tag{18}$$

- $NF_i$ is the Noise Figure of stage i
- $G_i$ is the gain of stage i

This equation is known as Friis' equation for noise. It is evident that the first stage must have a low noise figure and high gain in order to minimize the overall Noise Figure of the system.

## 3.3 Nonlinearities

RF circuits are typically approximated by a linear model. However, in reality, their behaviour is inherently nonlinear and can be described using a polynomial system approximation, as follows:

$$u_{\text{out}} = k_0 + k_1 u_{\text{in}} + k_2 u_{\text{in}}^2 + k_3 u_{\text{in}}^3 + \dots \tag{19}$$

The term $k_1$ represents the small-signal gain, while the higher-order terms $k_2$, $k_3$, ... can be neglected when the input signal is sufficiently small [6].

### 3.3.1 Harmonic Distortion

If the input signal is $u_{in} = u\cos(\omega t)$, then:

$$\cos^2(\omega t) = \frac{1 + \cos(2\omega t)}{2} \tag{20}$$

$$\cos^3(\omega t) = \frac{3}{4}\cos(\omega t) + \frac{1}{4}cos(3\omega t) \tag{21}$$

By taking into consideration only the terms $k_0, k_1, k_2, k_3$, we get:

$$u_{out} = k_0 + \frac{k_2 u^2}{2} + \left(k_1 u + \frac{3k_3 u^3}{4}\right)\cos(\omega t) + \frac{k_2 u^2}{2}\cos(2\omega t) + \frac{k_3 u^3}{4}\cos(3\omega t) \tag{22}$$

- $k_0 + \frac{k_2 u^2}{2}$ is the DC component
- $k_1 u + \frac{3k_3 u^3}{4}$ is the fundamental term
- $\frac{k_2 u^2}{2}$ is the second harmonic term
- $\frac{k_3 u^3}{4}$ is the third harmonic term

It is evident that the gain of the fundamental frequency component is given by:

$$k_1 + \frac{3k_3 u^2}{4}$$

This expression shows that the gain depends on the input signal's amplitude.

When $k_1 \cdot k_3 > 0$, the gain increases with input level, and the output signal exhibits expansion for sufficiently large inputs (Figure 3.1(a)). On the other hand, when $k_1 \cdot k_3 < 0$, the gain decreases as the input grows, resulting in compression of the output signal at high input levels (Figure 3.1(b)).

### 3.3.2 1-dB Compression Point

When the amplifier characteristic is compressive, the concept of the 1-dB compression point is introduced.

The *1-dB compression point* is defined as the output power level, $A_{\text{out}}$, at which the small-signal gain $G$ has decreased by 1 dB from its linear value, observed under low input power conditions.

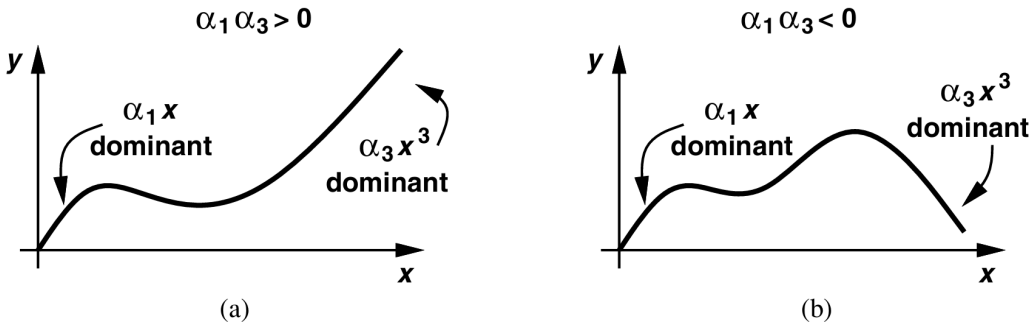



Figure 3.1: (a) Expansive and (b) Compressive characteristics [1]

Figure 3.2 illustrates the input-output power characteristic of a nonlinear system on a logarithmic scale.

The input-referred 1-dB compression point can be calculated by equating the compressed gain, $k_1 + \frac{3k_3u^2}{4}$, with the ideal linear gain $k_1$ reduced by 1 dB, as follows:

$$20\log\left|k_1 + \frac{3k_3u^2}{4}\right| = 20\log|k_1| - 1 \tag{23}$$

Therefore:

$$u_{\text{in, 1dB}} = \sqrt{0.145\left|\frac{k_1}{k_3}\right|} \tag{24}$$

### 3.3.3 Intermodulation

When two interfering signals at frequencies $\omega_1$ and $\omega_2$ are applied to a nonlinear system, the output contains components that are not harmonics of either frequency. Some of these

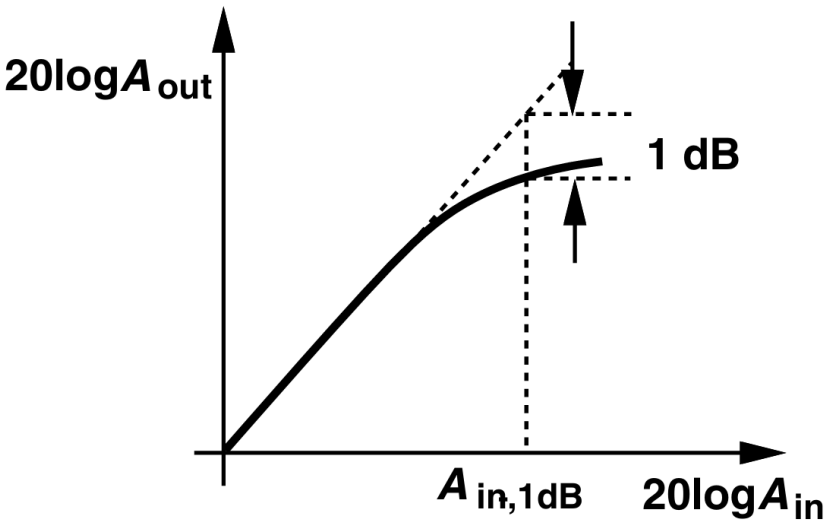



Figure 3.2: Input-output power characteristic of a nonlinear system [1]

components may fall near or directly interfere with the desired signal at frequency $\omega_0$. This phenomenon is known as intermodulation.

In the following, we will compute the output of a nonlinear system by retaining only the terms $k_0$, $k_1$, $k_2$, and $k_3$, when the input signal is given by:

$$u_{\text{in}} = u_1 \cos(\omega_1 t) + u_2 \cos(\omega_2 t).$$

At the output, we obtain the following components:

- Fundamental components at frequencies $\omega_1$ and $\omega_2$:

$$\left(k_1 u_1 + \frac{3}{4} k_3 u_1^3 + \frac{3}{2} k_3 u_1 u_2^2\right) \cos(\omega_1 t) + \left(k_1 u_2 + \frac{3}{4} k_3 u_2^3 + \frac{3}{2} k_3 u_2 u_1^2\right) \cos(\omega_2 t) \quad (25)$$

- Third order intermodulation products:

$$\frac{3 k_3 u_1^2 u_2}{4} \cos\big((2\omega_1 + \omega_2)t\big) + \frac{3 k_3 u_1^2 u_2}{4} \cos\big((2\omega_1 - \omega_2)t\big) \quad (26)$$

$$\frac{3 k_3 u_1 u_2^2}{4} \cos\big((2\omega_2 + \omega_1)t\big) + \frac{3 k_3 u_1 u_2^2}{4} \cos\big((2\omega_2 - \omega_1)t\big) \quad (27)$$

Thus, we observe intermodulation products at frequencies $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$. The components $2\omega_1 - \omega_2$, $2\omega_2 - \omega_1$ may fall near the desired signal frequency and cause significant distortion.

### 3.3.4 Third Order Intercept Point (IP3)

The most common method for testing a circuit's linearity is to apply two input signals of equal amplitude, spaced apart in frequency. By observing the output power levels of the fundamental components and the intermodulation products as a function of the input power, we can assess the linearity of the circuit (Figure 3.3).

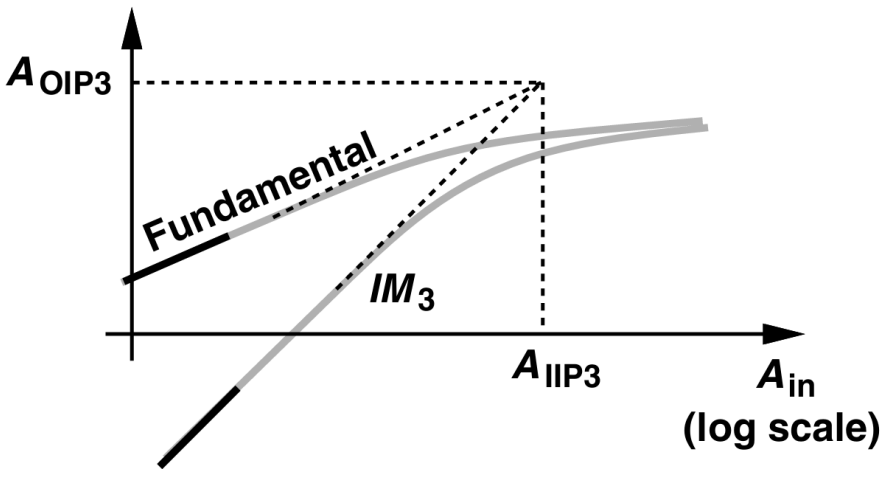



Figure 3.3: Definition of IP3 based on extrapolation [1]

The *Third-Order Intercept Point* (IP3) is defined as the theoretical point at which the amplitudes of the third-order intermodulation products at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ become equal to the amplitudes of the fundamental tones at $\omega_1$ and $\omega_2$.

To calculate the input-referred Third-Order Intercept Point (IIP3), we equate the linear term from the fundamental component, $k_1 u_i$, with the third-order intermodulation term, $IM_3 = \frac{3}{4} k_3 u_i^3$. Solving for the input voltage gives:

$$u_{\text{IIP3}} = 2\sqrt{\frac{k_1}{3|k_3|}} \tag{28}$$

In practice, the IIP3 cannot be measured directly, as it corresponds to a hypothetical point where the amplifier would be driven into severe nonlinearity or even damage. Therefore, it is extrapolated from measurements at lower power levels.

Consider a system with gain $G$, and suppose that at a certain input power level $P_i$ (dBm), the output power of the fundamental is $P_1$ (dBm), and the output power of the third-order intermodulation product is $P_3$ (dBm). On a logarithmic scale, the slope of the intermodulation products is three times that of the fundamental components. Hence, the following relationship holds:

$$\frac{OIP3 - P_3}{IIP3 - P_i} = 3 \cdot \frac{OIP3 - P_1}{IIP3 - P_i} \tag{29}$$

Additionally, the gain of the system is:

$$G = OIP3 - IIP3 = P_1 - P_i \tag{30}$$

Combining the above expressions, we derive the IIP3 as:

$$\text{IIP3} = P_i + \frac{1}{2}(P_1 - P_3) \tag{31}$$

By comparing equations (24) and (28), we observe that the input-referred Third-Order Intercept Point (IIP3) is approximately 3.04 times higher than the input-referred 1-dB Compression Point.

Similarly, the *Second-Order Intercept Point* (IP2) is defined in the same manner as the third-order intercept point, but it relates to the amplitudes of the second-order intermodulation products instead of the third-order terms.

### 3.3.5 Linearity of Cascaded Stages

It can be shown that the input-referred Third-Order Intercept Point (IIP3) of $N$ cascaded stages is given by the following equation:

$$\frac{1}{\text{IIP3}_{\text{total}}} = \frac{1}{\text{IIP3}_1} + \frac{G_1}{\text{IIP3}_2} + \frac{G_1 G_2}{\text{IIP3}_3} + \cdots + \frac{G_1 G_2 \ldots G_{N-1}}{\text{IIP3}_N} \tag{32}$$

- $G_i$ is the gain of stage $i$
- $\text{IIP3}_i$ is the input-referred Third-Order Intercept Point of stage $i$

We observe that the IIP3 of the later stages becomes more critical, since it is divided by the total gain of all preceding stages. A high gain in the early stages significantly amplifies the nonlinearity of the subsequent ones, making their intercept point a dominant factor in the overall system performance.

## 3.4 Performance Metrics of Power Amplifiers

A power amplifier is, in general, a nonlinear circuit. In order to characterize its performance, the quantities defined in the previous section are used, as well as additional parameters introduced in this section.

### 3.4.1 Saturated Power

Due to the output power compression caused by nonlinearities, a power amplifier cannot increase its output indefinitely. Instead, it reaches a maximum output power level, which is referred to as the *saturated power* $P_{\text{sat}}$.

It is important to note that power amplifiers are typically operated at output power levels below saturation. This is done mainly to maintain better linearity and also for reasons of energy efficiency.

### 3.4.2 Power Gain

Power gain is defined as the ratio of output power to input power and is usually expressed in decibels (dB):

$$G = \frac{P_{\text{out}}}{P_{\text{in}}} \tag{33}$$

$$G(\text{dB}) = P_{\text{out}}(\text{dB}) - P_{\text{in}}(\text{dB}) \tag{34}$$

### 3.4.3 Efficiency

The term efficiency refers to the ratio of the useful RF output power to the supplied DC power. It is defined as:

$$\eta = \frac{P_{\text{out}}}{P_{\text{DC}}} \cdot 100\% \tag{35}$$

### 3.4.4 Power-Added Efficiency (PAE)

The efficiency of a power amplifier, as previously defined, does not take into account the power required to drive the amplifier. As a result, it is possible to achieve high efficiency values without delivering significant power amplification. To address this limitation, a more comprehensive performance metric has been established: the Power-Added Efficiency (PAE). It is defined as:

$$\text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \cdot 100\% \tag{36}$$

Substituting the efficiency definition from equation (35) into the above equation, we get:

$$\text{PAE} = \frac{1 - \frac{P_{\text{in}}}{P_{out}}}{\frac{P_{\text{DC}}}{P_{out}}} \cdot 100\% = \eta \left(1 - \frac{1}{G}\right) \tag{37}$$

# Chapter 4

# RF Circuits as Microwave Networks

The analysis, approximation, and measurement of RF circuits and components are usually carried out using scattering parameters (S-parameters). Although the basic and well-known parameters for the analysis and design of electrical circuits are those of impedance (Z-parameters) and admittance (Y-parameters), their use is rather limited in RF circuit design. This is due to the fact that open and short circuits, which are required for the determination of these parameters, are difficult or even impossible to implement at high frequencies, especially over wide frequency ranges, creating measurement problems due to high parasitic impedances and admittances.

## 4.1 Scattering Parameters

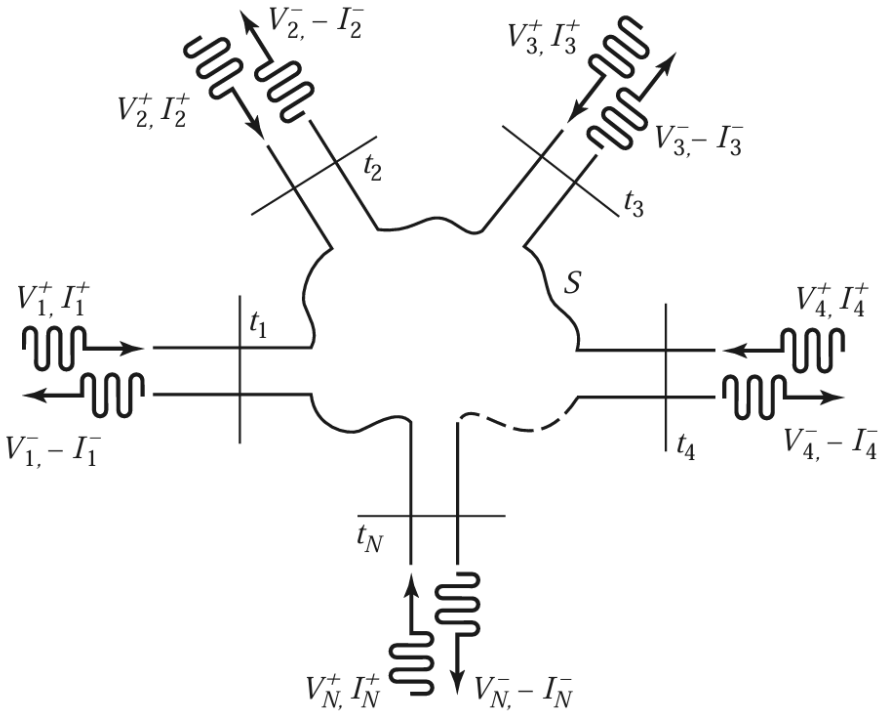



Figure 4.1: N-port microwave network [2]

Consider the $N$-port network shown in Figure 4.1, where $V_n^+$ is the amplitude of the voltage wave incident on port $n$, and $V_n^-$ is the amplitude of the voltage wave reflected from port $n$. By simplifying the analysis and assuming the same characteristic impedance $Z_0$ in all branches of the $N$-port network, the normalized incident and reflected power waves are expressed respectively as follows:

$$a_i = \frac{V_i^+}{\sqrt{Z_0}} \tag{1}$$

$$b_i = \frac{V_i^-}{\sqrt{Z_0}} \tag{2}$$

The above definition of the $i$-th incident wave $a_i$ and reflected wave $b_i$ is not unique. The relationship between the vectors $\mathbf{a}$ and $\mathbf{b}$ can be described using the following scattering matrix:

$$\mathbf{b} = \mathbf{S} \cdot \mathbf{a} \tag{3}$$

which is expanded as:

$$\begin{pmatrix} b_1 \\ \vdots \\ b_n \end{pmatrix} = \begin{pmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{nn} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ \vdots \\ a_n \end{pmatrix} \tag{4}$$

where

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k=0,\, \forall k \neq j} \tag{5}$$

The above equation represents the transmission coefficient from port $j$ to port $i$ and is determined by driving port $j$ with an incident wave $a_j$ and measuring the reflected wave $b_i$ at port $i$, while all other ports are terminated in the characteristic impedance $Z_0$ (i.e., $a_k = 0$ for $k \neq j$) to avoid reflections.

If the network is a two-port one, then:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{6}$$

Analyzing the matrix in Equation (6), we obtain the following equations:

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{7}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{8}$$

Assuming an incident power wave at port 1 ($a_1$), this will result in reflected waves at each port ($b_1$, $b_2$). However, according to the definition of the S-parameters, port 2 is terminated with a load equal to the system's characteristic impedance $Z_0$, maximizing power transfer to the load and making the reflected wave $a_2$ at port 2 equal to zero. Defining the incident and reflected power waves as in Equations (1) and (2), we derive the following:

- $S_{11} = \frac{b_1}{a_1}\big|_{a_2=0} = \frac{V_1^-/\sqrt{Z_0}}{V_1^+/\sqrt{Z_0}}\big|_{a_2=0} = \frac{V_1^-}{V_1^+}\big|_{a_2=0}$
- $S_{21} = \frac{b_2}{a_1}\big|_{a_2=0} = \frac{V_2^-/\sqrt{Z_0}}{V_1^+/\sqrt{Z_0}}\big|_{a_2=0} = \frac{V_2^-}{V_1^+}\big|_{a_2=0}$

Similarly, if port 1 is terminated with a load $Z_0$, then $a_1 = 0$ (i.e., no reflected wave at port 1), and we obtain:

- $S_{12} = \frac{b_1}{a_2}\big|_{a_1=0} = \frac{V_1^-/\sqrt{Z_0}}{V_2^+/\sqrt{Z_0}}\big|_{a_1=0} = \frac{V_1^-}{V_2^+}\big|_{a_1=0}$
- $S_{22} = \frac{b_2}{a_2}\big|_{a_1=0} = \frac{V_2^-/\sqrt{Z_0}}{V_2^+/\sqrt{Z_0}}\big|_{a_1=0} = \frac{V_2^-}{V_2^+}\big|_{a_1=0}$

With this process, we derive the scattering matrix, whose elements are ratios of normalized voltage waveforms.

Looking more closely, we can draw several critical conclusions about the behavior of the microwave two-port network:

- The parameter $S_{11} = \frac{V_1^-}{V_1^+}$ is known as the input reflection coefficient of the two-port.
- The parameter $S_{12} = \frac{V_1^-}{V_2^+}$ is known as the reverse gain or isolation from the output to the input.
- The parameter $S_{21} = \frac{V_2^-}{V_1^+}$ represents the power gain of the two-port under matched conditions.
- The parameter $S_{22} = \frac{V_2^-}{V_2^+}$ is known as the output reflection coefficient of the two-port.

## 4.2 Stability

Consider the two-port network shown in Figure 4.2.

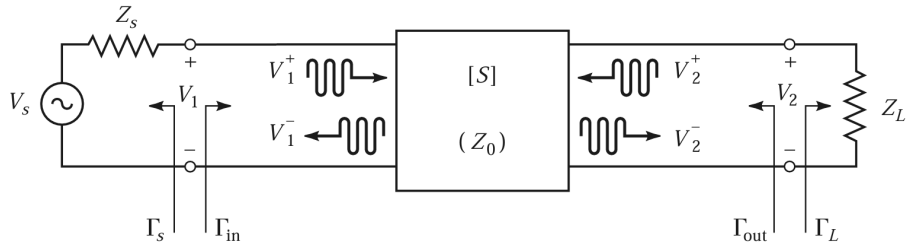



Figure 4.2: Two-port network with an AC voltage source $V_s$ at the input, a source resistance $Z_s$, and a load resistance $Z_L$ at the output [2]

After deriving the scattering matrix of the two-port network and considering $Z_S$ and $Z_L$ as the source and load impedances respectively, we can determine the reflection coefficients, which are shown in the figure as $\Gamma_S$, $\Gamma_{\text{in}}$, $\Gamma_{\text{out}}$, and $\Gamma_L$.

With reference to the above figure, the reflection coefficient looking towards the load is defined as:

$$\Gamma_L = \frac{V_2^-}{V_2^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{9}$$

while the reflection coefficient looking towards the source is defined as:

$$\Gamma_S = \frac{V_1^-}{V_1^+} = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{10}$$

where $Z_0$ is the characteristic impedance used in the definition of the scattering parameters.

As is well known from microwave analysis, maximum power transfer between two two-port networks is achieved through impedance matching. Assuming each two-port has a complex input and output impedance, matching is achieved when the output impedance of the previous stage is the complex conjugate of the input impedance of the next. If the output impedance of the first two-port is purely real (i.e., resistive), then maximum power transfer occurs when the input impedance of the next two-port is also purely real and equal in value.

Using the definitions of the $S$-parameters and reapplying equations (7) and (8), and substituting $a_1$, $a_2$, $b_1$, $b_2$ from equations (1) and (2), we get:

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ = S_{11}V_1^+ + S_{12}\Gamma_L V_2^- \tag{11}$$
$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ = S_{21}V_1^+ + S_{22}\Gamma_L V_2^- \tag{12}$$

Substituting equation (12) into equation (11) and solving for $\Gamma_{\text{in}} = \frac{V_1^-}{V_1^+}$ gives:

$$\Gamma_{\text{in}} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{Z_{\text{in}} - Z_0}{Z_{\text{in}} + Z_0} \tag{13}$$

where $\Gamma_{\text{in}}$ is the input reflection coefficient and $Z_{\text{in}}$ is the impedance seen at the input of the two-port.

Similarly, the output reflection coefficient is defined as:

$$\Gamma_{\text{out}} = \frac{V_2^-}{V_2^+} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} = \frac{Z_{\text{out}} - Z_0}{Z_{\text{out}} + Z_0} \tag{14}$$

where $\Gamma_{\text{out}}$ is the output reflection coefficient and $Z_{\text{out}}$ is the impedance seen at the output of the two-port.

### 4.2.1 Unconditional Stability and Stability Circles

Returning to Figure 4.2 and analyzing the stability criteria of the two port network, we know that oscillation—and by extension, instability—arises when either the input or the output port of the two-port presents an impedance with a negative real part. Such a condition implies that $|\Gamma_{\text{in}}| > 1$ or $|\Gamma_{\text{out}}| > 1$.

Since, as previously shown, the reflection coefficients $\Gamma_{\text{in}}$ and $\Gamma_{\text{out}}$ depend on the input and output matching networks of the two-port, the amplifier's stability is influenced by the source and load reflection coefficients $\Gamma_S$ and $\Gamma_L$, respectively. Therefore, we define two types of stability:

- Unconditional stability: This occurs when $|\Gamma_{\text{in}}| < 1$ and $|\Gamma_{\text{out}}| < 1$ for all possible values of $\Gamma_S$ and $\Gamma_L$ at a given frequency.
- Conditional stability: This occurs when $|\Gamma_{\text{in}}| < 1$ and $|\Gamma_{\text{out}}| < 1$ only for specific values of $\Gamma_S$ and $\Gamma_L$ at a given frequency.

Applying the unconditional stability requirements to equations (13) and (14) yields the following conditions for $\Gamma_S$ and $\Gamma_L$:

$$|\Gamma_{\text{in}}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{15}$$
$$|\Gamma_{\text{out}}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{16}$$

If the amplifier is unilateral (i.e., $S_{12} = 0$), the above conditions simplify to the basic and sufficient conditions $|S_{11}| < 1$ and $|S_{22}| < 1$ for unconditional stability.

Otherwise, inequalities (15) and (16) define a range of values for $\Gamma_S$ and $\Gamma_L$ over which the amplifier remains stable. The boundaries of this range can be found graphically using the Smith chart by plotting the input and output stability circles.

Stability circles are defined as the loci in the $\Gamma_L$ (or $\Gamma_S$) plane for which $|\Gamma_{\text{in}}| = 1$ (or $|\Gamma_{\text{out}}| = 1$). These circles determine the boundaries between stable and potentially unstable regions of $\Gamma_S$ and $\Gamma_L$.

To derive the output stability circle, we start with:

$$|\Gamma_{\text{in}}| = 1 \Leftrightarrow \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| = 1 \Leftrightarrow |S_{11}(1 - S_{22}\Gamma_L) + S_{12}S_{21}\Gamma_L| = |1 - S_{22}\Gamma_L| \quad (17)$$

Define the determinant of the $S$-matrix as:

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (18)$$

Then equation (17) becomes:

$$|S_{11} - \Delta\Gamma_L| = |1 - S_{22}\Gamma_L| \quad (19)$$

From equation (19), after algebraic manipulation we obtain the geometric form of the reflection coefficient locus $\Gamma_L$, which leads to:

$$\left| \Gamma_L - \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \right| = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \quad (20)$$

This equation has the form $|\Gamma - C| = R$, representing a circle with center $C$ and radius $R$. Thus, we define the output stability circle with:

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \quad (21)$$

$$R_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \quad (22)$$

Similarly, we can derive the input stability circle, defined by:

$$C_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \quad (23)$$

$$R_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \quad (24)$$

### 4.2.2 Unconditional Stability Verification Using Mathematical Criteria

The stability circles discussed above can be used to determine the regions in the $\Gamma_S$ and $\Gamma_L$ planes where the amplifier will be conditionally stable. However, simpler checks exist for determining unconditional stability. One such method is the K–$\Delta$ test, which establishes that a device is unconditionally stable if the Rollet stability factor, defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (25)$$

and the auxiliary condition:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{26}$$

are both satisfied simultaneously.

These two conditions are necessary and sufficient for unconditional stability and can be easily evaluated from the $S$-parameters of the device. If the $S$-parameters do not satisfy the K–$\Delta$ test, the device is not unconditionally stable, and the stability circles must be used to determine whether there exist values of $\Gamma_S$ and $\Gamma_L$ for which the device is conditionally stable.

Another widely used stability criterion is the μ-stability facto, defined as:

$$\mu = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} \tag{27}$$

A two-port network is unconditionally stable at a given frequency if and only if:

$$\mu > 1 \tag{28}$$

The μ-factor provides a more direct and often numerically stable method of assessing unconditional stability, particularly in automated design tools or when evaluating broadband behavior.

## 4.3 High-Frequency Model of the MOS Transistor

The electrical behavior of the MOS transistor at high frequencies can be approximated by the simplified equivalent circuit shown in Figure 4.3. The resistance $r_g$ represents the gate resistance, while $g_{ds}$ denotes the output conductance. The parameter $g_m$ corresponds to the transistor's transconductance, and $g_s$ represents the body-effect transconductance.

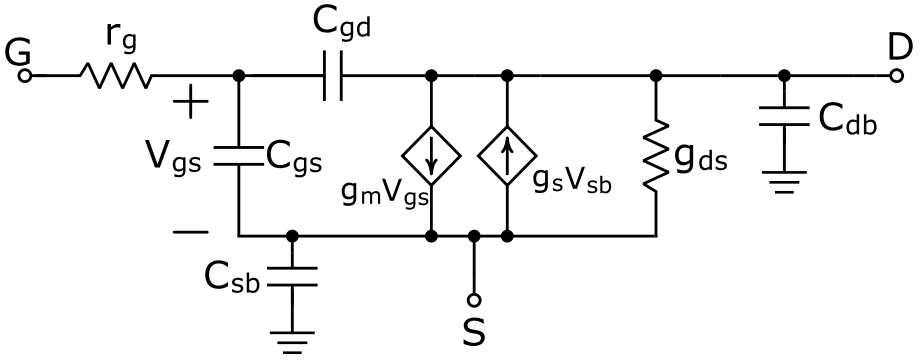



Figure 4.3: Equivalent high-frequency model of the MOS transistor

The overlap capacitance between the gate and the source/drain regions, due to the gate's lateral extension over these regions with overlap length $L_D$, is given by:

$$C_{ov} = \frac{\epsilon_{ox}}{t_{ox}} W L_D \tag{29}$$

The gate-channel capacitance $C_{gc}$, corresponding to the effective channel length reduced by the two overlap regions, is expressed as:

$$C_{gc} = C_{ox}W(L - 2L_D) \tag{30}$$

In strong inversion, the surface charge carriers are of opposite type compared to the substrate. Between them lies a depletion layer of depth $x_d$, resulting in a depletion capacitance between the channel and the substrate, defined as:

$$C_{db} = \frac{\epsilon_{Si}}{x_d}W(L - 2L_D), \quad \text{where} \quad x_d = \sqrt{\frac{2\epsilon_{Si}}{qN_{sub}}\left|\phi_s - \phi_F\right|} \tag{31}$$

where $\phi_s$ is the surface potential, and $\phi_F$ is the Fermi potential of the substrate.

The source and drain contacts to the substrate are reverse-biased junctions and thus exhibit junction capacitances, modeled respectively as:

$$C_{jsb} = \frac{C_{sb0}}{\sqrt{1 + \frac{V_{SB}}{V_0}}} \tag{32}$$

$$C_{jdb} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{V_0}}} \tag{33}$$

where $C_{sb0}$ and $C_{db0}$ are the zero-bias junction capacitances of the source and drain, respectively, $V_{SB}$ and $V_{DB}$ are the corresponding reverse-bias voltages, and $V_0$ is the built-in potential of the junction.

The capacitances of the equivalent circuit model of the MOS transistor can be derived from Table 4.1 for the three main operating regions of the device.

Table 4.1: Capacitance values of the MOS transistor in different operating regions

| **Capacitance** | **Cut-off** | **Triode Region** | **Saturation** |
|---|---|---|---|
| $C_{gs}$ | $C_{ov}$ | $C_{gc}/2 + C_{ov}$ | $2C_{gc}/3 + C_{ov}$ |
| $C_{gd}$ | $C_{ov}$ | $C_{gc}/2 + C_{ov}$ | $C_{ov}$ |
| $C_{sb}$ | $C_{jsb}$ | $C_{jsb} + C_{cb}/2$ | $C_{jsb} + 2C_{cb}/3$ |
| $C_{db}$ | $C_{jdb}$ | $C_{jdb} + C_{cb}/2$ | $C_{jdb}$ |

# Chapter 5

# Power Amplifiers

## 5.1 Fundamental Principles of Power Amplifiers

The best way to understand the behavior of a power amplifier, and the fastest method for calculating its key electrical characteristics—such as output power, power gain, efficiency and stability—is through spectral domain analysis. Generally, such an analysis is based on determining the output response of the nonlinear active device when a signal, composed of multiple harmonics, is applied at its input port. The output response is expressed as follows:

$$i(t) = f[v(t)] \tag{1}$$

where $i(t)$ is the output current, $v(t)$ is the input voltage, and $f[v]$ is the nonlinear transfer function of the device.

In contrast to spectral analysis, time-domain analysis determines the voltage and current relationships across each circuit element as a function of time. A system of equations is then obtained by applying Kirchhoff's laws to the circuit under analysis. If the circuit includes nonlinear components, the resulting system will consist of nonlinear integro-differential equations. The solution to such a system can be found using numerical integration methods.

In spectral analysis, the input voltage $v(t)$, representing a signal composed of multiple harmonic components, is expressed as:

$$v(t) = V_0 + \sum_{k=1}^{N} V_k \cos(\omega_k t + \phi_k) \tag{2}$$

where $V_0$ is the DC input voltage, $V_k$ is the amplitude of the $k$-th harmonic component, $\phi_k$ is its phase, $\omega_k$ is the angular frequency, and $N$ is the number of harmonics in the input signal.

Frequency-domain analysis, based on substituting equation (2) into equation (1), determines the output signal spectrum as the sum of the fundamental harmonic and higher-order harmonics. This process is quite complex; however, when only an estimation of the power amplifier's behavior is required, an analytical solution can be obtained by replacing the nonlinearity with a piecewise linear approximation.

The piecewise linear approximation of the current–voltage transfer characteristic of the active device results from replacing the actual nonlinear function $i = f(v_{\text{in}})$ with an

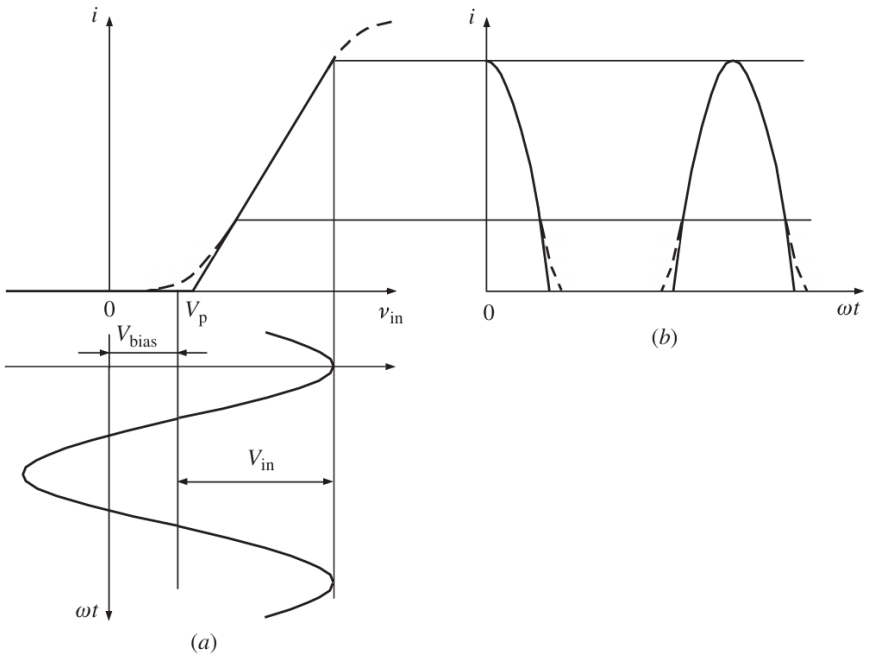



Figure 5.1: Piecewise linear approximation technique [3]

approximation composed of tangent straight-line segments at specific points along the real characteristic curve.

Such a piecewise linear approximation, using two straight-line segments, is shown in Figure 5.1(a). The output current waveforms corresponding to the actual transfer characteristic (dashed curve) and its partial linear approximation using two linear segments (solid curve) are illustrated in Figure 3.1(b).

Under large-signal operation, the waveforms corresponding to the actual nonlinear transfer characteristic and its piecewise linear approximation are practically identical over most of the signal period, with negligible deviation for small output current values—near the cutoff region of device operation—and significant deviation near the saturation region. However, the latter case leads to considerable nonlinear distortion and is only used in high-efficiency operation, when the active conduction time of the device is minimized.

Therefore, at least the first two components of the output current—the DC and fundamental—can be accurately estimated using a Fourier series expansion. Consequently, such a two-segment linear approximation can be effective for quickly estimating the output power and efficiency of a linear power amplifier.

The piecewise linear transfer characteristic of the device shown above can be mathematically described as follows:

$$i(t) = \begin{cases} 0, & v_{\text{in}} \leq V_p \\ g_m(v_{\text{in}} - V_p), & v_{\text{in}} > V_p \end{cases} \tag{3}$$

where $g_m$ is the transconductance of the device and $V_p$ is the threshold voltage.

Assuming the input signal is sinusoidal, we have:

$$v_{\text{in}}(t) = V_{\text{bias}} + V_{\text{in}} \cos(\omega t) \tag{4}$$

where $V_{\text{bias}}$ is the DC bias voltage of the device.

At the point where the input voltage $v_{\text{in}}(t)$ becomes equal to the cutoff voltage $V_p$ of the transistor—defined to occur at time $\omega t = \theta$—the output current drops to zero because the active device enters cutoff. Therefore:

$$V_p = V_{\text{bias}} + V_{\text{in}} \cos\theta, \quad \text{with } i(\theta) = 0 \tag{5}$$

Hence, the conduction angle $\theta$ can be calculated as:

$$\cos\theta = \frac{V_{\text{p}} - V_{bias}}{V_{\text{in}}} \quad \Rightarrow \quad \theta = \cos^{-1}\left(\frac{V_{\text{p}} - V_{bias}}{V_{\text{in}}}\right) \tag{6}$$

or equivalently:

$$\theta = \pi - \cos^{-1}\left(\frac{V_{\text{bias}} - V_p}{V_{\text{in}}}\right) \tag{7}$$

The output current is a periodic waveform of amplitude $I_{\max}$ and range $2\theta$, as illustrated in Figure 3.1. It is analytically expressed as:

$$i(\omega t) = \begin{cases} I_q + I\cos(\omega t), & -\theta \le \omega t \le \theta \\ 0, & \theta \le \omega t < 2\pi - \theta \end{cases} \tag{8}$$

When the output current becomes zero, we have:

$$i = I_q + I\cos\theta = 0 \tag{9}$$

Assuming $I = g_m V_{\text{in}}$, due to the piecewise linear approximation, equation (8) for $i > 0$ becomes:

$$i(\omega t) = g_m V_{\text{in}} \left(\cos(\omega t) - \cos\theta\right) \tag{10}$$

At $\omega t = 0$, the output current reaches its maximum value:

$$I_{\max} = I(1 - \cos\theta) \tag{11}$$

Expanding the output current $i(\omega t)$ into a Fourier series gives:

$$i(\omega t) = I_0 + I_1\cos(\omega t) + I_2\cos(2\omega t) + \cdots + I_n\cos(n\omega t) \tag{12}$$

The Fourier coefficients are calculated as follows:

$$I_0 = \frac{1}{2\pi}\int_{-\theta}^{\theta} g_m V_{\text{in}} \left(\cos(\omega t) - \cos\theta\right) d(\omega t) = I\gamma_0(\theta) \tag{13}$$

$$I_1 = \frac{1}{\pi}\int_{-\theta}^{\theta} g_m V_{\text{in}} \left(\cos(\omega t) - \cos\theta\right)\cos(\omega t) d(\omega t) = I\gamma_1(\theta) \tag{14}$$

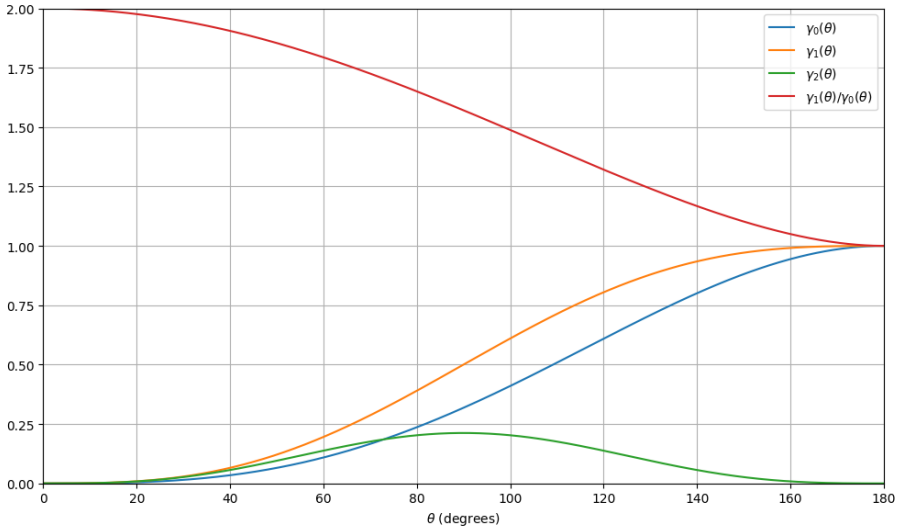
$$I_n = \frac{1}{\pi}\int_{-\theta}^{\theta} g_m V_{\text{in}} \left(\cos(\omega t) - \cos\theta\right)\cos(n\omega t) d(\omega t) = I\gamma_n(\theta) \tag{15}$$

where $\gamma_n(\theta)$ are the current coefficients. After solving the integrals, we obtain:

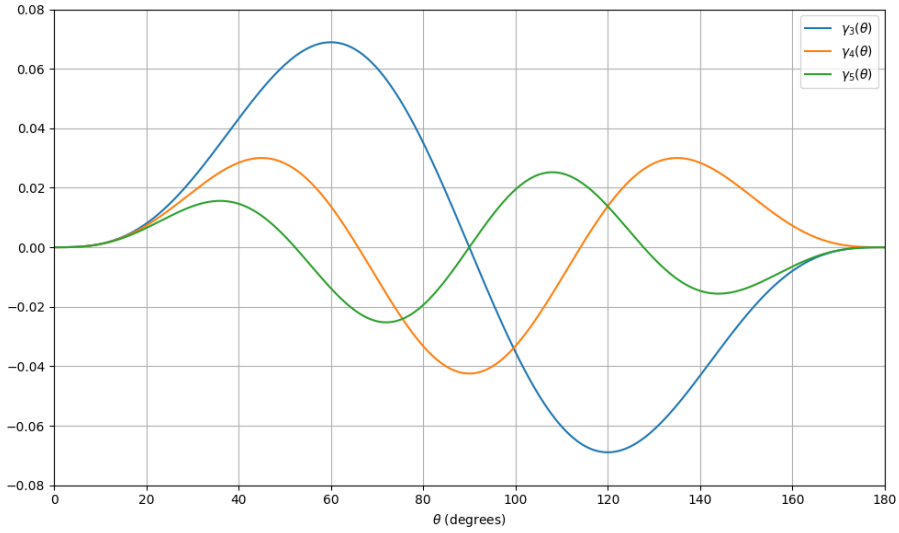
$$\gamma_0(\theta) = \frac{1}{\pi}\left(\sin\theta - \theta\cos\theta\right) \tag{16}$$

$$\gamma_1(\theta) = \frac{1}{\pi}\left(\theta - \frac{\sin(2\theta)}{2}\right) \tag{17}$$

$$\gamma_n(\theta) = \frac{1}{\pi}\left[\frac{\sin((n-1)\theta)}{n(n-1)} - \frac{\sin((n+1)\theta)}{n(n+1)}\right], \quad n = 2, 3, \ldots \tag{18}$$




(a)




(b)

Figure 5.2: Plots of the current coefficients $\gamma_n(\theta)$ for the DC, the fundamental, and higher-order harmonic components

The influence of the factor $\gamma_n(\theta)$ on the amplitudes of the output current harmonics is shown in Figure 5.2. As observed, the maximum value of the factor $\gamma_n(\theta)$ is achieved when $\theta = \frac{180^\circ}{n}$. It is worth noting that when $\theta = 90^\circ$, the odd harmonics in the Fourier

analysis become zero (i.e., $\gamma_3(\theta) = \gamma_5(\theta) = \cdots = 0$). Additionally, the ratio $\gamma_1(\theta)/\gamma_0(\theta)$ ranges from 1 to 2, reaching its minimum at $\theta = 180°$ and its maximum at $\theta = 0°$.

It is important to note that the current coefficient of the third harmonic $\gamma_3(\theta)$ becomes negative for angles $90° < \theta < 180°$.

In conclusion, if the harmonic components for which $\gamma_n(\theta) > 0$ reach their maximum positive values at the instants corresponding to the average values of the current waveform, the harmonic components for which $\gamma_n(\theta) < 0$ can reach maximum negative values. As a result, a combination of different harmonic components with suitable weighting coefficients can create a more square-shaped current and voltage waveform, thereby improving the amplifier's efficiency.

The amplitude of the corresponding current harmonic is given by:

$$a_n = \frac{I_n}{I_{\max}} \tag{19}$$

In some cases, it is necessary for an active device to maintain a constant value of $I_{\max}$ for each value of $\theta$, which requires an appropriate adjustment of the input voltage amplitude $V_{\text{in}}$. In such cases, it is more practical to use the coefficients $a_n$. The following holds:

$$I_n = \gamma_n I = \gamma_n g_m V_{\text{in}} = \gamma_n I \tag{20}$$

From equations (11), (19) and (20), we derive:

$$a_n = \frac{\gamma_n(\theta)}{1 - \cos\theta} \tag{21}$$

The coefficient $a_n$ reaches its maximum when $\theta = \frac{120°}{n}$, as shown in Figure 5.3.

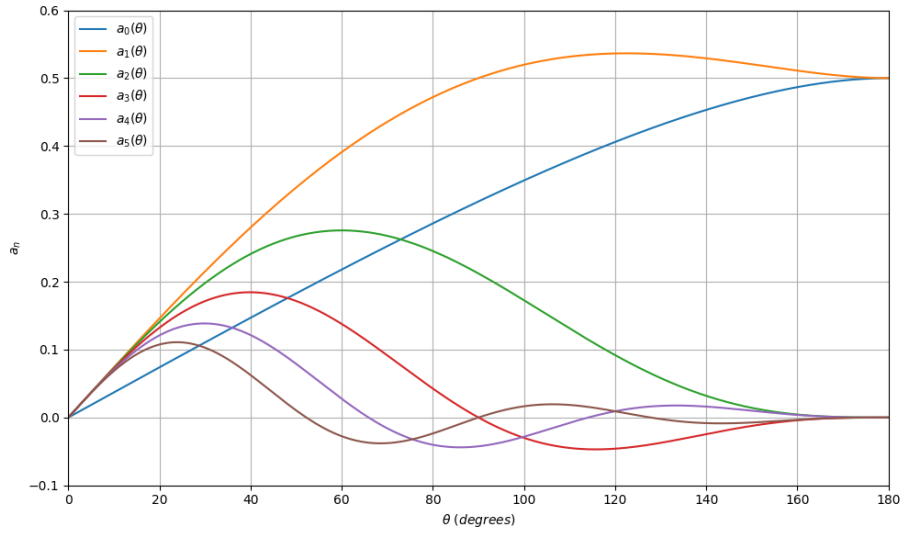



Figure 5.3: Plots of the harmonic amplitude coefficients $a_n(\theta)$ for the DC, the fundamental, and higher-order harmonic components

## 5.2 Basic Classes of Operation: A, AB, B, and C

Power amplifiers can be classified into three categories according to their mode of operation:

- Linear operation: When the active device operates only within the linear region of its transfer characteristic curve.
- Critical operation: When the current flow ceases, but the operation extends beyond the linear region into the cutoff and saturation regions.
- Non-linear operation: When the current flow stops during a portion of each cycle, depending on the device's biasing conditions.

When high efficiency is required, power amplifiers of the third category are used, as the presence of harmonics boosts efficiency. To suppress voltage harmonics at the load and obtain a pure sinusoidal signal, a parallel high-$Q$ resonating circuit is employed. Class A power amplifiers fall into the first category (linear operation), while Class B amplifiers are representative of the third category (non-linear operation).

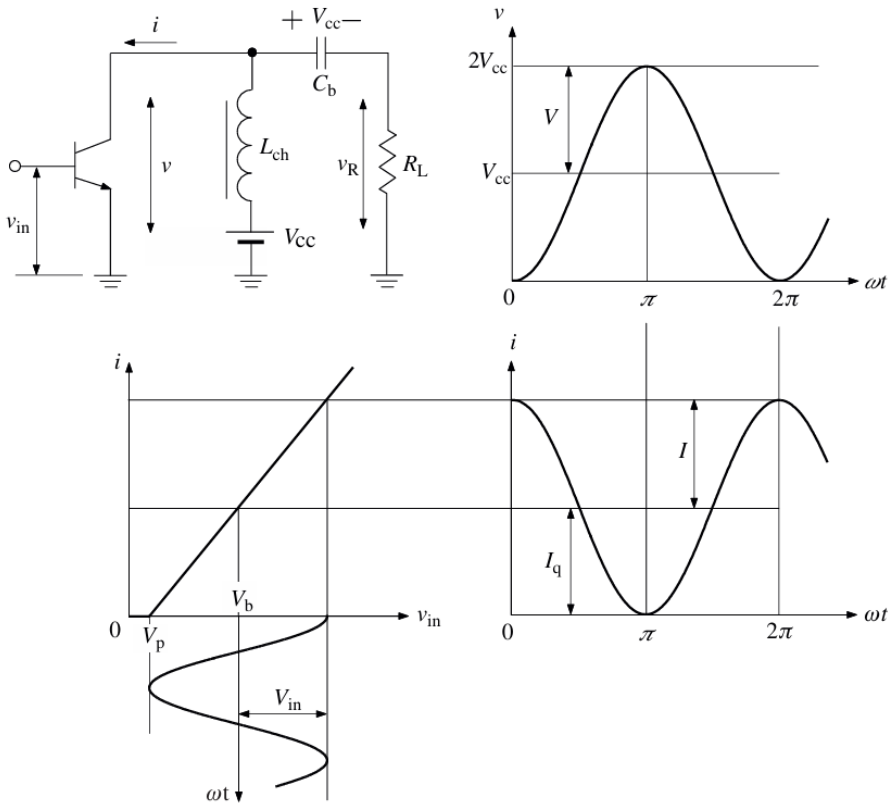



Figure 5.4: Voltage and current waveforms in Class A operation [3]

In order to analyze the operating classes of a power amplifier, we consider a simple stage shown in Figure 5.4, where $L_{ch}$ is an ideal RF choke, theoretically having a very large inductance and therefore a very large (ideally infinite) inductive reactance $\omega L_{ch}$ at the operating frequency. The component $C_b$ is an ideal capacitor that blocks DC current and has very large (ideally infinite) capacitance, thus a negligible (ideally zero) capacitive reactance $1/(\omega C_b)$ at the operating frequency. $R_L$ is the load resistance, also assumed to be ideal.

The DC supply voltage $V_{CC}$ is applied across both plates of the blocking capacitor and remains constant throughout the signal cycle. The active device behaves as an ideal current source controlled by voltage or current.

Given a sinusoidal voltage input waveform, as defined by Equation (4), the operating point of the amplifier is set exactly at the middle of the linear region of the transistor's transfer characteristic, with $V_{\text{in}} \leq V_{\text{bias}} - V_p$, where $V_p$ is the cutoff voltage of the device. By using the piecewise linear approximation of the transfer function, the output current is also sinusoidal and can be expressed as:

$$i = I_q + I\cos(\omega t) \tag{22}$$

where the quiescent current satisfies $I_q \geq I$.

The output voltage $v$, measured between the collector and ground, represents the sum of the DC supply voltage $V_{\text{cc}}$ and the sinusoidal voltage $v_R$ across the load resistance $R_L$. Therefore, the higher the output current $i$, the larger the voltage drop $v_R$ across the load resistor, and consequently, the lower the output voltage $v$. Thus, for a purely resistive load $Z_L = R_L$, the collector voltage $v$ is phase-shifted by 180° relative to the input voltage $v_{\text{in}}$, and can be written as:

$$v = V_{\text{cc}} + V\cos(\omega t + 180^\circ) = V_{\text{cc}} - V\cos(\omega t) \tag{23}$$

where $V$ is the amplitude of the output voltage.

Substituting Equation (22) into Equation (23), we arrive at the following expression for the voltage $v$:

$$v = V_{\text{cc}} - (1 - I_q)R_L \tag{24}$$

where $R_L = \frac{V}{I}$

Equation (24) can be transformed into:

$$v = \left(I_q + \frac{V_{\text{cc}}}{R_L}\right) - \frac{v}{R_L} \tag{25}$$

The above relation highlights the linear dependence between the collector current and the collector voltage. Such a combination of sinusoidal voltage and current at the collector is known as Class-A operation.

The efficiency at the collector node is:

$$\eta = \frac{P}{P_0} \tag{26}$$

where $P$ is the output DC power and $P_0 = I_q V_{\text{cc}}$ is the total supplied power. The power delivered to the load resistance $R_L$ at the fundamental frequency $f_0$ is given by:

$$P = \frac{1}{2}IV \tag{27}$$

Therefore, collector efficiency becomes:

$$\eta = \frac{IV}{2I_q V_{\text{cc}}} \tag{28}$$

We define the collector voltage peak factor as:

$$\xi = \frac{V}{V_{\text{cc}}} \tag{29}$$

Under ideal conditions, assuming zero saturation voltage, $\xi = 1$, and maximum output current amplitude $I = I_q$, Equation (28) yields a maximum collector efficiency for Class-A operation of:

$$\eta = 50\% \tag{30}$$

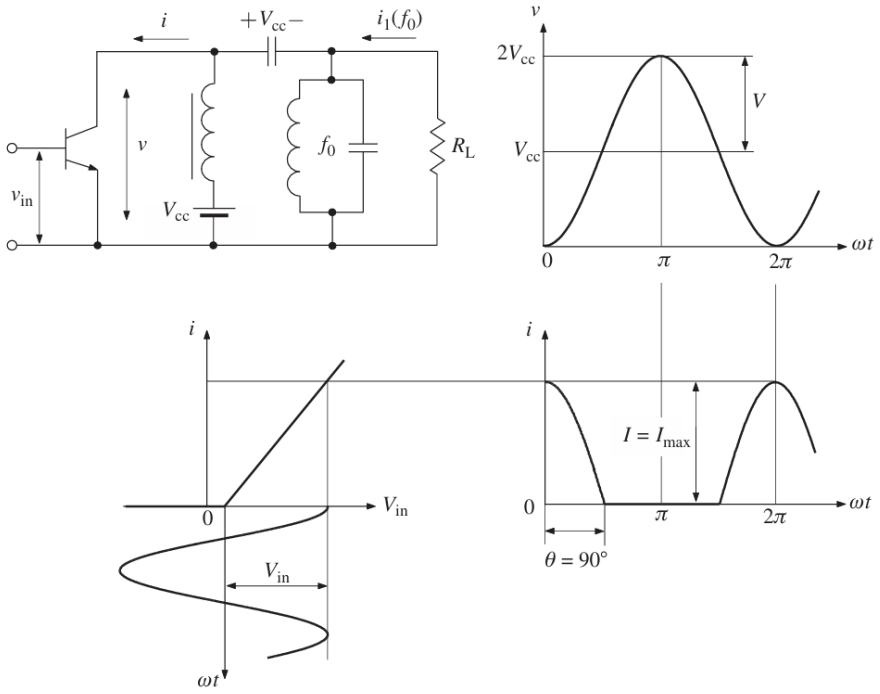



Figure 5.5: Voltage and current waveforms in Class B operation [3]

However, as also seen from Equation (28), increasing the ratio $I/I_q$ can further improve the collector efficiency. This leads progressively to a nonlinear transformation of the sinusoidal current waveform at the collector into a pulsed waveform, where the collector current becomes non-zero for only part of the signal period. In this case, the transistor operates in the active region following cutoff, where the collector current is zero, as illustrated in Figure 5.5.

As a result, the output frequency spectrum contains second, third, and higher-order harmonics. However, due to the high-quality factor $Q$ of the parallel LC resonant circuit, only the fundamental frequency flows through the load, while higher-order components are ideally short-circuited. Thus, the collector voltage can be represented as a purely sinusoidal waveform with an amplitude $V \leq V_{\text{cc}}$.

Equation (22) for the output current can be rewritten using the ratio of quiescent current $I_q$ and current amplitude $I$ as:

$$\cos\theta = -\frac{I_q}{I} \tag{31}$$

As a result, the fundamental classification of nonlinear power amplifier operation can be expressed in terms of the conduction angle $\theta$:

- When $\theta > 90°$, then $\cos\theta < 0$ and $I_q > 0$: the amplifier operates in Class-AB.
- When $\theta = 90°$, then $\cos\theta = 0$ and $I_q = 0$: the amplifier operates in Class-B.
- When $\theta < 90°$, then $\cos\theta > 0$ and $I_q < 0$: the amplifier operates in Class-C.

From Eq. 13, it follows that the DC component of the current is a function of $\theta$ for $\theta < 180°$, unlike Class-A operation where $\theta = 180°$ and the DC component is equal to the quiescent current throughout the period.

The collector efficiency of a power amplifier with a parallel resonant circuit, biased in the nonlinear region, is given by:

$$\eta = \frac{P_1}{P_0} = \frac{1}{2} \cdot \frac{I_1}{I_0} \cdot \xi = \frac{1}{2} \cdot \frac{\gamma_1}{\gamma_0} \cdot \xi \tag{32}$$

This expression depends on $\theta$ only:

$$\frac{\gamma_1}{\gamma_0} = \frac{\theta - \sin\theta\cos\theta}{\sin\theta - \theta\cos\theta} \tag{33}$$

For Class-B operation, where $\xi = 1$ and $\theta = 90°$, the maximum theoretical efficiency is:

$$\eta = \frac{\pi}{4} \approx 78.5\% \tag{34}$$

The efficiency as a function of the conduction half-angle $\theta$ is shown in Figure 5.6.

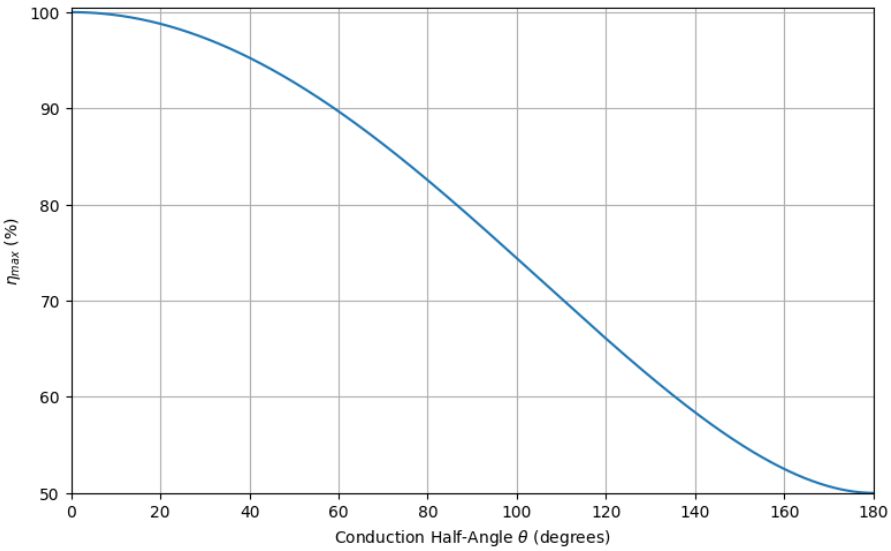



Figure 5.6: Maximum theoretical efficiency as a function of the conduction half-angle $\theta$

The power delivered to the load $P_L = P_1$, at the fundamental frequency, is defined as:

$$P_1 = \frac{VI_1}{2} = \frac{VI\gamma_1(\theta)}{2} \tag{35}$$

This shows direct dependence on the conduction angle $2\theta$. Thus, reducing the conduction angle lowers the value of $\gamma_1$, and in order to increase the power delivered to the load at the fundamental frequency, the current amplitude $I$ must be increased. Since the current amplitude depends on the input voltage amplitude $V_{\text{in}}$, the input power $P_{\text{in}}$ must also increase.

The collector efficiency increases as the conduction angle $\theta$ decreases and reaches its maximum when $\theta = 0°$, where the ratio $\gamma_1/\gamma_0$ is maximized. For instance, the efficiency rises from 78.5% to 92% when $\theta$ decreases from 90° to 60°. However, this necessitates a 2.5x increase in $V_{\text{in}}$ in order to maintain constant power to the load, which reduces overall efficiency when considering Power Added Efficiency (PAE):

$$\text{PAE} = \frac{P_1 - P_{\text{in}}}{P_0} = \frac{P_1}{P_0}\left(1 - \frac{1}{G_p}\right) \tag{36}$$

where $G_p = \frac{P_1}{P_{\text{in}}}$ is the power gain.

By combining equations (11), (14) and (35), the output power becomes:

$$P_1 = \frac{VI_1}{2} = \frac{VI_{\max}(\theta - \sin\theta\cos\theta)}{2\pi(1 - \cos\theta)} \tag{37}$$

The output power normalized to the output power delivered to the load in Class A operation is given by:

$$P_{\text{norm}} = \frac{2(\theta - \sin\theta\cos\theta)}{\pi(1 - \cos\theta)} \tag{38}$$

The variation of $P_{\text{norm}}$ as a function of the conduction half-angle $\theta$ is illustrated in Figure 5.7.

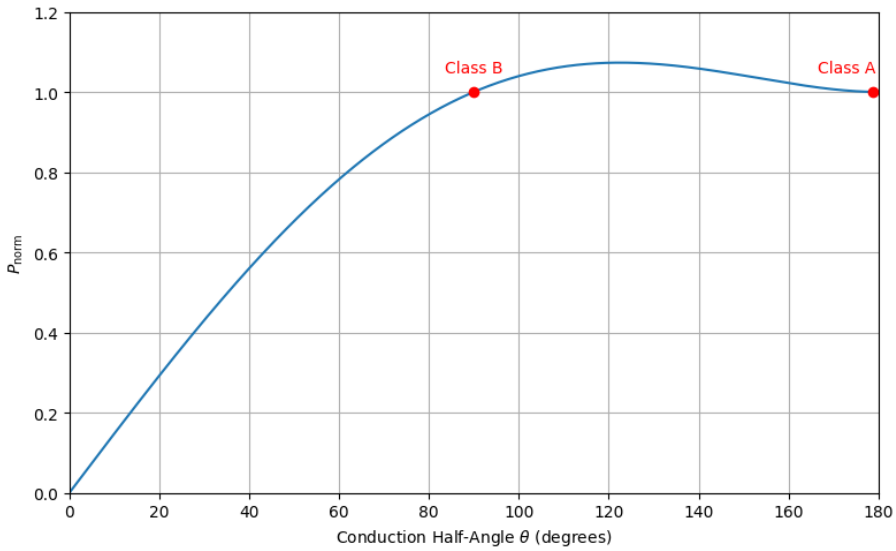



Figure 5.7: Normalized output power $P_{\text{norm}}$ as a function of the conduction half-angle $\theta$.

We observe that the normalized output power $P_{\text{norm}}$ equals 1 in Class B, while it exceeds 1 in Class AB and reaches a maximum at $\theta = 122.5°$. Clearly, in Class C it is lower than 1 and continues to decrease as the conduction angle decreases.

The main distinction between Class-B and Class-C lies in the duration of the output current pulses, which are shorter in Class-C operation, where the active device is biased below cutoff. It should be noted that for the active device's transfer characteristic — ideally modeled as square-law — the current coefficients $\gamma_n(\theta)$ of even harmonics are non-zero in this case, although the difference from a linear approximation is not significant. To achieve maximum efficiency in Class-C amplifiers, the active device must be biased well below the pinch-off point to yield sufficiently low conduction angles.

To balance high power gain and high PAE, the conduction angle should be chosen in the range $120° \leq 2\theta \leq 190°$. If high collector efficiency is required from a high-gain active device, operation in Class-C mode with $\theta \approx 60°$ is optimal. However, when input power

is limited and gain is inadequate, Class-AB operation with small quiescent current (i.e., $\theta$ slightly greater than 90°) is recommended.

## 5.3 Load Line and Output Impedance

When the power amplifier operates in Class A and there is no parallel resonant circuit at the load, then, given the input voltage, determining the collector voltage and current requires solving the following nonlinear system:

$$\begin{cases} i = f(u_{in}, u_c) \\ i = \left(I_q + \dfrac{V_{CC}}{R_L}\right) - \dfrac{u_c}{R_L} \end{cases} \tag{39}$$

The second equation is known as the load line. In other classes of operation, where only the fundamental harmonic survives at the load due to the parallel resonant circuit, and the current is non-zero only during a portion of the period, the load line is modified. From equations (8), (14), and (23), it follows that for $-\theta \leq \omega t \leq \theta$, the load line is expressed as:

$$i = \left(I_q + \frac{V_{CC}}{\gamma_1 R_L}\right) - \frac{u_c}{\gamma_1 R_L} \tag{40}$$

Figure 5.8 shows the I-V characteristics of an ideal transistor along with the load lines corresponding to different classes of operation.

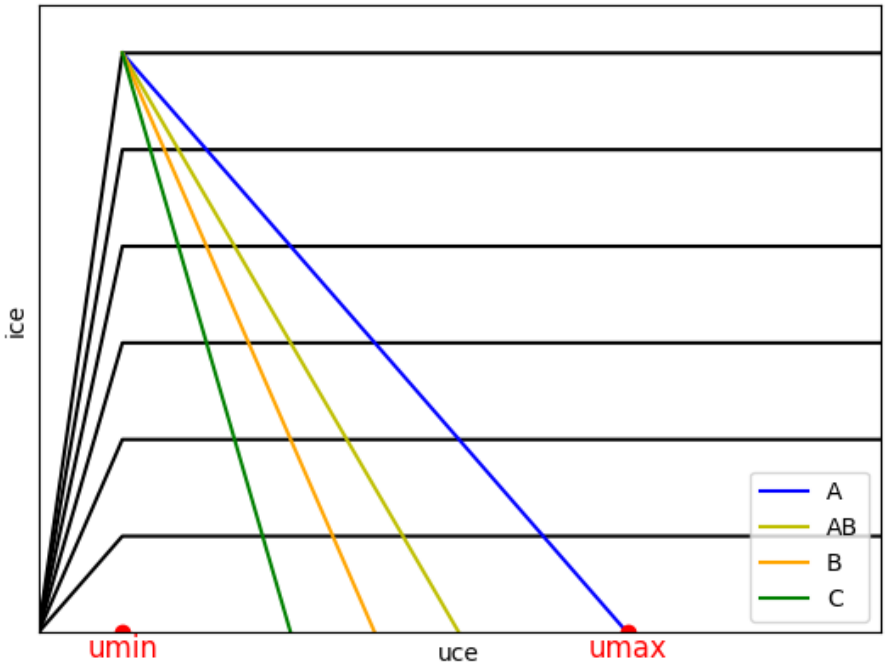



Figure 5.8: IV curves with corresponding load lines for different amplifier classes

To maximize the output power, the load resistance must be set to an optimal value. In Class A, this value can be easily determined from the slope of the load line. For other classes of operation, the optimal load resistance is given by:

$$R_{L,\text{opt}} = \frac{V}{\gamma_1(\theta) I} \tag{41}$$

This relation also applies to Class A.

When the actual load resistance is not optimal, a matching network is required to transform it into the optimal value. However, this matching network introduces losses. The higher the transformation ratio between the optimal and actual load resistance, the greater the losses. Therefore, power amplifiers are typically designed so that the optimal load resistance is as close as possible to the actual load resistance.

The relationships previously provided for estimating the optimal load resistance serve as a first-order approximation. In practice, designers employ load-pull simulations using dedicated software tools to accurately determine the optimal load resistance. Load-pull simulations not only reveal the resistance value that maximizes the output power, but also the one that maximizes the Power-Added Efficiency (PAE). These two objectives, however, cannot generally be achieved simultaneously. It is emphasized that the optimal load resistance values for all power amplifiers presented in the following sections were determined through load-pull simulations and the central frequency of the system is 7.76 GHz.

## 5.4 Design of Basic PA Classes in 22nm CMOS FD-SOI

In this section, a power amplifier was implemented using the 22nm CMOS FD-SOI technology. The amplifier consists of a single transistor in a common-source (CS) topology, as shown in Figure 5.9.

The inductor $L_{\text{ch}}$ is modeled as an ideal RF choke, theoretically exhibiting a very large inductance and, therefore, a very high (ideally infinite) inductive reactance $\omega L_{\text{ch}}$ at the operating frequency. The capacitor $C_b$ is also considered ideal, effectively blocking DC current while presenting a very large (ideally infinite) capacitance, resulting in negligible (ideally zero) capacitive reactance $1/(\omega C_b)$ at the operating frequency. $R_L$ denotes the load resistance.

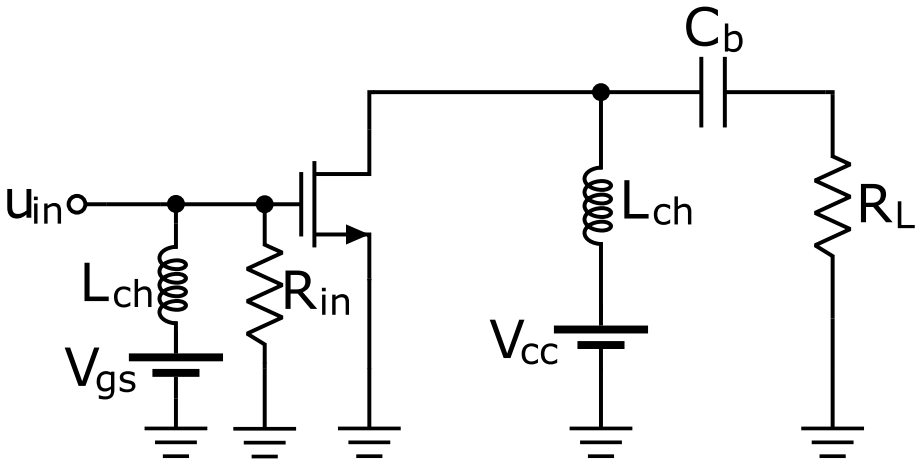



Figure 5.9: Common-source power amplifier

By appropriately adjusting the gate bias voltage and setting the load resistance to the optimal value obtained through load-pull simulations for maximum output power, the

amplifier was configured to operate in all four fundamental classes, enabling a comparative performance analysis. Additionally, an input resistor $R_{\text{in}}$ was included to ensure unconditional stability. Finally, the transistor width was chosen to be 400 µm, and the supply voltage was set to 0.8 V, corresponding to the nominal drain-source voltage at DC.

### 5.4.1 Class A

To correctly bias the transistor, the I–V curves along with the load line were used. The slope of the load line provided an initial estimate of the optimal load resistance, which was later refined through load-pull simulations, as previously discussed. The results are presented in Figure 5.10 and summarized in Table 5.1.

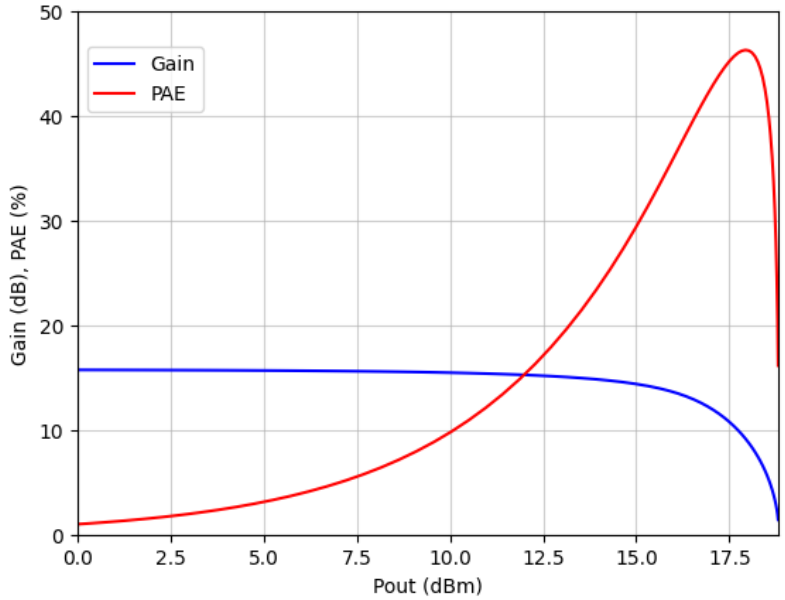



Figure 5.10: Gain and PAE versus output power for Class A operation

Table 5.1: Performance Summary for Class A Power Amplifier

| **Parameter** | **Value** |
|---|---|
| Supply Voltage ($V_{DD}$) | 0.8 V |
| Gain | 15.76 dB |
| Saturated Output Power ($P_{\text{sat}}$) | 18.8 dBm |
| 1 dB Compression Point ($OP_{1\,\text{dB}}$) | 14.22 dBm |
| PAE at 1 dB Compression ($PAE_{1\,\text{dB}}$) | 24.92% |
| Maximum PAE ($PAE_{\text{max}}$) | 46.31% |

From Figure 5.11 it is evident that the transistor conducts continuously, and its drain current is a pure sine wave, as is the drain-source voltage.

### 5.4.2 Class AB

To operate the power amplifier in Class AB, the gate was biased at a voltage halfway between the Class A bias point and the Class B bias point, which is close to the transistor's

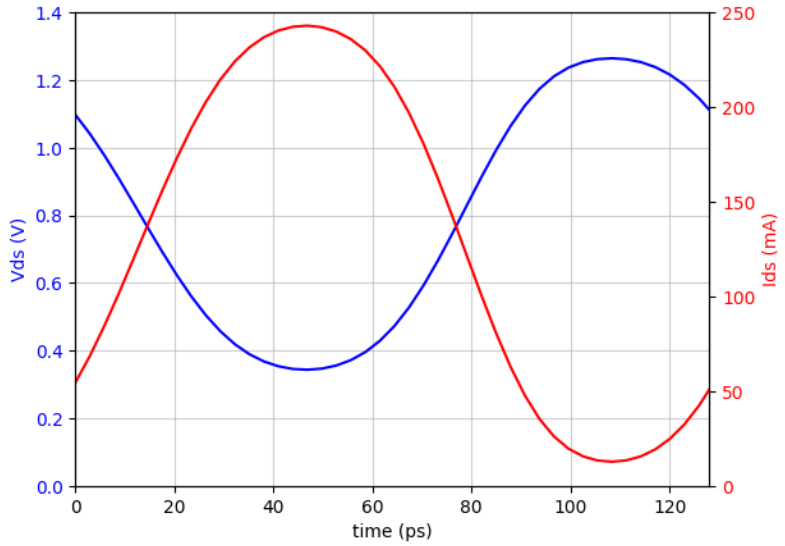



Figure 5.11: Voltage and current waveforms at the 1 dB compression point in Class A operation

threshold voltage. The load resistance was set equal to the optimal load-pull impedance. Additionally, a parallel resonant circuit was added at the output to suppress higher-order harmonics, ensuring that only the fundamental frequency reaches the load. The results are presented in Figure 5.12 and summarized in Table 5.2.

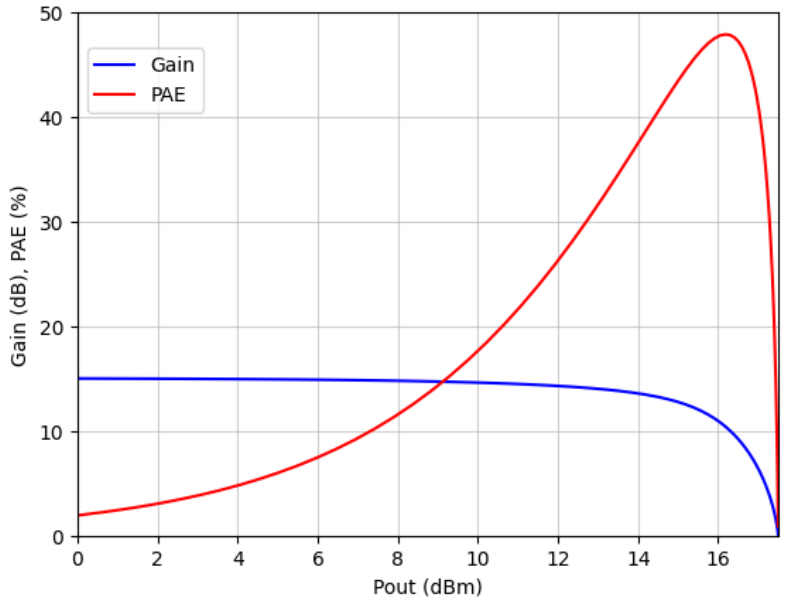



Figure 5.12: Gain and PAE versus output power for Class AB operation

From Figure 5.13, we observe that the drain current waveform is not a pure sinusoid and takes values very close to zero for a duration shorter than half a period. On the other hand, the drain-source voltage is sinusoidal due to the parallel resonant circuit.

Table 5.2: Performance Summary for Class AB Power Amplifier

| Parameter | Value |
|---|---|
| Supply Voltage ($V_{DD}$) | 0.8 V |
| Gain | 15.05 dB |
| Saturated Output Power ($P_{\text{sat}}$) | 17.5 dBm |
| 1 dB Compression Point ($OP_{1\,\text{dB}}$) | 13.02 dBm |
| PAE at 1 dB Compression ($PAE_{1\,\text{dB}}$) | 31.76% |
| Maximum PAE ($PAE_{\text{max}}$) | 47.9% |

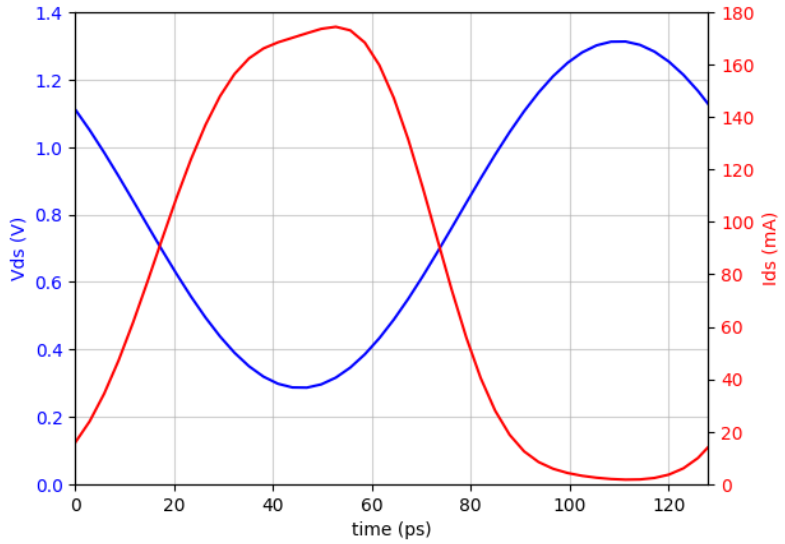



Figure 5.13: Voltage and current waveforms at the 1 dB compression point in Class AB operation

### 5.4.3 Class B

The gate of the power amplifier was biased near the threshold voltage. Similarly to before, the load resistance was set equal to the optimal load-pull impedance. Additionally, again a parallel resonant circuit was added to the load. The results are presented in Figure 5.14 and summarized in Table 5.3.

Table 5.3: Performance Summary for Class B Power Amplifier

| Parameter | Value |
|---|---|
| Supply Voltage ($V_{DD}$) | 0.8 V |
| Gain | 10.12 dB |
| Saturated Output Power ($P_{\text{sat}}$) | 17.52 dBm |
| 1 dB Compression Point ($OP_{1\,\text{dB}}$) | 15.65 dBm |
| PAE at 1 dB Compression ($PAE_{1\,\text{dB}}$) | 50.07% |
| Maximum PAE ($PAE_{\text{max}}$) | 50.19% |

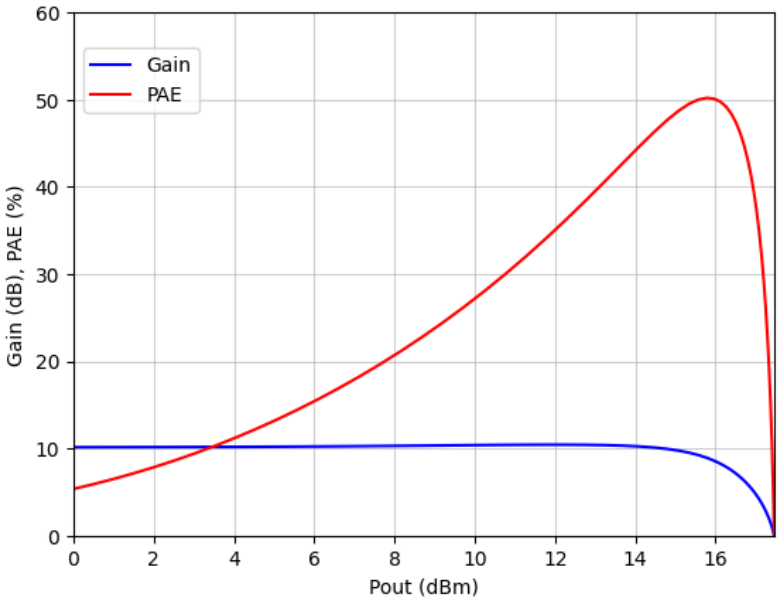



Figure 5.14: Gain and PAE versus output power for Class B operation

By observing Figure 5.15, we see that the current waveform is even more distorted this time. It is evident that the current is zero for a duration approximately equal to half a period. However, the drain-source voltage remains a perfect sinusoid again due to the parallel resonant circuit.

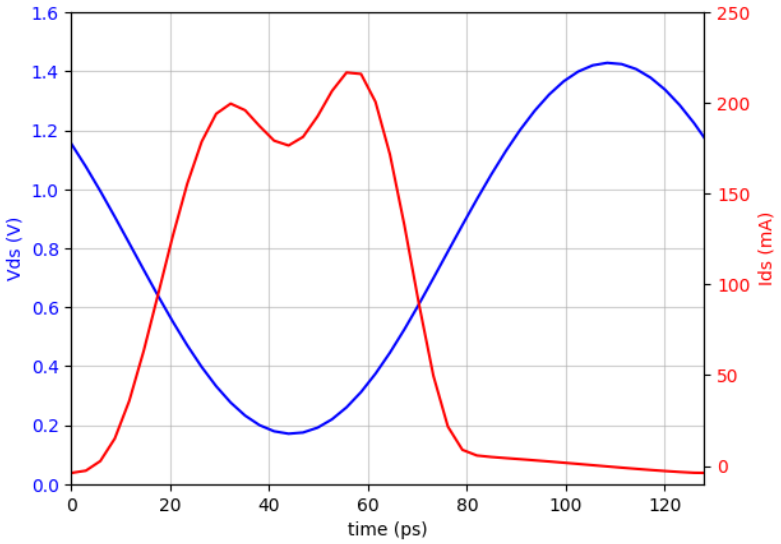



Figure 5.15: Voltage and current waveforms at the 1 dB compression point in Class B operation

### 5.4.4 Class C

This time, the transistor's gate was biased below the threshold voltage. Once again, a parallel resonant circuit was added to the load. The results are presented in Figure 5.16 and summarized in Table 5.4.

Table 5.4: Performance Summary for Class C Power Amplifier

| **Parameter** | **Value** |
|---|---|
| Supply Voltage ($V_{DD}$) | 0.8 V |
| Gain | 3.89 dB |
| Saturated Output Power ($P_{\text{sat}}$) | 16.85 dBm |
| 1 dB Compression Point ($OP_{1\,\text{dB}}$) | 16.44 dBm |
| PAE at 1 dB Compression ($PAE_{1\,\text{dB}}$) | 28.62% |
| Maximum PAE ($PAE_{\text{max}}$) | 52.22% |

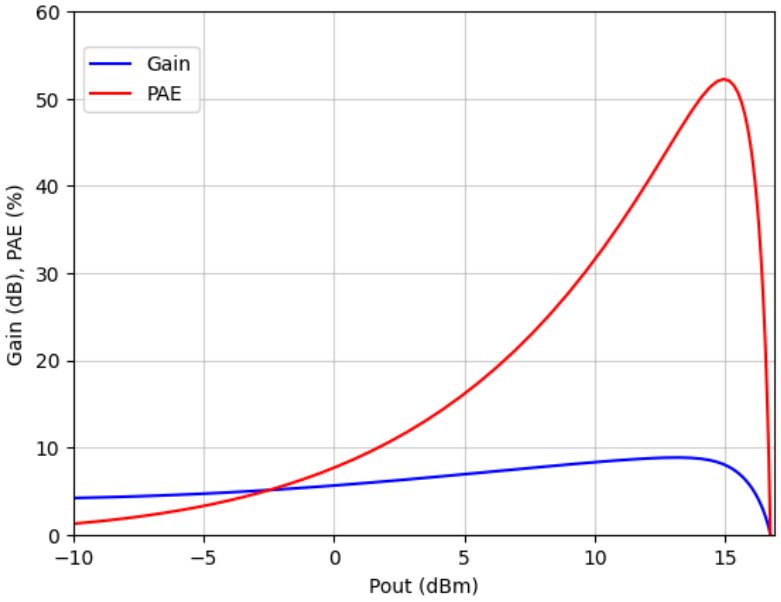



Figure 5.16: Gain and PAE versus output power for Class C operation

From Figure 5.17, it is evident that the current waveform is significantly more distorted, while the drain-source voltage remains a perfect sinusoid, once again due to the parallel resonant circuit.

### 5.4.5 Comparison of the Basic Classes

In Figure 5.18, the performance metrics of the four basic power amplifier classes implemented in 22 nm CMOS FD-SOI technology are compared. The saturated output power decreases progressively from Class A to Class C, as the nonlinearities become increasingly pronounced, leading to stronger compression. At the same time, the gain also decreases. On the other hand, the PAE increases, as expected, with the exception of $PAE_{1\,\text{dB}}$ in Class C, which is lower than that of Class B due to the reduced gain exhibited by the amplifier in this operating class. Finally, the 1 dB compression point is lowest in Class AB, while it is maximized in Classes B and C, with Class C exhibiting a higher value than Class B.

In conclusion, Class B achieves the best trade-off among all performance metrics.

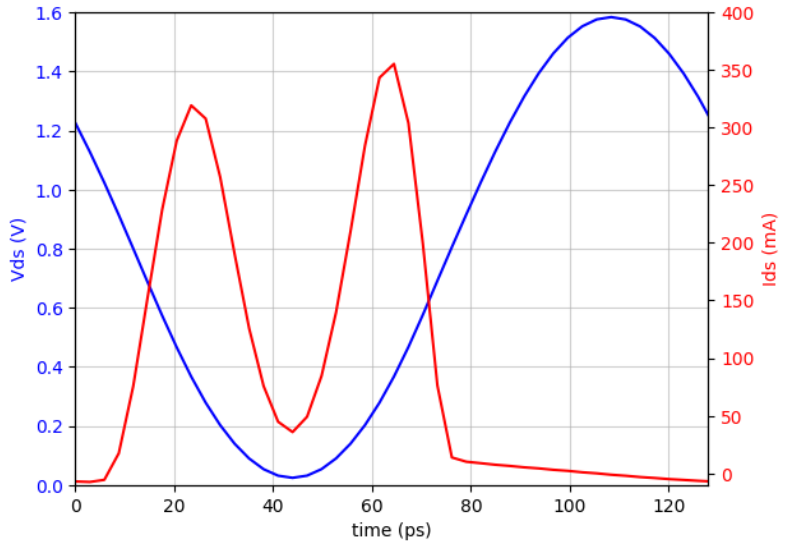



Figure 5.17: Voltage and current waveforms at the 1 dB compression point in Class C operation

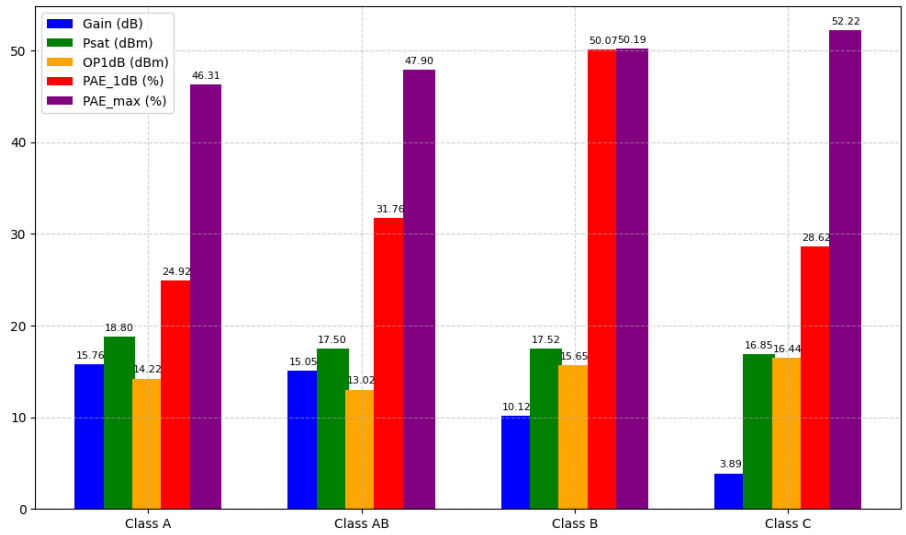



Figure 5.18: Performance Comparison Across Basic Power Amplifier Classes

## 5.5 Differential Power Amplifiers

The saturated output power of the previous Class B amplifier is not sufficiently high. Therefore, techniques that enhance output power must be employed. One such approach is the implementation of a differential amplifier, as shown in Figure 5.19.

Differential amplifiers offer approximately double the output power compared to single-ended amplifiers using transistors of the same size. Moreover, they provide the advantage of incorporating neutralization capacitors ($C_x$), which ensure unconditional stability and allow gain enhancement [7].

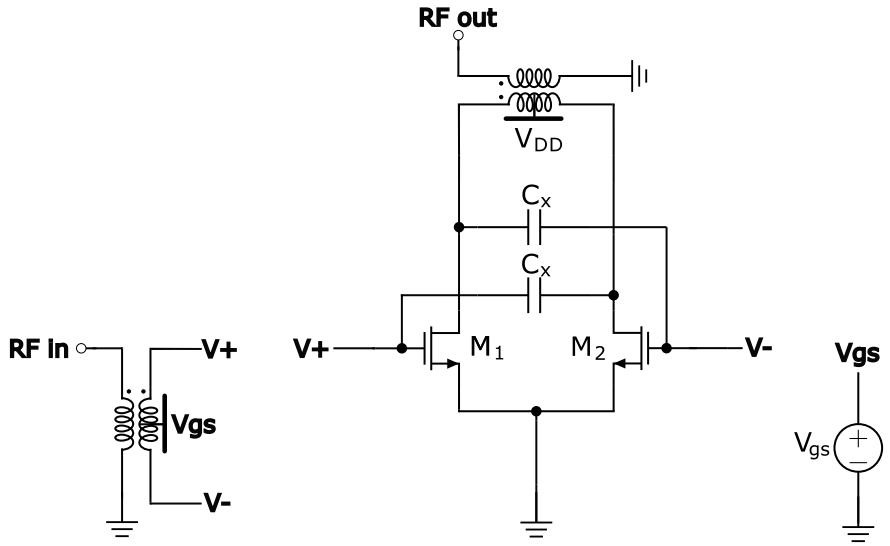



Figure 5.19: Differential common-source power amplifier

### 5.5.1 Neutralization Capacitors

The small-signal equivalent circuit of the differential power amplifier with cross-coupling capacitors $C_x$ is shown in Figure 5.20. The Y-parameters of this two-port network are given by:

$$Y_{11} = \frac{1}{R_G} + j\omega C_{gs} + j\omega(C_{gd} + C_x) \tag{42}$$

$$Y_{12} = -j\omega(C_{gd} - C_x) \tag{43}$$

$$Y_{21} = g_m - j\omega(C_{gd} - C_x) \tag{44}$$

$$Y_{22} = \frac{1}{R_D} + j\omega C_{db} + j\omega(C_{gd} + C_x) \tag{45}$$

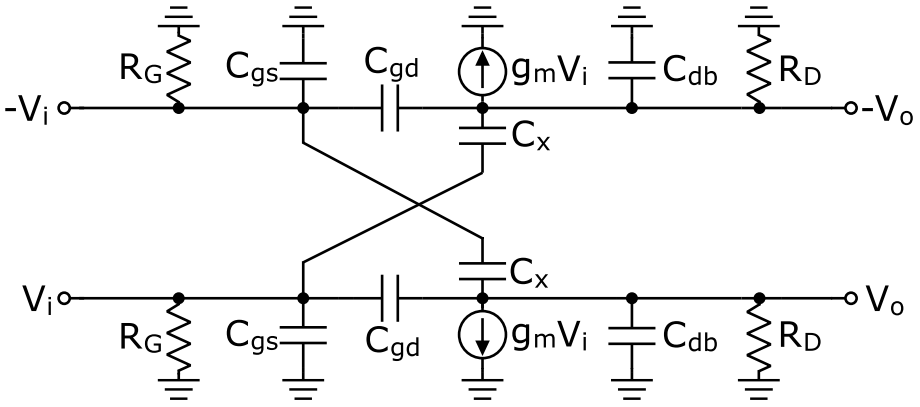



Figure 5.20: Small signal equivalent circuit of capacitive cross-coupled amplifier

The stability factor $k$ can be calculated using the following expression:

$$k = \frac{2\,\mathrm{Re}[Y_{11}]\,\mathrm{Re}[Y_{22}] - \mathrm{Re}[Y_{12}Y_{21}]}{|Y_{12}Y_{21}|} \tag{46}$$

Substituting equations (42)–(45) into the above expression, the stability factor of capacitive cross-coupled amplifiers becomes:

$$k = \frac{2 + \omega^2(C_{gd} - C_x)^2 R_G R_D}{\omega|C_{gd} - C_x| R_G R_D \sqrt{\omega^2(C_{gd} - C_x)^2 + g_m^2}} \tag{47}$$

In addition, the maximum stable gain is given by:

$$G_{MS} = \left|\frac{Y_{21}}{Y_{12}}\right| = \frac{\sqrt{\omega^2(C_{gd} - C_x)^2 + g_m^2}}{\omega|C_{gd} - C_x|} \tag{48}$$

Therefore, when $C_x = C_{gd}$, both the stability factor $k$ and the maximum stable gain $G_{MS}$ are maximized.

### 5.5.2 Differential Power Amplifier in 22nm CMOS FD-SOI

A differential power amplifier was implemented in 22 nm CMOS FD-SOI technology. The circuit is shown in Figure 5.19. Ideal baluns were used at both the input and output. The neutralization capacitors were selected to maximize the $\mu$-factor. Their value is indeed very close to the gate-drain capacitance ($C_{gd}$) of the transistors. In addition, a resistor was inserted between the gates of the two transistors to ensure unconditional stability over a wide frequency range [0, 100 GHz]. The gates of the transistors were biased near the threshold voltage, enabling Class B operation. Finally, the load resistor was set equal to the optimal load-pull impedance. The results are presented in Figure 5.21 and summarized in Table 5.5. It is evident that the output power has increased by approximately 3 dB, as expected. Furthermore, improvements in both gain and Power Added Efficiency (PAE) are observed, demonstrating the enhanced performance of the differential architecture.

Table 5.5: Performance Comparison Between Single-Ended and Differential Class B Power Amplifiers

| **Parameter** | **Single-Ended** | **Differential** |
|---|---|---|
| Supply Voltage ($V_{DD}$) | 0.8 V | 0.8 V |
| Gain | 10.12 dB | 13.22 dB |
| Saturated Output Power ($P_{\mathrm{sat}}$) | 17.52 dBm | 20.55 dBm |
| 1 dB Compression Point ($OP_{1\,\mathrm{dB}}$) | 15.65 dBm | 18.83 dBm |
| PAE at 1 dB Compression ($PAE_{1\,\mathrm{dB}}$) | 50.07% | 59.12% |
| Maximum PAE ($PAE_{\mathrm{max}}$) | 50.19% | 61.46% |

## 5.6 Stacked Power Amplifiers

The nominal drain-source voltage in modern technologies is low. Therefore, the supply voltage must also be low. Consequently, the transistor current must be increased to

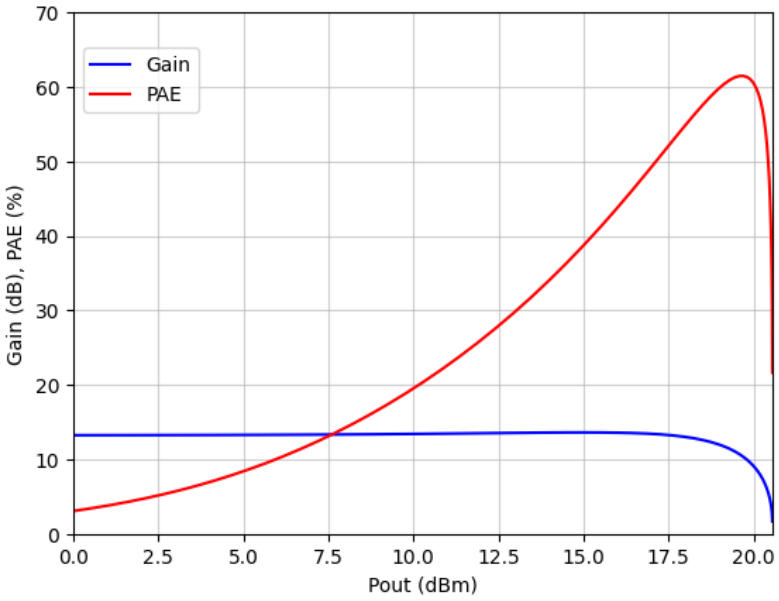



Figure 5.21: Gain and PAE versus output power for the Differential Power Amplifier in Class B operation

achieve sufficient output power. However, the increased current lowers the optimal load-pull impedance, requiring matching networks with a large transformation ratio, which introduce significant losses [8].

One effective method to increase the output power and mitigate these issues is to use stacked transistors. Stacking transistors allows for a higher supply voltage. However, the design becomes more complex and must be carefully implemented to avoid reliability problems [9].

In the following, the mathematical analysis of stacked power amplifiers is presented.

### 5.6.1 Stacking Transistors

In Figure 5.22, a differential three-stacked power amplifier is presented. The RC networks at the gates of the upper transistors allow these gates to swing at AC, thereby keeping the gate-drain voltage ($V_{gd}$) below the breakdown voltage. These networks are also essential for establishing an equal distribution of the drain-source voltages, as will be explained later.

To equally distribute the drain-source voltages across the stack and optimize performance, each transistor's drain must see the appropriate optimal impedance. The voltage swing of the $k$-th transistor must be $k$ times higher than that of the lowest transistor, while all transistors carry approximately the same drain current. Therefore, the optimal impedance for the $k$-th transistor is given by:

$$Z_{d,k} = k \cdot R_{\text{opt}} \tag{49}$$

where $R_{\text{opt}}$ is the optimal load impedance for the lowest transistor.

Neglecting $r_{ds}$ and assuming the resistor $R_{f,k}$ is sufficiently large, the small-signal equivalent circuit of the $k$-th transistor is shown in Figure 5.23. A test voltage source $v_x$ is applied at the source node of the transistor in order to calculate the impedance seen from the drain of the $(k-1)$-th transistor, defined as:

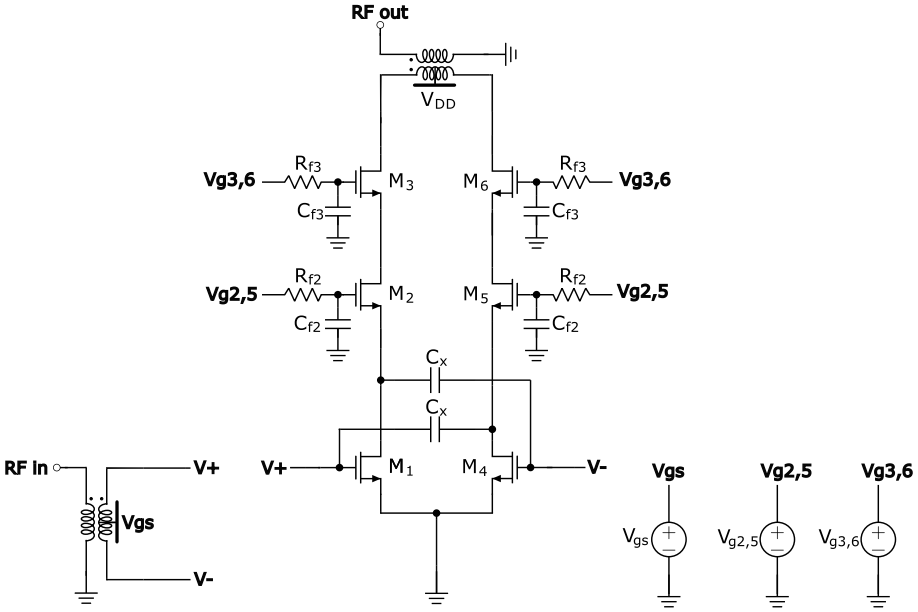



Figure 5.22: Three-stacked power amplifier

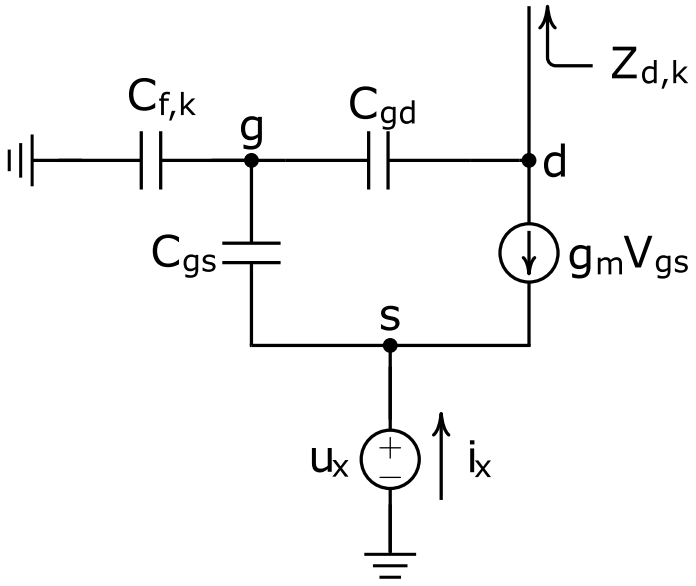



Figure 5.23: Small-signal equivalent circuit of the $k$-th transistor

$$Z_{d,k-1} = \frac{v_x}{i_x} \tag{50}$$

Applying node voltage method to the small-signal model yields the following linear system of equations:

$$\begin{bmatrix} sC_{gs,k} + g_{m,k} & -sC_{gs,k} - g_{m,k} & 0 \\ -C_{gs,k} & C_{f,k} + C_{gd,k} + C_{gs,k} & -C_{gd,k} \\ -g_{m,k} & g_{m,k} - sC_{gd,k} & \dfrac{1}{Z_{d,k}} + sC_{gd,k} \end{bmatrix} \begin{bmatrix} u_x \\ u_g \\ u_d \end{bmatrix} = \begin{bmatrix} i_x \\ 0 \\ 0 \end{bmatrix} \tag{51}$$

The voltage $u_x$ as a function of $i_x$ can be obtained by solving this system using Cramer's

rule. Therefore:

$$Z_{d,k-1} = \frac{v_x}{i_x} = \frac{C_{f,k}(1 + sC_{gd,k}Z_{d,k}) + C_{gs,k} + C_{gd,k}(1 + sC_{gd,k}Z_{d,k} + g_{m,k}Z_{d,k})}{(g_{m,k} + sC_{gs,k})(C_{f,k}(1 + sC_{gd,k}Z_{d,k}) + C_{gd,k})} \tag{52}$$

Furthermore, assuming that $\omega C_{\mathrm{gd},k} Z_{d,k} \ll 1$, which is valid at the operating frequency of 7.76 GHz and even at mmWave frequencies, the previous expression can be simplified as:

$$Z_{d,k-1} = \frac{C_{f,k} + C_{\mathrm{gs},k} + C_{\mathrm{gd},k}(1 + g_{m,k}Z_{d,k})}{(g_{m,k} + sC_{\mathrm{gs},k})(C_{f,k} + C_{\mathrm{gd},k})} \tag{53}$$

Moreover, assuming that $\omega C_{\mathrm{gs},k} \ll g_{m,k}$, which is also valid at the operating frequency of 7.76 GHz and even at mmWave frequencies, we get:

$$Z_{d,k-1} = \frac{C_{f,k} + C_{\mathrm{gs},k} + C_{\mathrm{gd},k}(1 + g_{m,k}Z_{d,k})}{g_{m,k}(C_{f,k} + C_{\mathrm{gd},k})} \tag{54}$$

The impedance $Z_{d,k-1}$ is purely resistive. Assuming also that $R_{\mathrm{opt}}$ is purely resistive and substituting $Z_{d,k} = k \cdot R_{\mathrm{opt}}$ and $Z_{d,k-1} = (k-1)R_{\mathrm{opt}}$, we obtain:

$$C_{f,k} = \frac{C_{\mathrm{gs},k} + C_{\mathrm{gd},k}(1 + g_{m,k}R_{\mathrm{opt}})}{(k-1)g_{m,k}R_{\mathrm{opt}} - 1} \tag{55}$$

With this method, the drain-source voltage is equally distributed at AC. By appropriately adjusting the DC voltages at the gates of the upper transistors, equal distribution of the drain-source voltages across the stack at DC can be achieved.

Under optimal conditions, the gate-drain voltage of the $k$th transistor is given by the following expression:

$$V_{gd,k} = -\frac{1 + g_{m,k}R_{\mathrm{opt}}}{g_{m,k}R_{\mathrm{opt}}} V_{ds} \tag{56}$$

Therefore, in order to prevent $V_{gd}$ from exceeding the breakdown voltage, the transistor must be sufficiently thick. It is also advisable to avoid large values of the capacitor $C_{f,k}$, so that the gates of the upper transistors can swing adequately and ensure that $V_{gd}$ remains below the breakdown voltage.

It is worth noting that at mmWave frequencies, the amplifier performance degrades due to parasitic effects. These parasitics draw part of the current, preventing the full current from reaching the load. In addition, they cause phase misalignments in the voltage waveforms. The most common technique to address this issue is the insertion of a shunt inductance between two transistors in the stack.

### 5.6.2 Cascode Differential Power Amplifier in 22nm CMOS FD-SOI

A cascode differential power amplifier was implemented in 22 nm CMOS FD-SOI technology. The circuit is shown in Figure 5.24. Ideal baluns were used at both the input and output. The neutralization capacitors were again selected to maximize the $\mu$-factor. Their value is indeed very close to the gate-drain capacitance ($C_{gd}$) of the bottom transistors. The RC network at the gates of the upper transistors along with the input resistor that was added between the gates of the lower transistors ensure unconditional stability over a wide frequency range [0, 100 GHz].

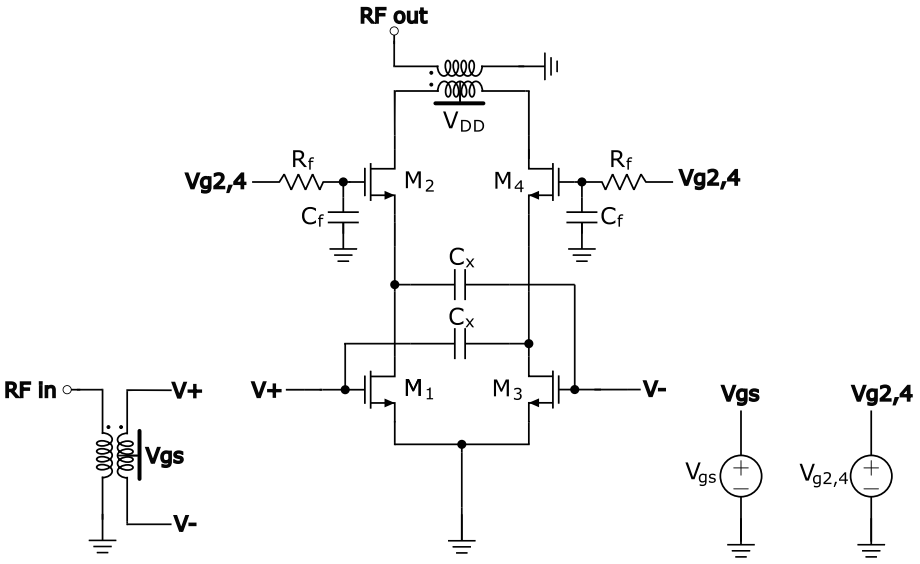



Figure 5.24: Cascode differential power amplifier

The gates of the lower transistors were biased near the threshold voltage, enabling Class B operation. The gates of the upper transistors were biased in such a way as to achieve an equal distribution of the drain-source voltage ($V_{DS}$) under DC conditions. Finally, the load resistor was set equal to the optimal load-pull impedance. The results are presented in Figure 5.25 and summarized in Table 5.6. The output power and gain have approximately doubled. On the other hand, the Power-Added Efficiency (PAE) decreased slightly due to the added parasitics of the upper transistors, which draw a small portion of the drain current and prevent it from fully flowing through the load.

Table 5.6: Performance comparison between differential and cascode differential power amplifiers

| **Parameter** | **Differential** | **Cascode** |
|---|---|---|
| Supply Voltage ($V_{DD}$) | 0.8 V | 1.6 V |
| Gain | 13.22 dB | 16.18 dB |
| Saturated Output Power ($P_{\text{sat}}$) | 20.55 dBm | 23.11 dBm |
| 1 dB Compression Point ($OP_{\text{1dB}}$) | 18.83 dBm | 21.64 dBm |
| PAE at 1 dB Compression Point ($PAE_{\text{1dB}}$) | 59.12% | 58.14% |
| Maximum PAE ($PAE_{\text{max}}$) | 61.46% | 60.55% |

## 5.7 Two-Stage Power Amplifier

In some cases, the power provided by the stage preceding the power amplifier is insufficient to drive it at its 1 dB compression point. In such cases, a driver stage must be added before the power amplifier to deliver sufficient input power. A two-stage power amplifier, consisting of a differential driver and a differential PA stage, is shown in Figure 5.26. A

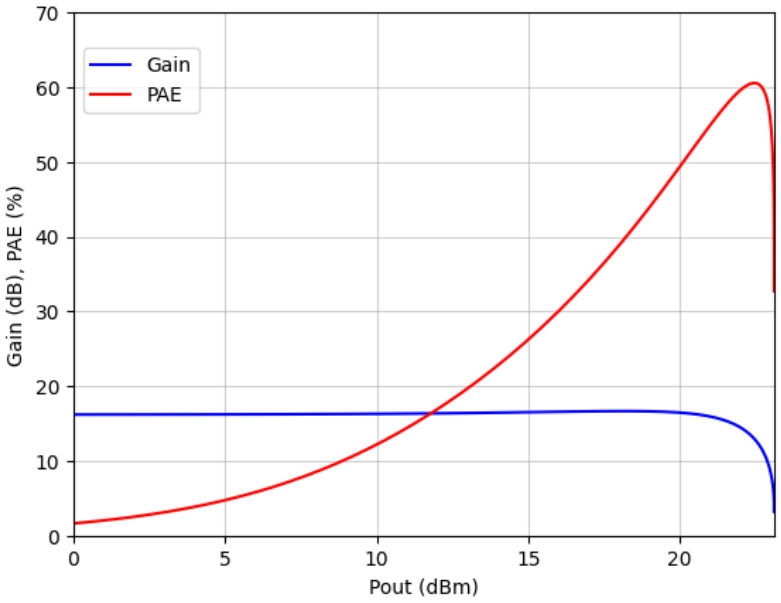



Figure 5.25: Gain and PAE versus output power for the cascode differential power amplifier in Class B operation

balun is used at both the input and the output, while a transformer is inserted between the two stages to achieve interstage matching.

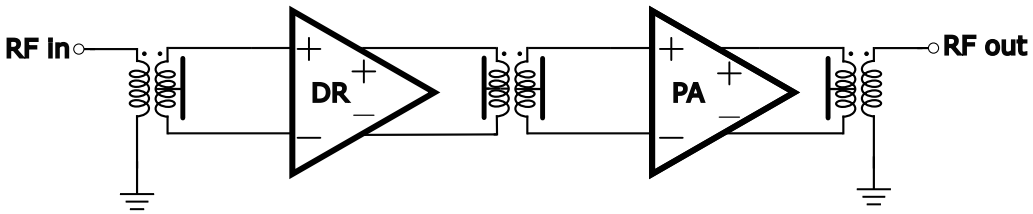



Figure 5.26: Two-Stage Power Amplifier

However, the driver stage degrades the overall Power Added Efficiency of the amplifier. The Power Added Efficiency of the driver stage is given by:

$$PAE_{DR} = \frac{P_{DR} - P_{in}}{P_{DC,DR}} \tag{57}$$

The Power Added Efficiency of the PA stage is given by:

$$PAE_{PA} = \frac{P_{out} - P_{DR}}{P_{DC,PA}} \tag{58}$$

From equation (57), the output power of the driver stage can be written as:

$$P_{DR} = PAE_{DR} \cdot P_{DC,DR} + P_{in} \tag{59}$$

Substituting into equation (58), we obtain the total output power:

$$P_{out} = PAE_{PA} \cdot P_{DC,PA} + P_{DR} = PAE_{PA} \cdot P_{DC,PA} + PAE_{DR} \cdot P_{DC,DR} + P_{in} \tag{60}$$

Therefore, the Power Added Efficiency of the two-stage power amplifier is:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC,DR} + P_{DC,PA}} = \frac{PAE_{DR} \cdot P_{DC,DR} + PAE_{PA} \cdot P_{DC,PA}}{P_{DC,DR} + P_{DC,PA}} \tag{61}$$

Since it generally holds that $PAE_{DR} < PAE_{PA}$, the overall PAE of the two-stage power amplifier lies between $PAE_{DR}$ and $PAE_{PA}$.

In this work, a two-stage power amplifier was implemented in 22 nm CMOS FD-SOI technology. The central frequency is 7.76 GHz, while the bandwidth ranges from 7.125 GHz to 8.4 GHz. The following chapter presents the design of the PA stage in detail.

# Chapter 6

# Design of the Power Amplifier Stage

## 6.1 Topology

The circuit of the power amplifier stage is presented in Figure 6.1. The topology of the power amplifier is a differential three-stack, chosen due to the advantages of both stacked transistors and differential amplifier configurations. The central frequency is 7.76 GHz, while the bandwidth ranges from 7.125 GHz to 8.4 GHz.

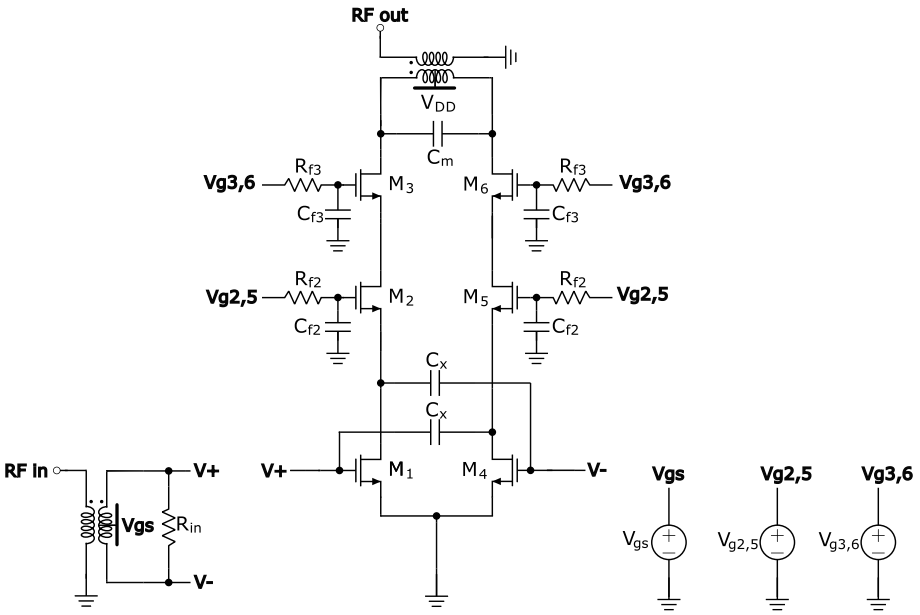



Figure 6.1: Power amplifier stage

## 6.2 Design Flow

The Power Amplifier was biased in Class B, since it offers the best trade-off among all considered performance metrics, as concluded in Chapter 5.4.5.

### 6.2.1 Transistor Sizing

Figure 6.2 presents the maximum output power at the 1 dB compression point and the peak Power-Added Efficiency (PAE) as a function of the total gate width of the transistors. The output power increases with the gate width, while the PAE reaches its maximum at 350 $\mu$m and decreases for larger widths due to increased parasitic effects.

The transistors' width was selected to be 400 $\mu$m in order to provide a high current capable of delivering sufficient output power. Additionally, at this width, the optimal load-pull impedance is very close to 50 Ω. Thick transistors were also chosen to ensure that the gate-drain voltage $V_{gd}$ remains below the breakdown voltage, as discussed in Chapter 5.6.1.

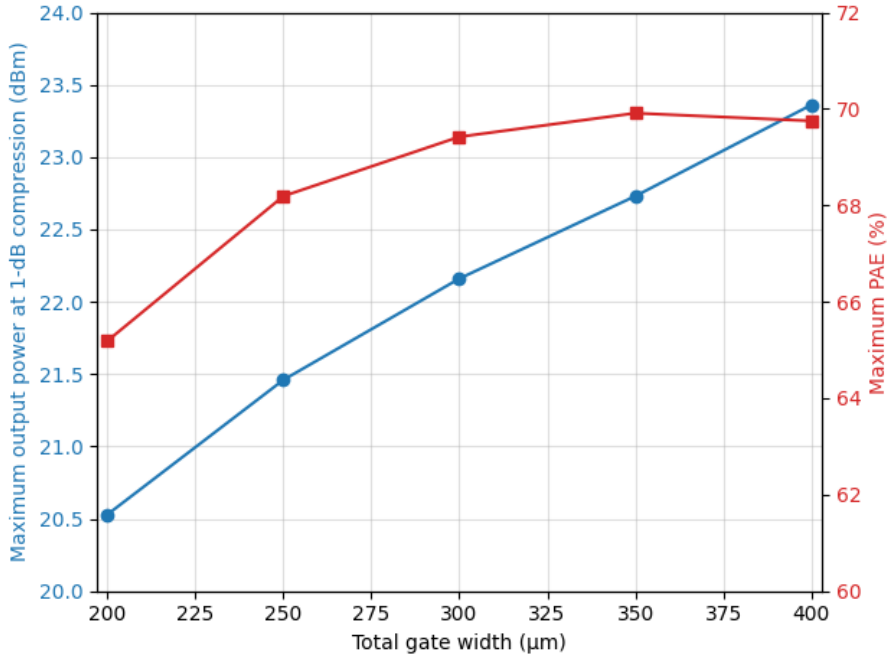



Figure 6.2: Maximum output power at 1 dB compression point and maximum PAE versus total gate width

### 6.2.2 Neutralization Capacitors

The values of the neutralization capacitors were selected to maximize the $\mu$-factor. Figure 6.3 shows the $\mu$-factor as a function of the capacitor $C_x$, while Figure 6.4 presents the maximum gain and the maximum stable gain (MSG) also as functions of $C_x$.

It is observed that both MSG and the $\mu$-factor are maximized when $C_x = 73$ fF. This value is very close to the gate-drain capacitance $C_{gd}$ of the bottom transistors in the stack, as theory predicts (see Chapter 5.5.1).

Furthermore, it is noted that the overall stability was improved through the inclusion of RC networks on the upper transistors, the addition of an input resistor, and the implementation of a real balun at the output.

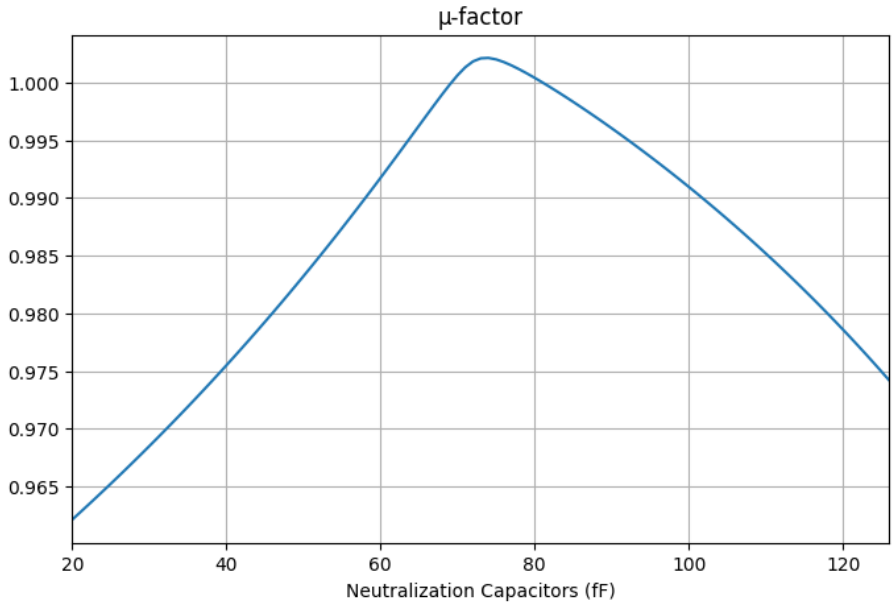



Figure 6.3: $\mu$-factor versus $C_x$.

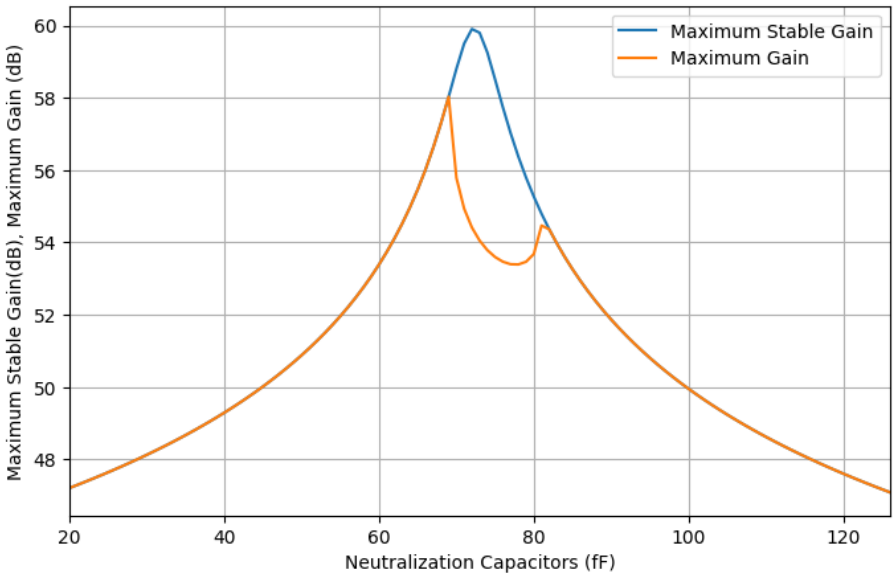



Figure 6.4: Maximum gain and maximum stable gain versus $C_x$.

### 6.2.3 Load Pull Simulation

Load-pull simulations are performed for a specific input power level. Therefore, in order to accurately determine the optimal load impedance, the optimal input-referred 1 dB compression point must be known.

As a first step, using load-line theory and the IV curves, the optimal Class-A load impedance of a single transistor with width 400 $\mu$m was estimated. Then, the optimal load impedance for the differential three-stack topology operating in Class A is eight times larger than that of the single device. In Class B, the optimal load is theoretically twice the Class-A value, according to equation (41) in Chapter 5.3.

Using this value as a first estimate of the load resistance, an initial approximation of the optimal input-referred 1 dB compression point was obtained. A first load-pull simulation was then run using this input power. By performing successive load-pull simulations while adjusting the input power accordingly, the optimal input-referred 1 dB compression point was accurately determined.

Figure 6.5 shows the result of the load-pull simulation for an input power equal to the final optimal input-referred 1 dB compression point.

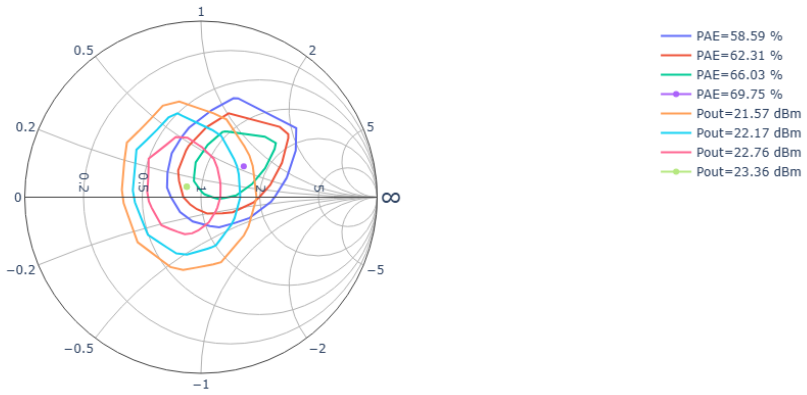



Figure 6.5: Load-pull simulation at the optimal input-referred 1 dB compression point

### 6.2.4 Output Balun

The output balun is shown in Figure 6.6. It is implemented as a stacked transformer with two turns on both the primary and secondary windings, aiming to achieve a high coupling coefficient and minimize insertion losses. The inner diameter is 130 $\mu$m, and the metal width of both windings is 10 $\mu$m. The detailed balun characteristics are provided in A.2.

A capacitor $C_m$ was included to ensure proper input matching. Taking this capacitor into account, the input impedance of the balun is shown in Figure 6.7, while the corresponding insertion losses are depicted in Figure 6.8.

### 6.2.5 RC Networks

As a first approximation, the resistance values of the RC networks were chosen to be relatively high, initially set to 1 k$\Omega$. The initial estimates for the capacitances $C_{f,2}$ and $C_{f,3}$ were derived using the analytical expression presented in Chapter 5.6.1. However, in order to improve the performance and ensure reliable operation, the final component values were somewhat adjusted from their theoretical values. The final values used are $C_{f,2} = 640$ fF, $C_{f,3} = 215$ fF, and $R_{f,2} = R_{f,3} = 360$ $\Omega$.

Figure 6.9 shows the drain voltages across the stacked transistors in the absence of the RC network, while Figure 6.10 presents the corresponding voltages when the RC networks

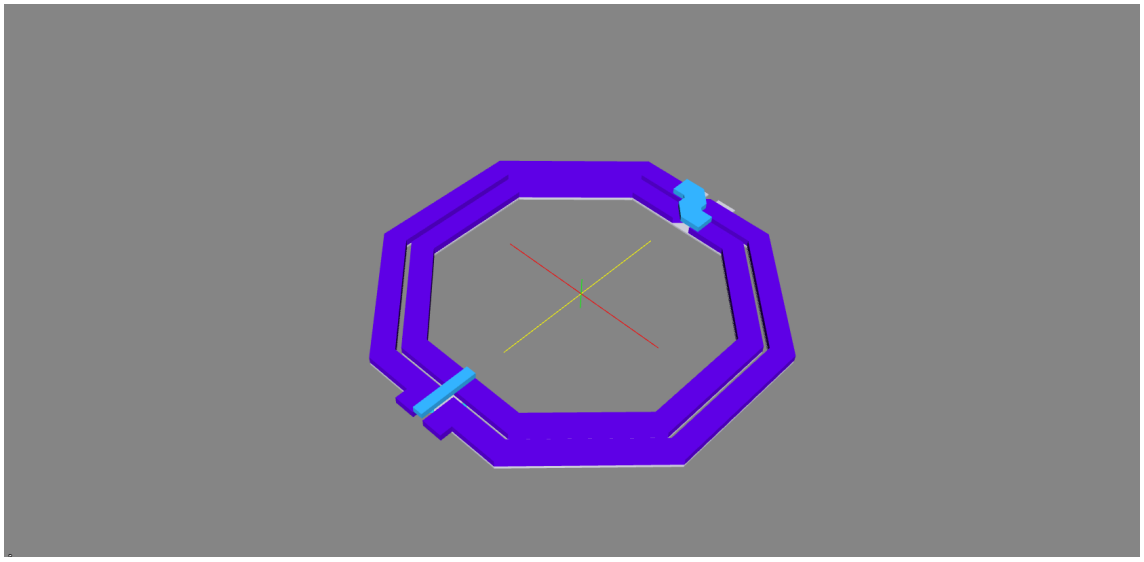


Figure 6.6: Stacked output balun layout

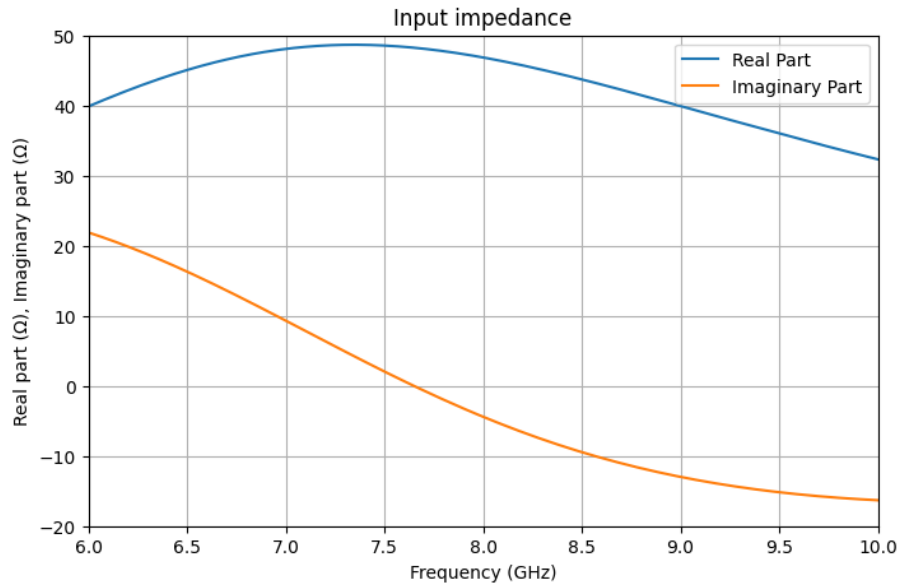



Figure 6.7: Input impedance of the output balun including the matching capacitor $C_m$

are included. It is evident that the voltage distribution across the stack is significantly more uniform in the latter case, and the $V_{ds}$ of all transistors remains safely below the breakdown voltage.

### 6.2.6 Input Resistor

Without the input resistor, the input impedance of the power amplifier is $Z_{in} = 5.4 - j124\ \Omega$. This extremely low real part and highly capacitive imaginary part make interstage matching very difficult. Moreover, such an impedance severely degrades the bandwidth. Figures 6.11 and 6.12 illustrate how the amplifier's performance and input impedance vary

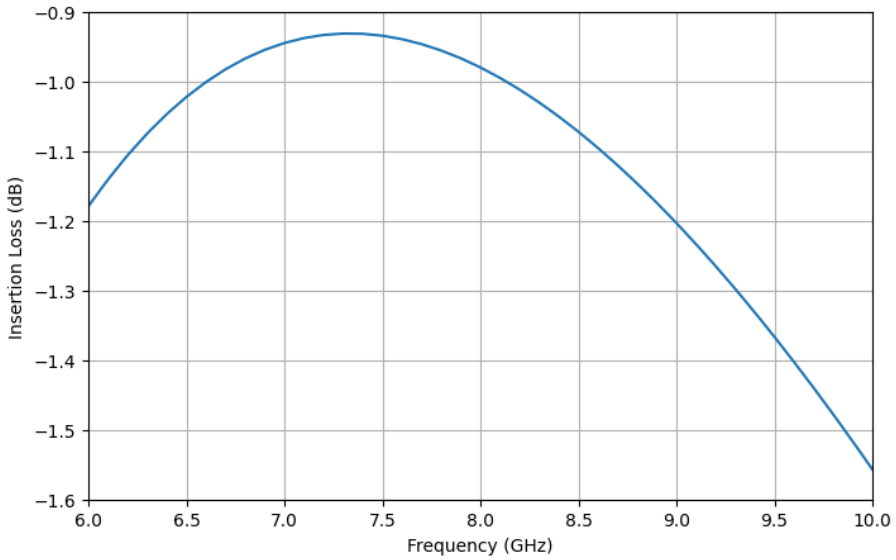



Figure 6.8: Insertion loss of the interstage balun including the matching capacitor $C_m$

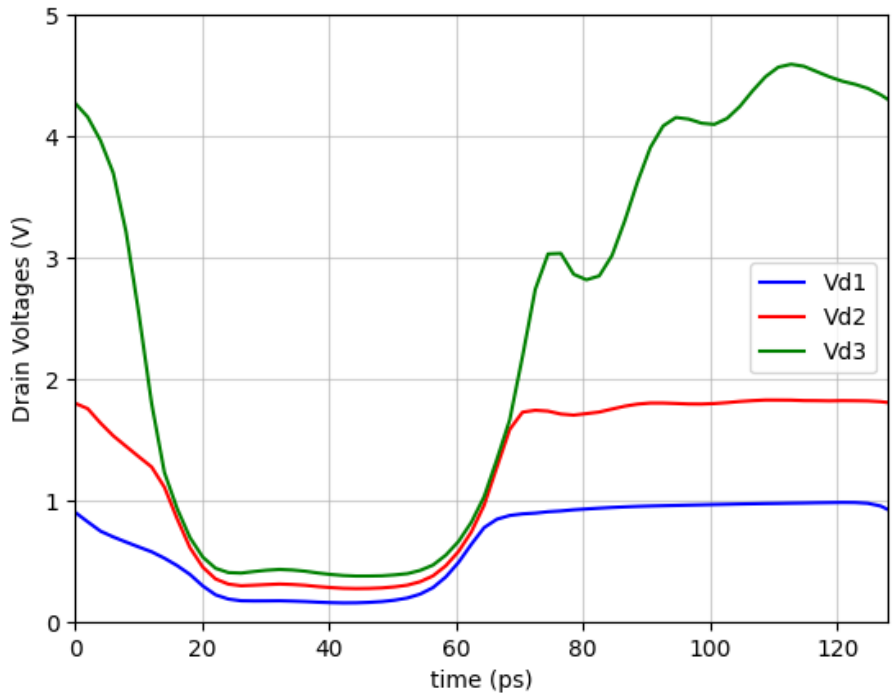



Figure 6.9: Drain voltages without the RC network

as a function of the input resistor value.

The output power remains nearly constant regardless of the input resistor value. However, the gain increases as the resistor value increases, since less current is drawn from the input resistor. Consequently, the Power-Added Efficiency also improves due to the higher gain.

The input resistor value was selected to be 80 Ω, where the gain is satisfactory and the

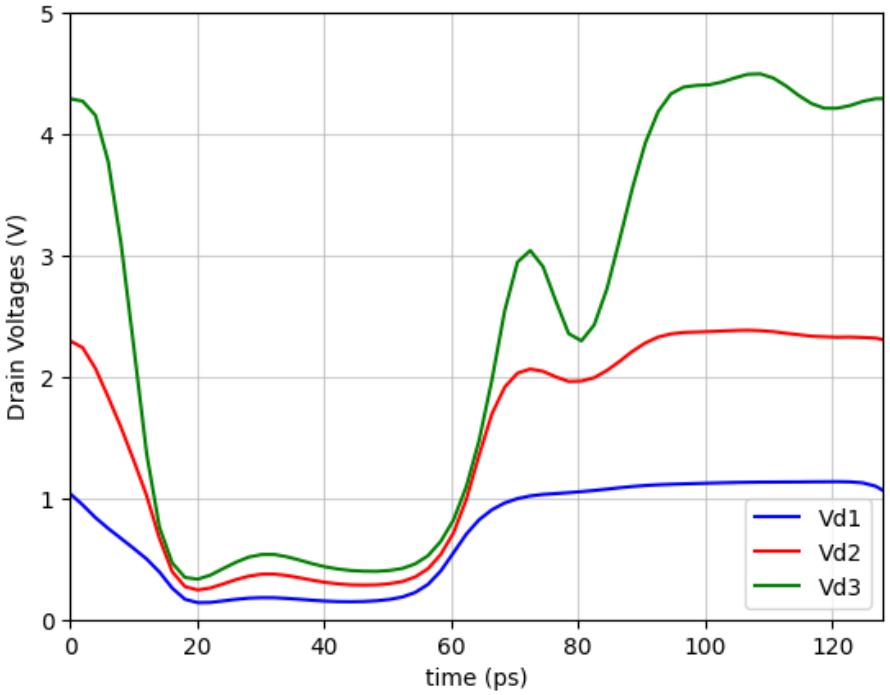



Figure 6.10: Drain voltages with the RC network included

input impedance is $Z_{in} = 57.03 - j36.84\ \Omega$.

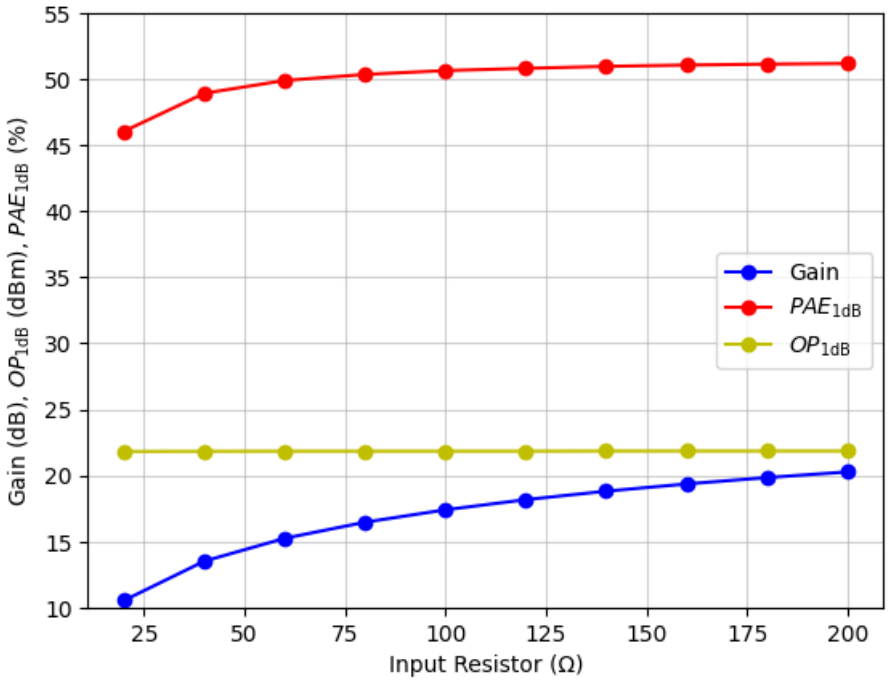



Figure 6.11: Performance metrics versus input resistor value

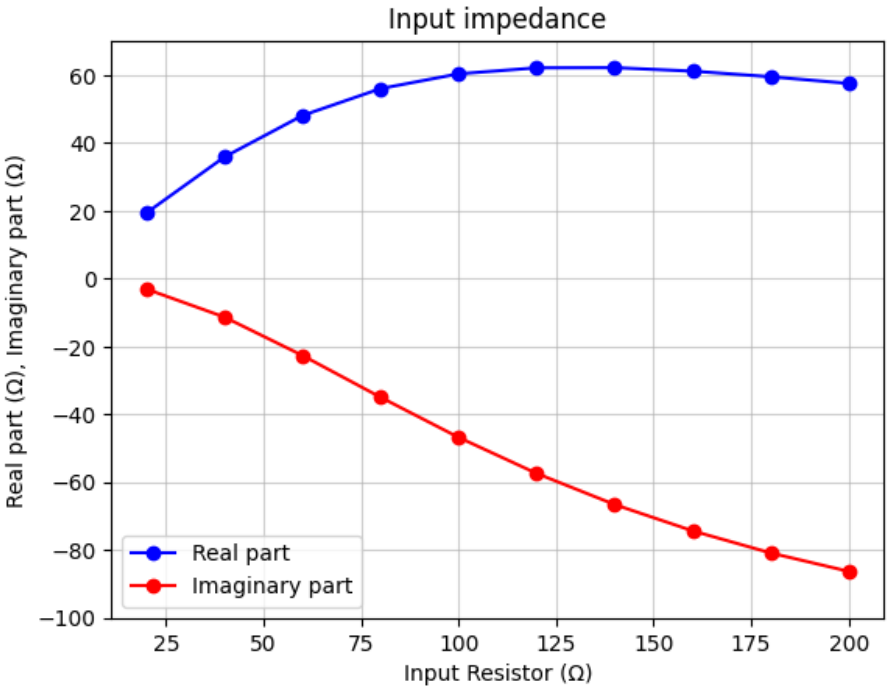



Figure 6.12: Input impedance versus input resistor value

## 6.3 Results

### 6.3.1 Nominal

When the source impedance is set equal to the complex conjugate of the input impedance of the power amplifier stage at the center frequency, the performance results are illustrated in Figures 6.13, 6.14, and 6.15, and are summarized in Table 6.1.

Table 6.1: Summary of the power amplifier stage performance

| **Parameter** | **Value** |
|---|---|
| Supply Voltage ($V_{DD}$) | 2.4 V |
| Gain | 16.62 dB |
| Saturated Output Power ($P_{\text{sat}}$) | 23.31 dBm |
| 1 dB Compression Point ($OP_{1\text{dB}}$) | 22.04 dBm |
| PAE at 1 dB Compression Point ($PAE_{1\text{dB}}$) | 51.34% |
| Maximum PAE ($PAE_{\text{max}}$) | 51.51% |
| Difference Between $IIP_3$ and $IP_{1\text{dB}}$ | 6 dB |

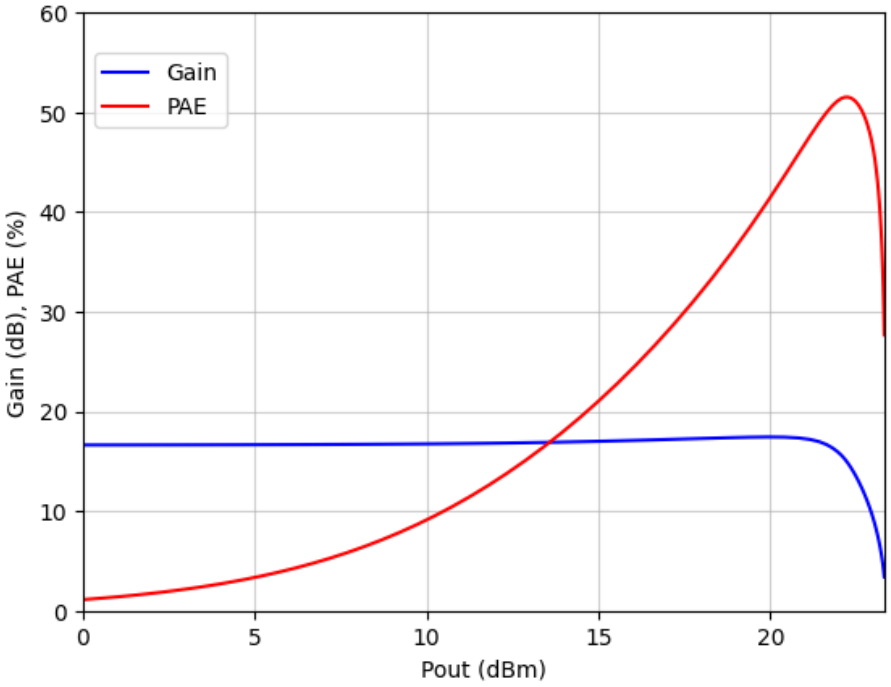



Figure 6.13: Gain and PAE versus output power of the power amplifier stage

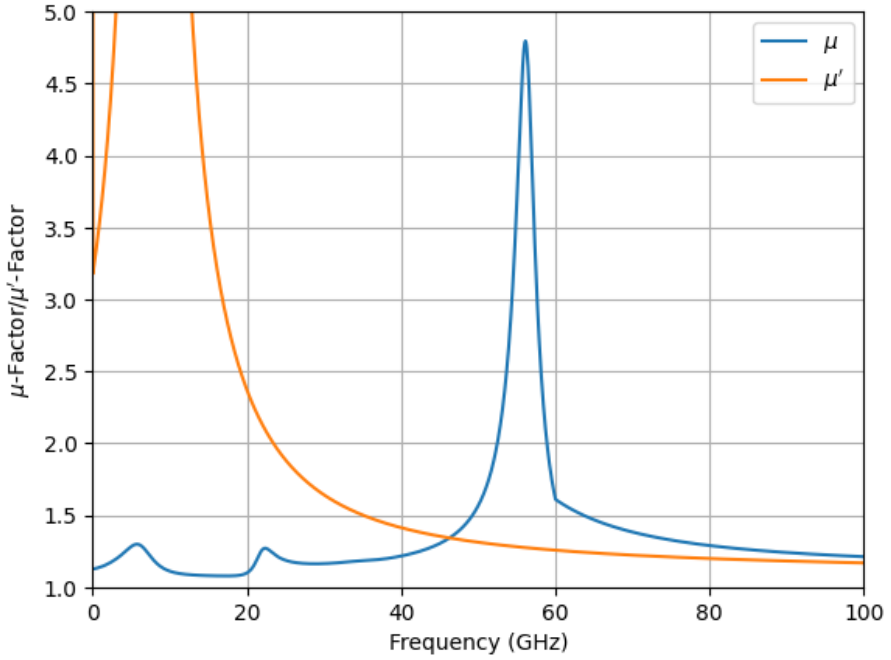



Figure 6.14: Stability factors $\mu$ and $\mu'$ of the power amplifier stage

### 6.3.2 Corners

Figures 6.16–6.18 illustrate the performance of the power amplifier stage under various process and temperature corners. In some corners, the output power at the 1dB compression point decreases while the gain increases. In others, the opposite occurs, and in some

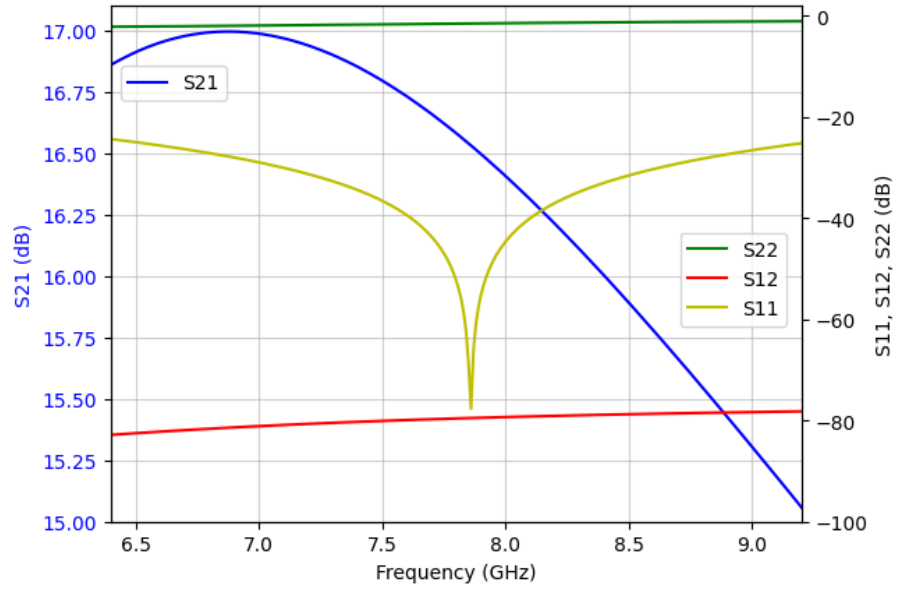



Figure 6.15: S-parameters of the power amplifier stage

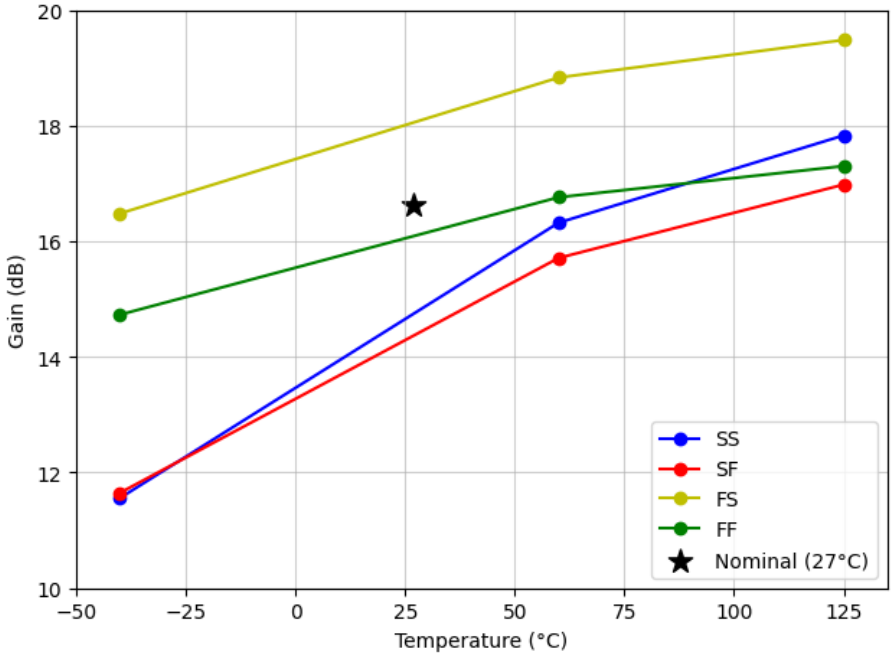



Figure 6.16: Gain performance across process and temperature corners for the power amplifier stage

cases, the behavior is very close to the nominal. In the first case, the amplifier operates closer to Class AB due to a reduced threshold voltage ($V_{th}$), while in the latter, it shifts toward Class C operation as a result of an increased $V_{th}$.

The performance of the power amplifier in cases where the threshold voltage is lower than nominal can be improved by reducing the DC gate bias voltage of the lower transistors, so that the amplifier operates closer to Class B. On the other hand, in cases where the threshold voltage is higher than nominal, the back gate of the lowest transistors should not

be connected to ground. Instead, it should be biased with a sufficiently high DC voltage to reduce the threshold voltage.

It should be emphasized that one of the advantages of the technology 22nm CMOS FD-SOI is that the back gate of each transistor is not connected to the substrate; instead,

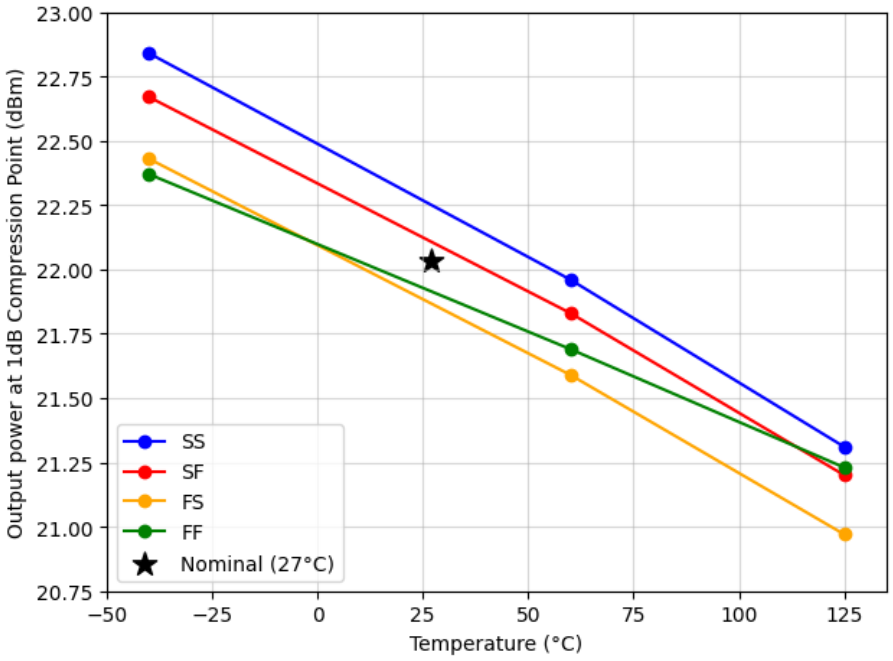



Figure 6.17: Output power at 1dB compression point across process and temperature corners for the power amplifier stage

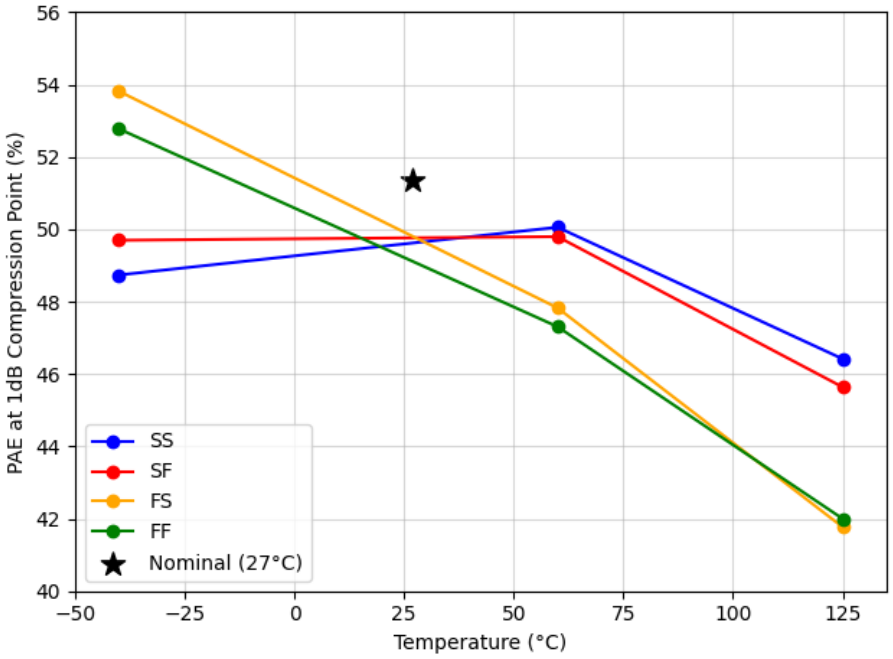



Figure 6.18: PAE at 1dB compression point across process and temperature corners for the power amplifier stage

each transistor has its own back gate whose DC bias can be adjusted arbitrarily. This allows us to improve the performance of the power amplifier under certain corners.

Figures 6.19 and 6.20 illustrate how adaptive back gate biasing and adaptive gate biasing steer the amplifier to the desired Class B operation.

Lastly, the power amplifier stage is unconditionally stable in all corners.

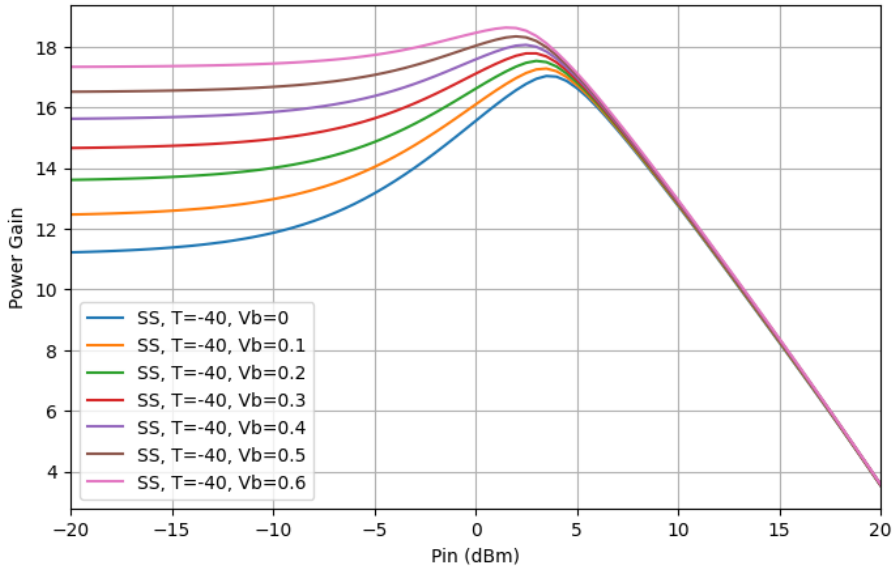



Figure 6.19: Adaptive back gate biasing

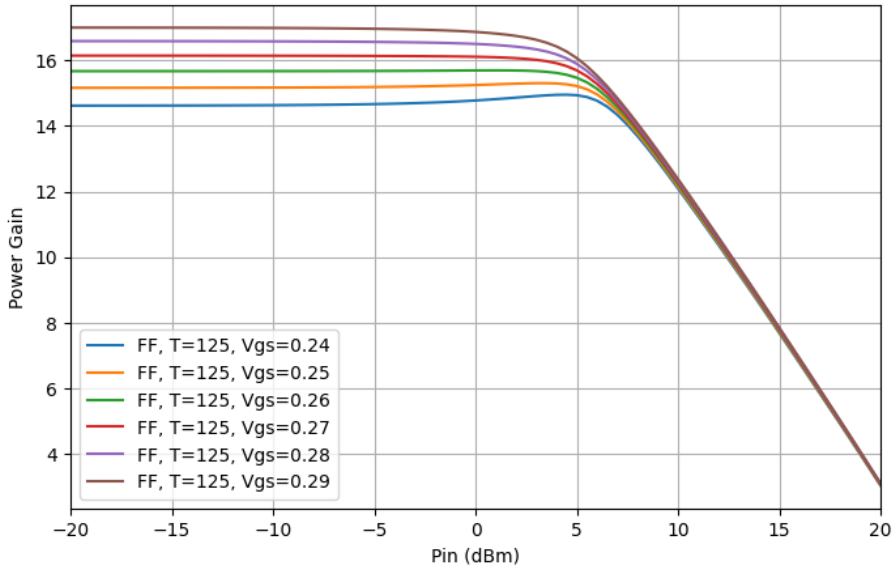



Figure 6.20: Adaptive gate biasing

## 6.4 Layout

The layout of the power amplifier stage is presented in Figure 6.21.

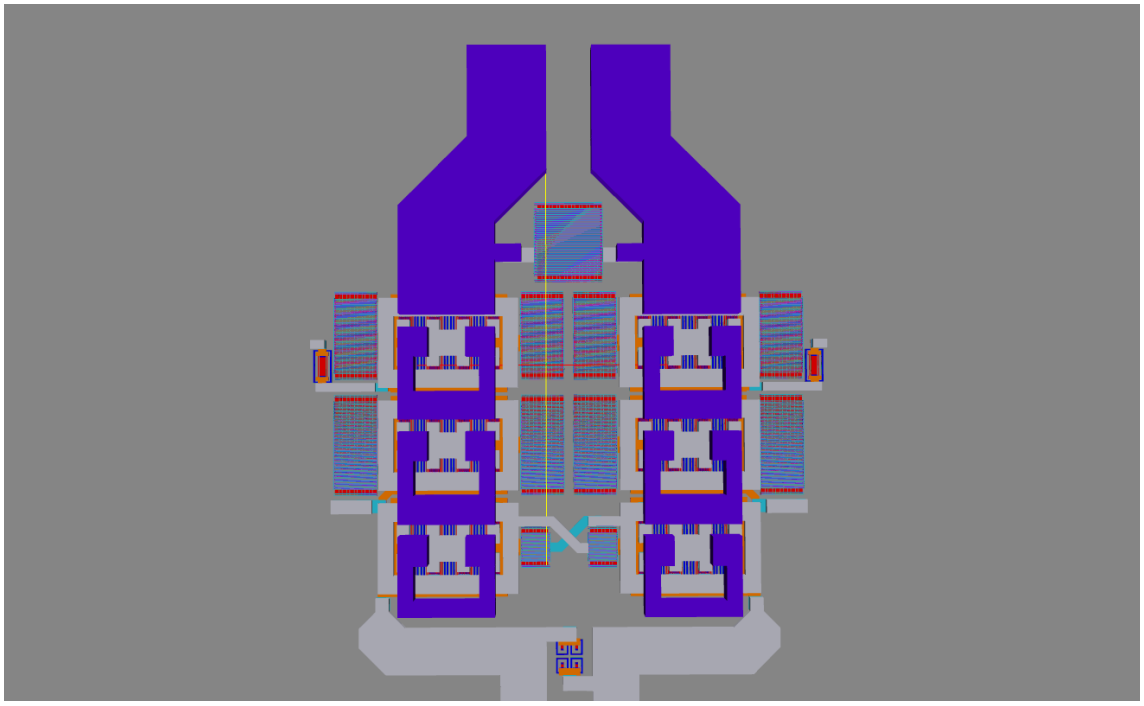


Figure 6.21: Power amplifier stage layout

The technology provides eight metal layers, of which the top three—Metal 6, Metal 7, and Metal 8—are thick. Among them, Metal 7 exhibits the highest conductivity. To minimize conduction losses across the transistor stack—from the drain of the bottom-most transistor to the drain of the top-most one—and to maximize the power delivered to the output, a combination of Metals 6 and 7 was employed for both the drain and source interconnections.

Metal 8 was not utilized due to its significantly greater minimum thickness and more restrictive Design rules, which would have made the layout less compact and more difficult to implement.

Due to layout limitations and restricted access to higher metal layers for routing, the first four metal layers were used to route the gate signals. While this choice was necessary, it introduced increased resistive losses, resulting in a slight degradation in gain.

Additionally, the current flowing through the drain and source terminals is considerably higher than that through the gate. Therefore, thick metal layers were employed for the drain and source interconnections to satisfy electromigration rules and minimize conduction losses. This design choice is critical, as conduction losses increase proportionally with current for a given resistance introduced by the layout. If not properly managed, these losses can significantly degrade the overall performance and efficiency of the power amplifier.

The capacitors at the gates of the transistors in the second and third tiers were split into two equal parts to achieve a more compact layout.

Furthermore, due to modifications introduced by the interconnects, the capacitances of the capacitors in the second and third tiers had to be increased in order to enhance performance and achieve a more uniform distribution of the drain-source voltages ($V_{DS}$) across the stack. Additionally, reducing the resistance at the gates of the transistors in the second tier was necessary to improve both performance and voltage balancing.

However, voltage swings still appear on the gate terminals of the transistors in the

second tier. As a result, the gate-drain voltage ($V_{GD}$) remains below the breakdown voltage, as required. These swings are caused by the non-zero resistance between the gate nodes and the DC voltage source, which is inevitably introduced by the interconnect metals.

## 6.5 Post Layout Results

The post-layout results are presented in Figures 6.22, 6.24, and 6.23, and are summarized in Table 6.2, where they are compared against the schematic-level results. It is evident that the layout has slightly degraded the overall performance of the power amplifier stage in terms of gain, output power, and efficiency. However, the linearity has improved, as indicated by the increased separation between the 1 dB compression point and the third-order intercept point.

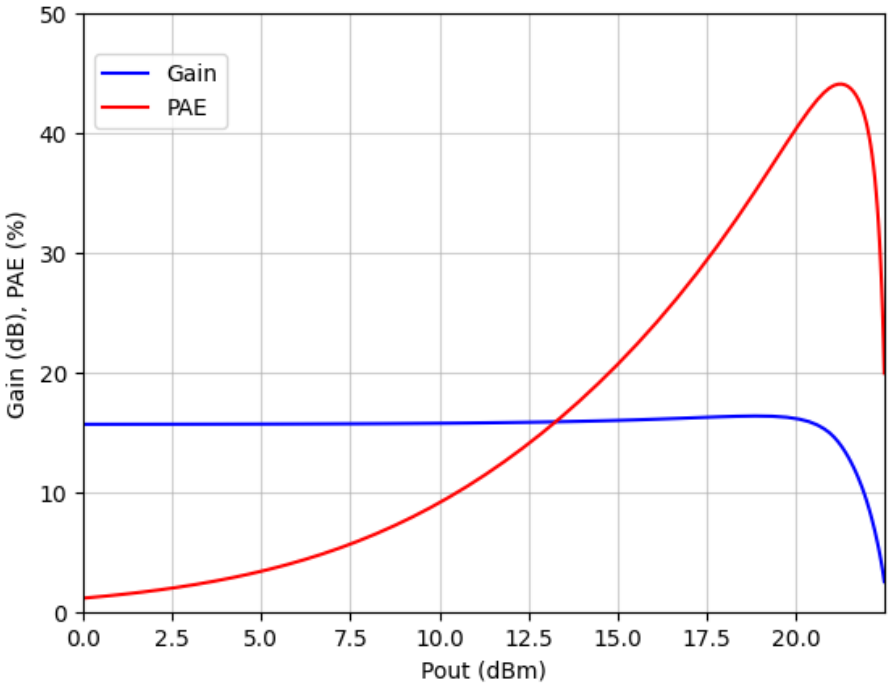



Figure 6.22: Post-layout Gain and PAE versus output power of the power amplifier stage

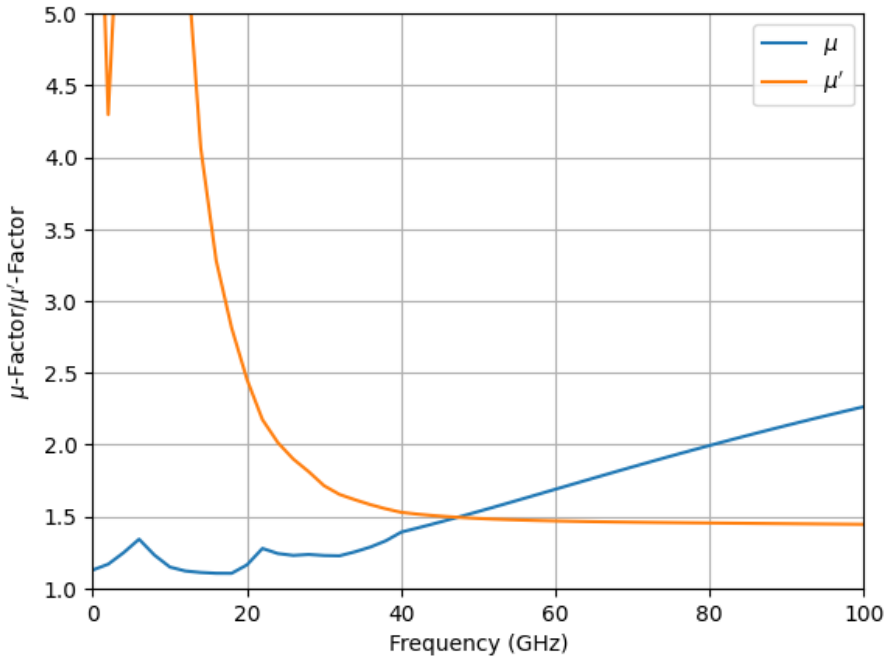



Figure 6.23: Post-layout stability factors $\mu$ and $\mu'$ of the power amplifier stage

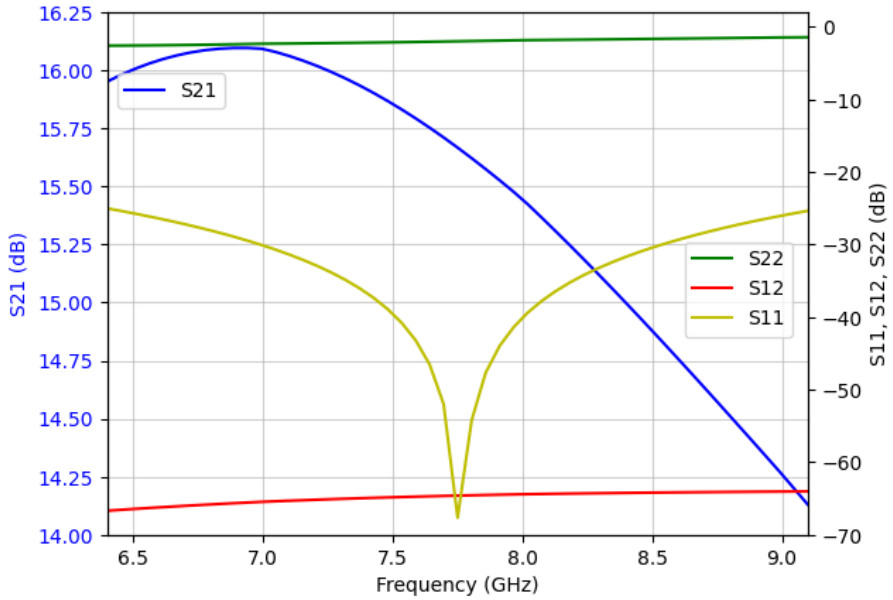



Figure 6.24: Post-layout $S$-parameters of the power amplifier stage

Table 6.2: Performance comparison between schematic and post-layout results

| **Parameter** | **Schematic** | **Post-Layout** |
|---|---|---|
| Supply Voltage ($V_{DD}$) | 2.4 V | 2.4 V |
| Gain | 16.62 dB | 15.66 dB |
| Saturated Output Power ($P_{\text{sat}}$) | 23.31 dBm | 22.45 dBm |
| 1 dB Compression Point ($OP_{\text{1dB}}$) | 22.04 dBm | 21.03 dBm |
| PAE at 1 dB Compression Point ($PAE_{\text{1dB}}$) | 51.34% | 43.93% |
| Maximum PAE ($PAE_{\text{max}}$) | 51.51% | 44.10% |
| Difference Between $IIP_3$ and $IP_{\text{1dB}}$ | 6 dB | 10.18 dB |

# Chapter 7

# Design of the Driver Stage

## 7.1 Topology

The circuit of the driver stage is presented in Figure 7.1. The driver cell is implemented as a differential amplifier, incorporating neutralization capacitors and an input resistor. In the following section, the rationale behind the selection of this specific topology for the driver stage will be discussed.

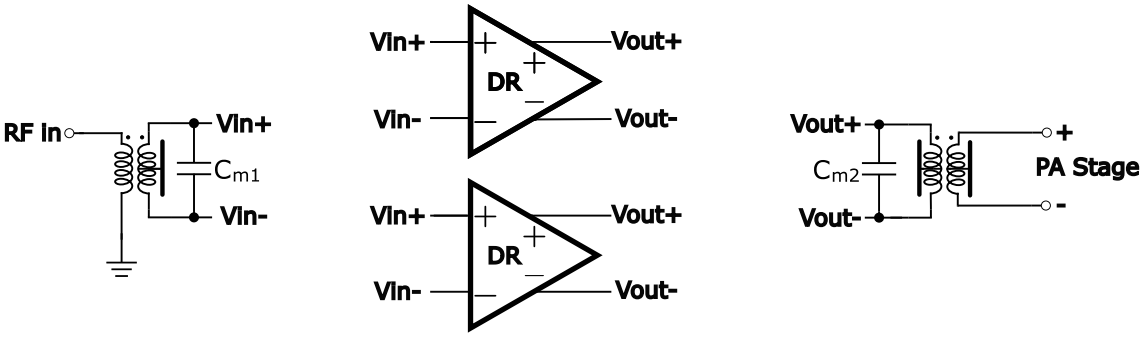



Figure 7.1: Driver stage

## 7.2 Design Approach

To design the driver stage, it must be taken into consideration that the driver's gain should remain linear at the input-referred 1 dB compression point of the power amplifier (PA) stage. Consequently, the driver's output-referred 1 dB compression point should be at least 3 dB higher than the PA's input-referred 1 dB compression point. Additionally, the driver's output-referred 1 dB compression point should not be excessively high in order to minimize degradation of the overall PA's power added efficiency.

The input-referred 1 dB compression point, both in schematic and post-layout, is approximately 6.4 dBm. As a first step to simplify the design and improve overall performance, the PA stage operation was shifted closer to Class C by reducing the bias $V_{GS}$ by 0.01 V. This adjustment increased the output power at the 1 dB compression point and the PAE at this point, but resulted in a reduction of gain. Simultaneously, the input-referred 1 dB compression point increased to approximately 7 dBm.

To design a differential pair driver stage delivering an output power of 11 dBm at the 1 dB compression point (11 and not 10 because this value will drop when actual components and layout are introduced), while ensuring that the PAE at the 1 dB compression point is close to the maximum PAE, the transistor width had to be small. This resulted in insufficient gain and required a relatively large optimal load-pull impedance.

Therefore, to increase the gain, the transistor width of the differential pair was set to 200 $\mu$m. Additionally, two driver cells were connected in parallel. In this configuration, each cell sees twice the impedance of the interstage transformer input along with the matching capacitor, facilitating easier interstage matching since the optimal load-pull impedance is relatively large, as will be shown later.

With this topology, the 1 dB compression point of each cell had to be at least 8 dBm, since the PA will receive double the power that each cell delivers. We want 8 dBm and not 7 dBm because potential losses from the actual components and layout will reduce the power.

The 1 dB compression point contours of the driver cell are presented in Figure 7.2. From these contours, it can be concluded that the driver cell must see an impedance close to 150 Ω or smaller. Therefore, the input impedance of the interstage transformer, along with the matching capacitor, should be 75 Ω or smaller.

Additionally, an input resistor was added between the gates of each driver cell for the same reason it was included in the power amplifier stage.

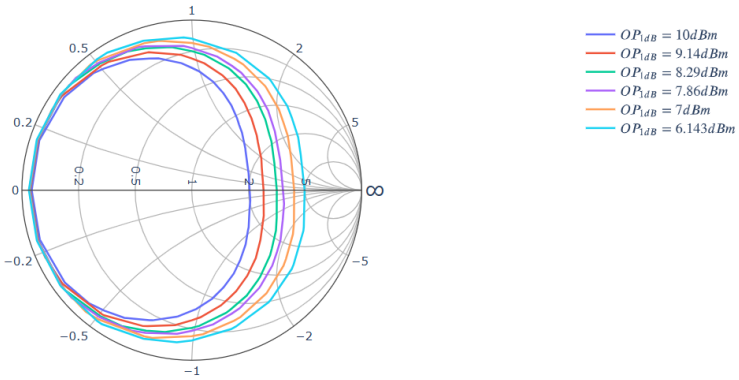



Figure 7.2: 1 dB compression point contours

## 7.3 Interstage Transformer

The interstage transformer is shown in Figure 7.3. It is implemented as a stacked transformer with two turns on both the primary and secondary windings, aiming to achieve a high coupling coefficient and minimize insertion losses. The inner diameter is 130 $\mu m$, and the metal width of both windings is 10 $\mu m$. This is exactly the same component as the output balun of the power amplifier stage.

A capacitor $C_{m2}$ was included to ensure proper input matching. Taking this capacitor into account and terminating the transformer at the input resistance of the power amplifier stage at the central frequency, the input impedance of the transformer is shown in Figure 7.4, while the corresponding insertion losses are depicted in Figure 7.5.

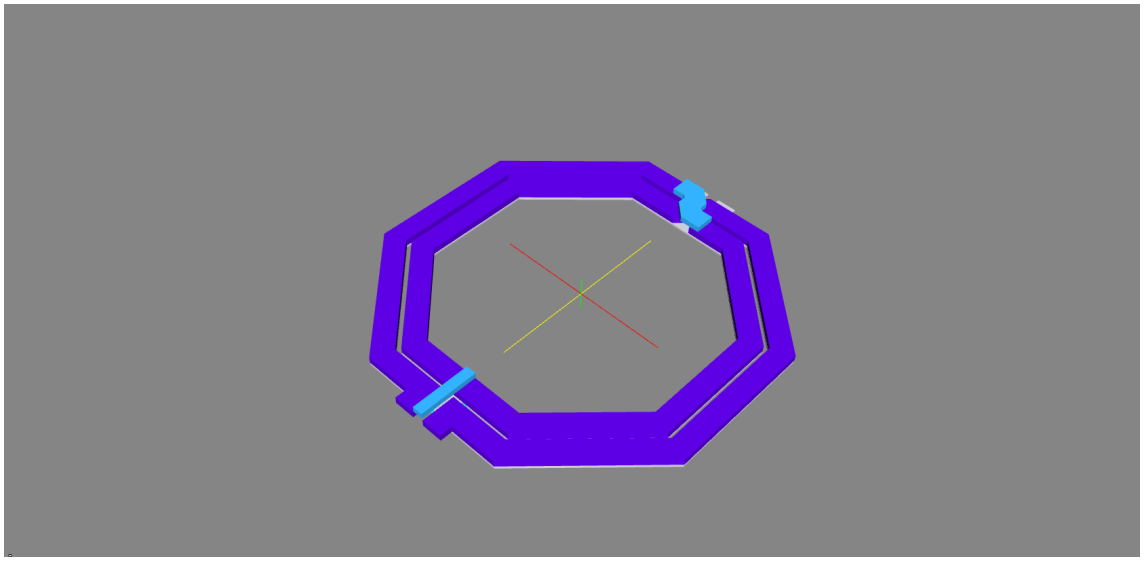


Figure 7.3: Stacked interstage transformer layout

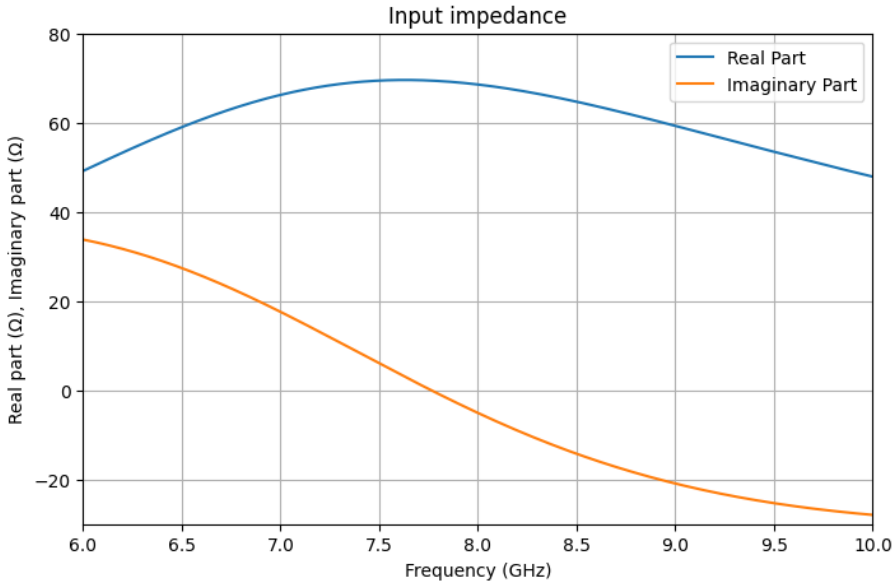



Figure 7.4: Input impedance of the interstage transformer including the matching capacitor $C_{m2}$

## 7.4 Input Balun

The input balun is shown in Figure 7.6. It is implemented as a stacked transformer with two turns on both the primary and secondary windings, aiming to achieve a high coupling coefficient and minimize insertion losses. The inner diameter is 110 $\mu m$, and the metal width of both windings is 6 $\mu m$. The detailed balun characteristics are provided in A.3.

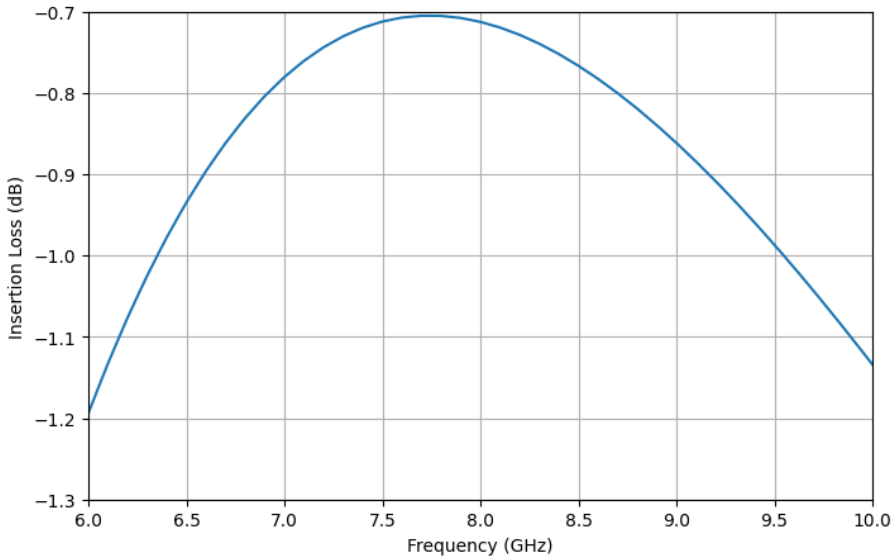



Figure 7.5: Insertion loss of the interstage transformer including the matching capacitor $C_{m2}$

A capacitor $C_{m1}$ was included to ensure proper input matching. Taking this capacitor into account and terminating the balun at the input impedance of the driver stage, the $S_{11}$ scattering parameter of the balun is shown in Figure 7.7, while the corresponding insertion losses are depicted in Figure 7.8.

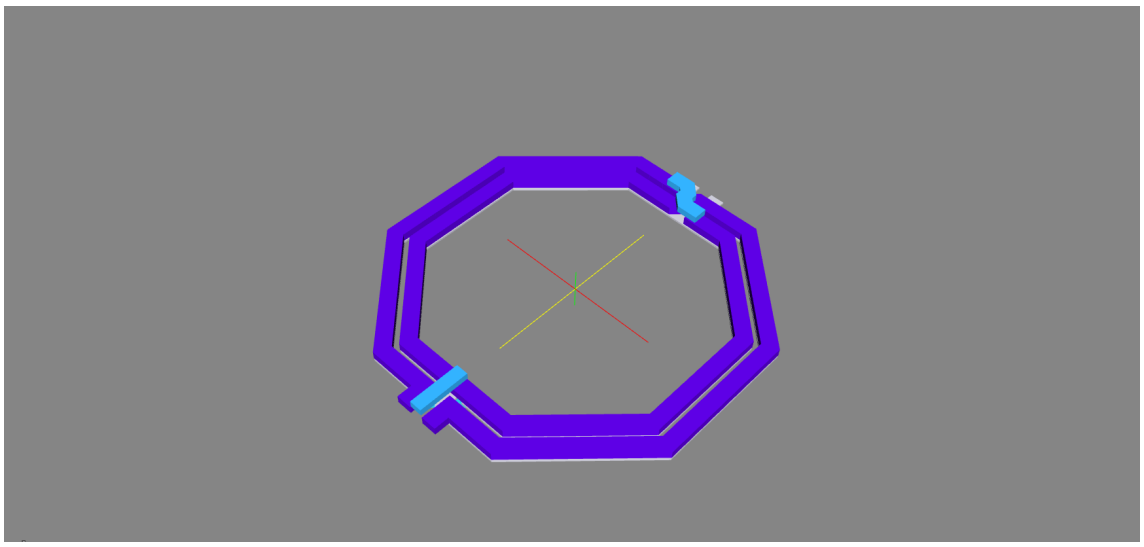


Figure 7.6: Stacked input balun layout

## 7.5 Layout

The layout of the driver stage is shown in Figure 7.9. The transistor interconnects were designed in the same manner as those in the power amplifier stage. Additionally, the matching capacitor $C_{m1}$ was split into two equal parts. At the same time, capacitor $C_{m2}$

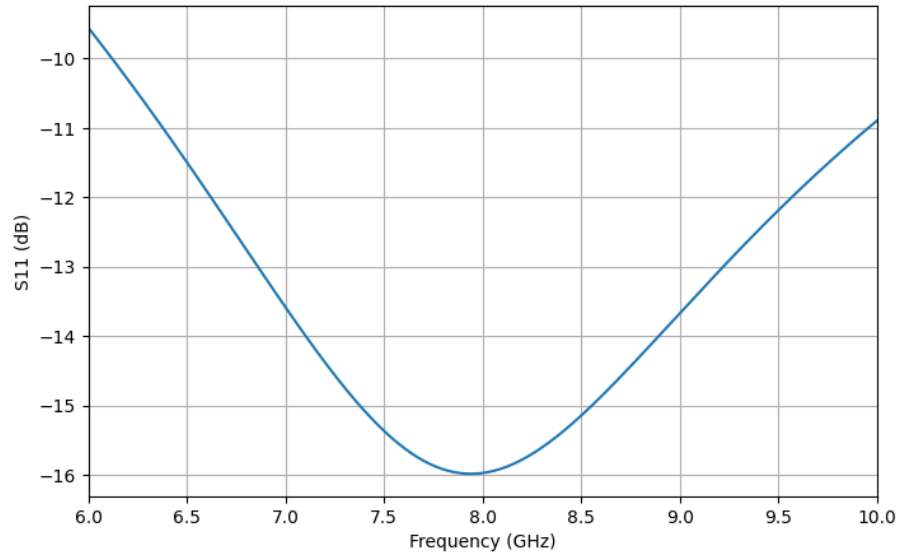



Figure 7.7: $S_{11}$ parameter of the input balun including the matching capacitor $C_{m1}$

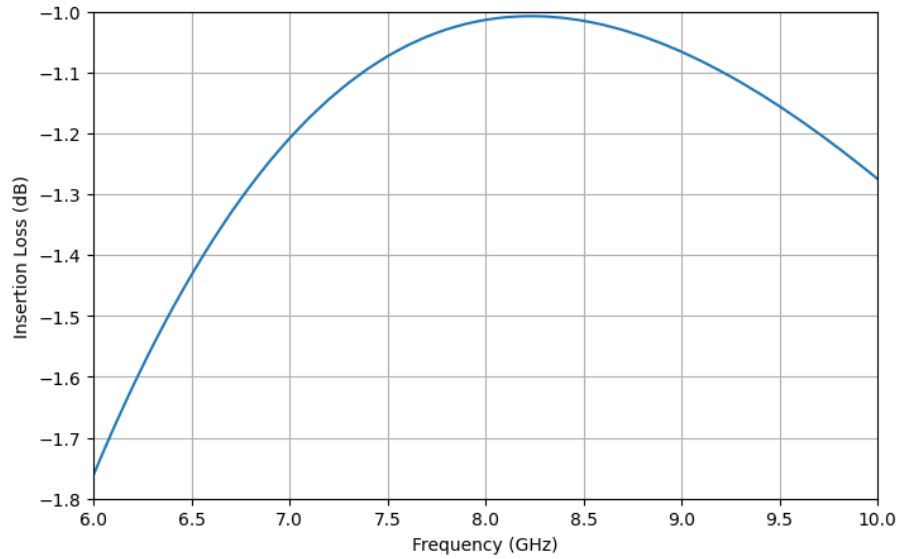



Figure 7.8: Insertion loss of the input balun including the matching capacitor $C_{m1}$

was ultimately removed, as its absence improved the gain, albeit with a slight reduction in the overall PAE.

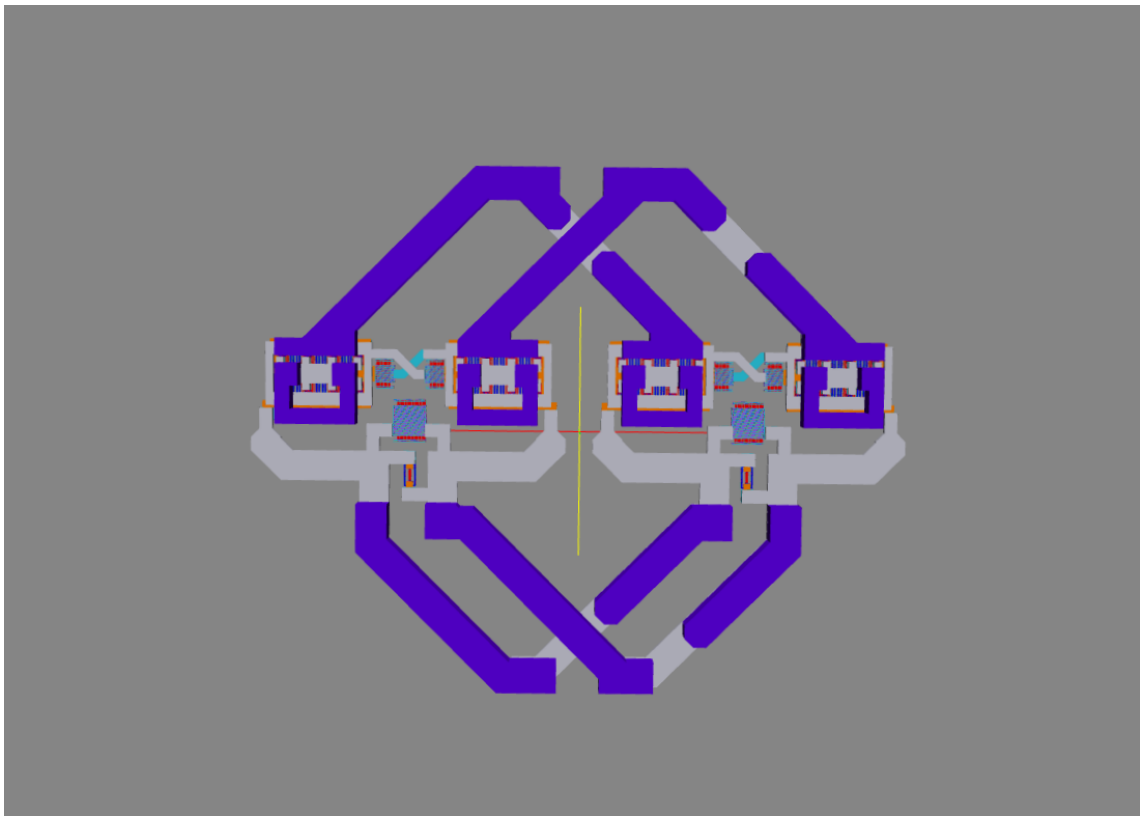


Figure 7.9: Driver stage layout

# Chapter 8

# Two Stage Power Amplifier

The design of the driver and power amplifier stages was completed, so it was time to evaluate the performance of the two-stage power amplifier.

## 8.1 Schematic Results

The schematic results of the final two-stage power amplifier are presented in Figures 8.1, 8.2 and 8.3, and are summarized in Table 8.1. It is evident that the output power was not affected by the insertion of the driver. At the same time, the gain increased significantly, while the PAE was slightly reduced and linearity also worsened.

Table 8.1: Summary of the two-stage power amplifier performance

| **Parameter** | **Value** |
|---|---|
| Supply Voltage | 2.4 V |
| Gain | 29.1 dB |
| Saturated Output Power ($P_{sat}$) | 23.22 dBm |
| 1 dB Compression Point ($OP_{1dB}$) | 22.19 dBm |
| PAE at 1 dB Compression Point ($PAE_{1dB}$) | 47.57% |
| Maximum PAE ($PAE_{max}$) | 47.81% |
| Difference Between $IIP_3$ and $IP_{1\text{dB}}$ | 4 dB |

## 8.2 Corners

Figures 8.4–8.6 illustrate the performance of the power amplifier stage under various process and temperature corners. Similarly to the power amplifier stage (Chapter 6.3.2), in some corners, the output power at the 1 dB compression point decreases while the gain increases. In others, the opposite occurs, and in some cases, the behavior remains close to the nominal. In the first case, the issue is addressed by reducing the gate biasing of both

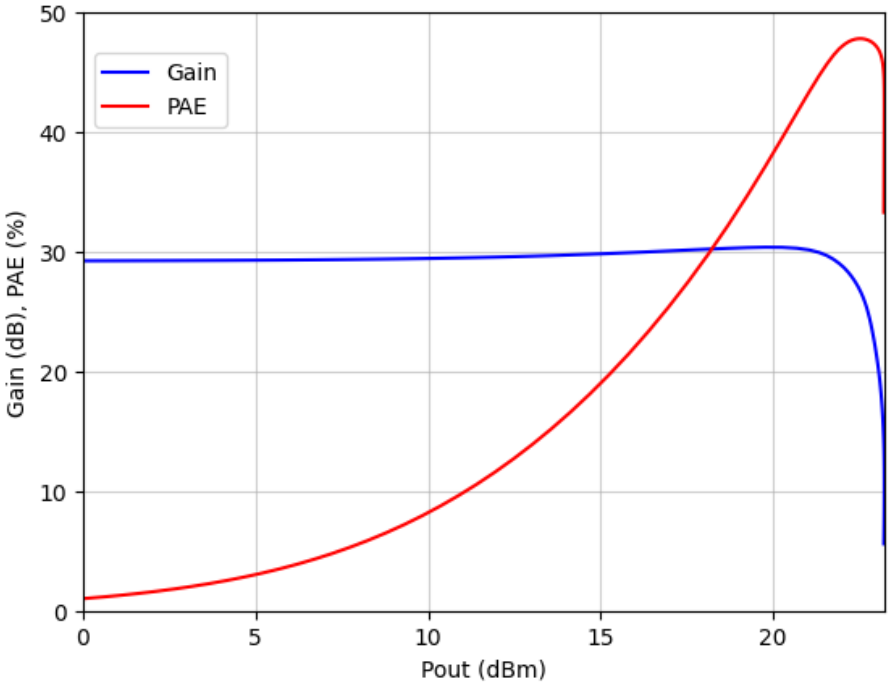



Figure 8.1: Gain and PAE versus output power of the two-stage power amplifier

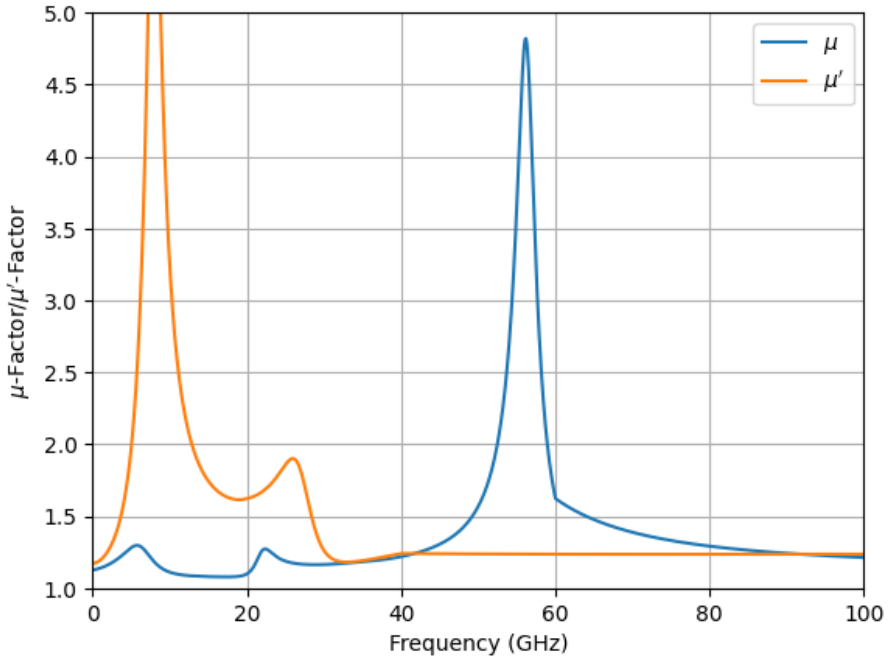



Figure 8.2: Stability factors $\mu$ and $\mu'$ of the two-stage power amplifier

stages, whereas in the second case, it is mitigated by applying a positive back-gate bias to both stages. Lastly, the two stage power amplifier is unconditionally stable in all corners.

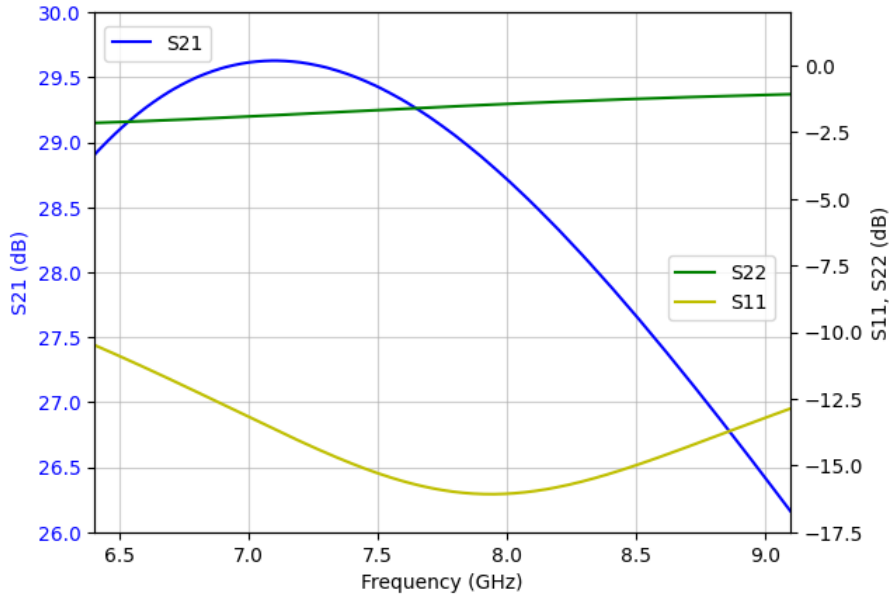



Figure 8.3: S-parameters of the two-stage power amplifier

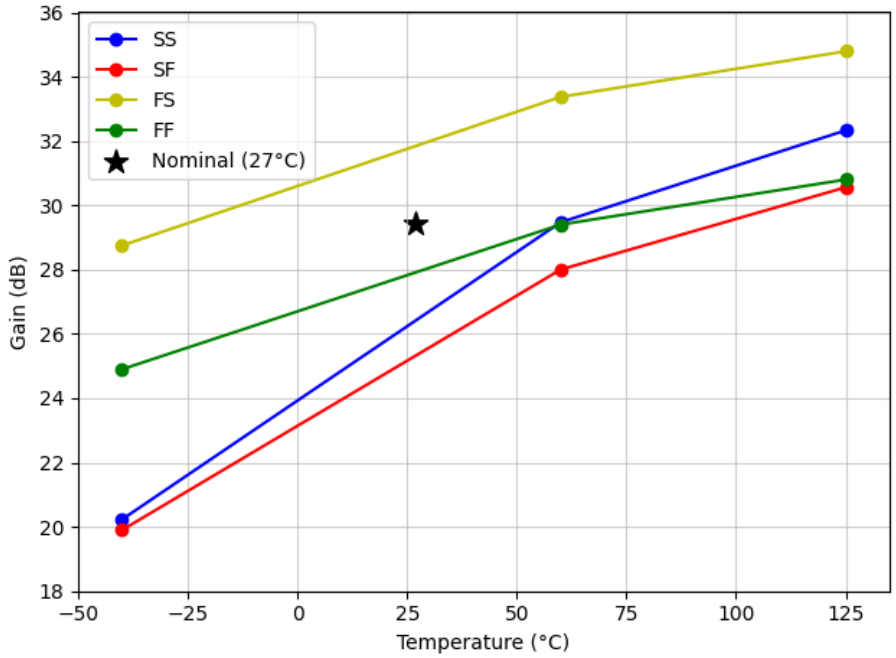



Figure 8.4: Gain performance across process and temperature corners for the two-stage power amplifier

## 8.3 Post Layout Results

The layout is shown in Figure 8.7. At each center tap of the baluns and the transformer, capacitors were added, with one terminal connected to the center tap and the other to ground. This was done to eliminate the inductance introduced by the center tap and thereby improve the overall performance of the circuit.

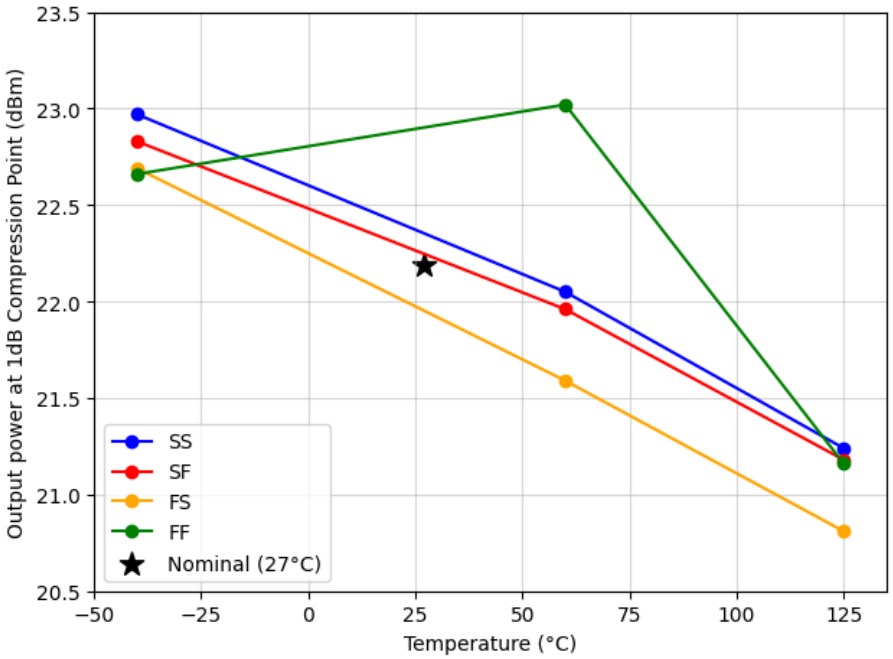



Figure 8.5: Output power at 1 dB compression point across process and temperature corners for the two-stage power amplifier

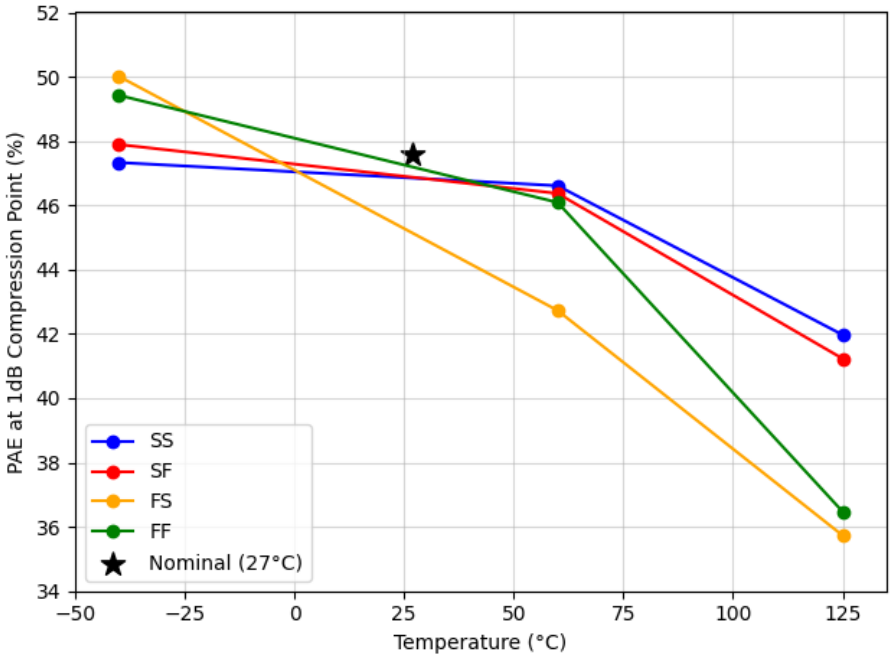



Figure 8.6: PAE at 1 dB compression point across process and temperature corners for the two-stage power amplifier

The post-layout results are presented in Figures 8.8, 8.9, and 8.10, and are summarized in Table 8.2, where they are compared against the schematic-level results. It is evident that the layout has slightly degraded the overall performance of the power amplifier stage in terms of gain, output power, and efficiency. However, the linearity has improved, as

indicated by the increased separation between the 1 dB compression point and the third-order intercept point.

Table 8.2: Comparison between schematic-level and post-layout simulation results

| **Parameter** | **Schematic** | **Layout** |
|---|---|---|
| Supply Voltage | 2.4 V | 2.4 V |
| Gain | 29.1 dB | 27.74 dB |
| Saturated Output Power ($P_{sat}$) | 23.22 dBm | 22.66 dBm |
| 1 dB Compression Point ($OP_{1\text{dB}}$) | 22.19 dBm | 21.26 dBm |
| PAE at 1 dB Compression Point ($PAE_{1\text{dB}}$) | 47.57% | 41.38% |
| Maximum PAE ($PAE_{\text{max}}$) | 47.81% | 41.76% |
| Difference Between $IIP_3$ and $OP_{1\text{dB}}$ | 4 dB | 7.55 dB |

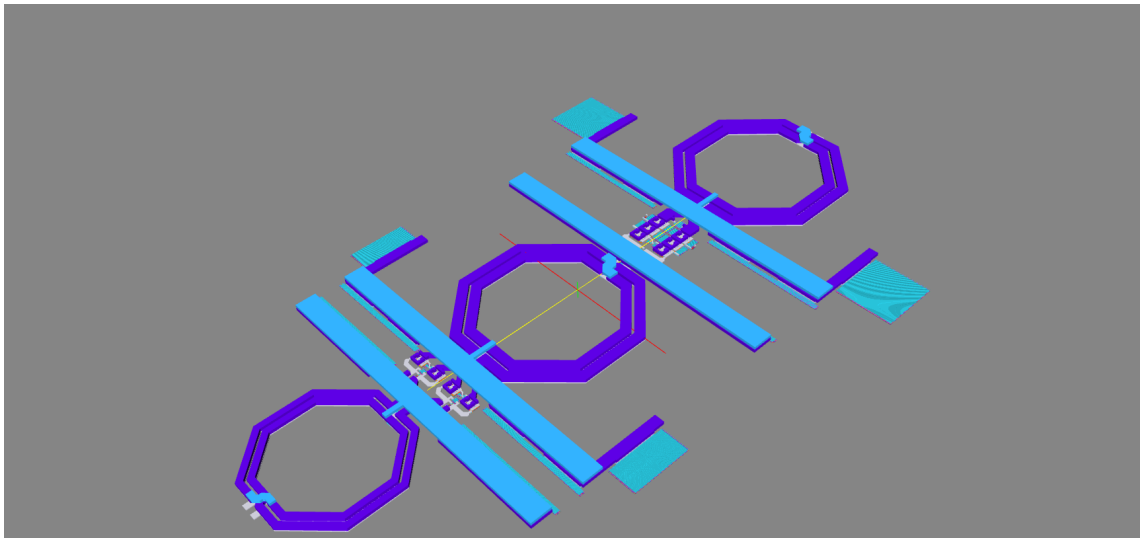


Figure 8.7: Layout of the complete two-stage power amplifier

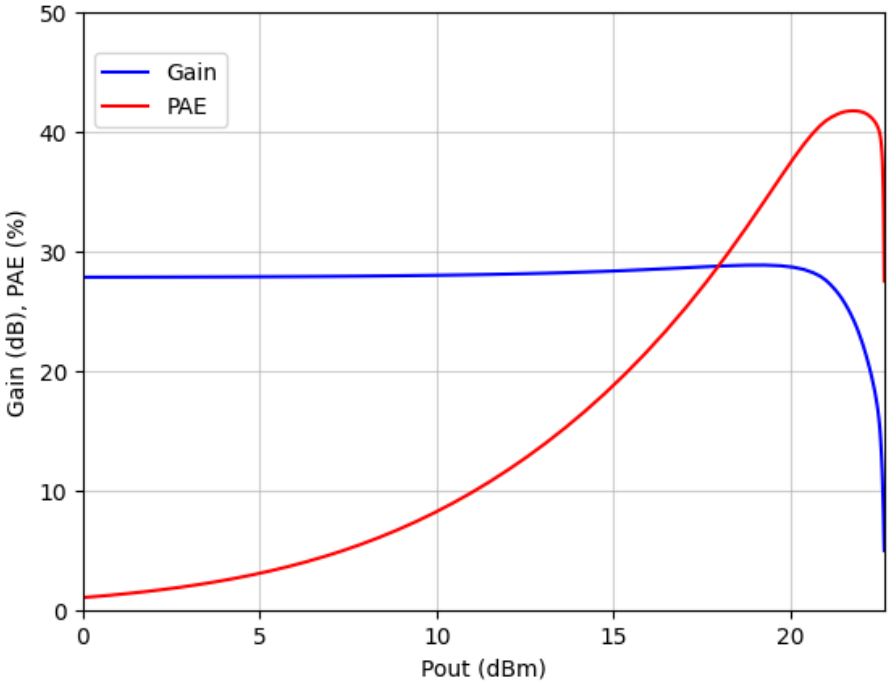



Figure 8.8: Post-layout gain and PAE versus output power of the two-stage power amplifier

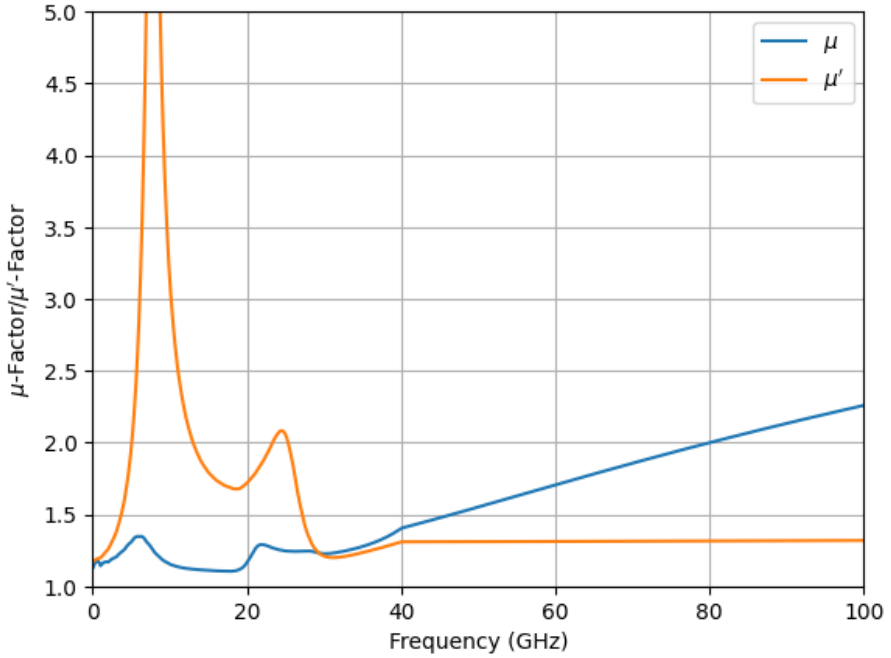



Figure 8.9: Post-layout stability factors $\mu$ and $\mu'$ of the two-stage power amplifier

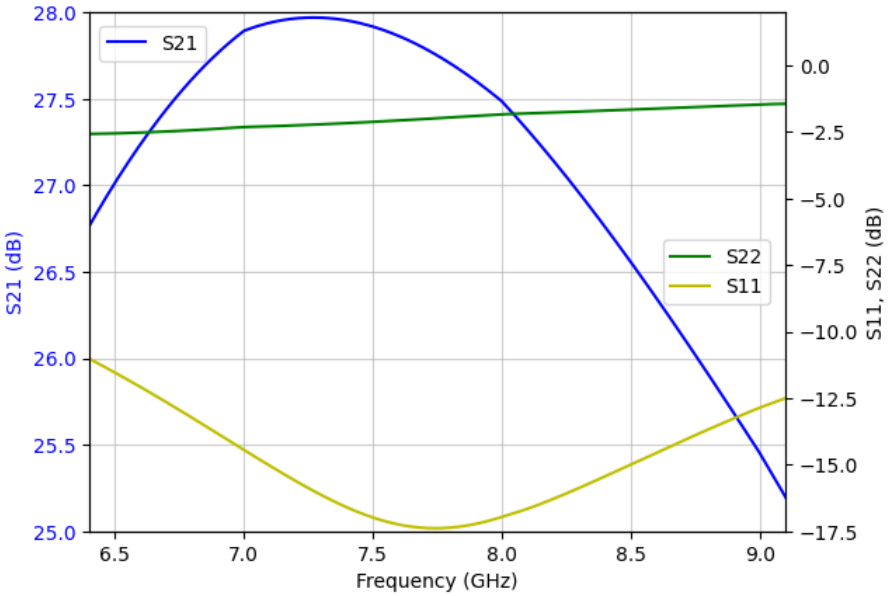



Figure 8.10: Post-layout S-parameters of the two-stage power amplifier

# Chapter 9

# Conclusions and Future Work

The power amplifier is one of the most critical stages in the transmitter of a telecommunication system. It is the most power-hungry block of the entire system and must deliver sufficiently high output power with high Power Added Efficiency (PAE) to ensure efficient power management. At the same time, the power amplifier must exhibit high gain so that the preceding stages can effectively drive it to its 1 dB compression point. Moreover, good linearity is essential to maintain high link quality and to support modern dense high-order modulation schemes with varying envelope signals, which are commonly used in contemporary digital communication systems.

In this work, the power amplifier was implemented in Class B operation, one of the four classical amplifier classes, which provides a balance between output power, gain, efficiency, and linearity. To address the limitations of modern silicon technologies—namely, the low nominal drain-source voltage ($V_{DS}$)—a differential power amplifier topology was adopted, utilizing stacked transistors. This approach enables sufficiently high output power while careful design choices ensured that both $V_{DS}$ and $V_{GD}$ remain below the breakdown voltages, maintaining device reliability. Furthermore, a driver was added to increase the gain.

Dense high-order modulation schemes with varying envelope signals demand excellent linearity. Therefore, the power amplifier is often required to operate under Power Back-Off (PBO) conditions—typically 3, 6, or even 9 dB below the 1 dB compression point. However, PAE tends to decrease significantly in back-off conditions. Consequently, the next research step is to develop a power amplifier architecture that improves efficiency during PBO. The most widely adopted technique for this purpose is the Doherty architecture. Nevertheless, exploring a broader range of ideas and experimenting with alternative amplifier classes beyond the conventional ones—such as Class J or Class F [4]—may lead to innovative solutions in power amplifier design.

# Appendix A

# Transformers

Integrated transformers are particularly useful, as they can be employed for impedance matching, AC coupling, and for converting single-ended to differential signals and vice versa. However, their design and the development of accurate equivalent models can be quite challenging.

A well-designed transformer is characterized by a high coupling coefficient, low capacitive coupling between the primary and secondary windings, low series resistance on both the primary and secondary sides, and minimal capacitive coupling to the substrate.

## A.1 Simplified Transformer Equivalent Circuit

In Figure A.1, a simplified transformer equivalent circuit is presented, where $C_F$ denotes the coupling capacitance between the primary and secondary windings [6]. The input and output equations are:

$$V_{in} = L_1 s I_1 + M s I_2 \tag{1}$$

$$V_{out} = M s I_1 + L_2 s I_2 \tag{2}$$

Applying Kirchhoff's current law at the output node:

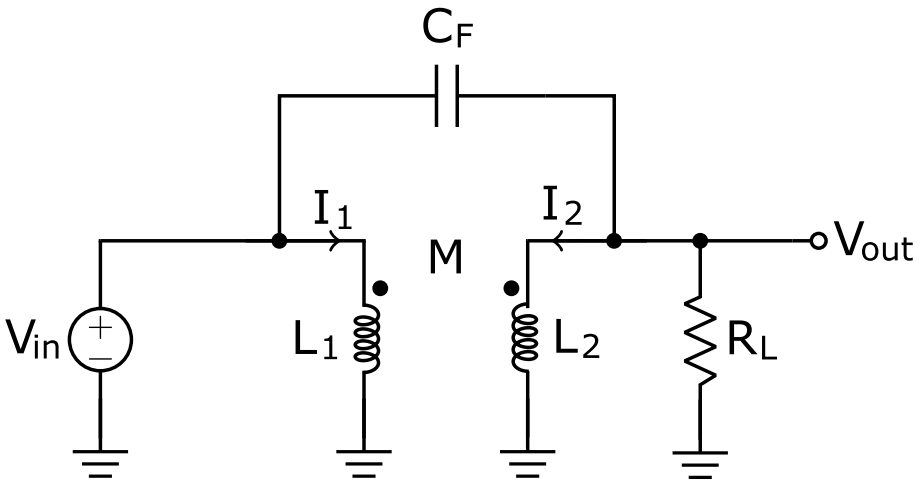



Figure A.1: Simplified transformer equivalent circuit

$$(V_{in} - V_{out})sC_F = \frac{V_{out}}{R_L} + I_2 \tag{3}$$

Solving for $I_2$ from the above equations and substituting into the previous equation yields:

$$\frac{V_{out}}{V_{in}} = \frac{L_1L_2\left(1 - \frac{M^2}{L_1L_2}\right)s^2C_F + M}{L_1L_2\left(1 - \frac{M^2}{L_1L_2}\right)s^2C_F + \frac{L_1L_2}{R_L}\left(1 - \frac{M^2}{L_1L_2}\right)s + L_1} \tag{4}$$

In the special case where $C_F = 0$, this reduces to:

$$\frac{V_{out}}{V_{in}} = \frac{M}{\frac{L_1L_2}{R_L}\left(1 - \frac{M^2}{L_1L_2}\right)s + L_1} \tag{5}$$

This shows that, assuming the coupling factor $k = \frac{M}{\sqrt{L_1L_2}}$ is less than 1, the transfer function behaves as a low-pass filter with a real pole at the frequency:

$$\omega_p = \frac{-R_L}{L_2\left(1 - \frac{M^2}{L_1L_2}\right)} \tag{6}$$

The input impedance $Z_{in}$ is given by:

$$Z_{in} = L_1s - \frac{M^2s^2}{R_L + L_2s} \tag{7}$$

Thus, inductance values must be chosen to ensure the input impedance is appropriate in the desired frequency range.

The coupling capacitance $C_F$ between the primary and secondary windings has an opposite effect to that of magnetic coupling. This is evident when writing the numerator of equation (4) as $s = j\omega$:

$$N(j\omega) = -L_1L_2\left(1 - \frac{M^2}{L_1L_2}\right)C_F\omega^2 + M \tag{8}$$

If $M$ is positive, the numerator becomes zero at frequency:

$$\omega_z = \sqrt{\frac{M}{L_1L_2\left(1 - \frac{M^2}{L_1L_2}\right)C_F}} \tag{9}$$

This means that a notch appears at this frequency. However, if $M$ is negative, the notch may appear at very high frequencies, and the transformer behaves as non-resonant in practical ranges. Thus, inverting transformers operate at higher frequencies compared to non-inverting ones.

Transformers can be implemented using one or more metal layers. Typically, they are realized in two or three layers. Multi-level transformers offer the following advantages over planar ones:

- Smaller overall area
- Better magnetic coupling due to precise alignment of the two windings
- It is easier to achieve a turns ratio greater than one between primary and secondary

- Multiple secondary windings can be implemented to realize combiners

However, they also have some disadvantages:

- Metal traces on lower layers have higher sheet resistance due to thinner metal thickness
- Capacitance between the lower metal layers and the substrate is higher
- Capacitance between primary and secondary windings is increased

The inductance Lp of the primary and the inductance Ls of the secondary, along with the quality factors Qp and Qs and the coupling factor of a real transformer simulated in a electromagnetics computational solver can be determined from Z-parameters as follows:

$$L_p = \frac{\mathrm{Im}(Z_{11})}{\omega} \tag{10}$$

$$L_s = \frac{\mathrm{Im}(Z_{22})}{\omega} \tag{11}$$

$$Q_p = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \tag{12}$$

$$Q_s = \frac{\mathrm{Im}(Z_{22})}{\mathrm{Re}(Z_{22})} \tag{13}$$

$$k = \frac{\mathrm{Im}(Z_{12})}{\sqrt{\mathrm{Im}(Z_{11})\,\mathrm{Im}(Z_{22})}} \tag{14}$$

## A.2 Output Balun and Interstage Transformer

The balun is a type of transformer where one of the two terminals at the input or output is connected to ground. In other words, the balun converts a single-ended signal into a differential one. The output balun and the interstage transformer used in the two-stage power amplifier are exactly the same components. Their characteristics versus frequency are shown in Figures A.2–A.5.

## A.3 Input Balun

The characteristics of the input balun used in the two-stage power amplifier versus frequency are shown in Figures A.6–A.9.

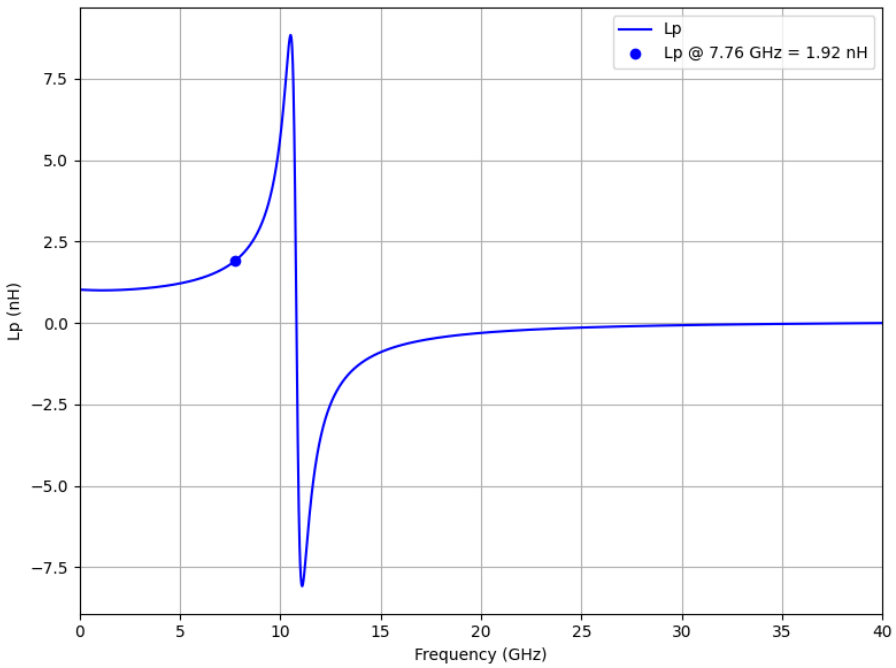



Figure A.2: Primary Inductance ($L_p$) versus frequency for the output balun

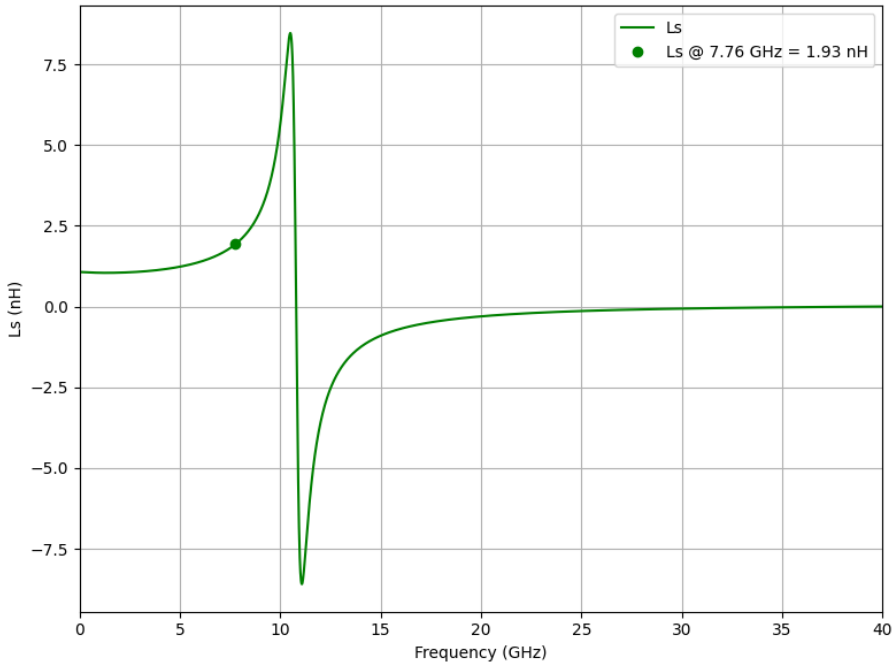



Figure A.3: Secondary Inductance ($L_s$) versus frequency for the output balun

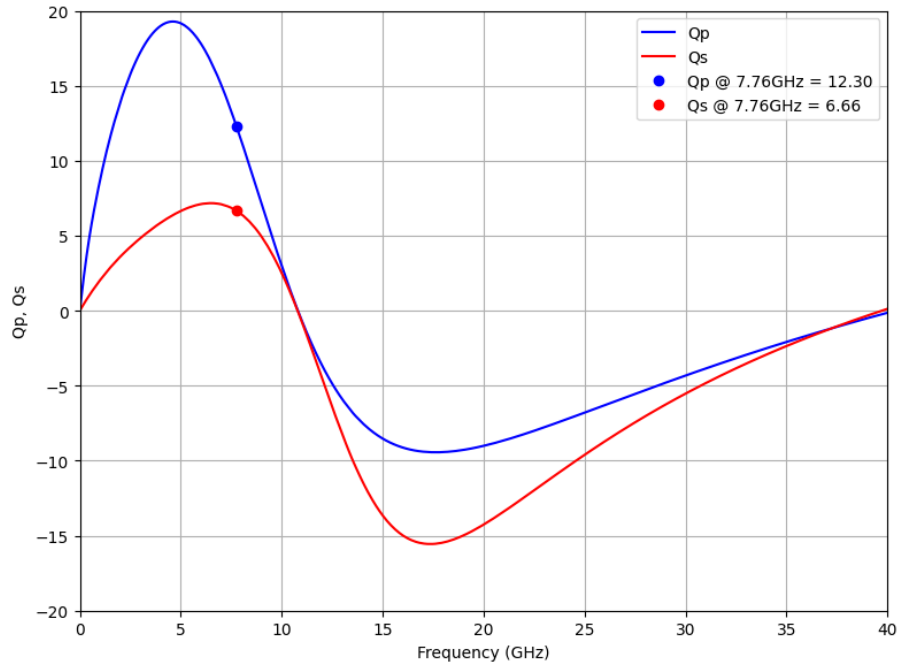



Figure A.4: Quality Factors ($Q_p$, $Q_s$) versus frequency for the output balun

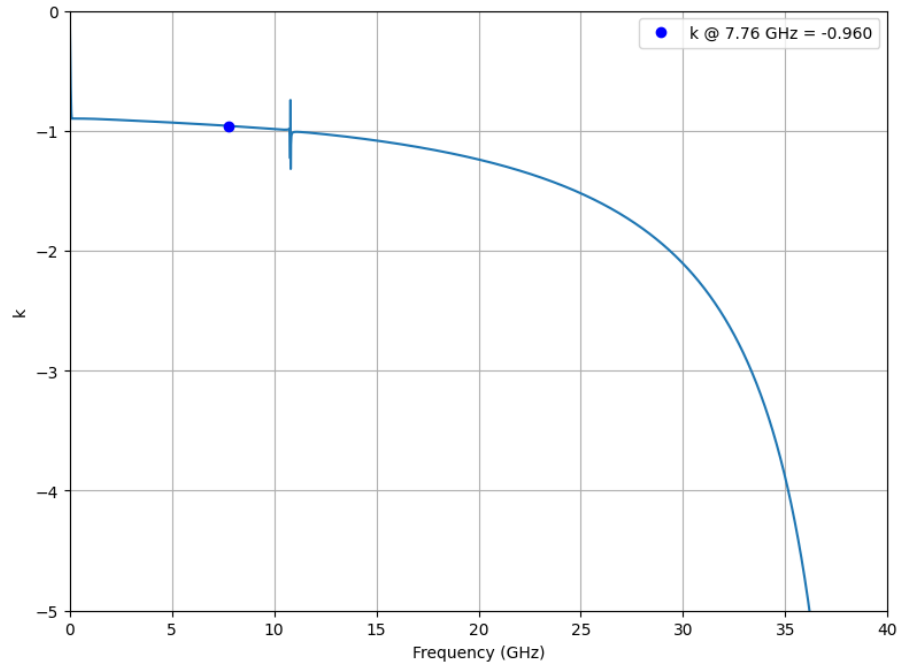



Figure A.5: Coupling Factor ($k$) versus frequency for the output balun

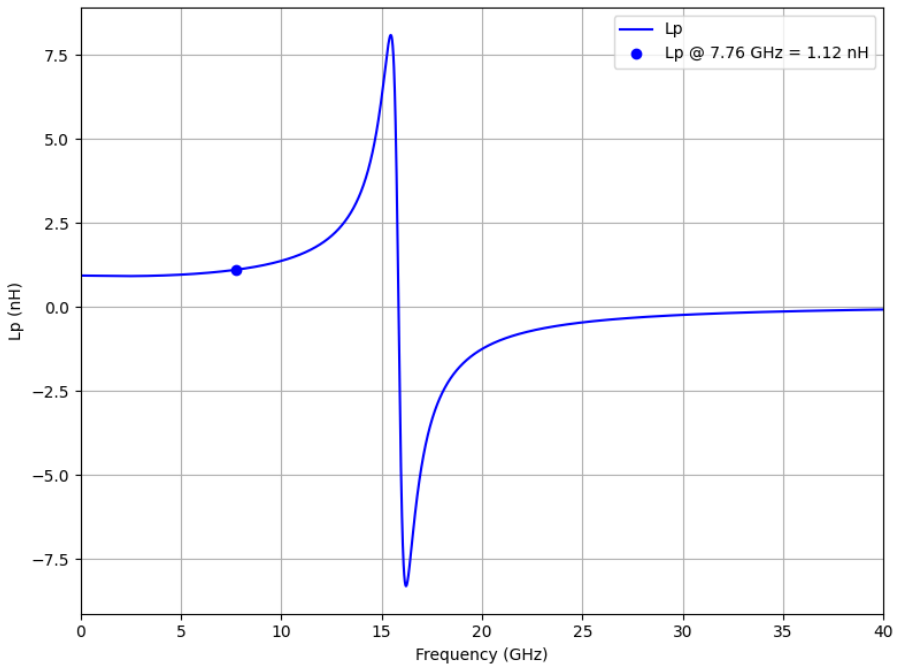



Figure A.6: Primary Inductance ($L_p$) versus frequency for the input balun

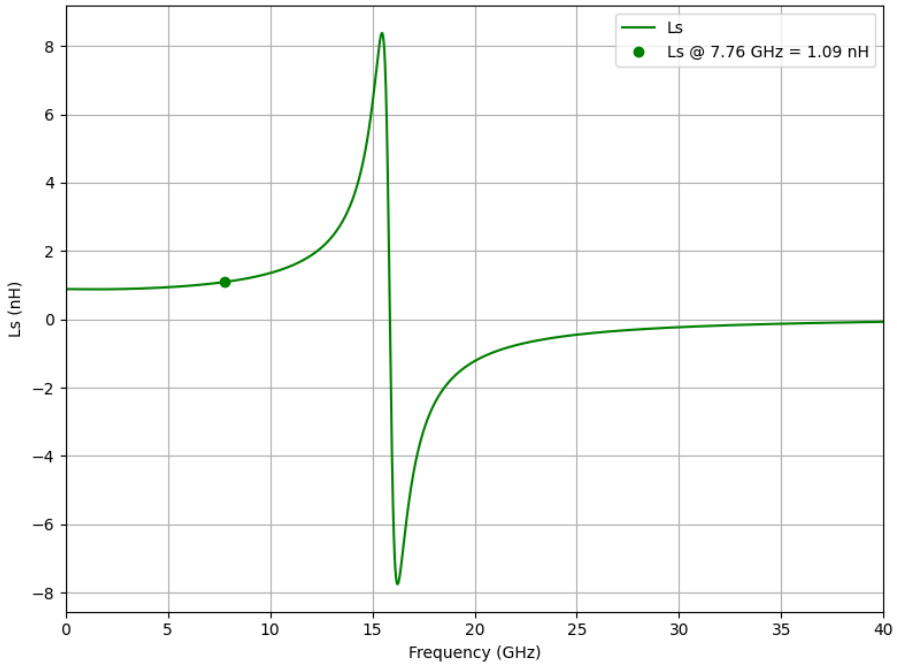



Figure A.7: Secondary Inductance ($L_s$) versus frequency for the input balun

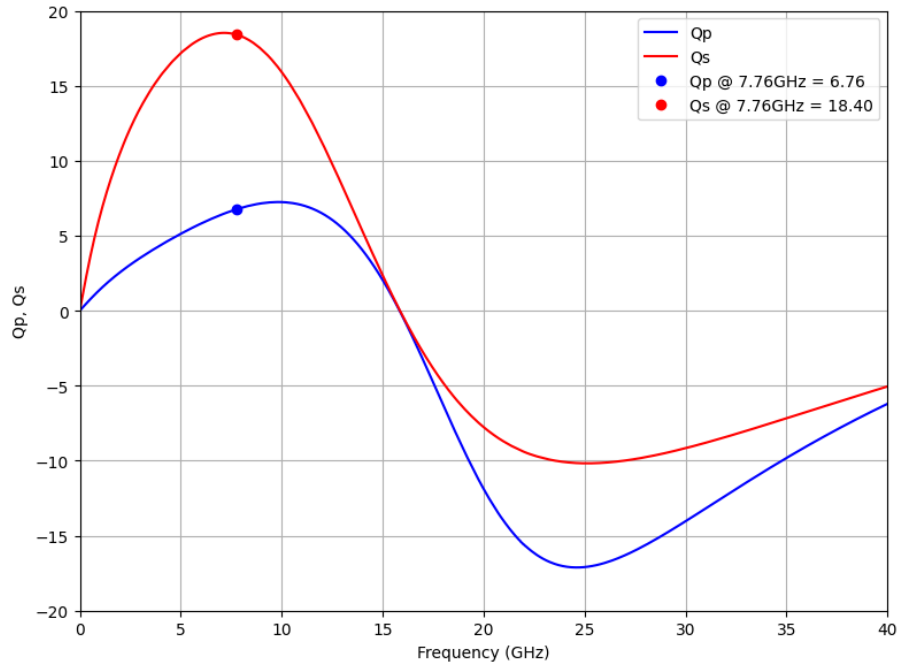



Figure A.8: Quality Factors ($Q_p$, $Q_s$) versus frequency for the input balun

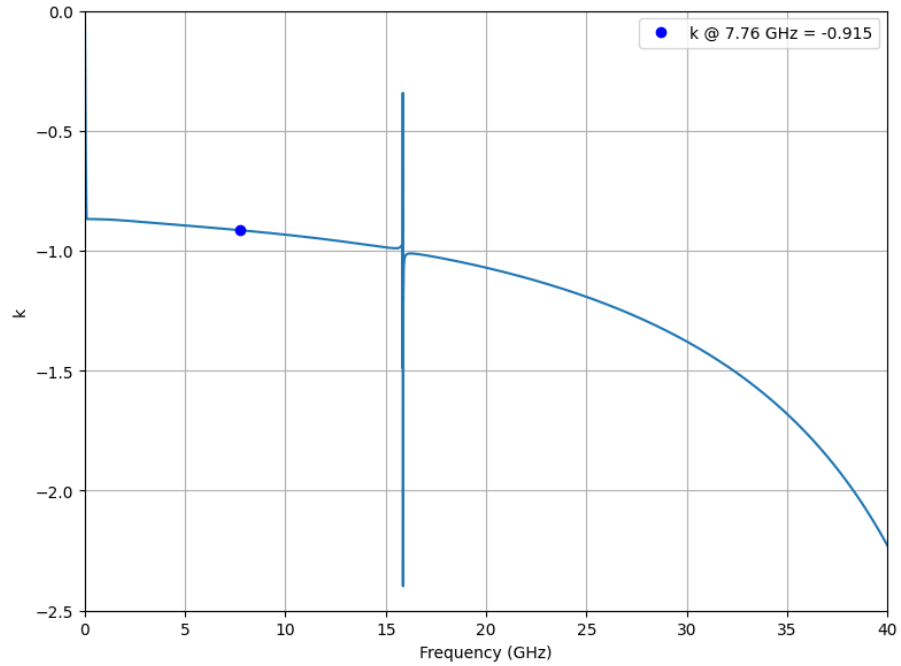



Figure A.9: Coupling Factor ($k$) versus frequency for the input balun

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