National Technical University of Athens

School of Electrical and Computer Engineering

Division of Communication, Electronic and Information Engineering
Laboratory of Electronics

Design and implementation of a low noise amplifier operating in the 7-8.4 GHz frequency band for 5G/6G applications using a 22 nm CMOS FD-SOI process

DIPLOMA THESIS

of

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Εθνικο Μετσοβιο Πολυτεχνειο
ΤΜΗΜΑ ΗΛΕΚΤΡΟΛΟΓΩΝ ΜΗΧΑΝΙΚΩΝ ΚΑΙ
ΜΗΧΑΝΙΚΩΝ ΥΠΟΛΟΓΙΣΤΩΝ
Τομέας Επικοινωνιών, Ηλεκτρονικής και Συστημάτων
Πληροφορικής
Εργαστήριο Ηλεκτρονικής

Σχεδίαση και υλοποίηση ενισχυτή χαμηλού θορύβου στη ζώνη συχνοτήτων 7-8.4 GHz για εφαρμογές 5G/6G σε τεχνολογία 22nm CMOS FD-SOI

ΔΙΠΛΩΜΑΤΙΚΗ ΕΡΓΑΣΙΑ

του

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Περίληψη

Η παρούσα διπλωματική εργασία παρουσιάζει τη σχεδίαση και την υλοποίηση ενός ενισχυτή χαμηλού θορύβου που λειτουργεί στη ζώνη συχνοτήτων $7 - 8.4$GHz, με στόχο εφαρμογές ασύρματης επικοινωνίας 5ης και 6ης γενιάς (5G και 6G). Ο ενισχυτής σχεδιάστηκε χρησιμοποιώντας το PDK της τεχνολογίας $22\,nm$ CMOS FD-SOI της GlobalFoundries, η οποία υπόσχεται υψηλή απόδοση με μειωμένη κατανάλωση ισχύος. Η διαδικασία σχεδίασης περιλάμβανε τη σχεδίαση σε επίπεδο σχηματικού, τη φυσική σχεδίαση της διάταξης (layout) και την επαλήθευση της ορθής λειτουργίας με προσομοιώσεις μετά τη φυσική σχεδίαση (post-layout simulations). Ιδιαίτερη έμφαση δόθηκε στην ακριβή μοντελοποίηση παθητικών στοιχείων και παρασιτικών φαινομένων. Για παράδειγμα, μοντελοποιήθηκαν πηνία, μετασχηματιστες, bondwires και pads, μέσω ηλεκτρομαγνητικών προσομοιώσεων. Η ροή της σχεδίασης παρουσιάζεται και συνοδεύεται από θεωρητικό υπόβαθρο, αποτελέσματα προσομοιώσεων και σχόλια για την απόδοση, με στόχο το κείμενο αυτό να αποτελέσει ένα πρακτικό εγχειρίδιο για μελλοντικούς φοιτητές που ασχολούνται με τον σχεδιασμό ενισχυτών χαμηλού θορύβου σε τεχνολογίες CMOS. Η εργασία γράφτηκε στα Αγγλικά με στόχο να μπορεί να αξιοποιηθεί από μεγαλύτερο κοινό. Εκτεταμένη περίληψή της στα Ελληνικά παρατίθεται στη συνέχεια.

Λέξεις κλειδιά: Ενισχυτής Χαμηλού Θορύβου (LNA), Σχεδίαση Ολοκληρωμένων Κυκλωμάτων Ραδιοσυχνοτήτων, Ασύρματες Επικοινωνίες 5G, Ασύρματες Επικοινωνίες 6G, Ολοκληρωμένα Κυκλώματα CMOS, Ενισχυτές Υψηλών Συχνοτήτων, Συντελεστής Θορύβου, Ηλεκτρομαγνητική Προσομοίωση, Μοντελοποίηση Παθητικών Στοιχείων

Abstract

This thesis presents the design and implementation of a low noise amplifier operating in the $7 - 8.4$GHz frequency band, targeting 5G and 6G wireless communication applications. The low noise amplifier was designed using the PDK of GlobalFoundries $22\,nm$ CMOS FD-SOI process, which promises high performance with reduced power consumption. The design process included schematic level development, layout implementation, and post-layout verification. Particular emphasis was placed on the accurate modeling of passive components and parasitics. For example, inductors, transformers, bondwires, and pads, were modeled using electromagnetic simulations. The design flow is documented, accompanied by theoretical foundations, simulation results and comments on performance, with the aim of providing future students with a practical reference guide for LNA design in CMOS technologies. This thesis was written in English in order to be useful to a wider audience. A comprehensive summary in Greek follows.

Keywords: Low Noise Amplifier (LNA), RF IC Design, 5G Wireless Communications, 6G Wireless Communications, CMOS Integrated Circuits, High-Frequency Amplifiers, Noise Figure, Electromagnetic Simulation, Passive Component Modeling

Ευχαριστίες

Με την παρούσα εργασία ολοκληρώνονται οι πενταετείς σπουδές μου στη σχολή Ηλεκτρολόγων Μηχανικών και Μηχανικών Υπολογιστών του Εθνικού Μετσοβίου Πολυτεχνείου. Οι σπουδές αυτές αποτελούν εξαιρετικά σημαντικό κεφάλαιο της ζωής μου λόγω των γνώσεων, των εμπειριών και των ικανοτήτων που απέκτησα, καθώς και των ευκαιριών για το μέλλον που μου πρόσφεραν. Προτού συνεχίσω την ακαδημαϊκή μου πορεία σαν υποψήφιος διδάκτορας στις Ηνωμένες Πολιτείες της Αμερικής, θα ήθελα να ευχαριστήσω θερμά όλους όσους συνέβαλαν στην ακαδημαϊκή και ερευνητική μου πορεία έως τώρα.

Αρχικά, ευχαριστώ όλους τους διδάσκοντες της Σχολής Ηλεκτρολόγων Μηχανικών και Μηχανικών Υπολογιστών των οποίων μαθήματα παρακολούθησα για τη μετάδοση πολύτιμων γνώσεων και για τη διαρκή στήριξη κατά τη διάρκεια των σπουδών μου. Ιδιαίτερες ευχαριστίες οφείλω στον επιβλέποντα καθηγητή μου, τον κύριο Παπανάνο, για την καθοδήγησή του και τις συμβουλές του με τις οποίες μου μετέδωσε τμήμα από τη μεγάλη εμπειρία του στη βιομηχανία, αλλά και στον ακαδημαϊκό τομέα. Εύχομαι η ερχόμενη συνταξιοδότησή του να είναι ευχάριστη, αλλά και να συνεχίσει να είναι παρών δυναμικά στο Εργαστήριο Ηλεκτρονικής, εφόσον και ο ίδιος το θέλει, καθώς η απουσία του θα είναι σίγουρα μεγάλη απώλεια.

Ιδιαίτερες ευχαριστίες οφείλω και στα άλλα δύο μέλη της τριμελούς επιτροπής μου, η οποία καθόλου τυχαία δεν επιλέχθηκε. Ευχαριστώ πολύ τον κύριο Παναγόπουλο για τις συμβουλές και τη γνώση που μου προσέφερε κατά τη διάρκεια των συζητήσεών μας είτε σχετικά με τη διπλωματική μου, με μαθήματα που διδάσκει και παρακολούθησα, ή με ερευνητικά και βιομηχανικά θέματα. Εύχομαι να έχει καλή συνέχεια στη νέα του καριέρα στο Εθνικό Μετσόβιο Πολυτεχνείο και ελπίζω να μου δοθεί η ευκαιρία να συνεργαστούμε ξανά στο μέλλον.

Φυσικά δε θα μπορούσα να μην ευχαριστήσω θερμά τον κύριο Σούντρη που, όπως σχολιάζει συχνά και ο ίδιος, παρακολούθησα μόνο ένα μάθημά του για ένα εξάμηνο, αλλά έχουμε κάνει αμέτρητες συζητήσεις μαζί κατά τη διάρκεια των εξαμήνων που ακολούθησαν. Οι συμβουλές του και η καθοδήγησή του σε προσωπικό επίπεδο συντέλεσαν σημαντικά στο ότι κατάφερα να εξασφαλίσω μεταπτυχιακές σπουδές στις Ηνωμένες Πολιτείες. Επίσης, τον ευχαριστώ που ανέχτηκε τα διαρκή παράπονά μου κατά την περίοδο των αιτήσεων για θέσεις διδακτορικού, καθώς και που μου ανέδειξε έμπρακτα τη σημασία των κοινωνικών και των διοικητικών δεξιοτήτων στον τομέα μας. Εύχομαι και σε εκείνον καλή συνέχεια και να εξακολουθεί να έχει την όρεξη να γίνεται μέντορας των φοιτητών, διότι το χρειάζονται.

Ευχαριστώ επίσης τα μέλη του τομέα Ηλεκτρομαγνητικών Εφαρμογών Ηλεκτροοπτικής και Ηλεκτρονικών Υλικών, διότι συνεργαστήκαμε στενά και με καθοδήγησαν πολλές φορές κατά τη διάρκεια των σπουδών μου. Παρότι δεν εκπόνησα τη διπλωματική μου σε εκείνον τον τομέα οι γνώσεις που μου μετέδωσαν είναι θεμελιώδεις και εφαρμόζονται κατά κόρον στο αντικείμενο με το οποίο εν τέλει επέλεξα να ασχοληθώ. Ο Δρ. Γρηγόριος Ζούρος προσφέρθηκε να με εισαγάγει στην επιστημονική έρευνα και καταλήξαμε να δημοσιεύσουμε μαζί δύο εργασίες οι οποίες σίγουρα συνέβαλαν καθοριστικά στην αποδοχή μου για διδακτορικές σπουδές και τον ευχαριστώ θερμά.

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Gkrimpogiannis Georgios
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Κεφάλαιο 1

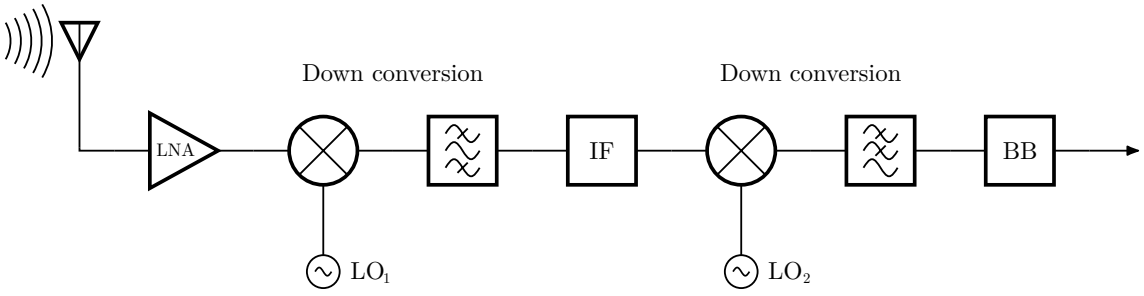
Εκτεταμένη περίληψη στα Ελληνικά

1.1 Εισαγωγή

Οι τηλεπικοινωνίες αποτελούν θεμέλιο λίθο της σύγχρονης κοινωνίας, επιτρέποντας την ανταλλαγή πληροφοριών σε μεγάλες αποστάσεις χωρίς την ανάγκη φυσικής επαφής. Η εξέλιξη των τεχνολογιών μετάδοσης έχει οδηγήσει από τα πρώτα αναλογικά σήματα σε σύγχρονα ψηφιακά συστήματα, με τη χρήση ηλεκτρομαγνητικών κυμάτων για μετάδοση της πληροφορίας να παίζει καθοριστικό ρόλο.

Η συνεχής αύξηση των απαιτήσεων για υψηλές ταχύτητες μετάδοσης δεδομένων και η ανάγκη για αξιόπιστη ασύρματη επικοινωνία οδήγησαν στην ανάπτυξη των δικτύων πέμπτης και έκτης γενιάς (5G/6G). Η τεχνολογία των δικτύων αυτών λειτουργεί σε υψηλές συχνότητες όπως η πρόσφατα προτεινόμενη ζώνη $7.125 - 8.4\,\text{GHz}$, η οποία θεωρείται πολλά υποσχόμενη για την υλοποίηση εφαρμογών δικτύων έκτης γενιάς. Η λειτουργία σε τόσο υψηλές συχνότητες συνεπάγεται σημαντικές προκλήσεις, όπως αυξημένες απώλειες διάδοσης και περιορισμένη εμβέλεια, γεγονός που απαιτεί πυκνότερη δικτύωση και βελτιστοποιημένο σχεδιασμό συστημάτων.

Σε κάθε ασύρματο δέκτη βρίσκεται το κύκλωμα του ενισχυτή χαμηλού θορύβους (Low Noise Amplifier - LNA), το οποίο ενισχύει τα αδύναμα σήματα που λαμβάνονται από την κεραία, προσθέτοντας τον ελάχιστο δυνατό θόρυβο. Η επίδοση του ενισχυτή χαμηλού θορύβου ως προς τον θόρυβο επηρεάζει καθοριστικά τον συντελεστή θορύβου του δέκτη, καθιστώντας τον σχεδιασμό του κρίσιμο.



Σχήμα 1.1: Τυπική αλυσίδα δέκτη

$$F_{\text{δέκτη}} = F_{\text{LNA}} + \frac{F_{\text{υπολοίπων}}}{G_{\text{LNA}}} \tag{1.1}$$

Στην παρούσα διπλωματική εργασία εξετάζεται ο σχεδιασμός ενός ενισχυτή χαμηλού θορύβου που λειτουργεί στη συχνότητα 7.7 GHz, κοντά στο κέντρο της ζώνης $7.125 - 8.4$ GHz, με στόχο την επίτευξη υψηλής επίδοσης συμβαδίζοντας με τις απαιτήσεις των σύγχρονων και μελλοντικών ασύρματων επικοινωνιών.

1.2 Προδιαγραφές

Η σχεδίαση ενός ενισχυτή χαμηλού θορύβου βασίζεται σε συγκεκριμένες προδιαγραφές που εξασφαλίζουν τη βέλτιστη λειτουργία του στην επιλεγμένη συχνότητα λειτουργίας. Ιδιαίτερη έμφαση δίνεται στον συντελεστή θορύβου, στο κέρδος, καθώς και στη σωστή προσαρμογή εισόδου και εξόδου για τη μέγιστη μεταφορά ισχύος. Επιπλέον, λαμβάνονται υπόψη παράμετροι όπως η ευστάθεια, η γραμμικότητα και η κατανάλωση ισχύος, προκειμένου να ανταποκρίνεται στις απαιτήσεις σύγχρονων συστημάτων. Για τη συγκεκριμένη διπλωματική αξιοποιήθηκαν στοιχεία από τη βιβλιογραφία για την αξιολόγηση επιδόσεων.

Εργασία	**Τεχνολογία**	**Frequency (GHz)**	**Gain (dB)**	**NF (dB)**
Gholami [1]	22nm FD-SOI	16–21.2	20	3.3
Ouyang [2]	22nm FD-SOI	17.8–42.4	18.3	2.9–4.9
Fu [3]	22nm FD-SOI	23.3-30.3 / 38-44.7	22 / 16	2.55 / 4.75
Xu [4]	22nm FD-SOI	60	20	3.3
Spasaro [5]	22nm FD-SOI	30	8-18	6-7
Cui [6]	22nm FD-SOI	22–32	21.5	1.7 - 2.2
Mousavi [7]	180nm CMOS	3-8	18.7	3.7
Han [8]	45nm SOI	17-38	23	4

Πίνακας 1.1: Επισκόπηση σύγχρονων σχεδιάσεων LNA σε νανομετρικές τεχνολογίες CMOS: τεχνολογία, συχνότητα, κέρδος, εικόνα θορύβου

Εργασία	**Ποωερ (mW)**	**IP1dB / IIP3 (dBm)**	**S11 / S22 (dB)**
Gholami [1]	15	-20 / –	-10 / -10
Ouyang [2]	15.8	-17.9 / -8.5	-10 / -10
Fu [3]	18	-17.2 – -30.6 / -10.3 – -21.6	-10 / -10
Xu [4]	8.1	-29.3 / –	-20 / -20
Spasaro [5]	0.52	-25.5 / -15	-20 / -20
Cui [6]	17.3	– / -13.4	-10 / -10
Mousavi [7]	14.6	– / -9.5	-10 / –
Han [8]	59	– / –	-10 / –

Πίνακας 1.2: Επισκόπηση σύγχρονων σχεδιάσεων LNA σε νανομετρικές τεχνολογίες CMOS: κατανάλωση ισχύος και γραμμικότητα

1.3 Σχεδίαση σχηματικού

Δεδομένου ότι στόχος ήταν η μέγιστη δυνατή επίδοση, επιλέχθηκε η κασκοδική τοπολογία. Για την επίτευξη βέλτιστης συμπεριφοράς σε θόρυβο και γραμμικότητα, ακολουθήθηκε μία προσέγγιση δύο σταδίων, όπως φαίνεται στο σχήμα 1.2. Το πρώτο στάδιο αποτελείται από κασκοδική συνδεσμολογία μονής εισόδου και εξόδου, βελτιστοποιημένη για χαμηλό θόρυβο με επαρκές κέρδος ώστε να καταστείλει τον θόρυβο του δεύτερου σταδίου. Το δεύτερο στάδιο είναι διαφορικό κασκοδικό, σχεδιασμένο να πετύχει καλή γραμμικότητα καταστέλλοντας αρμονικές άρτιας τάξης λόγω της διαφορικής λειτουργίας του. Η μετάβαση από μονή σε διαφορική λειτουργία και αντίστροφα επιτυγχάνεται με τη χρήση balancing units (baluns), τα οποία υλοποιούνται με ολοκληρωμένους μετασχηματιστές.

Σημειώνεται ότι ακόμα και σε σχηματικό επίπεδο πολλά κομμάτια του κυκλώματος προσομοιώθηκαν ηλεκτρομαγνητικά και χρησιμοποιήθηκαν μοντέλα με ρεαλιστική συμπεριφορά για όλα τα στοιχεία. Στο σχηματικό δε συμπεριλήφθηκαν μόνο οι διασυνδέσεις. Ακολουθήθηκε η παρακάτω πορεία σχεδίασης.

Γενικά βήματα:

- Μελέτη transistors: θόρυβος, κέρδος.
- Μελέτη επαγωγέων: ηλεκτρομαγνητική προσομοίωση, επαλήθευση μοντέλων.

Σχεδίαση πρώτου σταδίου:

- Πόλωση για βέλτιστη λειτουργία ως προς τον θόρυβο και επαρκές κέρδος.
- Προσαρμογή εισόδου και προσαρμογή θορύβου.

Σχεδίαση δευτέρου σταδίου:

- Πόλωση για καλή συμπεριφορά ως προς τη γραμμικότητα.
- Προσαρμογή εξόδου.

Προσαρμογή μεταξύ σταδίων:

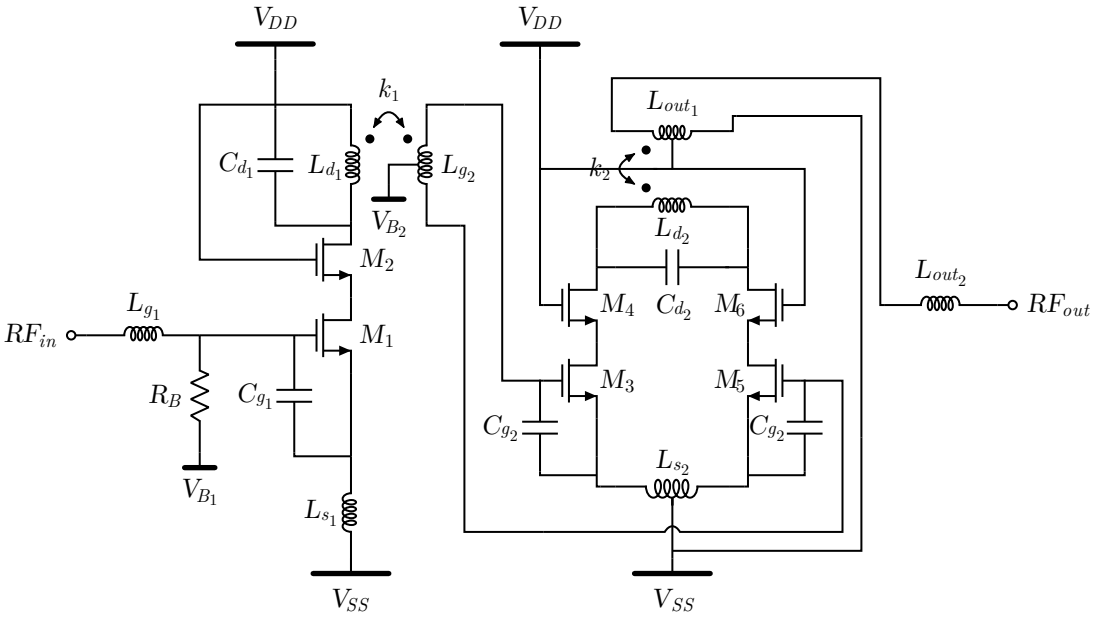
- Μελέτη μετασχηματιστών: ηλεκτρομαγνητική προσομοίωση.
- Ρύθμιση εμπεδήσεων και προσαρμογή.

1.4 Φυσική σχεδίαση

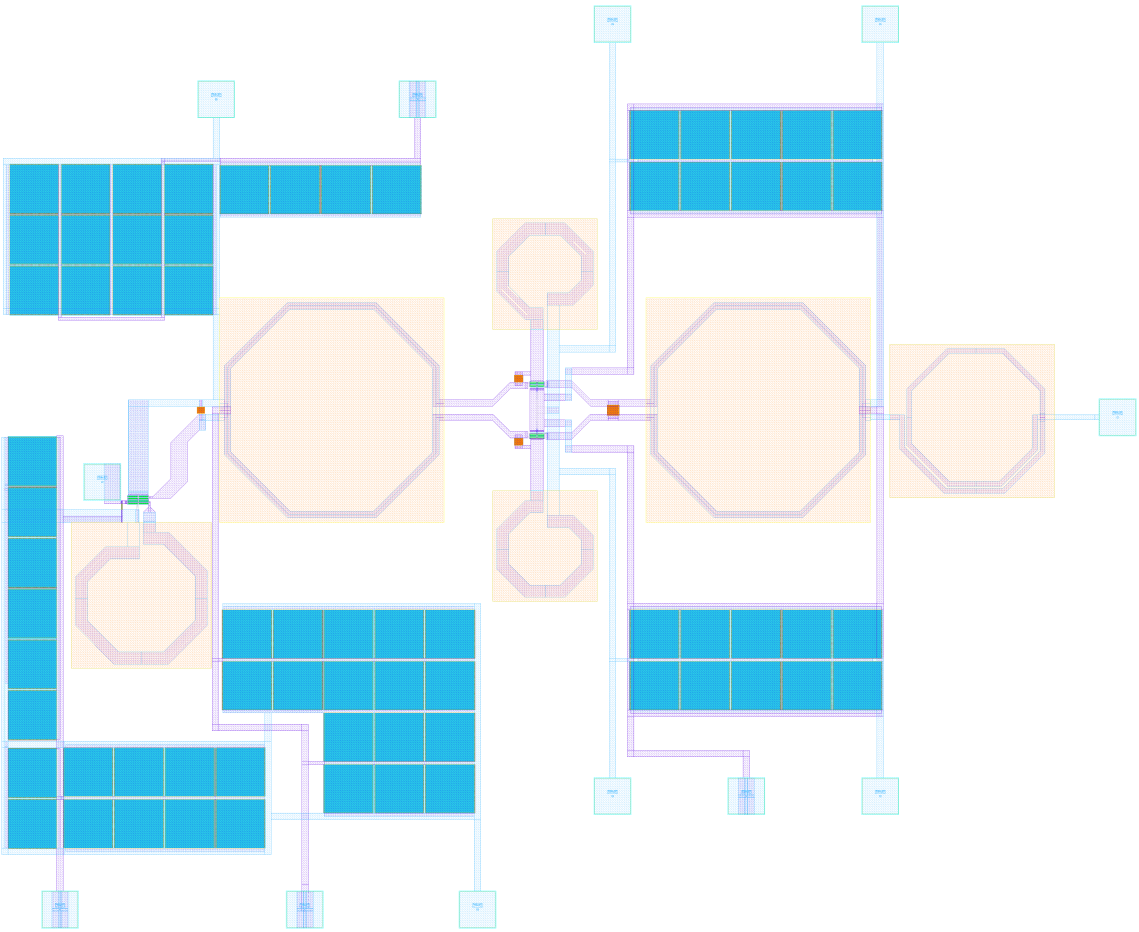
Μετά την επίτευξη καλών επιδόσεων σε επίπεδο σχηματικού σειρά είχε η φυσική σχεδίαση του LNA, η οποία φαίνεται στο σχήμα 1.3. Ακολουθήθηκε η παρακάτω πορεία.

Φυσική σχεδίαση:

- Επαφή των transistors με μέταλλα σε υψηλό επίπεδο.
- Διασυνδέσεις μεταξύ transistors.
- Τοποθέτηση στοιχείων, ειδικά επαγωγέων.
- Διασυνδέσεις και pads.



Σχήμα 1.2: Η τοπολογία του LNA αυτής της διπλωματικής



Σχήμα 1.3: Φυσικό σχέδιο του LNA

1.5 Τελικά αποτελέσματα

Τα αποτελέσματα των προσομοιώσεων μετά το layout σε ονομαστικές συνθήκες φαίνονται στον παρακάτω πίνακα και στα διαγράμματα που ακολουθούν.

Μετρική	**Σχηματικό**	**Επανασχεδίαση**	**Post-Layout**
NF	0.585 dB	0.867 dB	1.192 dB
NF_{min}	0.579 dB	0.811 dB	1.006 dB
Z_{opt}	$(43.06 + j\,0.812)\,\Omega$	$(69.82 - j\,14.28)\,\Omega$	$(99.42 - j\,0.61)\,\Omega$
$\lvert S_{21}\rvert_{\mathrm{dB}}$	33.78 dB	30.52 dB	22.37 dB
$-\lvert S_{11}\rvert_{\mathrm{dB}}$	33.05 dB	23.27 dB	16.4 dB
$-\lvert S_{22}\rvert_{\mathrm{dB}}$	37.3 dB	37.91 dB	22.28 dB
$-\lvert S_{12}\rvert_{\mathrm{dB}}$	65.49 dB	58.12 dB	55.58 dB
$\mathrm{IP1dB}_{\mathrm{dBm}}$	−31.15 dBm	−30.13 dBm	−24.73 dBm
$\mathrm{OP1dB}_{\mathrm{dBm}}$	1.63 dBm	−0.611 dBm	−3.363 dBm
$\mathrm{IIP3}_{\mathrm{dBm}}$	−7.21 dBm	−9.407 dBm	−6.372 dBm
$\mathrm{OIP3}_{\mathrm{dBm}}$	26.64 dBm	21.15 dBm	16.02 dBm
K / B_1	19.25 / 0.9996	11.96 / 1.003	22.26 / 1.016
μ / μ'	25.41 / 20.8	18.83 / 9.093	10.33 / 5.811
I_Q	39.82 mA	29.54 mA	22.72 mA
P_{DC}	31.86 mW	23.63 mW	18.18 mW

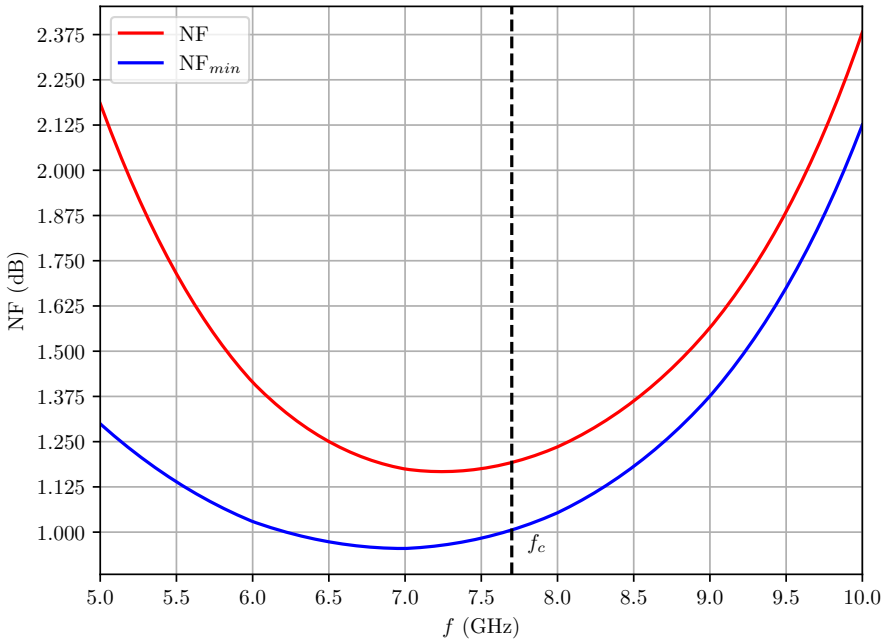
Πίνακας 1.3: Σύγκριση αποτελεσμάτων σχηματικού, επανασχεδίασης μετά τη φυσική σχεδίαση των transistors και τελικής σχεδίασης

Στον παρακάτω πίνακα φαίνονται οι επιδόσεις του κυκλώματος σε διάφορες ακραίες περιπτώσεις (corner cases). Το κύκλωμα λειτουργεί ως LNA με σχετικά χαμηλό κέρδος σε ορισμένες περιπτώσεις, διατηρώντας όμως την ευστάθεια σε κάθε περίπτωση.

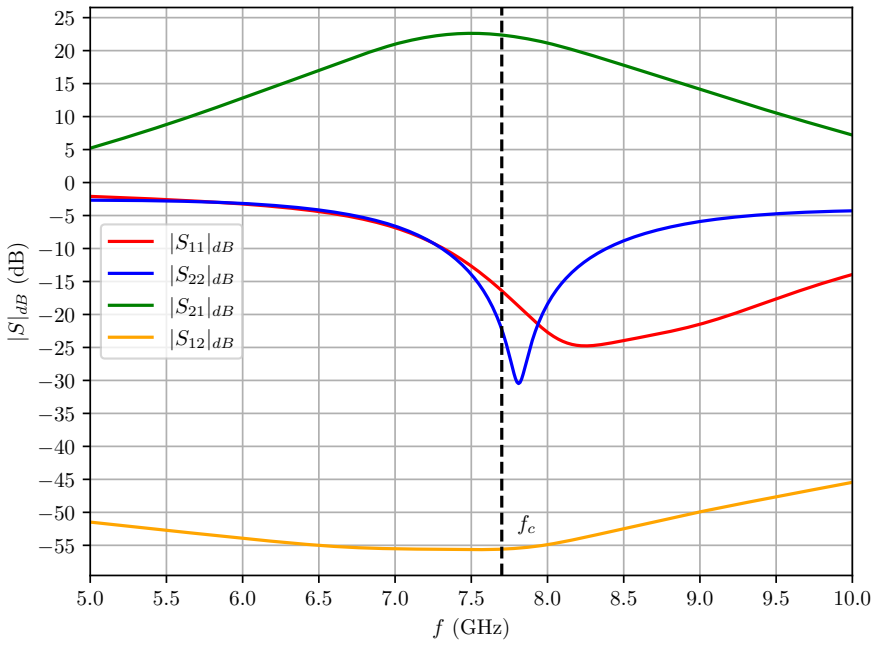
Μετρική	**Ελάχιστο**	**Ονομαστικό**	**Μέγιστο**
NF	0.872 dB	1.192 dB	1.787 dB
NF_{min}	0.719 dB	1.006 dB	1.591 dB
$\lvert S_{21}\rvert_{\mathrm{dB}}$	16.21 dB	23.37 dB	23.38 dB
$-\lvert S_{11}\rvert_{\mathrm{dB}}$	12.87 dB	16.4 dB	24.84 dB
$-\lvert S_{22}\rvert_{\mathrm{dB}}$	10.13 dB	22.28 dB	22.96 dB
$-\lvert S_{12}\rvert_{\mathrm{dB}}$	53.76 dB	55.58 dB	58.07 dB
K / B_1	17.65 / 0.941	22.26 / 1.016	36.52 / 1.021
μ / μ'	2.997 / 4.016	10.33 / 5.811	11.38 / 13.67
I_Q	10.3 mA	22.72 mA	43.08 mA
P_{DC}	7.419 mW	18.18 mW	37.91 mW

Πίνακας 1.4: Αποτελέσματα τελικών προσομοιώσεων του LNA σε ακραίες περιπτώσεις

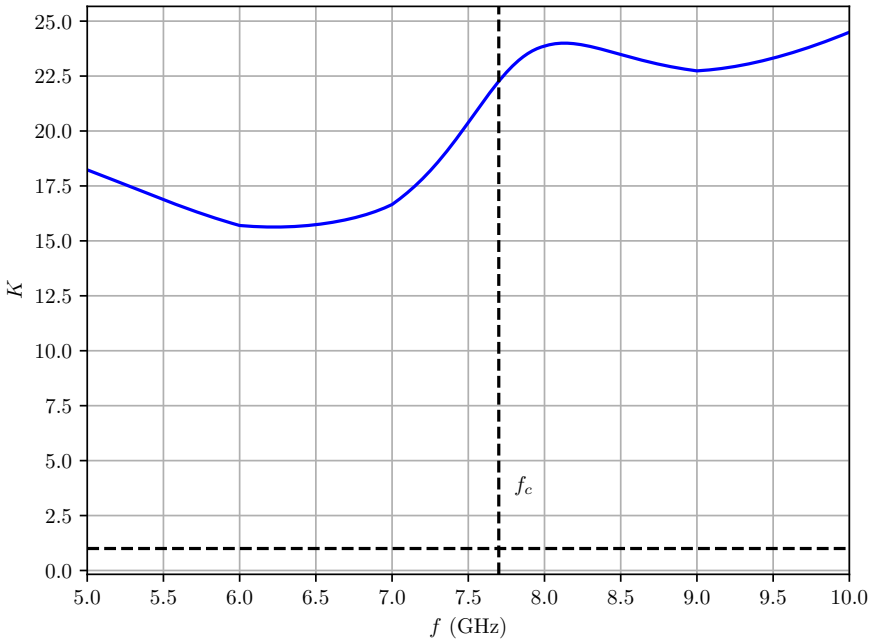
Τέλος, παρατίθενται και αποτελέσματα προσομοιώσεων Monte Carlo αναδεικνύοντας μικρή διακύμανση στον θόρυβο και το κέρδος, με σχεδόν βέβαιη ευστάθεια στη συχνότητα λειτουργίας.



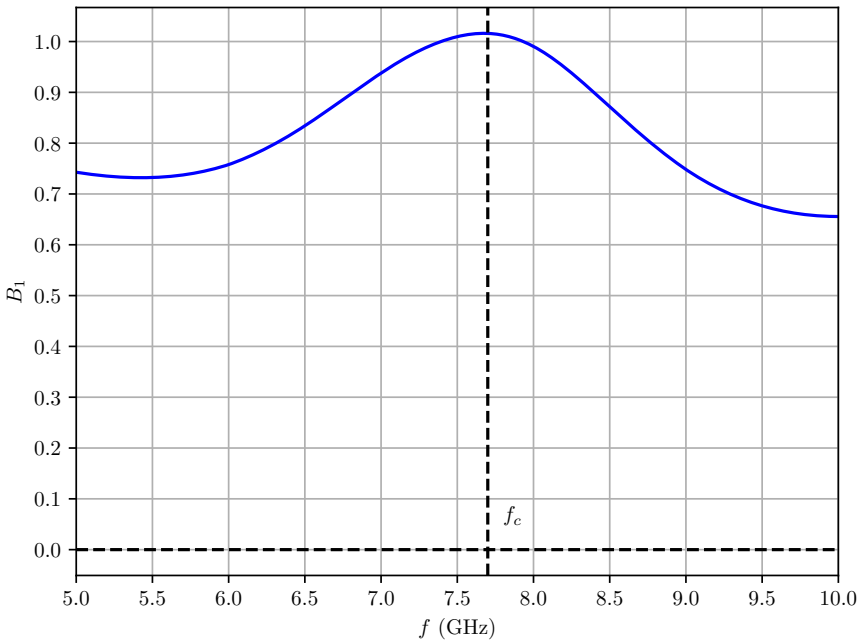
Σχήμα 1.4: Εικόνα θορύβου



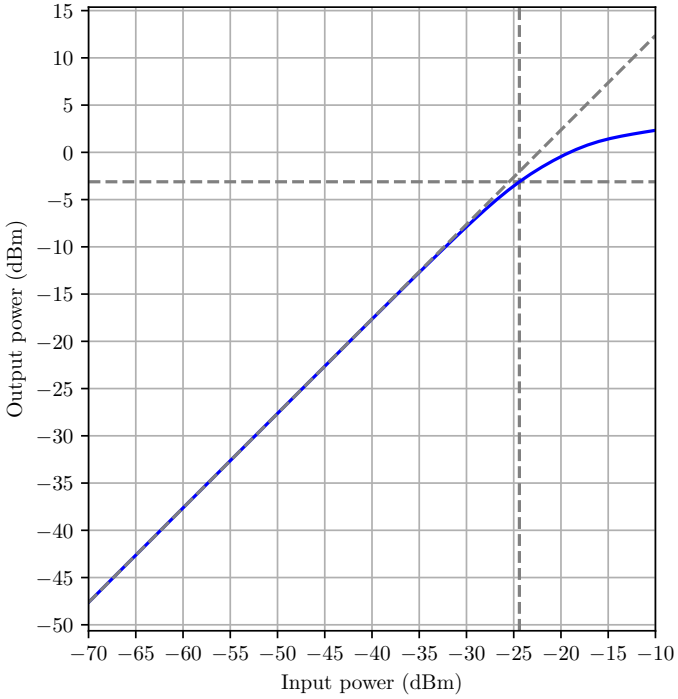
Σχήμα 1.5: Παράμετροι σκέδασης



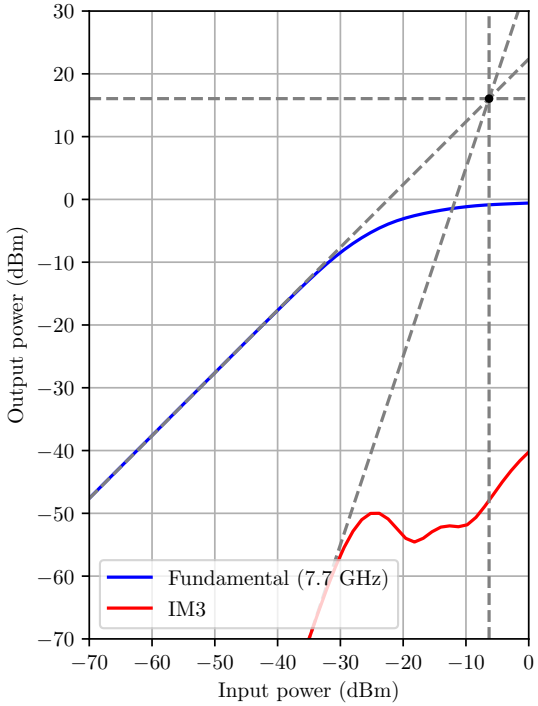
Σχήμα 1.6: Παράγοντας ευστάθειας K



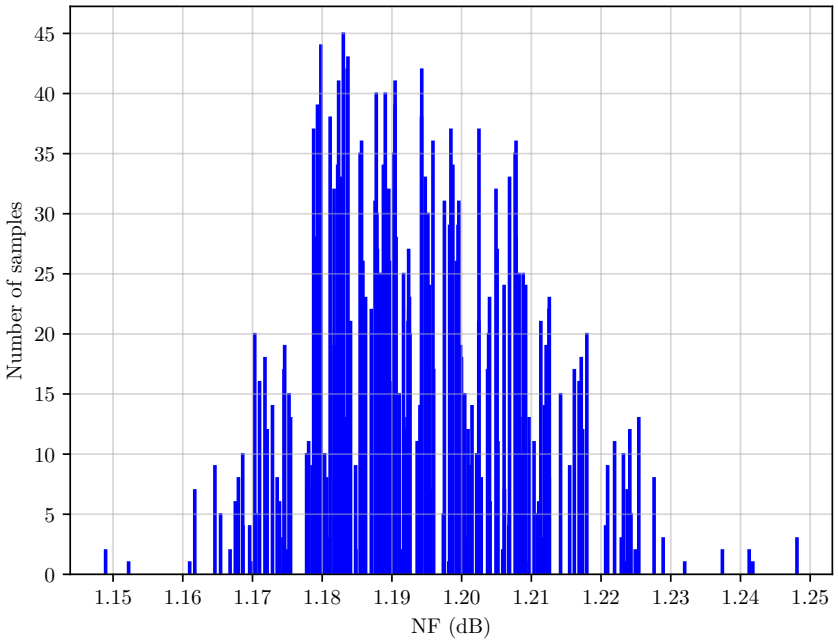
Σχήμα 1.7: Παράγοντας ευστάθειας B_1



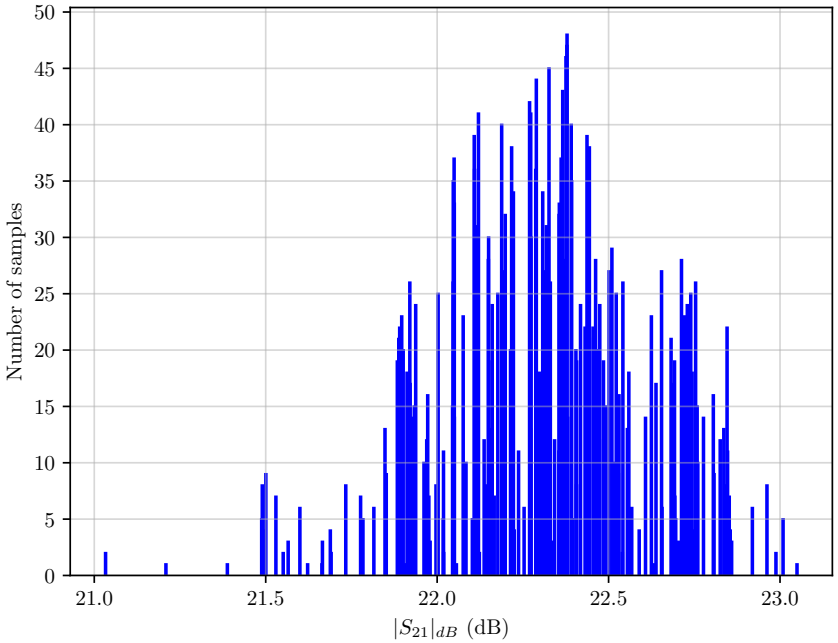
Σχήμα 1.8: Συμπίεση κέρδους



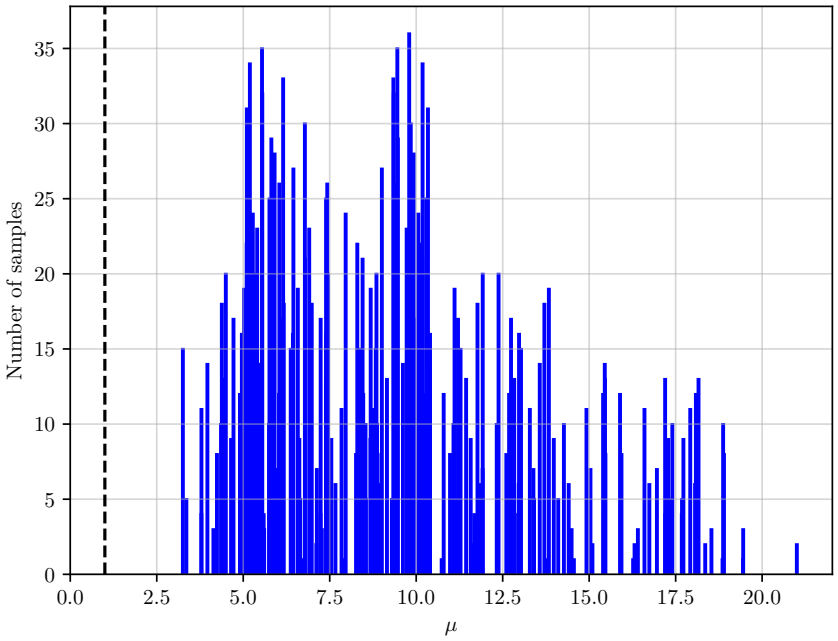
Σχήμα 1.9: Παρεμβολή τρίτης τάξης



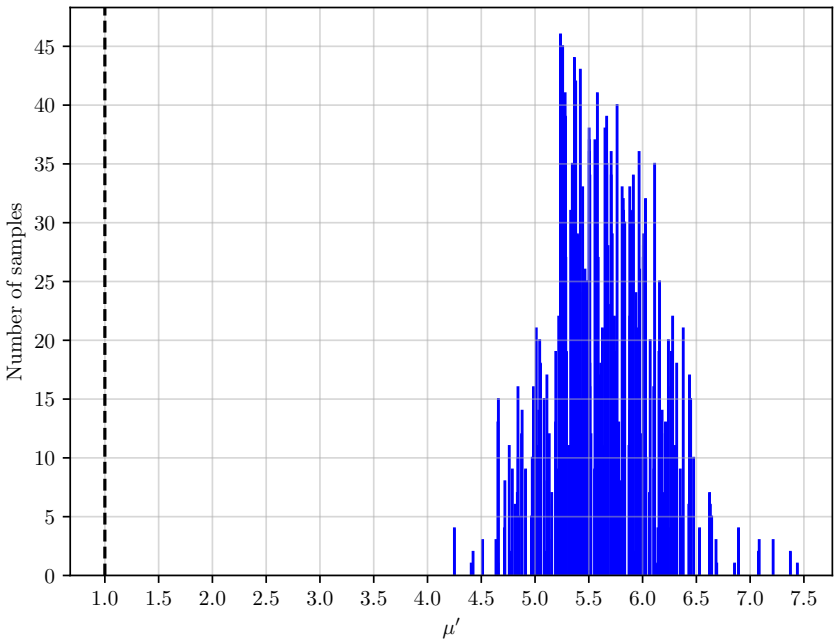
Σχήμα 1.10: Αποτελέσματα Monte Carlo για την εικόνα θορύβου



Σχήμα 1.11: Αποτελέσματα Monte Carlo για το κέρδος



Σχήμα 1.12: Αποτελέσματα Monte Carlo για τον παράγοντα ευστάθειας μ



Σχήμα 1.13: Αποτελέσματα Monte Carlo για τον παράγοντα ευστάθειας μ'

Chapter 2

Introduction

2.1 Telecommunication

Communication is fundamental to human society. The exchange of information, the transmission of knowledge, and coordination of activities are necessary for civilization, but telecommunication means something more than all this. The word telecommunication is derived from the Greek word "tele-" (τῆλε-) meaning "far away" and the Latin word "communico" meaning "to share", so it should be interpreted as the exchange of information at distances, which is necessary due to the inefficiency of physically closing the distance in order to communicate.

The way humans communicate from a distance has changed a lot throughout the centuries. Ancient people used semaphore systems, such as the phryctoriae in Ancient Greece. However, in recent centuries, the most efficient ways to share information across large distances have proven to be through the transmission of electromagnetic signals, properly modulated to carry information. Initially, electrical signals on metal wires used to carry information in telegraphy and telephony. After the discovery of electromagnetic wave propagation through space, wireless technologies, such as antennas, were implemented and the breakthrough of radio communications followed. Today, intense bandwidth demands are not met by wireless technology, due to high power losses inherent to free space propagation, and electromagnetic wave transmission across optical fibers has become vital. Nonetheless, wireless communication is indispensable because of applications unsuitable for wires, such as mobile communications.

Whatever the medium for electromagnetic wave propagation might have been, the transmitted signals used to be in properly modulated analog form. For example, in telephony and radio a sound signal was converted to voltage, it was carried as voltage along the wire and converted back to sound at a receiver. However, analog signals face serious issues of fidelity. They are highly susceptible to corruption from noise and difficult to store, requiring specialized equipment like magnetic tape. Furthermore, analog signal processing equipment is not very versatile.

The transition from analog to digital information began with the Nyquist-Shannon sampling theorem, which paved the way for robust signal discretization and reconstruction without loss of information. As technology progressed, data resolution became so high that even quantization errors did not pose a problem. The versatility of digital computers and the principles of digital signal processing allowed for precise processing of signals, along with the application of error correction codes for robust transmission and storage. As a result, every signal today is converted to digital form and treated by general purpose

equipment designed to handle data, regardless of what information it encodes.

Although in almost all modern telecommunication systems signals are converted to digital data and transmission is carried out by data modulated signals, the physical nature of any transmissible signal remains inherently analog, as it must be represented by a continuous time physical quantity, typically a voltage, current, or electromagnetic wave, to propagate through a medium. Each transmission medium, for example copper wires, the air, optical fibers, has unique physical properties and is usually frequency selective. Thus, different frequency bands are used for each application.

The radio spectrum is the part of the electromagnetic spectrum with frequencies from 3 Hz to 3 THz. To prevent interference, the generation and transmission of radio waves is strictly regulated by laws coordinated by the International Telecommunication Union (ITU). In the following tables, categorizations of frequency bands by ITU and IEEE are presented, as well as some physical transmission media with their operating frequency range and some of their applications.

Band	**Range**	**Etymology**	**Applications**
HF	3 – 30 MHz	High Frequency	Long-range radar, ionospheric communication
VHF	30 – 300 MHz	Very High Frequency	Long-range radar, TV broadcasting, FM radio
UHF	0.3 – 1 GHz	Ultra High Frequency	Military communications, tactical radar, mobile networks
L	1 – 2 GHz	Long wavelength	GPS, mobile telephony, early warning radar
S	2 – 4 GHz	Short wavelength	Weather radar, satellite communication systems
C	4 – 8 GHz	Compromise between S & X	Satellite TV, 5 GHz Wi-Fi, marine radar
X	8 – 12 GHz	Crosshair (military term)	Military radar, satellite downlinks, some Wi-Fi
K_u	12 – 18 GHz	Kurz-under	VSAT terminals, satellite uplinks, Doppler radar
K	18 – 27 GHz	Kurz (short in German)	Experimental radar, automotive sensors
K_a	27 – 40 GHz	Kurz-above	High-resolution satellite links, deep-space communication
V	40 – 75 GHz		Millimeter-wave radar, 5G+, passive imaging
W	75 – 110 GHz	After V	Imaging radar, collision-avoidance systems
mm (G)	110 – 300 GHz	Millimeter-wave band	Research, spectroscopy, ultra-wideband radar

Table 2.1: IEEE Radar Frequency Bands

Band	Range	Etymology	Key Applications
ELF	0.3 – 3 Hz	Extremely Low Frequency	Submarine communication, geophysical sensing
VLF	3 – 30 kHz	Very Low Frequency	Submarine communications, navigation, time signals
LF	30 – 300 kHz	Low Frequency	Navigation beacons (e.g., LORAN), RFID systems
MF	300 – 3000 kHz	Medium Frequency	AM broadcasting, maritime communications
HF	3 – 30 MHz	High Frequency	Shortwave broadcasting, aviation communications
VHF	30 – 300 MHz	Very High Frequency	FM radio, VHF TV, air traffic control, amateur radio
UHF	0.3 – 3 GHz	Ultra High Frequency	Mobile phones, UHF TV, Wi-Fi, RFID
SHF	3 – 30 GHz	Super High Frequency	Radar, satellite communications, point-to-point microwave links
EHF	30 – 300 GHz	Extremely High Frequency	Millimeter-wave radar, 5G, high-resolution sensing

Table 2.2: ITU Radio Frequency Bands

Transmission Medium	Typical Frequency Range - Applications
Twisted Pair (Copper Wires)	Baseband signals and DSL technologies up to ~ 30 MHz. Telephone lines, Ethernet, DSL.
Power Line Communication	Data transmission through electrical wiring. From 3 kHz to ~ 86 MHz depending on standard.
Coaxial Cable	From a few MHz up to several GHz. Cable TV (up to ~ 1 GHz), DOCSIS, RF intermediate links.
Free Space / Air (Radio)	From VLF to EHF. Radio, cellular, Wi-Fi, radar, satellite.
Microwave Point-to-Point Links	SHF bands, typically from 3 GHz to 30 GHz. Wireless backhaul, military links, high-capacity point-to-point communications.
Millimeter-Wave Links	EHF range, often from 30 GHz to more than 100 GHz. Short-range high-speed communication, 5G, automotive radar.
Optical Fiber	Infrared light at wavelengths like 850 nm, 1310 nm, and 1550 nm, equivalent to $\sim 200 - 375$ THz. Ultra-high-speed data transmission.

Table 2.3: Transmission media and their frequency ranges

2.2 The necessity for low noise amplifiers

Wireless telecommunication is indispensable in modern society, enabling connectivity across great distance, without the constraints of physical cables. It is necessary for mobile communication, Wi-Fi, satellite systems and Internet of Things (IoT). At the core of any wireless system lies the radio receiver, which captures transmitted electromagnetic signals and converts them into usable information. A typical receiver chain is shown in Fig. 2.1 with the radio frequency (RF) front end followed by processing at an intermediate frequency (IF) and eventually processing in the base-band (BB). Frequency up conversion of a signal is necessary for transmission through air or free space, therefore after the reception from an antenna, down conversion must follow. Usually, at the end of a receiver chain analog to digital conversion of the signal occurs.

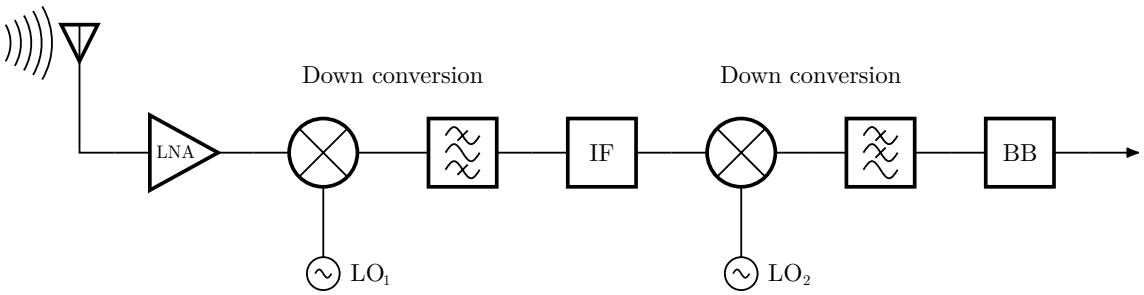


Figure 2.1: Typical receiver chain

Wireless propagation implies great power loss as distance increases. Additionally, as a signal propagates through space it is susceptible to corruption from a lot of noise sources. Therefore, antennas are sources of very weak signals already compromised by a lot of noise. In order to combat this, an amplifier is required after the antenna, providing necessary power so that the signal can be processed by the rest of the receiver blocks, while introducing as little additional noise to the signal as possible.

$$L_{\text{fs}} = \left(\frac{4\pi d}{\lambda}\right)^2 = \left(\frac{4\pi df}{c}\right)^2 \tag{2.1}$$

Since the signal is at its weakest right after the antenna, the noise performance of the whole receiver greatly depends on the noise factor of the following amplifier. This can be shown with Friis' formula for noise and is more thoroughly explained in 4.2.2. Therefore, there is need for an amplifier with sufficiently high gain and sufficiently low noise factor in accordance with application demands. It is critical to maintain a low noise factor of the receiver, therefore these blocks are called low noise amplifiers. The figures of merit of a low noise amplifier are noise factor, gain, input matching, bandwidth, linearity, and power consumption.

$$F_{\text{receiver}} = F_{\text{LNA}} + \frac{F_{\text{rest}}}{G_{\text{LNA}}} \tag{2.2}$$

In summary, the indispensable nature of wireless communications makes the design of high-performance low noise amplifiers a cornerstone for enabling robust and efficient radio receivers in modern communication systems.

2.3 5G/6G cellular communications

The acronyms 5G and 6G are used to refer to the fifth and sixth generations of cellular network technology. The fifth generation has been deployed by mobile operators worldwide since 2019 and the sixth is upcoming. A generation is a distinct phase or iteration of mobile network standards characterized by technological features and performance capabilities. Each generation typically introduces new innovations in areas such as modulation schemes, frequency bands, data rates, network architecture, latency, and supported applications. This leads to improvements in data throughput and spectral efficiency, enhanced quality of service (QoS). In the following table, some information for each generation is presented.

Generation	Data Rates	Key Features and Applications
1G	2.4 kbps	Analog voice-only cellular systems. Basic mobile telephony
2G	64 kbps	Digital voice, SMS, early data services like GPRS and EDGE
3G	2 Mbps	Mobile internet, video calls, multimedia services
4G	1 Gbps	High-speed mobile internet, IP-based voice and video
5G	20 Gbps	Ultra-reliable, low-latency communications and massive IoT connectivity
6G (Future)	0.1 – 1 Tbps	AI integration, terahertz communications, sensing and imaging

Table 2.4: Cellular communication generations

In order to meet increasing data rate demands, larger bandwidth is required necessitating the use of higher carrier frequencies. Current 5G systems already operate within a broad millimeter wave spectrum utilizing architectures relying heavily on technologies like massive MIMO, beamforming, and network slicing. Future 6G technology is currently in the research and development phase aiming to operate well into the sub-terahertz and terahertz ranges, enabling data rates in the terabit per second range and integration with emerging technologies, such as Artificial Intelligence (AI).

Operating at high frequencies introduces significant challenges, such as increased propagation losses, stronger atmospheric absorption, and limited signal penetration resulting in smaller cell sizes and reduced coverage areas. This necessitates the deployment of dense networks of base stations and small cells to maintain reliable connectivity. Both 5G and future 6G systems place increasing demands on hardware design, especially on RF front end design. This means lower noise factors, higher gain, better linearity all at very high frequencies while keeping power consumption at a minimum. This makes low noise amplifier design a vital part of future wireless communication technology.

In late 2023, a band spanning from 7.125 up to 8.4 GHz was proposed by the World Radio Conference for IMT identification, meaning designation for use in International Mobile Telecommunications systems. This band was considered the most promising for deployment of 6G technology systems by the end of the decade. Considering all of the above, the design of a low noise amplifier operating at 7.7 GHz, in the middle of the 7-8.4 GHz band, was decided to be the subject of this thesis.

Chapter 3

Microwave Networks and Amplifiers

Classic lumped element network theory can only be applied to systems operating at relatively low frequencies of the electromagnetic spectrum. Specifically, use of the lumped element approximation requires the operating wavelength of the system to be much larger than the characteristic length of the system, which basically indicates its size. The system must be electrically small ($d \ll \lambda$) for Kirchhoff's laws to hold. Therefore, in order to study and design high-frequency systems a distributed element model treating conductors as transmission lines is necessary.

Furthermore, the characterization of n-port networks at high frequencies using traditional n-port parameters, such as Z or Y, becomes impossible due to the difficulty of achieving short circuits or open circuits over a broadband range of frequencies. This led to the use of S-parameters which are defined in terms of traveling waves that propagate along transmission lines. Lumped element theory is contained within the distributed element model, therefore S-parameters can be used over any frequency band and there are transformations mapping S-parameters to classic parameters and back, leading to a kind of lumped element representation of distributed networks as well. The study of microwave networks, including the design high frequency amplifiers like the subject of this thesis, is performed with S-parameters.

3.1 Transmission lines

In order to extract the transmission line model one assumes a source driving a load through a transmission line of length L, as in Fig. 3.1. The voltage and the current change along the line, as electromagnetic waves do not propagate instantly.

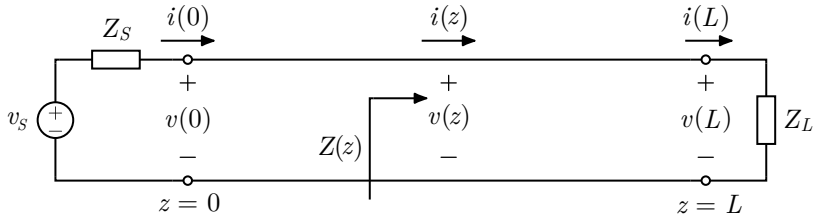


Figure 3.1: Transmission line

Dividing the line into small segments of length $\Delta z \ll \lambda$ allows for local use of lumped elements and setting $\Delta z \to 0$ leads to the following equations.

$$-\frac{\partial \mathrm{v}}{\partial z}(z,t) = L\frac{\partial \mathrm{i}}{\partial t}(z,t) + R\mathrm{i}(z,t) \tag{3.1}$$

$$-\frac{\partial \mathrm{i}}{\partial z}(z,t) = C\frac{\partial \mathrm{v}}{\partial t}(z,t) + G\mathrm{v}(z,t) \tag{3.2}$$

- L: self-inductance per unit length (H/m)
- C: capacitance per unit length (F/m)
- R: resistance per unit length (Ω/m), due to lossy conductors
- G: conductance per unit length (S/m), due to lossy dielectric between conductors

Uncoupling the system leads to the following wave equations, proving that voltage and current waves, governed by exactly the same equation, propagate along the line.

$$\frac{\partial^2 \mathrm{v}}{\partial z^2}(z,t) = RG\mathrm{v}(z,t) + (RC+LG)\frac{\partial \mathrm{v}}{\partial t}(z,t) + LC\frac{\partial^2 \mathrm{v}}{\partial t^2}(z,t) \tag{3.3}$$

$$\frac{\partial^2 \mathrm{i}}{\partial z^2}(z,t) = RG\mathrm{i}(z,t) + (RC+LG)\frac{\partial \mathrm{i}}{\partial t}(z,t) + LC\frac{\partial^2 \mathrm{i}}{\partial t^2}(z,t) \tag{3.4}$$

Under sinusoidal excitation, phasors can be utilized to simplify the equations provided that transient phenomena are unimportant.

$$\frac{dv}{dz}(z) = -(R+j\omega L)i(z) \tag{3.5}$$

$$\frac{di}{dz}(z) = -(G+j\omega C)i(z) \tag{3.6}$$

$$\frac{d^2 v}{dz^2}(z) = \gamma^2 v(z) \tag{3.7}$$

$$\frac{d^2 i}{dz^2}(z) = \gamma^2 i(z) \tag{3.8}$$

$$\gamma = \sqrt{(R+j\omega L)(G+j\omega C)} = \alpha + j\beta \tag{3.9}$$

- γ: propagation constant (m^{-1})
- α: attenuation constant (m^{-1})
- β: phase constant (m^{-1})

With the following boundary conditions the solutions can be found.

$$v_S - i(0)Z_S = v(0) \quad \wedge \quad v(L) = i(L)Z_L \tag{3.10}$$

$$v(z) = A_+ e^{-\gamma z} + A_- e^{\gamma z} \quad \wedge \quad i(z) = \frac{A_+}{Z_0}e^{-\gamma z} - \frac{A_-}{Z_0}e^{\gamma z} \tag{3.11}$$

$$Z_0 = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \tag{3.12}$$

$$A_+ = v_S \frac{Z_0}{Z_0 + Z_S} \frac{1}{1 - \Gamma_S \Gamma_L e^{-2\gamma L}} \quad \wedge \quad A_- = A_+ \Gamma_L e^{-2\gamma L} \tag{3.13}$$

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \quad \wedge \quad \Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.14}$$

$$v(z) = A_- e^{-\gamma z} \left[1 + \Gamma_L e^{-2\gamma(l-z)}\right] \tag{3.15}$$

$$\Gamma(z) = \frac{v_r(z)}{v_i(z)} = \Gamma_L e^{-2\gamma(l-z)} = \frac{Z(z) - Z_0}{Z(z) + Z_0} \tag{3.16}$$

$$Z(z) = \frac{v(z)}{i(z)} = Z_0 \frac{1 + \Gamma_L e^{-2\gamma(l-z)}}{1 - \Gamma_L e^{-2\gamma(l-z)}} = Z_0 \frac{1 + \Gamma(z)}{1 - \Gamma(z)} \tag{3.17}$$

- Z_0: characteristic impedance of the line (Ω), typically 50Ω
- $\Gamma(z)$: reflection coefficient

Consequently, any transmission line can be seen as a 2-port network with the following T-parameters. This allows treatment of electrically long lines as simple 2-ports, while the rest of the network can possibly be treated as lumped or described with other n-ports. Furthermore, if the line is terminated with a load, it can simply be seen as an impedance.

$$\begin{bmatrix} v(0) \\ i(0) \end{bmatrix} = \begin{bmatrix} \cosh(\gamma L) & Z_0 \sinh(\gamma L) \\ Y_0 \sinh(\gamma L) & \cosh(\gamma L) \end{bmatrix} \begin{bmatrix} v(L) \\ i(L) \end{bmatrix} \tag{3.18}$$

$$Z_L = \frac{v(L)}{i(L)} \implies Z_{in} = \frac{v(0)}{i(0)} = Z(0) = Z_0 \frac{Z_L + Z_0 \tanh(\gamma L)}{Z_0 + Z_L \tanh(\gamma L)} \tag{3.19}$$

If a transmission line is lossless, meaning $R = 0$ and $G = 0$, then $\alpha = 0$ and $\gamma = j\beta$, which means that the amplitude of the waves remains constant along the line. Any other wave properties hold as well, matching occurs when $Z_L = Z_0$ and the Smith chart is used for convenient calculations.

Depending on the properties of the materials comprising the transmission line, there could be dispersive phenomena. Therefore, phase velocity and group velocity can be defined. Transmission without distortion is achieved when the Heaviside condition $LG = RC$ is met. In that case, despite frequency dependency of parameters, the group velocity and attenuation are constant over frequency. Additionally, the standing wave ratio is defined as a measure of reflections.

$$v_p = \frac{\omega}{\beta(\omega)} \quad \wedge \quad v_g = \frac{1}{\frac{\partial \beta}{\partial \omega}(\omega)} \tag{3.20}$$

$$\frac{\partial \alpha}{\partial \omega} = 0 \quad \wedge \quad \frac{\partial v_g}{\partial \omega} = 0 \implies LG = RC \tag{3.21}$$

$$LG = RC \implies \alpha = \sqrt{RG} \quad \wedge \quad \beta = \omega\sqrt{LC} \quad \wedge \quad v_p = v_g = \frac{1}{\sqrt{LC}} \tag{3.22}$$

$$\text{SWR} = \frac{1 - |\Gamma(z)|}{1 + |\Gamma(z)|} = \frac{1 - |\Gamma_L|}{1 + |\Gamma_L|} \tag{3.23}$$

3.2 Scattering parameters

Given the nature of the signals propagating within microwave networks the definition of traveling waves as separate entities emerge.

$$v(z) = \sqrt{2Z_0}\,[a(z) + b(z)] \quad \wedge \quad i(z) = \sqrt{\frac{2}{Z_0}}\,[a(z) - b(z)] \tag{3.24}$$

- $a(z)$: normalized incident voltage wave ($\sqrt{\mathrm{W}}$)
- $b(z)$: normalized reflected voltage wave ($\sqrt{\mathrm{W}}$)

$$a(z) = \frac{v(z) + Z_0 i(z)}{2\sqrt{2Z_0}} \quad \wedge \quad b(z) = \frac{v(z) - Z_0 i(z)}{2\sqrt{2Z_0}} \tag{3.25}$$

The reflection coefficient can be expressed in terms of these waves and the power at position z traveling towards increasing z can be seen as the power carried by the incident wave minus the power carried by the reflected wave.

$$\Gamma(z) = \frac{Z(z) - Z_0}{Z(z) + Z_0} = \frac{b(z)}{a(z)} \tag{3.26}$$

$$S(z) = \frac{1}{2} v(z) i^*(z) = |a(z)|^2 - |b(z)|^2 + 2j\ \mathrm{Im}[a^*(z) b(z)] \tag{3.27}$$

$$P(z) = \mathrm{Re}[S(z)] = |a(z)|^2 - |b(z)|^2 = |a(z)|^2 \left[1 - |\Gamma(z)|^2\right] \tag{3.28}$$

- $S(z)$: complex power at point z traveling towards increasing z ($\mathrm{V} \cdot \mathrm{A}$)
- $P(z)$: real power at point z traveling towards increasing z (W)

Additionally, from their definition, the voltage waves can be calculated anywhere along a transmission line if they are known at some point of it.

$$a(z) = a(z_0) e^{-\gamma(z - z_0)} \quad \wedge \quad b(z) = b(z_0) e^{\gamma(z - z_0)} \tag{3.29}$$

The description of voltages and currents in microwave networks with traveling waves necessitates the establishment of relationships between them when n-ports are present analogous to the traditional n-port parameters interrelating voltages and currents. This leads to the definition of the scattering parameters. For a linear microwave network, such as the one in Fig. 3.2, with n ports connected to transmission lines with each transmission line having $z_k = 0$ exactly on the port and z_k increasing towards the n-port, the S-parameters are defined as follows, due to linearity. The scattering matrix of the n-port is defined to have its S-parameters as its elements.

$$b_k(0) = \sum_{l=0}^{n} S_{kl} a_l(0) \tag{3.30}$$

$$S_{kl} = \left.\frac{b_k(0)}{a_l(0)}\right|_{a_m(0)=0\,,\, m \neq l} \tag{3.31}$$

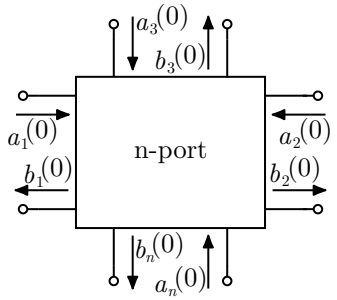


Figure 3.2: Microwave n-port network

If $\mathbf{Z_0}$ and $\mathbf{Y_0}$ are the diagonal matrices containing the characteristic impedances of each port then the Z and Y parameters of the n-port can be extracted. Consequently, every other set of n-port parameters of the network can be extracted.

$$\mathbf{Z} = \mathbf{Z_0^{\frac{1}{2}}}(\mathbb{I}_n + \mathbf{S})(\mathbb{I}_n - \mathbf{S})^{-1}\mathbf{Z_0^{\frac{1}{2}}} \quad \wedge \quad \mathbf{Y} = \mathbf{Y_0^{\frac{1}{2}}}(\mathbb{I}_n - \mathbf{S})(\mathbb{I}_n + \mathbf{S})^{-1}\mathbf{Y_0^{\frac{1}{2}}} \tag{3.32}$$

The definition of S-parameters implies that they can be measured by driving a signal into one port while matching all the others. This is easier to achieve in high frequencies compared to short circuits and open circuits.

$$\Gamma_{Sm} = \frac{a_m(0)}{b_m(0)} = 0 \implies a_m(0) = 0 \tag{3.33}$$

Therefore, any linear network containing lumped and distributed elements can be represented by its S-parameters from which all traditional parameters can be extracted. The scattering matrix of a transmission line has the following simple form.

$$\mathbf{S} = \begin{bmatrix} 0 & e^{-\gamma L} \\ e^{-\gamma L} & 0 \end{bmatrix} \tag{3.34}$$

A 2-port microwave network is shown in Fig. 3.3, since it is the most common one and amplifier design is a main concern. The notation of $z_k = 0$ is dropped as usual.

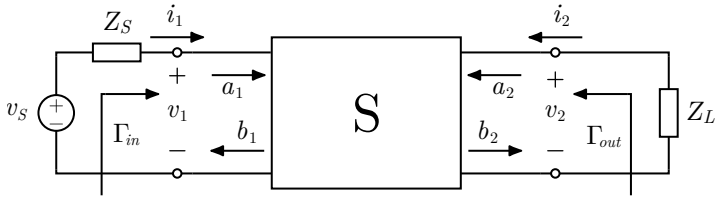


Figure 3.3: Microwave 2-port network

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.35}$$

- S_{11}: input port reflection coefficient
- S_{12}: reverse power gain
- S_{21}: forward power gain
- S_{22}: output port reflection coefficient,

- Input return loss: $-20\log(|S_{11}|)\,\text{dB}$
- Reverse isolation: $-20\log(|S_{12}|)\,\text{dB}$
- Gain: $20\log(|S_{21}|)\,\text{dB}$
- Output return loss: $-20\log(|S_{22}|)\,\text{dB}$

When the 2-port is terminated as shown in Fig. 3.3 the reflection coefficients seen at the ports depend on the terminations. Note that for the calculation of Γ_{out} the source need to be short circuited. The following hold and are useful for the design of microwave amplifiers, in which case the 2-port is an active element.

$$v_1 = v_S - i_1 Z_S \quad \wedge \quad v_2 = -i_2 Z_L \tag{3.36}$$

$$\Gamma_{in} = S_{11} + S_{12}S_{21}\frac{\Gamma_L}{1 - S_{22}\Gamma_L} \quad \wedge \quad \Gamma_{out} = S_{22} + S_{12}S_{21}\frac{\Gamma_S}{1 - S_{11}\Gamma_S} \tag{3.37}$$

3.3 Microwave Amplifier Design

Utilizing the fundamentals of lumped element and distributed element network theory, as well as the concepts of the terminated 2-port network, the principles of microwave amplifier design are laid out.

3.3.1 Maximum power transfer - Conjugate matching

A critical concept of microwave amplifier design is conjugate matching to a source, so that it can deliver the maximum possible power to a load. For example, an antenna collects electromagnetic power, but it can deliver only some of it to the load, which could be the input impedance of an amplifier. The rest of the power is reflected by the load back to the antenna. In the same way, an amplifier can deliver power to a load, such as an antenna, but some of it might be reflected back. Minimizing those reflections is required in microwave amplifier design. Considering the case in Fig. 3.4, the maximum power available can be calculated as well as the load for which it is delivered.

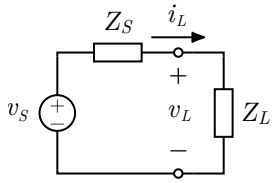


Figure 3.4: Load being driven by a source

$$P_L = \frac{1}{2}\text{Re}[v_L i_L^*] = \frac{1}{2}R_L|i_L|^2 = \frac{1}{2}\frac{R_L|v_S|^2}{|Z_S + Z_L|^2} = \frac{1}{2}\frac{R_L|v_S|^2}{(R_S + R_L)^2 + (X_S + X_L)^2} \tag{3.38}$$

$$\frac{\partial P_L}{\partial R_L} = 0 \quad \wedge \quad \frac{\partial X_L}{\partial R_L} = 0 \implies Z_L = Z_S^* \quad \wedge \quad P_{L_{max}} = \frac{|v_S|^2}{8R_S} \tag{3.39}$$

It is obvious why the condition for maximum power transfer is called conjugate matching. The maximum possible power delivered to the load is also called available power from the source.

3.3.2 Power gain definitions

During the design of microwave amplifiers the topology of Fig. 3.5 is of main concern. The 2-port network shown is an active element, for instance a transistor, a cascode combination of transistors or more complex structures.

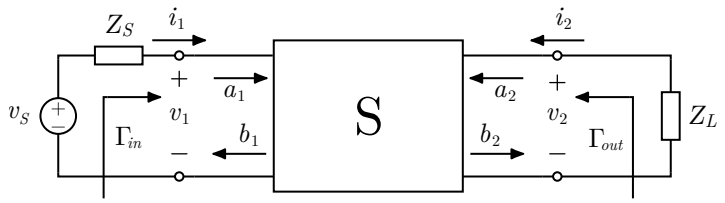


Figure 3.5: Microwave amplifier

A source drives the 2-port which is terminated with a load. Using matching networks the source and load impedances, equivalently the source and load reflection coefficients, viewed from the 2-port can be manipulated. There are three different definitions of power gain.

$$G_P = \frac{P_L}{P_{in}} = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{3.40}$$

- G_P: Power gain
- P_L: Power delivered to the load
- P_{in}: Input power to the network

$$G_T = \frac{P_L}{P_{S,av}} = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{out}\Gamma_L|^2} \tag{3.41}$$

- G_T: Transducer gain
- P_L: Power delivered to the load
- $P_{S,av}$: Available power from the source

$$G_A = \frac{P_{N,av}}{P_{S,av}} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{out}|^2} \tag{3.42}$$

- G_A: Available gain
- $P_{N,av}$: Available power from the 2-port network
- $P_{S,av}$: Available power from the source

Note that given the S-parameters of the 2-port, each gain is a function of either Γ_S or Γ_L or both. In the case of conjugate matching at the input and the output, the following hold.

$$\Gamma_{in} = \Gamma_S^* \quad \wedge \quad \Gamma_{out} = \Gamma_L^* \implies G_P = G_A = G_T = G_{T_{max}} \tag{3.43}$$

3.3.3 Stability

The stability of a microwave amplifier is a vital consideration during its design. A 2-port network is unstable and might begin to oscillate uncontrollably when either its input or its output presents negative resistance. For unconditional stability the following are necessary. The first two hold under proper termination, thus only the rest are a concern.

$$|\Gamma_S| < 1 \quad \wedge \quad |\Gamma_L| < 1 \quad \wedge \quad |\Gamma_{in}| < 1 \quad \wedge \quad |\Gamma_{out}| < 1 \tag{3.44}$$

$$|\Gamma_{in}| = 1 \iff \left|\Gamma_L - \frac{S_{22}^* - \Delta^* S_{11}}{|S_{22}|^2 - |\Delta|^2}\right| = \left|\frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2}\right| \tag{3.45}$$

$$|\Gamma_{out}| = 1 \iff \left|\Gamma_S - \frac{S_{11}^* - \Delta^* S_{22}}{|S_{11}|^2 - |\Delta|^2}\right| = \left|\frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2}\right| \tag{3.46}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.47}$$

Therefore, the load impedances that provide marginal stability at the input lie on a circle in the complex plane. The analogous is true with source impedances for stability at the output. In each case the complex plane is divided into two sub-regions, one stable and one unstable. By calculating $|\Gamma_{in}|$ and $|\Gamma_{out}|$ at $\Gamma_L = 0$ and $\Gamma_S = 0$ respectively the character of each region can be determined.

$$\Gamma_L = 0 \implies |\Gamma_{in}| = |S_{11}| \quad \wedge \quad \Gamma_S = 0 \implies |\Gamma_{out}| = |S_{22}| \tag{3.48}$$

Provided that source impedance and load impedance are passive, the following criteria are necessary and sufficient for unconditional stability.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad \wedge \quad |\Delta| < 1 \tag{3.49}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad \wedge \quad B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \tag{3.50}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad \wedge \quad B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 > 0 \tag{3.51}$$

The following criterion is sufficient for unconditional stability, provided passive source and load impedances.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \quad \wedge \quad \mu' = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} > 1 \tag{3.52}$$

3.4 Signal distortion - Nonlinearity

A microwave amplifier's purpose is to increase the amplitude of a high frequency signal. This is achieved by biasing an active device at an operating point where it is able to provide an AC gain by consuming DC power. Inevitably, the signal gets delayed as well. In addition to that, if the signal power becomes too high, the small signal linear approximation begins to fail and nonlinear effects dominate.

3.4.1 Linear systems - Distortionless transmission

A deterministic system can be described by an operator F mapping input signals $x(t)$ to output signals $y(t)$. The system is called linear if the following holds for arbitrary constants and signals.

$$F[a_1x_1(t) + a_2x_2(t)] = a_1F[x_1(t)] + a_2F[x_2(t)] \tag{3.53}$$

The system is called time-invariant if the operator F commutes with the time shift operator. Generally, amplifiers are time-invariant systems, since their topology does not change over time. In the case of linear time-invariant systems, transfer functions in the Laplace domain can be defined.

$$F[x(t)] = y(t) \implies F[x(t - t_0)] = y(t - t_0) \tag{3.54}$$

The output is said to be an undistorted version of the input when the system applies only a constant gain A and constant delay t_0. In other words, the system must be linear, time-invariant and its frequency response should have constant amplitude and linear phase, or equivalently constant group delay.

$$F[x(t)] = Ax(t - t_0) \iff H(j\omega) = Ae^{-j\omega t_0} \tag{3.55}$$

Therefore, the presence of nonlinearity causes distortion, but even a linear, time-invariant system can distort signals with a frequency spectrum spanning a bandwidth. Sinusoidal signals on the other hand do not get distorted by linear, time-invariant systems, since complex exponentials are eigenfunctions of the linear operators, due to their Fourier transform being a Dirac delta.

$$F_{\text{LTI}}[e^{j\omega_0 t}] = |H(j\omega_0)|e^{j\{\omega_0 t - \arg[H(j\omega_0)]\}} \tag{3.56}$$

$$F_{\text{LTI}}[A\cos(\omega_0 t + \theta)] = A|H(j\omega_0)|\cos\{\omega_0 t + \theta + \arg[H(j\omega_0)]\} \tag{3.57}$$

3.4.2 Harmonic distortion

In general, a time-invariant system with a periodic signal of period T at the input produces a periodic signal with the same period at the output.

$$y(t + T) = F[x(t + T)] = F[x(t)] = y(t) \tag{3.58}$$

Therefore, when a possibly nonlinear, time-invariant system, such as a realistic model of an amplifier, is being driven by a sinusoidal input, the output is also periodic with the same period as the sinusoid.

Any regular periodic signal can be represented by a Fourier series. Harmonic distortion of order n compares the amplitude of the harmonic of order n to that of the fundamental. As a measure of the presence of nonlinearity in the output, the total harmonic distortion is defined. The total harmonic distortion compares the presence of higher order harmonics to that of the fundamental, which would be the only one present if the system were linear.

$$x(t) = A\cos(\omega_0 t + \theta) \implies y(t) = \sum_{n=0}^{\infty} A_n \cos(n\omega_0 t + \phi_n) \tag{3.59}$$

$$\mathrm{HD}_n = \frac{A_n}{A_1} \quad \wedge \quad \mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} A_n^2}}{A_1} \tag{3.60}$$

When the small AC signal approximation holds, total harmonic distortion is very low, the system can be treated as linear and a transfer function can be defined. The small signal power gain can be derived from that.

3.4.3 Gain compression

When the input signal to a nonlinear, time-invariant system has relatively large amplitude, or equivalently the input power is relatively high, the small signal approximation fails and nonlinear effects can be observed at the output. For amplifiers, this usually means that output power begins to saturate as shown in Fig. 3.6 or in other words gain is starting to compress as shown in Fig. 9.20.

Power gain is defined as the ratio of output power to input power. This leads to a linear relationship in decibels as shown below. The 1dB compression point is the point where the power gain of the amplifier drops by 1dB from the small signal power gain and can be referred to either the input power or the output power.

$$G = \frac{P_{out}}{P_{in}} \iff P_{out,\mathrm{dBm}} = P_{in,\mathrm{dBm}} + G_{\mathrm{dB}} \tag{3.61}$$

Generally, speaking the 1dB compression point signifies the onset of nonlinearity in an amplifier, so the IP1dB and OP1dB are desired to be large. While an amplifier delivers its maximum output power at saturation, it exhibits highly non linear behaviour in that region. Consequently, since linearity is quite important in most applications, the 1dB compression point along with the minimum detectable signal level define the dynamic range of the amplifier. This range indicates the span of input powers over which the amplifier can operate with acceptable linearity and signal integrity.

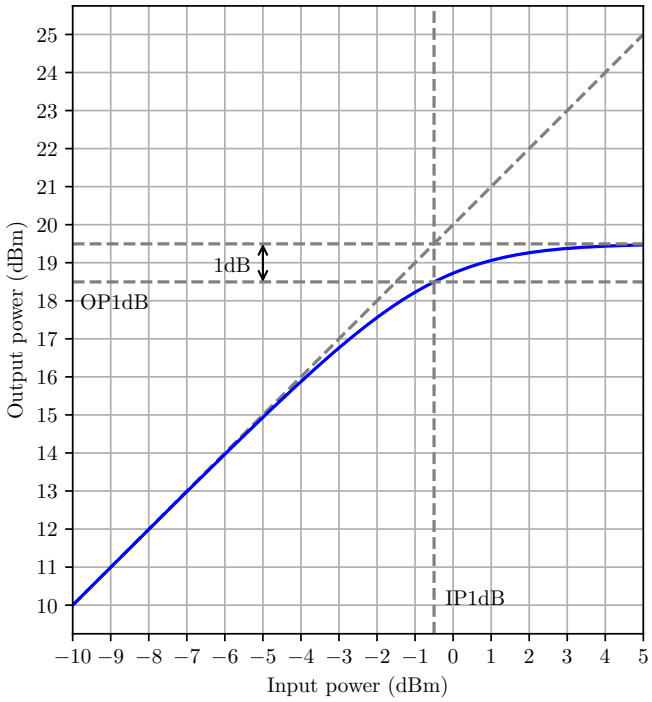


Figure 3.6: Output power saturation

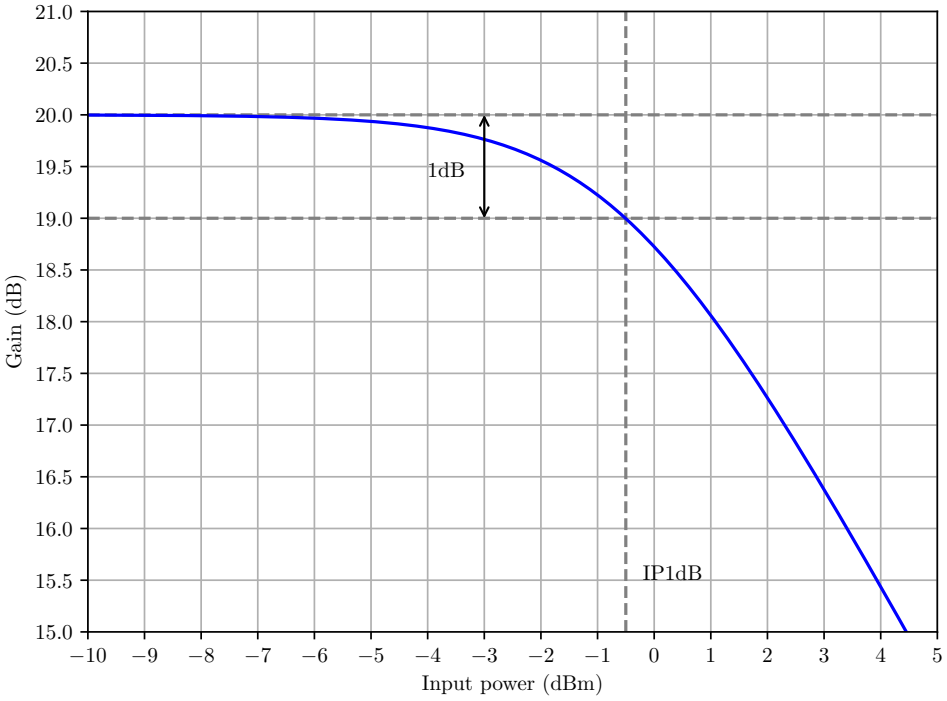


Figure 3.7: Gain compression

3.4.4 Intermodulation distortion

Intermodulation distortion is a phenomenon that occurs when a nonlinear system, like an amplifier, takes as input the sum of two or more signals of different frequencies. This creates additional frequency components at the sums and differences of the input frequencies and their harmonics. For example, when two tones are present at the input with frequencies f_1 and f_2, signals at many more frequencies are observed at the output. These frequencies are calculated as shown below, and the signals at the non fundamental frequencies are called intermodulation products.

$$f_{\text{IMD}} = mf_1 \pm nf_2 \quad , \quad m, n \in \mathbb{N} \quad \wedge \quad m + n \geq 2 \tag{3.62}$$

Considering a nonlinear system with a third degree polynomial transfer function, a special but very common case of intermodulation can be examined. This can be interpreted as a Taylor polynomial expansion of a more complex transfer function as a means of examining weak nonlinearities at input powers for which the linear approximation begins to fail but intense nonlinearities are still not present.

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \quad \wedge \quad x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \tag{3.63}$$

$$x^2(t) = \frac{A_1^2}{2} + \frac{A_2^2}{2} + \frac{A_1^2}{2}\cos(2\omega_1 t) + A_1 A_2 \cos[(\omega_1 - \omega_2)t] + \frac{A_2^2}{2}\cos(2\omega_2 t) + A_1 A_2 \cos[(\omega_1 + \omega_2)t] \tag{3.64}$$

$$\begin{aligned} x^3(t) = {} & \left(\frac{3A_1^3}{4} + \frac{3A_1 A_2^2}{2}\right)\cos(\omega_1 t) + \frac{A_1^3}{4}\cos(3\omega_1 t) + \frac{3A_1 A_2^2}{4}\cos\left[(\omega_1 - 2\omega_2)t\right] \\ & + \frac{3A_1^2 A_2}{4}\cos\left[(2\omega_1 - \omega_2)t\right] + \left(\frac{3A_1^2 A_2}{2} + \frac{3A_2^3}{4}\right)\cos(\omega_2 t) + \frac{A_2^3}{4}\cos(3\omega_2 t) \\ & + \frac{3A_1^2 A_2}{4}\cos\left[(2\omega_1 + \omega_2)t\right] + \frac{3A_1 A_2^2}{4}\cos\left[(\omega_1 + 2\omega_2)t\right] \end{aligned} \tag{3.65}$$

For the case of two input signals with similar frequencies, for instance carriers of adjacent channels within an operating frequency band, the concerning intermodulation products are those at frequencies $2f_1 - f_2$ and $f_2 - 2f_1$ because they lie close to the original frequencies thus they cannot be rejected by filtering. The rest of the products are out of band. Eventually, the output gets the following form and the third-order intermodulation product power can be calculated. These signals are normally weaker than the fundamental, because the linear terms dominate there, however due to the cubic nature of their coefficients their power rises with a slope of 3 instead of a slope of 1, as seen in Fig. 3.8.

$$\begin{aligned} y(t) = {} & \left(a_1 A_1 + \frac{3a_3 A_1^3}{4} + \frac{3a_3 A_1 A_2^2}{2}\right)\cos(\omega_1 t) \\ & + \left(a_1 A_2 + \frac{3a_3 A_1^2 A_2}{2} + \frac{3a_3 A_2^3}{4}\right)\cos(\omega_2 t) \\ & + \frac{3a_3 A_1^2 A_2}{4}\cos\left[(2\omega_1 + \omega_2)t\right] + \frac{3a_3 A_1 A_2^2}{4}\cos\left[(\omega_1 + 2\omega_2)t\right] \\ & + \frac{3a_3 A_1^2 A_2}{4}\cos\left[(2\omega_1 - \omega_2)t\right] + \frac{3a_3 A_1 A_2^2}{4}\cos\left[(\omega_1 - 2\omega_2)t\right] \end{aligned} \tag{3.66}$$

$$x(t) = \lambda_1 A\cos(\omega_1 t) + \lambda_2 A\cos(\omega_2 t) \quad \wedge \quad \lambda_1^2 + \lambda_2^2 = 1 \implies P_{in} = \frac{A^2}{2} \tag{3.67}$$

$$P_{\mathrm{IM}_3} = \frac{9a_3^2\lambda_1^2\lambda_2^2(\lambda_1^2+\lambda_2^2)}{16}A^6 = \frac{9}{2}a_3^2\lambda_1^2\lambda_2^2P_{in}^3 \tag{3.68}$$

$$P_{\mathrm{IM}_3,\mathrm{dBm}} = 3P_{in,\mathrm{dBm}} + 10\log\left[\frac{9}{2}a_3^2\lambda_1^2\lambda_2^2\right] \tag{3.69}$$

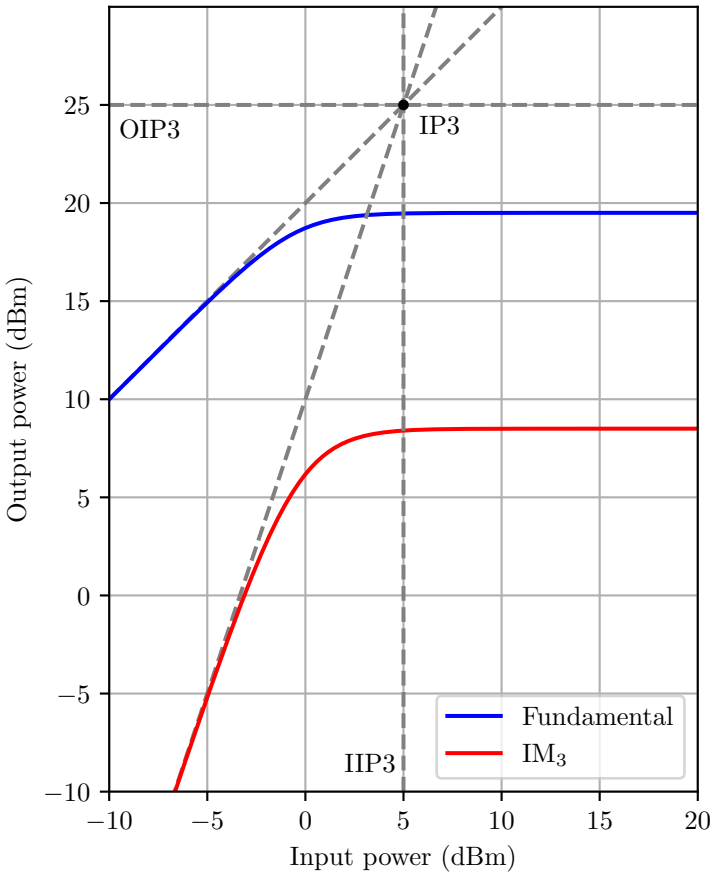


Figure 3.8: Intermodulation effects

3.4.5 Third order intercept point (IP3)

As a figure of merit of linearity, the third-order intercept point is defined by linear extrapolation of the nonlinear relationships between input power and output power of the fundamental and the third-order intermodulation products. The point where these lines meet is called the third-order intercept point, as shown in Fig. 3.8, and can be referred to either the input or the output. Larger IIP3 and OIP3 mean that the amplifier is more linear.

- IIP3: input referred third-order intercept point (mW or dBm)
- OIP3: output referred third-order intercept point (mW or dBm)

For a chain of n cascaded 2-port networks conjugately matched between each stage, like in Fig. 9.21, the third order intercept point of the total chain can be calculated from the third order intercept point and the available gain of each stage. In the following equations all the quantities are unitless numbers not in dB or dBm.

$$\frac{1}{\mathrm{IIP3}} = \frac{1}{\mathrm{IIP3}_1} + \frac{G_{A_1}}{\mathrm{IIP3}_2} + \frac{G_{A_1}G_{A_2}}{\mathrm{IIP3}_3} + \cdots + \frac{G_{A_1}G_{A_2}\cdots G_{A_{n-1}}}{\mathrm{IIP3}_n} \tag{3.70}$$

$$\frac{1}{\mathrm{OIP3}} = \frac{1}{\mathrm{OIP3}_n} + \frac{1}{G_{A_n}\mathrm{OIP3}_{n-1}} + \frac{1}{G_{A_n}G_{A_{n-1}}\mathrm{OIP3}_{n-2}} + \cdots + \frac{1}{G_{A_n}G_{A_{n-1}}\cdots G_{A_2}\mathrm{OIP3}_1} \tag{3.71}$$

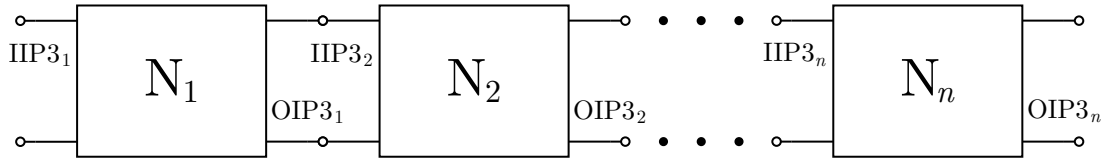


Figure 3.9: Chain of nonlinear 2-port networks

This formulation allows for the calculation of the third order intercept point for an entire receiver or transmitter chain. Furthermore, it highlights the definitive role of the last stage in the linearity of the total chain.

$$\frac{1}{\mathrm{IIP3}_{\mathrm{total}}} = \frac{1}{\mathrm{IIP3}_{\mathrm{rest}}} + \frac{G_{A_1}G_{A_2}\cdots G_{A_{n-1}}}{\mathrm{IIP3}_n} \tag{3.72}$$

$$\frac{1}{\mathrm{OIP3}_{\mathrm{total}}} = \frac{1}{\mathrm{OIP3}_n} + \frac{1}{G_{A_n}\mathrm{OIP3}_{\mathrm{rest}}} \tag{3.73}$$

Chapter 4

Noise theory

Noise is a random process that represents unpredictable and undesired variations added to a signal with which it shares the same nature. It originates from a variety of physical mechanisms and is modeled statistically, since it cannot be predicted deterministically. It is usually additive and directly interferes with signal measurement and transmission.

$$x(t) = s(t) + n(t) \tag{4.1}$$

- $x(t)$: observable signal
- $s(t)$: useful or desired signal
- $n(t)$: additive noise

4.1 Noise as a random process

In most cases, noise is added to a useful signal and is modeled as a wide sense stationary random process. Its expected value is usually zero, since if there is a bias it is subtracted and dealt with deterministically. Noise is almost always assumed to be ergodic in the mean and the autocorrelation, although there are some cases where noise is not ergodic. In practice, only one physical realization of noise in a system can be measured and in order to estimate statistical properties from time averages ergodicity is required, otherwise they may not be equal to ensemble averages.

$$\lim_{T\to+\infty}\left[\frac{1}{T}\int_0^T n(t)dt\right] = \mathbb{E}[n(t)] = 0 \tag{4.2}$$

$$\lim_{T\to+\infty}\left[\int_0^T n(t)n(t+\tau)dt\right] = \mathbb{E}[n(t)n(t+\tau)] = R_n(\tau) \tag{4.3}$$

$$n_{\text{rms}} = \sigma_n = \sqrt{\mathbb{V}[n(t)]} = \sqrt{\mathbb{E}[n^2(t)]} = \sqrt{R_n(0)} \tag{4.4}$$

4.1.1 Wide sense stationary stochastic processes

A stochastic process is called wide sense stationary if its expected value does not change over time and its autocorrelation is a function of only the time elapsed between samples. This is almost always a great model for noise.

$$\mathbb{E}[n(t)] = \int_{\mathbb{R}} x f_{n(t)}(x) dx = \mu_n \tag{4.5}$$

$$\mathbb{E}[n(t)n(t+\tau)] = \int_{\mathbb{R}^2} x_1 x_2 f_{n(t),n(t+\tau)}(x_1, x_2) dx_1 dx_2 = R_n(\tau) \tag{4.6}$$

Two random variables are jointly wide sense stationary if their expected values do not change with time and their autocorrelations as well as their cross-correlation depend only on the time elapsed between samples.

$$\mathbb{E}[x(t)y(t+\tau)] = \int_{\mathbb{R}^2} uv f_{x(t),y(t+\tau)}(u, v) du dv = R_{xy}(\tau) \tag{4.7}$$

4.1.2 Power spectral density

For wide sense stationary random processes, power spectral density is the Fourier transform of the autocorrelation, as shown by the Wiener–Khinchin theorem. Additionally, the cross power spectral density can be defined for two jointly wide sense stationary random processes.

$$S_n(f) = \lim_{T \to +\infty} \left\{ \frac{1}{T} \mathbb{E} \left[\left| \int_{-\frac{T}{2}}^{\frac{T}{2}} n(t) e^{-2\pi j f \tau} dt \right|^2 \right] \right\} = \int_{-\infty}^{+\infty} R_n(\tau) e^{-2\pi j f \tau} d\tau \geq 0 \quad \forall f \in \mathbb{R} \tag{4.8}$$

$$S_{xy}(f) = \int_{-\infty}^{+\infty} R_{xy}(\tau) e^{-2\pi j f \tau} d\tau \geq 0 \quad \forall f \in \mathbb{R} \tag{4.9}$$

The noise power in a band as well as the total noise power can be calculated from the power spectral density. Symmetry properties of Fourier transforms of real signals can be applied as well.

$$P_{\text{bandlimited}}(f_1, f_2) = 2 \int_{f_1}^{f_2} S_x(f) df \tag{4.10}$$

$$P_n = \int_{-\infty}^{+\infty} S_x(f) df = \int_{-\infty}^{+\infty} S_x(f) e^{2\pi j f \cdot 0} df = R_n(0) = \mathbb{E}[n^2(t)] = \mathbb{V}[n(t)] = \sigma_n^2 \tag{4.11}$$

A basic noise model used to mimic the effect of many random processes that occur in nature is additive white Gaussian noise (AWGN). Every sample of it follows the normal distribution with zero mean and its power spectral density is constant. In a system with finite bandwidth B, its variance can be calculated as follows.

$$n(t) \sim \mathcal{N}(0, \sigma^2) \quad \wedge \quad S_n(f) = \frac{N_0}{2} \tag{4.12}$$

$$\sigma^2 = P_n = \int_{-f_c - \frac{B}{2}}^{-f_c + \frac{B}{2}} S_x(f) df + \int_{f_c - \frac{B}{2}}^{f_c + \frac{B}{2}} S_x(f) df = B N_0 \tag{4.13}$$

4.1.3 Random processes in LTI systems

When a stable linear time-invariant system with impulse response $h(t)$ receives a wide sense stationary process at its input, as shown in Fig. 4.1, it outputs another wide sense stationary random process. The second order statistics of the output can be calculated as follows. An example of this would be noise filtering.

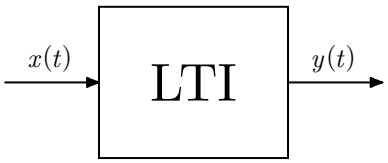


Figure 4.1: LTI system with a random process at its input

$$y(t) = h(t) * x(t) \tag{4.14}$$

$$\mu_y = \mathbb{E}[y(t)] = \mathbb{E}\left[\int_{-\infty}^{+\infty} h(\tau)\, x(t-\tau)\, d\tau\right] = \mu_x \int_{-\infty}^{+\infty} h(\tau)\, d\tau = H(0)\mu_x \tag{4.15}$$

$$R_y(\tau) = \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} h(u)\, h(v)\, R_x(\tau + u - v)\, du\, dv = R_x(\tau) * h(\tau) * h(-\tau) \tag{4.16}$$

$$S_y(f) = |H(f)|^2\, S_x(f) \tag{4.17}$$

If the linear time-invariant system has n inputs and one output, with each input having an impulse response $h_k(t)$, the following hold due to the superposition principle. This can be used in a system with multiple noise sources. Noise is usually a weak, relatively small amplitude signal so linear approximations usually hold well for it.

$$y(t) = \sum_{k=0}^{n} h_k(t) * x_k(t) \tag{4.18}$$

$$\mu_y = \sum_{k=0}^{n} H_k(0)\mu_{x_k} \tag{4.19}$$

$$S_y(f) = \sum_{k=1}^{n} |H_k(f)|^2\, S_{x_k}(f) + 2\sum_{k=1}^{n}\sum_{l=k+1}^{n} \mathrm{Re}\left[H_{x_k}(f) H_{x_l}^*(f) S_{x_k x_l}(f)\right] \tag{4.20}$$

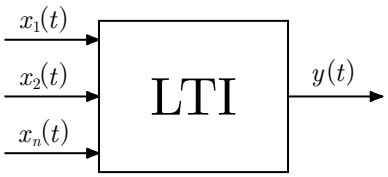


Figure 4.2: MISO LTI system with random processes at its inputs

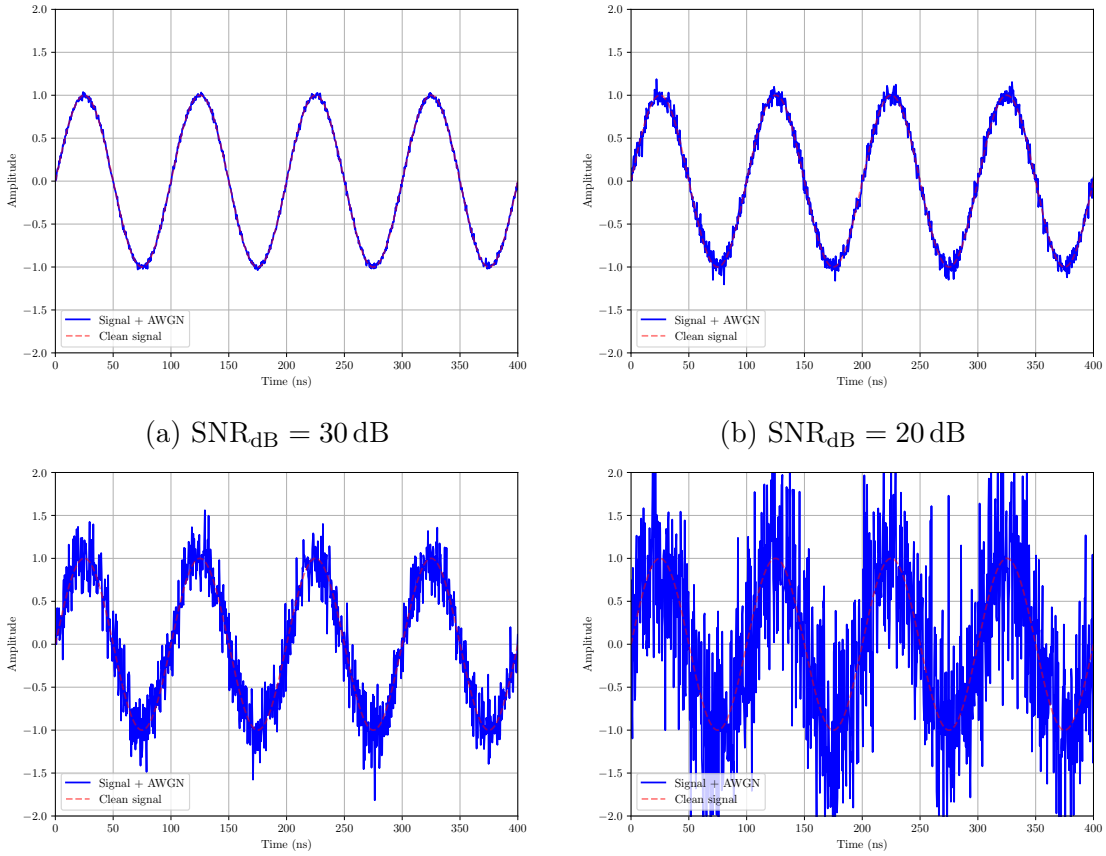
4.2 Signal integrity

Noise degrades the quality of every signal being transmitted or processed by any device. Due to thermodynamic principles, it is impossible to eliminate it completely. The signal to noise ratio (SNR) is defined to quantify the strength of a desired signal relative to its background noise. Furthermore, the noise factor of a device is defined as a measure of how much additional noise the device corrupts a signal with.

4.2.1 Signal to noise ratio (SNR)

For a signal corrupted by noise the signal to noise ratio is defined as the ratio of the useful signal power over the noise power. A higher signal to noise ratio indicates a cleaner signal, while a lower signal to noise ratio indicates significant degradation due to noise. This is demonstrated in Fig. 4.3 with a signal of some power and increasing noise power.

$$\mathrm{SNR} = \frac{S}{N} \iff \mathrm{SNR}_{\mathrm{dB}} = 10\log\left(\frac{S}{N}\right) = S_{\mathrm{dBm}} - N_{\mathrm{dBm}} \tag{4.21}$$



(a) $\mathrm{SNR}_{\mathrm{dB}} = 30\,\mathrm{dB}$

(b) $\mathrm{SNR}_{\mathrm{dB}} = 20\,\mathrm{dB}$

(c) $\mathrm{SNR}_{\mathrm{dB}} = 10\,\mathrm{dB}$

(d) $\mathrm{SNR}_{\mathrm{dB}} = 0\,\mathrm{dB}$

Figure 4.3: Signal corrupted by noise

4.2.2 Noise factor (F) - Noise figure (NF)

The noise factor is a figure of merit of a system defined as the ratio of output noise power of a device over the portion of it attributable to thermal noise of the input termination at standard noise temperature $T_0 = 290\,\mathrm{K}$. The noise factor is therefore the ratio of actual output noise power to that which would be there if the device itself did not introduce noise, which is equivalent to the ratio of input signal to noise ratio over output signal to noise ratio. Standard noise temperature is used so that noise factors of devices can be compared.

The noise factor quantifies the degradation in signal quality due to noise added by the system itself. Lower values indicate better performance with the ideal theoretical value being 1, due to thermodynamic principles. The noise figure of a system is simply defined as the value of the noise factor in decibels.

$$F = \frac{N_{out}}{GN_{in}} = \frac{\mathrm{SNR}_{in}}{\mathrm{SNR}_{out}} \tag{4.22}$$

$$\mathrm{NF} = F_{\mathrm{dB}} = 10\log(F)\,\mathrm{dB} = \mathrm{SNR}_{in,\mathrm{dB}} - \mathrm{SNR}_{out,\mathrm{dB}} \tag{4.23}$$

An amplifier inevitably amplifies noise power along with signal power. It inevitably adds its own noise as well. An attenuator at physical absolute temperature T attenuates both signal and noise power and it adds its own noise. Note the dependence on T_0, which necessitates a common reference temperature.

$$F_{\mathrm{amplifier}} = \frac{N_{out}}{GN_{in}} = \frac{GN_{in} + N_a}{GN_{in}} = 1 + \frac{N_a}{GN_{in}} = 1 + \frac{N_a}{Gk_BT_0B} \tag{4.24}$$

$$F_{\mathrm{attenuator}} = 1 + (L-1)\frac{T}{T_0} \tag{4.25}$$

- N_a: additional output referred noise power (W)
- $T_0 = 290\,\mathrm{K}$: standard noise temperature

For a chain of n cascaded 2-port networks conjugately matched between each stage, like in Fig. 4.4, the noise factor of the total chain can be calculated from the noise factor and the available gain of each stage with Friis' formula.

$$F = F_1 + \frac{F_2 - 1}{G_{A_1}} + \frac{F_3 - 1}{G_{A_1}G_{A_2}} + \cdots + \frac{F_n - 1}{G_{A_1}G_{A_2}\cdots G_{A_{n-1}}} \tag{4.26}$$

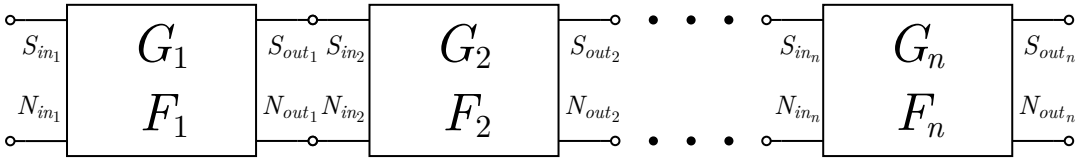


Figure 4.4: Chain of noisy 2-port networks

This formulation allows for the calculation of the noise factor for an entire receiver or transmitter chain. Furthermore, it highlights the definitive role of the first stage in the noise factor of the total chain and the fact that the noise factor of the last stage in unimportant. This shows the significance of the low noise amplifier in a receiver.

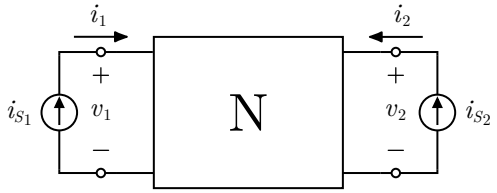
$$F_{\mathrm{total}} = F_1 + \frac{F_{\mathrm{rest}}}{G_{A_1}} \tag{4.27}$$

4.3 Noise matching

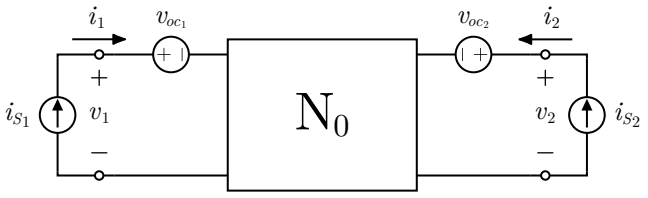
The concept of noise matching arises from the fact that a 2-port networks noise figure depends on the impedance of the source that drives it. In general, any linear 2-port network containing independent sources, possibly noise sources, is equivalent to a 2-port network comprised of the original with all independent sources set to zero and two independent sources connected to it. This is analogous to Thévenin's theorem. Also, since noise signals usually have small amplitudes, a small signal approximation even in nonlinear 2-port networks models their behavior quite well.

4.3.1 Two-port networks containing independent sources

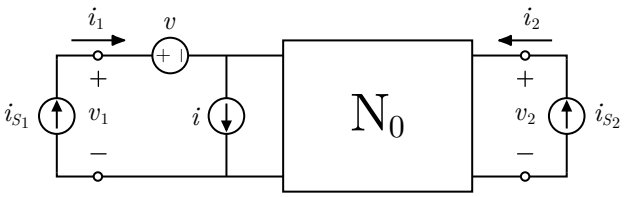
Due to the superposition principle, the linear 2-port network of Fig. 4.5a is equivalent to the other two linear 2-port networks of Fig. 4.5, provided that the ports are where the voltages and currents are annotated. The response of the network is the sum of its response when all the independent sources inside N are set to zero plus its response when the two independent current sources are set to zero. The 2-port resulting from setting all independent sources in N to zero is denoted N_0 and a Z-parameter representation for it is assumed.



(a) Independent sources inside N



(b) No independent sources inside N_0



(c) Independent sources moved to port 1

Figure 4.5: Current sources driving a linear 2-port network

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} + \begin{bmatrix} v_{oc_1} \\ v_{oc_2} \end{bmatrix} \tag{4.28}$$

For the circuit in Fig. 4.5c to be equivalent to that in Fig. 4.5b, v_1 and v_2 need to be the same. This results in the form v and i take.

$$\begin{bmatrix} v_1 - v \\ v_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} i_1 - i \\ i_2 \end{bmatrix} \tag{4.29}$$

$$Z_{11}i_1 + Z_{12}i_2 + v_{oc_1} = Z_{11}(i_1 - i) + Z_{12}i_2 + v \tag{4.30}$$

$$Z_{21}i_1 + Z_{22}i_2 + v_{oc_2} = Z_{21}(i_1 - i) + Z_{22}i_2 \tag{4.31}$$

$$i = \frac{-v_{oc_2}}{Z_{21}} \quad \wedge \quad v = v_{oc_1} - \frac{Z_{11}}{Z_{21}} v_{oc_2} \tag{4.32}$$

Consequently, a noisy linear 2-port network can be treated as a noiseless version of itself with two noise sources at its input, a voltage one and a current one.

4.3.2 Optimum noise impedance

A noisy linear 2-port network being driven by a current source with noisy internal admittance $Y_S = G_S + jB_S$ is shown in Fig. 4.6. Its internal noise sources have been drawn in their equivalent input referred form, therefore N_0 is noiseless. The following hold.

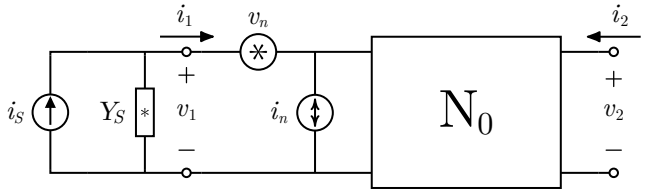


Figure 4.6: Noisy 2-port being driven by a noisy source

$$F = F_{min} + \frac{R_n}{G_S}|Y_S - Y_{opt}|^2 = F_{min} + 4\frac{R_n}{Z_0}\frac{|\Gamma_S - \Gamma_{opt}|^2}{|1 + \Gamma_{opt}|^2(1 - |\Gamma_S|^2)} \tag{4.33}$$

- F_{min}: minimum noise factor across source admittances
- R_n: equivalent noise resistance related to v_n (Ω)
- Y_{opt}: the source admittance which minimizes the noise factor (Ω^{-1})

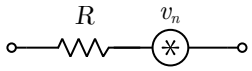
These quantities depend on a lot of parameters, however given a linear 2-port network at a specific operating frequency the optimum noise impedance Z_{opt} can be determined. An arbitrary source impedance Z_S can be transformed using matching networks to be close to the optimum noise impedance Z_{opt}, in order to achieve the minimum possible noise factor NF_{min}, usually trading-off with input matching.

4.4 Types of noise in electronic components

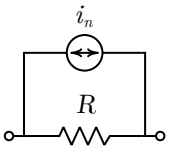
Every electronic component generates some intrinsic noise, even in the absence of an external signal. The most common sources of noise include thermal agitation of charge carriers, the discrete nature of electric charge, and irregularities in semiconductor behavior. Note that the following power spectral densities are bilateral ($f \in \mathbb{R}$).

4.4.1 Thermal noise

Thermal noise or Johnson–Nyquist noise is generated by the random thermal motion of charge carriers inside an electrical conductor or semiconductor. It is approximately white, meaning that its power spectral density is constant nearly throughout the frequency spectrum. In the following models the resistors and impedances are noiseless.

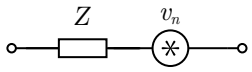


(a) $S_{v_n}(f) = 2\,k_B\,T\,R\,\eta(f)$

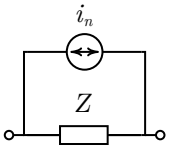


(b) $S_{i_n}(f) = 2\,k_B\,T\,G\,\eta(f)$

Figure 4.7: Thermal noise models for resistors



(a) $S_{v_n}(f) = 2\,k_B\,T\,\mathrm{Re}[Z(j2\pi f)]\,\eta(f)$



(b) $S_{i_n}(f) = 2\,k_B\,T\,\mathrm{Re}[Y(j2\pi f)]\,\eta(f)$

Figure 4.8: Thermal noise models for complex impedances

The quantum mechanical factor $\eta(f)$ is approximately 1 for the frequencies in conventional electronics.

$$\eta(f) = \frac{\dfrac{hf}{k_B T} - 1}{\exp\left(\dfrac{hf}{k_B T}\right) - 1} \tag{4.34}$$

A complex impedance delivers its available noise power under conjugate matching.

$$N_{av} = k_B T B \tag{4.35}$$

- $k_B = 1.380649 \cdot 10^{-23}\,\mathrm{J \cdot K^{-1}}$: Boltzmann's constant
- T: absolute temperature (K)
- B: signal bandwidth (Hz)
- $h = 6.62607015 \cdot 10^{-34}\,\mathrm{J \cdot s}$: Planck's constant

4.4.2 Shot noise

Shot noise results from fluctuations of the electric current when charge carriers cross a gap. If electrons flow across a barrier, they have discrete arrival times, which can be modeled by a Poisson process. Those discrete arrivals are the cause shot of noise. An example of such a barrier is the junction in a diode.

$$S_{i_n}(f) = qI_{DC} \tag{4.36}$$

- q: elementary charge (C)
- I_{DC}: bias current of the junction (A)

4.4.3 Flicker noise

Flicker noise occurs in almost all active electronic devices and results from a variety of effects. At high frequencies it is overshadowed by white noise from other sources.

$$S_{i_n}(f) = K\frac{I^b}{f^a} \tag{4.37}$$

- I: bias current (A)
- a, b, K: parameters, usually $a \approx 1$

4.4.4 Burst noise

Burst occurs in semiconductors and ultra-thin gate oxide films. It consists of sudden step-like transitions between two or more discrete voltage or current levels at random and unpredictable times. Each shift in offset voltage or current lasts for several milliseconds to seconds.

4.4.5 Generation - Recombination (G-R) noise

Generation–recombination noise is caused by the fluctuation of the generation and recombination of electrons in semiconductor based photon detectors.

$$S_{i_n}(f) = C\frac{I^c}{1 + (2\pi f\tau)^2} \tag{4.38}$$

- τ: charge carrier lifetime (s)
- I: bias current (A)
- c, C: parameters

4.5 Transistor noise

Transistors exhibit most of the types of noise already mentioned. A noise model for MOSFETs including thermal noise, shot noise, and flicker noise is shown in Fig. 4.9. Leakage current through the gate is typically very small, thus shot noise is usually omitted, as in Fig. 4.10. The following power spectral densities are unilateral ($f \geq 0$).

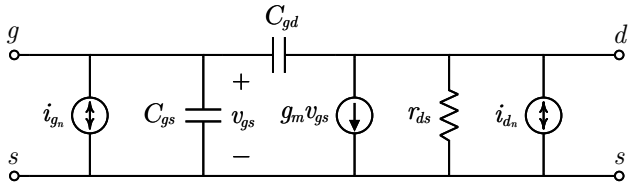


Figure 4.9: MOSFET small signal equivalent circuit with noise sources

$$S_{i_{g_n}}(f) = 2qI_G \quad \wedge \quad S_{i_{d_n}}(f) = 4k_BT\gamma g_m + K\frac{I_D^a}{f} \tag{4.39}$$

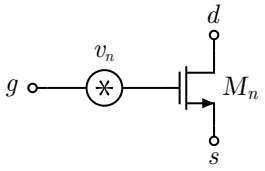


Figure 4.10: Gate referred noise neglecting shot noise

$$S_{v_n}(f) = \frac{4k_BT\gamma}{g_m} + \frac{K_f}{WLC_{ox}^2 f} \tag{4.40}$$

- I_D: drain DC current (A)
- I_G: gate DC leakage current (A)
- K, K_f: process dependent constants
- W, L: channel width and length of the MOSFET (m)
- C_{ox}: gate oxide capacitance per unit area (F/m^2)
- γ: excess noise factor, 2/3 to 1 for long channel MOSFETs, 2 to 3 for short channel devices due to velocity saturation

There is another component of noise that is usually insignificant at low frequencies but important at very high frequencies. At an arbitrary point in the channel, the gate to channel voltage has a random component due to fluctuations along the channel caused by thermal noise. These voltage variations generate a noisy AC gate current, due to the capacitance between the gate and channel. This noise is called violet noise and it is correlated with the thermal noise in the channel because both noise currents stem from thermal fluctuations in the channel.

$$S_{i_{g_n}}(f) = \frac{16}{15}k_BT\omega^2C_{gs}^2 \tag{4.41}$$

Having considered all of the above, the important takeaway for RFIC design is that the minimum noise figure of a given MOSFET as a 2-port element during small signal approximation at a specific frequency practically depends only on the ratio of the drain bias current over the channel width. For BJTs the minimum noise figure effectively depends only on the ratio of the collector bias current over the emitter area.

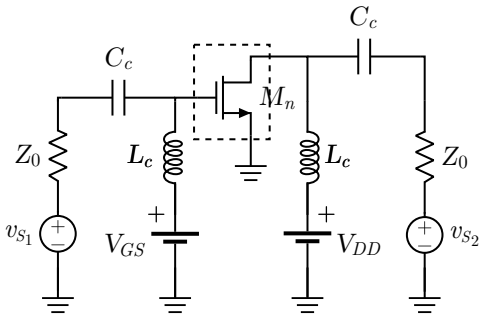


Figure 4.11: Transistor measurement setup

Utilizing the setup containing coupling capacitors and RF chokes presented in Fig. 4.11, the S-parameters of the transistor along with the minimum noise figure can be extracted. By varying V_{GS} the minimum noise factor at a specific operating frequency can be extracted as a function of drain current over channel width.

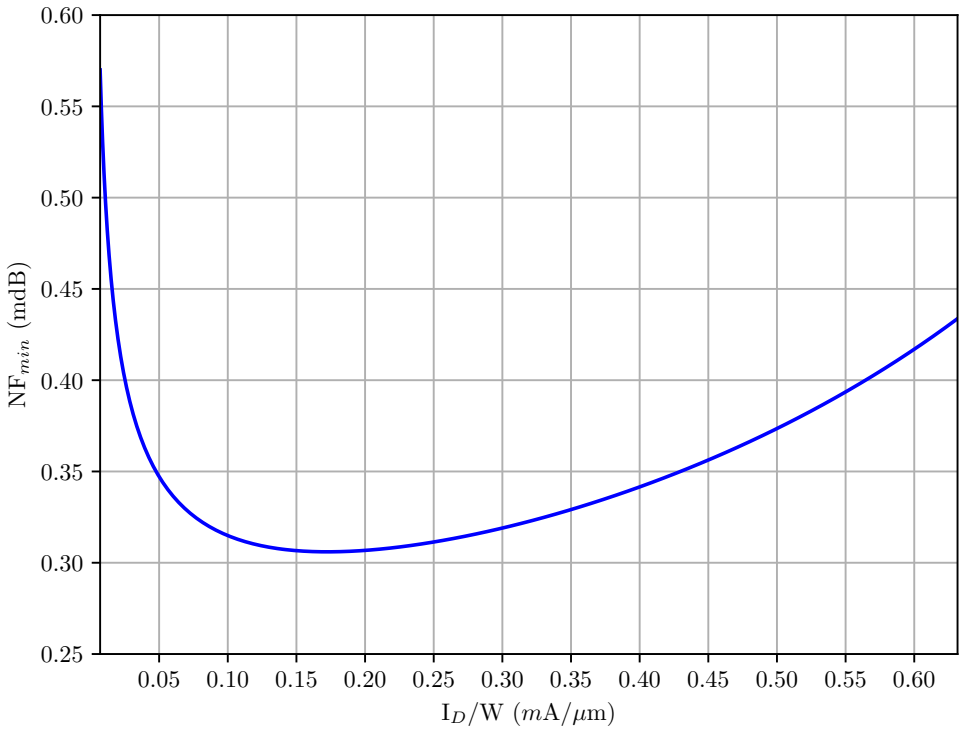


Figure 4.12: Minimum noise figure with respect to drain current over channel width at 7.7 GHz for a GF22 FD-SOI transistor

As shown in Fig. 4.12, the minimum noise figure of a transistor at a specific operating frequency minimizes at a certain value of I_D/W. This optimum value is around $0.15\,mA/\mu m$ for long channel devices and between 0.1 and $0.2\,mA/\mu m$ for deep sub-micron devices. Width is usually chosen in accordance with desired gain and for low noise performance, transistors should be biased at that optimum current "density", before noise matching.

Additionally, it should be noted that for a transistor at a specific bias point, its noise figure is larger at higher frequencies, as shown in Fig. 4.13, where the transistor being studied has been biased at the optimum current for operation at 7.7 GHz.

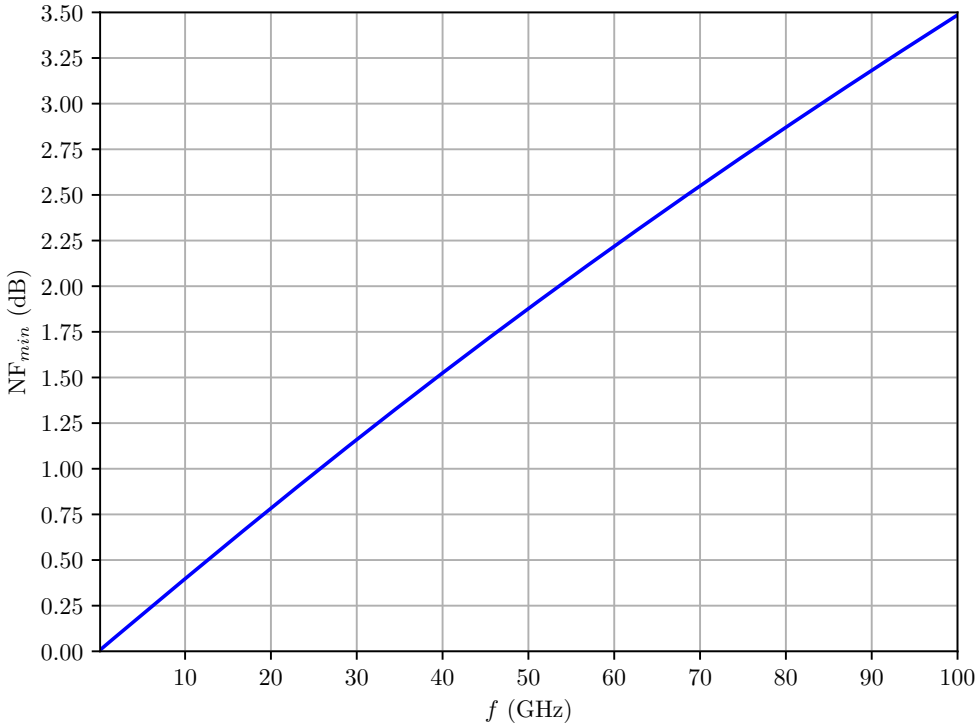


Figure 4.13: Minimum noise figure with respect to frequency for a GF22 FD-SOI transistor

Chapter 5

Low noise amplifier design

Traditionally, designing a low noise amplifier (LNA) was done with discrete components. This involved selecting a transistor which, at a specific operating frequency, could deliver gain with an appropriate optimum minimum noise figure, then it would be biased with the optimum current. This specified the S-parameters of the transistor as a 2-port, the minimum noise figure, and the optimum noise impedance at the operating frequency. Afterwards, the remaining design choices were about passive matching networks at the input and the output, trading off gain, noise matching, and impedance matching at the input and the output. This was performed with gain and noise circles in the complex plane, the Γ_S and Γ_L Smith charts.

The flexibility of modern IC design has allowed for the integration of the entire LNA architecture. This provides the advantage of directly interfering with the transistor's S-parameters and optimum noise impedance in order achieve better performance. Since finding balance between all the trade offs in traditional design was extremely difficult, modern design focuses on the trade off between input matching and noise matching, while achieving output matching independently and sufficient gain by transistor sizing. However, transistor sizing interferes with input matching and noise matching, therefore the trade off between them all still exists. There is greater flexibility with the cost of more challenging design.

Designs do not necessarily involve only a single transistor but an active 2-port network in general. This could be a cascode or multiple stages that could require matching between them. The key difference between traditional design and modern design is that traditionally the S-parameters referred to the active 2-port network providing the gain, while now they refer to the entire LNA as a 2-port network. This does not mean that traditional ideas and principles are inapplicable. On the contrary, the same methods are still in use only with different equipment.

The LNA design specifications involve the S-parameters of the LNA as a 2-port network, its noise figure, its stability, its linearity, and power consumption. The characteristic impedance of the system is assumed to be $50\,\Omega$ and the S-parameters are measured with $50\,\Omega$ terminations. The specification for S_{11} stems from input matching requirements, usually to an antenna, while S_{22} is specified according to output matching requirements of a load, which could be the input impedance of a mixer, not necessarily a $50\,\Omega$ termination. Instead of gain, S_{21} which is related to it is specified. Reverse isolation is given as a specification for S_{12}. Because source and load impedances might vary, such as an antennas when the environment changes, stability must be unconditional and could be given as a specification for K or μ across a frequency band much wider than the operating band. Power consumption is specified as an upper limit to quiescent power consumption.

5.1 Noise circles

Noise circles are contours of constant noise factor plotted on the Smith chart, specifically on the source reflection coefficient Γ_S plane. For an achievable fixed noise factor $F_0 > F_{min}$ the following hold.

$$F_0 = F_{min} + 4\frac{R_n}{Z_0}\frac{|\Gamma_S - \Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2(1-|\Gamma_S|^2)} \iff |\Gamma_S - \Gamma_{S_0}| = R_0 \tag{5.1}$$

$$\Gamma_{S_0} = \frac{\Gamma_{opt}}{1+N_0} \quad \wedge \quad R_0 = \sqrt{N_0\frac{N_0+1-|\Gamma_{opt}|^2}{(1+N_0)^2}} \quad \wedge \quad N_0 = \frac{|1+\Gamma_{opt}|^2}{4R_nY_0}(F_0 - F_{min}) \tag{5.2}$$

This implies that minimum noise factor is achievable only with the optimum noise impedance and a specific larger noise factor can be achieved by terminating with source reflection coefficients belonging to a circle in the complex plane centered at Γ_{S_0} with radius R_0. Every reflection coefficient within a noise circle belongs to a different noise circle with a noise factor smaller than the one corresponding to the initial noise circle. As noise factor grows, the circle's center moves towards zero along the optimum noise reflection coefficient vector and the radius grows approaching unity, encircling the entire Smith chart.

Traditionally, the source reflection coefficient seen by the active 2-port network would be tuned to a different value than the actual source's utilizing a passive matching network at the input in order to achieve a desired noise factor greater than the minimum.

In modern designs viewing the entire LNA as a 2-port the source impedance seen by the 2-port is always $50\,\Omega$, therefore the point is to tune the optimum noise impedance to be $50\,\Omega$ or for the smallest noise circle encircling the origin of the Smith chart ($\Gamma_S = 0$) to correspond to an acceptable noise factor.

In practice, the real part of the optimum noise impedance R_{opt} is tuned to $50\,\Omega$ by transistor sizing and the imaginary part of the optimum noise impedance X_{opt} is tuned out by an inductive element at the input. In general, at a specified frequency, making a device larger leads to a smaller R_{opt}.

Noise matching is always in a trade off with input matching because it is extremely difficult to ensure that a 2-port network's optimum noise reflection coefficient is the source's reflection coefficient ($\Gamma_{opt} = 0$, for $Z_S = 50\,\Omega$).

5.2 Gain circles

Gain circles are contours of constant gain plotted on a Smith chart. They help visualize how the gain of a 2-port network varies with different source or load terminations and they aid the design of matching networks.

$$G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2 - |S_{11} - \Delta\Gamma_L|^2} \implies G_P = G_L|S_{21}|^2 \tag{5.3}$$

$$G_S = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2 - |S_{22} - \Delta\Gamma_S|^2} \implies G_A = |S_{21}|^2 G_S \tag{5.4}$$

5.2.1 Power gain circles

For a specific achievable G_{L_0} the following hold in the case of unconditional stability. The load reflection coefficients achieving G_{L_0} belong in a circle. Every load reflection coefficient inside that gain circle belongs to a different gain circle corresponding to a larger value of G_{L_0}. Maximum G_L is achieved for a single load reflection coefficient.

$$|\Gamma_L - \Gamma_{L_{P_0}}| = R_{P_0} \tag{5.5}$$

$$\Gamma_{L_{P_0}} = \frac{G_{L_0}(S_{22}^* - \Delta^* S_{11})}{1 + G_{L_0}(|S_{22}|^2 - |\Delta|^2)} \quad \wedge \quad R_{P_0} = \frac{\sqrt{1 - 2K|S_{12}S_{21}|G_{L_0} + |S_{12}S_{21}|^2 G_{L_0}^2}}{|1 + G_{L_0}(|S_{22}|^2 - |\Delta|^2)|} \tag{5.6}$$

$$G_{L_{max}} = \frac{1}{|S_{12}S_{21}|}\left(K - \sqrt{K^2 - 1}\right) \implies G_{P_{max}} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right) \tag{5.7}$$

For a given load reflection coefficient Γ_L, maximum output power is achieved with conjugate matching at the input, $\Gamma_S = \Gamma_{in}^*$. In that case, transducer gain becomes equal to power gain $G_T = G_P$.

5.2.2 Available gain circles

For a specific achievable G_{S_0} the following hold in the case of unconditional stability. The source reflection coefficients achieving G_{S_0} belong in a circle. Every source reflection coefficient inside that gain circle belongs to a different gain circle corresponding to a larger value of G_{S_0}. Maximum G_S is achieved for a single source reflection coefficient.

$$|\Gamma_S - \Gamma_{S_{A_0}}| = R_{A_0} \tag{5.8}$$

$$\Gamma_{S_{A_0}} = \frac{G_{S_0}(S_{11}^* - \Delta^* S_{22})}{1 + G_{S_0}(|S_{11}|^2 - |\Delta|^2)} \quad \wedge \quad R_{A_0} = \frac{\sqrt{1 - 2K|S_{12}S_{21}|G_{S_0} + |S_{12}S_{21}|^2 G_{S_0}^2}}{|1 + G_{S_0}(|S_{11}|^2 - |\Delta|^2)|} \tag{5.9}$$

$$G_{S_{max}} = \frac{1}{|S_{12}S_{21}|}\left(K - \sqrt{K^2 - 1}\right) \implies G_{A_{max}} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right) \tag{5.10}$$

For a given source reflection coefficient Γ_S, maximum output power is achieved with conjugate matching at the input, $\Gamma_L = \Gamma_{out}^*$. In that case, transducer gain becomes equal to available gain $G_T = G_A$.

Since available gain circles and noise circles both refer to source reflection coefficients Γ_S, they can be plotted on the same Smith chart and the trade offs between gain and noise figure can be studied. Additionally, for conjugate matching both at the input and the output, all gains become equal and transducer gain takes its maximum value.

$$\Gamma_{in} = \Gamma_S^* \quad \wedge \quad \Gamma_{out} = \Gamma_L^* \implies G_P = G_A = G_T = G_{T_{max}} \tag{5.11}$$

5.3 Design specifications

In LNA design, specifications focus on optimizing performance for weak signal reception in RF systems. The most critical parameter is noise figure, which must be minimized. Gain is also important, in order to ensure sufficient amplification. Input and output matching to is necessary for maximum power transfer and minimal reflections. Additional specifications include stability over frequency and temperature, linearity metrics, bandwidth, and power consumption.

The subject of this thesis was decided to be the design of a LNA operating frequency at 7.7 GHz for reasons explained in 2.3, in GlobalFoundries' 22nm Fully Depleted Silicon on Insulator (22FDX) semiconductor process technology. This process was designed for low power, high performance applications, particularly in areas where cost, energy efficiency, and integration flexibility are key. It offers body biasing capability, reduced leakage, and better noise performance, due to a layer of buried oxide electrically isolating the bodies of transistors from the substrate. The aim was to push the design to the limit, especially regarding its noise figure. Additionally, it was decided that the LNA be matched to a 50 Ω impedance instead of another load, for example a capacitive mixer input impedance.

Since pushing to the limit was the goal, the cascode topology was selected for the job. In order to maximize noise performance and linearity, a two stage approach was followed, as shown in 5.4. This consisted of a single ended cascode as the first stage, optimized for noise performance with enough gain to suppress the noise of the second stage and a differential cascode as the second stage for better linearity suppressing second order harmonics, due to its differential nature. The transition from single ended to differential signaling and back necessitated the use of balancing units (baluns), formerly called balanced to unbalanced transformers.

In the following tables some, literature data from low noise amplifiers in deep submicron CMOS processes are presented. Especially those in 22nm CMOS FD-SOI can be used for comparison with the results of this thesis. It should be noted that many of these designs pursued goals such as wideband or multi-band operation, ultra low power consumption, gain and not strictly the minimization of noise figure. Additionally, these designs were fabricated, whereas the design presented in this thesis was not intended for tapeout.

Paper	**Process**	**Frequency (GHz)**	**Gain (dB)**	**NF (dB)**
Gholami [1]	22nm FD-SOI	16–21.2	20	3.3
Ouyang [2]	22nm FD-SOI	17.8–42.4	18.3	2.9–4.9
Fu [3]	22nm FD-SOI	23.3-30.3 / 38-44.7	22 / 16	2.55 / 4.75
Xu [4]	22nm FD-SOI	60	20	3.3
Spasaro [5]	22nm FD-SOI	30	8-18	6-7
Cui [6]	22nm FD-SOI	22–32	21.5	1.7 - 2.2
Mousavi [7]	180nm CMOS	3-8	18.7	3.7
Han [8]	45nm SOI	17-38	23	4

Table 5.1: Overview of modern nanometer CMOS LNA designs: process, frequency, gain, and noise figure

Paper	**Power (mW)**	**IP1dB / IIP3 (dBm)**	**S11 / S22 (dB)**
Gholami [1]	15	-20 / –	-10 / -10
Ouyang [2]	15.8	-17.9 / -8.5	-10 / -10
Fu [3]	18	-17.2 – -30.6 / -10.3 – -21.6	-10 / -10
Xu [4]	8.1	-29.3 / –	-20 / -20
Spasaro [5]	0.52	-25.5 / -15	-20 / -20
Cui [6]	17.3	– / -13.4	-10 / -10
Mousavi [7]	14.6	– / -9.5	-10 / –
Han [8]	59	– / –	-10 / –

Table 5.2: Overview of modern nanometer CMOS LNA designs: power consumption, linearity, and matching

Paper	**Notes**
Gholami [1]	Wideband LNA-filter design
Ouyang et al [2]	Broadband mmWave application
Fu [3]	Concurrent LNA for 5G with dual-band notch filter
Xu [4]	Gain-scalable mmWave with back-gate tuning
Spasaro [5]	Ultra low power variable gain LNA
Cui [6]	LNA with magnetic feedback matching network
Mousavi [7]	Ultra wideband design
Han [8]	High power mmWave with multi-band matching

Table 5.3: Overview of modern nanometer CMOS LNA designs: notes

5.4 Design topology

The cascode configuration is a popular topology in low noise amplifier design due to its favorable high-frequency performance. It exhibits high gain utilizing a common source stage followed by a common gate stage. It offers improved reverse isolation in comparison with the simple common source stage, which improves stability. It has reduced maximum output voltage swing, but performs better with regards to some non linear effects. All these come with the cost of more complex design, area consumption, and slightly higher noise figure than a single common source stage.

In order to achieve good performance in both noise figure and linearity with sufficiently high gain, while keeping design complexity relatively low, a two stage approach was appropriate. The first stage is optimized for noise performance, while the second one for linearity. If wideband performance is desired, two stages might not be enough and the idea of multiple stages tuned to perform at different frequencies within the band may be applicable.

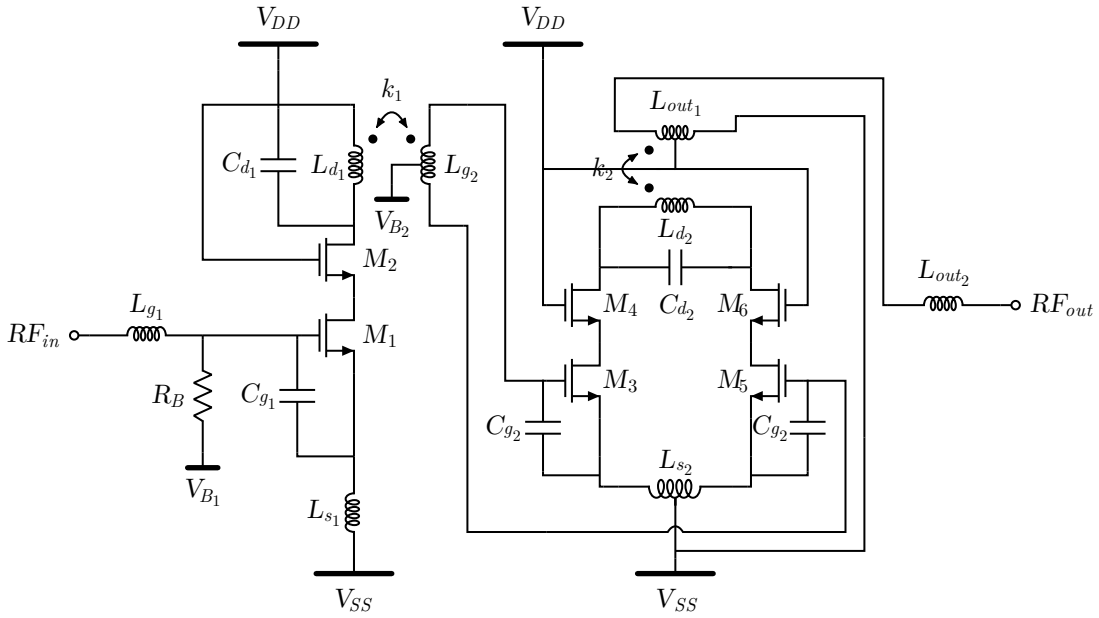


Figure 5.1: The LNA topology of this thesis

For this thesis, the topology chosen to be used is shown in Fig. 5.1. A supposed antenna delivers a single ended signal, therefore the first stage is single ended. The cascode is biased for high enough gain to suppress the noise of the second stage and optimum minimum noise figure. It is also noise matched. Linearity is mainly affected by the second stage, thus a differential stage is used, which suppresses all even order harmonics, while also rejecting common mode noise. The second stage is biased for linear performance and high gain, and its excess noise is suppressed by the gain of the first stage in the total noise figure. The design is supposed to be a standalone LNA, and thus the signal is converted back to single ended at the output.

The conversion of the signal from balanced to unbalanced and vice versa requires balancing units which are implemented with on chip transformers in RFIC design. These are an important part of the design and they require special attention, because the interface between stages can ruin performance if it is poorly implemented.

5.5 Design methodology

When a design process and a specific topology for a low noise amplifier design have been decided there are some general steps that need to be followed. First of all, transistor testbenches must be performed, utilizing the setup of Fig. 5.2. Minimum noise figures must be extracted and compared with design manual cases that have been measured. Transistor sizes that achieve sufficient gain must be explored.

Secondly, inductor testbenches must be performed, in order to verify potential PDK models. For inductors, the designer has the liberty to create their own models by electromagnetic simulation of structures. These structures can be custom made or contained in the PDK. Such matters are explained in detail in 6.

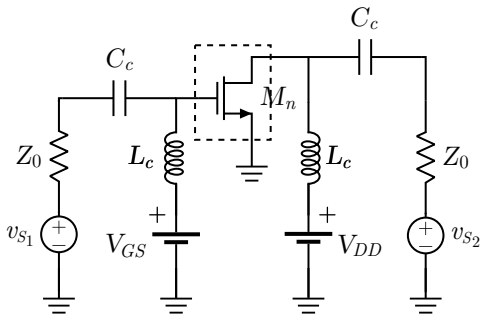


Figure 5.2: Transistor testbench

Schematic design with completely ideal elements can be done only very early on and only to give general ideas. Realistic models of structures, such as inductors, capacitors, resistors, and transformers should be used as early as possible. Regarding the specific topology of this thesis, the design flow goes as follows. After general testbenches, some input and output parasitics should be considered, especially since this block is the first in the RF front end. This is discussed in 8. Then the two stages are designed separately. The first stage is biased for optimal noise performance and sufficiently high gain, while noise matching is traded off with input matching. The second stage is biased for linear performance with high gain, and output matching is performed.

After achieving adequate performance with both stages, interstage matching needs to be performed. This entails design and simulation of transformers to be used for impedance matching and as balancing units. Such matters are explored in detail in 7. This is where all the extra capacitances at the drains and at the gates are used. They tune input and output impedances of stages in order to aid matching for maximum power transfer.

Finally, layout must be performed. Firstly, transistor interconnects need to be raised to top level metals, in order to make RF interconnects. Secondly, interconnects between the transistors in the cascodes need to be made. It can be argued that this should be done as early on as possible as well, before noise matching. However, transistor sizing is involved in noise matching, which would require changing the interconnects every time.

After transistor layout has taken place and everything has been modeled either with parasitic extraction or electromagnetic simulation, general placement of components is needed. Inductors need to be sufficiently spaced apart so that magnetic feedback that can cause instability is avoided. After all that, RF interconnects and pads are to be placed and modeled. Post layout simulations must follow. For this thesis, due to high frequency performance requirements and the general distrust towards the inductances provided by parasitic extraction, all interconnects are modeled by electromagnetic simulation.

The steps discussed are summarized in the following lists. Note that after every layout stage and modeling of interconnects, some components may need tuning in order to maintain performance. After all, before including the parasitic extraction or electromagnetic models of interconnects, they are considered ideal short circuits. It is critical that everything is properly modeled and performance is maintained after every step.

General first steps:

- Transistor testbenches: minimum noise figure, optimum noise impedance, sufficient gain, sizing.
- Inductor testbenches: electromagnetic simulation, verification of PDK models.

First stage design:

- Biasing for optimal noise performance and sufficient gain.
- Input matching and noise matching.

Second stage design:

- Biasing for linear performance and sufficient gain.
- Output matching.

Interstage matching design:

- Transformer testbenches: electromagnetic simulation.
- Input and output impedance tuning and matching.

Layout:

- Transistor contact to higher metals.
- Interconnects between transistors.
- Component placement, especially inductors.
- RF interconnects and pads.

Chapter 6

Integrated inductors

In circuit design and especially in microwave amplifier design, inductive elements are necessary. In distributed networks, they are required for impedance matching and can be implemented using transmission lines. In general, they can be implemented with coils of wires. Modern IC fabrication and the use of higher frequencies have allowed for full integration of inductors inside chips. At high frequencies, even a piece of interconnect metal can become inductive. Even more obviously, a spiral of interconnect metal behaves as an inductor at a specific range of high frequencies.

These integrated inductors are extremely difficult to model and evaluate, therefore thorough electromagnetic simulations using reliable EDA tools are required. For convenient use of results, the structure being simulated is treated as an n-port and its S-parameters are extracted from electromagnetic fields. Nevertheless, the extraction of lumped element models is also desired, because they can establish connections between geometric parameters of the inductor to circuit element parameters, while S-parameters are more abstract. This can eliminate the need for extensive simulation of a lot of structures. A good lumped element model verified for some structures can be predict the behavior of similar structures very well, without the need for time consuming electromagnetic simulations.

6.1 Layout and electromagnetic simulation

Integrated inductors are designed by making spirals out of metals normally intended for RF interconnects. These are thick metals usually higher in a design process stackup, because small sheet resistance and low capacitive coupling to substrate are required.

In Fig. 6.1, a 500 pH at 7.7 GHz inductor from the RF library of GF22 FD-SOI process is shown. It has an inner diameter of 95.04 μm, a turn width of 10.57 μm and consists of 1.5 turns of two stacked top level metals connected with continuous vias, in order to minimize its resistance. An electromagnetic simulator, such as HFSS, EMX, and Momentum, would be used to examine the behavior of this structure within a frequency range of interest.

For any electromagnetic simulation of integrated structures, the simulator needs information about local ground along with the process stackup. For instance, EMX by default assumes an infinite perfect ground plane under the substrate. For external excitation, pins need to be created on the structure defining the direction of incoming signals. These are treated by the simulator as ports. They are short circuited and fed external input in the form of voltage or current sources. Many simulators, such as HFSS, can show electromagnetic fields, but for circuit design the S-parameters are usually sufficient and they are extracted from electromagnetic fields.

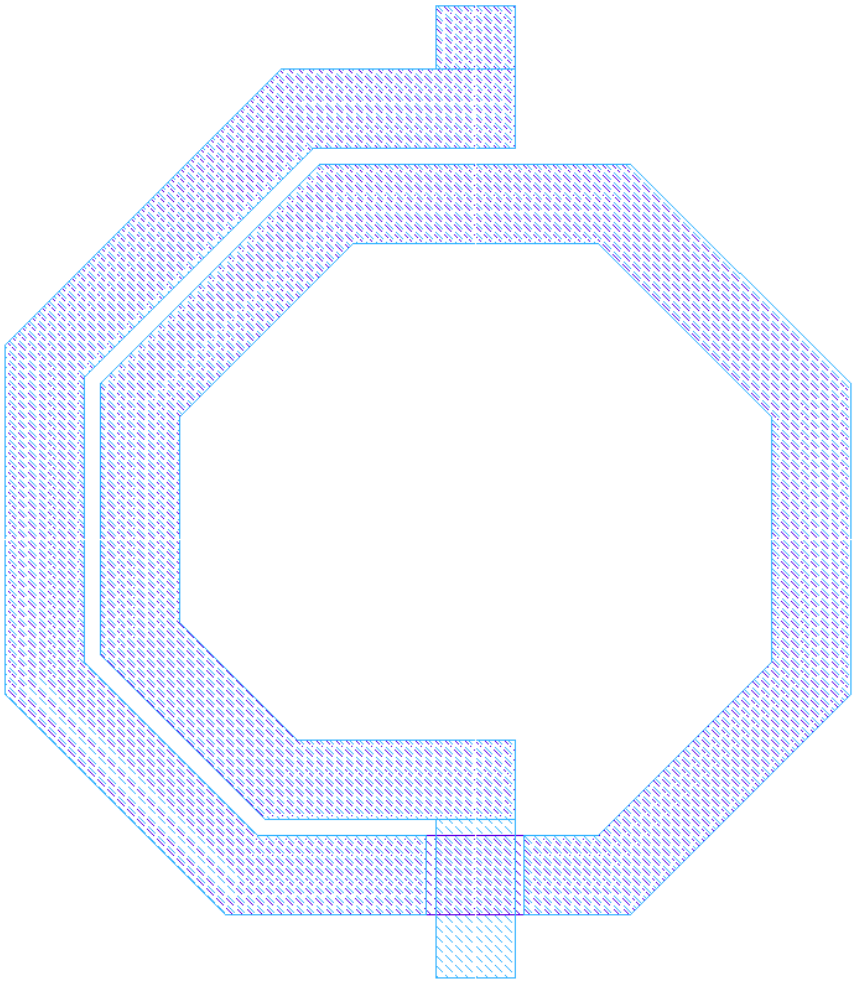


Figure 6.1: A 500 pH inductor from the GF22 FD-SOI RF library

6.2 Parameter extraction

After the extraction of S-parameters of an electromagentic structure, it is necessary to obtain some understanding about its behavior as a circuit element. For example, assuming the inductor of Fig. 6.1 has been simulated, this has resulted in a 2-port S-parameters file (.s2p). Suppose the setup of Fig. 6.2 for S-parameter extraction of a simple series impedance as a 2-port network. The Y-parameters can be extracted from the S-parameters, as explained in 3.2.

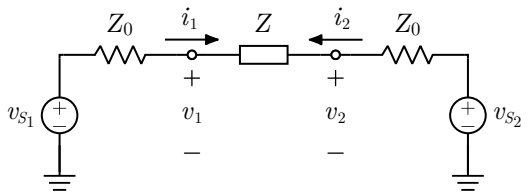


Figure 6.2: A series impedance as a 2-port network

$$\mathbf{Y} = \begin{bmatrix} Y & -Y \\ -Y & Y \end{bmatrix} \tag{6.1}$$

Therefore, in order to confirm that the electromagnetic structure simulated indeed behaves as an inductor, Y-parameter extraction from its S-parameters is performed. The matrix should be symmetric due to reciprocity anyway, and if the 4 Y-parameters are approximately equal and of the correct form, the structure indeed behaves as an inductor. The correct form of the Y-parameters for an inductor would be a hyperbolic magnitude as a function of frequency and $-90°$ phase.

The simplest realistic model for an inductor is its self inductance in series with its resistance, since any conductor exhibits some Ohmic resistance. The quality factor of such an inductor is defined as a measure of how strong the presence of said resistance is in comparison with said inductance. For high quality factor inductors, the resistance is negligible.

$$Q = \frac{\omega L}{R} \implies Z = R + j\omega L = j\omega L \left(1 - \frac{j}{Q}\right) \tag{6.2}$$

$$Y = \frac{1}{Z} = \frac{1}{R + j\omega L} \tag{6.3}$$

If the simulated 2-port behaves like an inductor, its parameters can be extracted as follows. For the inductor in Fig. 6.1, three different electromagnetic simulators were used to extract its parameters, in order to evaluate the available PDK models.

$$L = \frac{1}{2\pi f}\mathrm{Im}\left[\frac{1}{Y_{11}}\right] \quad \wedge \quad R = \mathrm{Re}\left[\frac{1}{Y_{11}}\right] \quad \wedge \quad Q = \frac{\mathrm{Im}\left[\frac{1}{Y_{11}}\right]}{\mathrm{Re}\left[\frac{1}{Y_{11}}\right]} \tag{6.4}$$

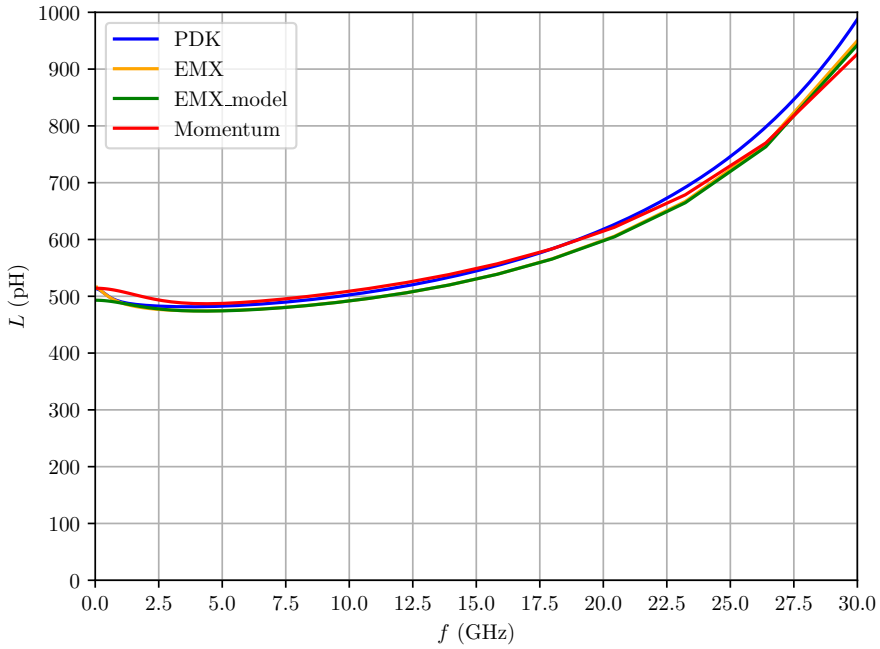


Figure 6.3: Self inductance with respect to frequency

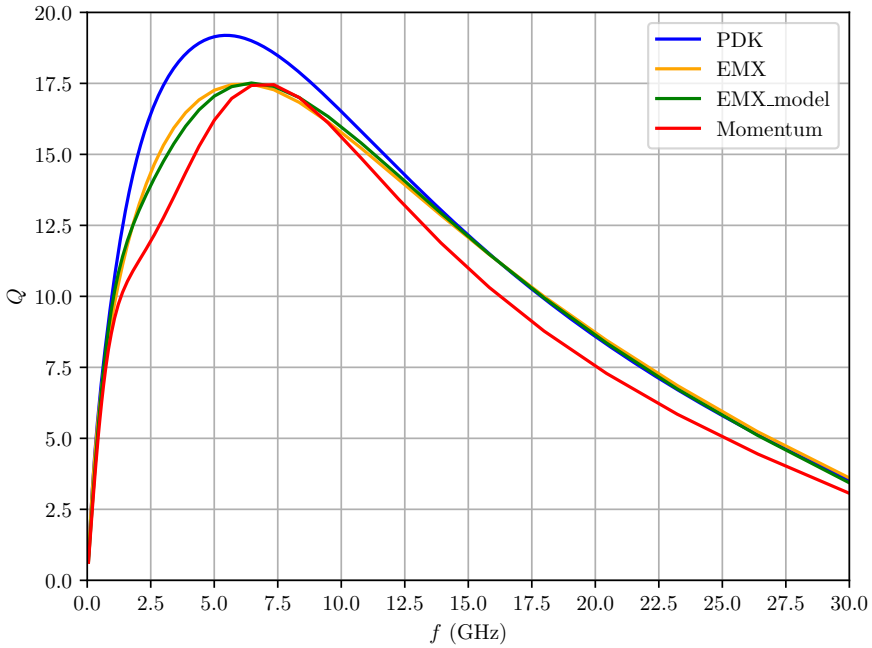


Figure 6.4: Quality factor with respect to frequency

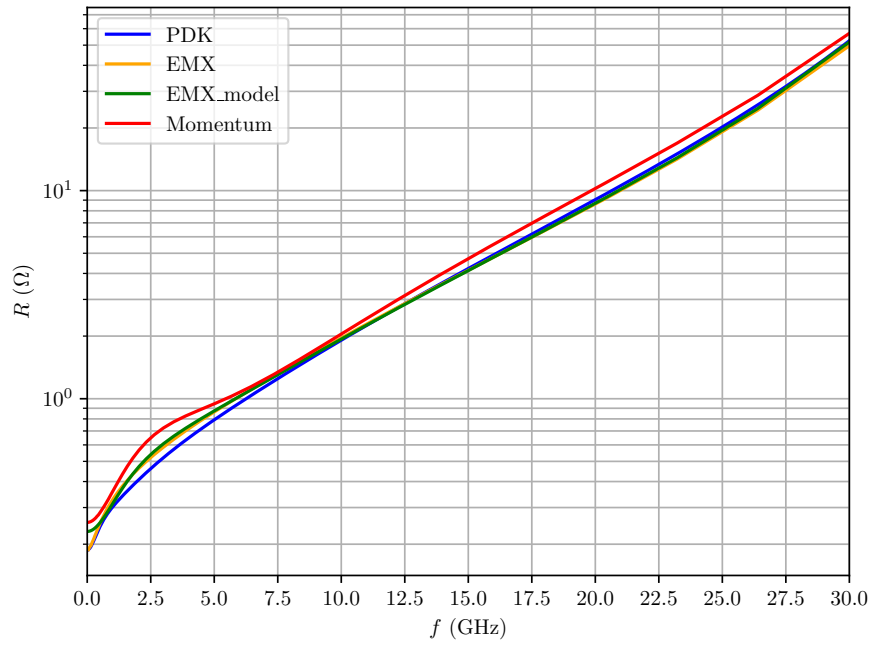


Figure 6.5: Resistance with respect to frequency

Of course, the inductor's parameters do not remain the same across frequency, because the structure's behavior is very complex. For example, resistance changes with frequency due to skin effect. However, for a frequency range around 7.7 GHz, the structure is a well behaved inductor.

As frequency increases, capacitive coupling becomes too strong and the whole structure begins behaving like a capacitor. This can be seen in Fig. 6.6, where what has been defined as self inductance becomes negative. The frequency at which the self inductance becomes zero is called self resonance frequency and it marks the transition between inductive and capacitive behavior. It is recommended that the operating frequencies of an inductor be below two thirds (2/3) of the self resonance frequency. For the inductor being studied the operating frequency is 7.7 GHz and the self resonance frequency is 44.35 GHz.

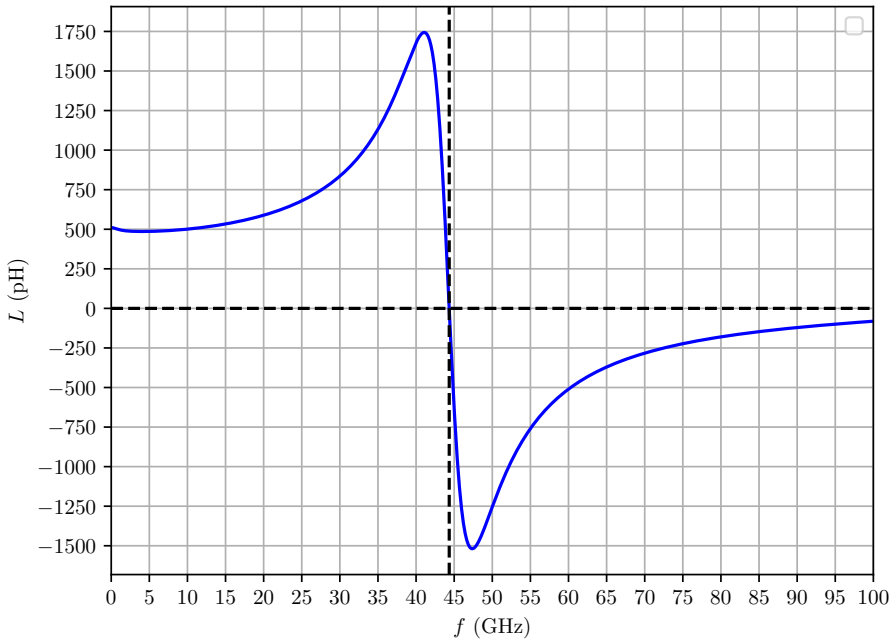


Figure 6.6: Self resonance frequency

The two simulators EMX and Momentum are in agreement with each other and the PDK model performs quite well according to them. The resulting S-parameter files from them can be loaded in a 2-port, like the one in Fig. 6.7, which can be measured in Cadence. Furthermore, EMX has the ability to create lumped element models, such as the on in Fig. 6.8. The lumped elements' parameters are found by curve fitting the S-parameters of the 2-port.

With a lumped element model one can gain intuition about physical phenomena that the abstraction of S-parameters conceals. For example, capacitive coupling is understood through capacitors and leakage currents through resistors. Additionally, it is understandable why such a structure self resonates, since the circuit of Fig.6.8 exhibits capacitive signal paths and at higher frequencies their impedance is much lower than that of inductive paths.

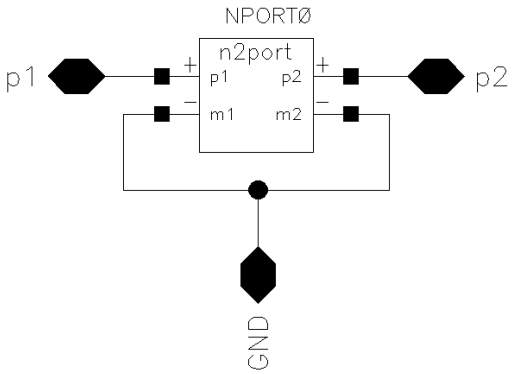


Figure 6.7: A 2-port with the inductor's S-parameter file loaded

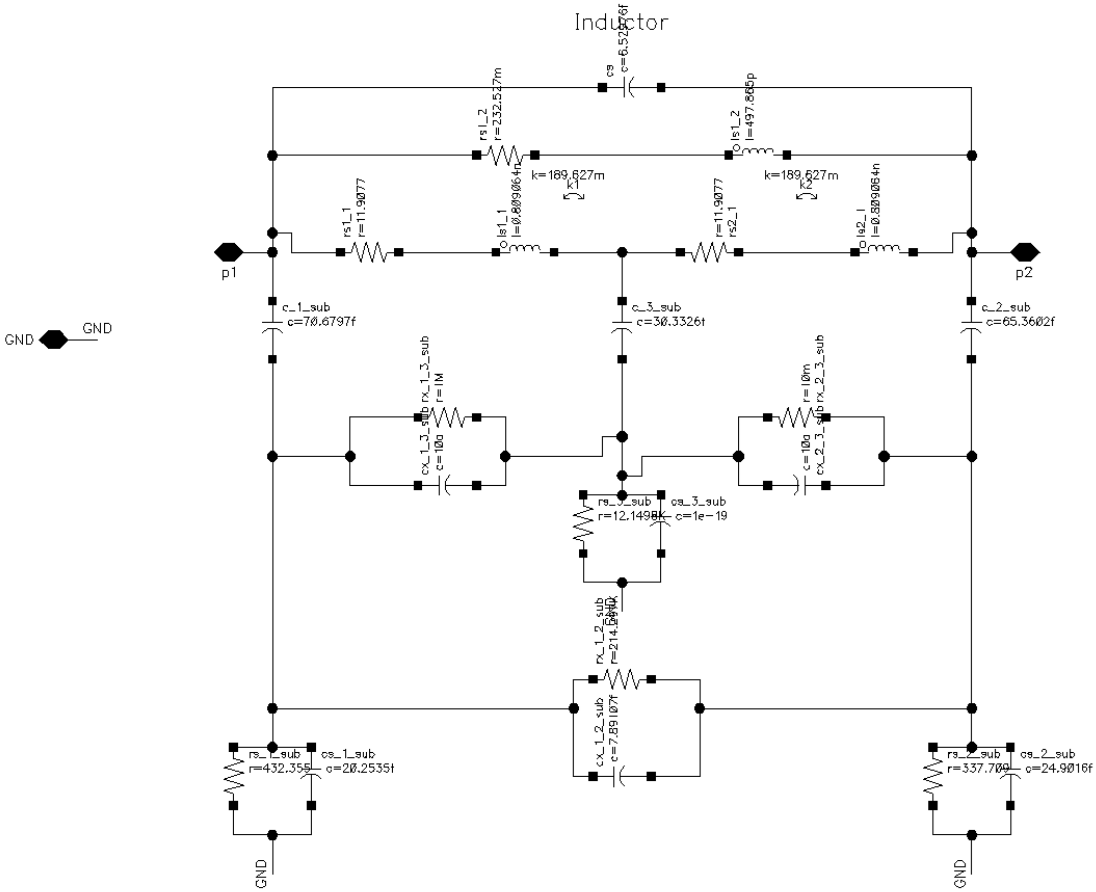


Figure 6.8: Inductor lumped element model

Chapter 7

Interstage matching

In microwave amplifier design, when a single stage does not provide enough gain, a multiple stage approach is necessary. However, this adds the complexity of having to achieve conjugate matching between stages, in order to have maximum power transfer between them. This can be attempted with matching networks containing inductors and capacitors or transmission line stubs. Furthermore, transformers can aid impedance matching through impedance transformation.

Differential amplifiers have some attractive qualities such as suppressing harmonics of even order better noise performance, and usually double the gain of the corresponding single ended stage. However, since antennas are usually single ended, in order to take advantage of a differential stage, a balancing unit (balun) is required to convert the single ended signal to differential.

In practice, there are no ideal transformers, especially on chip where parasitics dominate. The concept of the transformer is approximated by coupled inductors and they can be used as balancing units if they contain a center tap, which is an electrical connection to the middle of one of the windings. With a reference at the center tap the two terminals of the winding can provide a differential signal or be driven by a differential signal. The other winding must have one terminal at the reference and the other terminal is for the single ended signal. Note that a balancing unit is not necessarily a transformer, since there are other types as well.

7.1 Ideal transformers

The ideal transformer is a very simplified model of two magnetically coupled coils. It assumes perfect magnetic coupling without energy losses or magnetizing current, no winding resistance, and no capacitive effects. It can be treated as a 2-port network and its symbol is shown in Fig. 7.1.

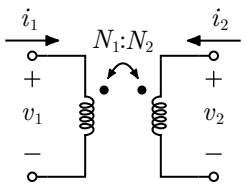


Figure 7.1: Ideal transformer

$$n = \frac{N_1}{N_2} \quad \wedge \quad a = \frac{N_2}{N_1} \tag{7.1}$$

- N_1: primary winding number of turns
- N_2: secondary winding number of turns

$$\frac{v_1}{v_2} = \frac{N_1}{N_2} = n = \frac{1}{a} \quad \wedge \quad \frac{i_1}{i_2} = -\frac{N_2}{N_1} = -\frac{1}{n} = -a \tag{7.2}$$

$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 & n \\ -n & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix} \quad \wedge \quad \begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} n & 0 \\ 0 & a \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \tag{7.3}$$

If an ideal transformer is terminated by a load, as shown in Fig. 7.2, it performs the following impedance transformation. This concept is used in practice, however in most cases, especially in IC design, the ideal transformer model is too crude.

$$Z_{in} = \frac{v_1}{i_1} = \frac{nv_2}{-ai_2} = n^2 Z_L \tag{7.4}$$

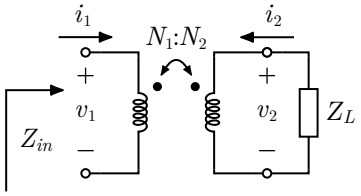


Figure 7.2: Ideal transformer terminated by a load Z_L

7.2 Coupled inductors

A more realistic model of magnetically coupled inductors utilizes the inductance matrix with the concept of mutual inductance. This model still ignores resistive losses in the windings and leads to the 2-port representation of coupled inductors shown in Fig. 7.3.

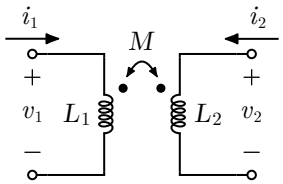


Figure 7.3: Coupled inductors

- L_1: self inductance of primary inductor (H)
- L_2: self inductance of secondary inductor (H)
- M: mutual inductance between primary and secondary inductors (H)

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} j\omega L_1 & j\omega M \\ j\omega M & j\omega L_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{7.5}$$

The dots appearing in Fig. 7.3 are a notational convention to simplify diagrams otherwise requiring to show magnetic flux coupling. The voltage induced by one inductor to the other, depends on the direction of current. If current enters the dot of one inductor, the induced voltage at the other dot is positive and vice versa.

Practically, since currents conventionally enter at the positive voltage terminal, if for both inductors the current enters at the dotted terminal, mutual voltage is conventionally positive and if for one inductor the current enters at the dotted terminal and for the other inductor the current leaves from the dotted terminal, mutual voltage is conventionally negative. The coupling factor between inductors is defined as follows and can take values from zero to one.

$$k = \frac{M}{\sqrt{L_1 L_2}} \quad \wedge \quad k \in [0, 1] \tag{7.6}$$

For solenoid coils self inductance can be calculated as follows and in general it is proportional to the square of the number of conductor turns forming the loop.

$$L = \mu_0 \mu_r \frac{A}{l} N^2 \quad \wedge \quad L \sim N^2 \tag{7.7}$$

- μ_0: vacuum permeability
- μ_r: relative permeability of the material in the core of the solenoid
- A: area of the solenoid
- l: lenght of the solenoid

Assuming perfect magnetic coupling ($k = 1$) and infinite permeability for the material containing the mutual magnetic flux, or equivalently no magnetizing current, it can be seen how coupled inductors behave like transformers by comparing their H-parameters. For perfect magnetic coupling and very large self inductances the following hold.

$$k = 1 \iff M = \sqrt{L_1 L_2} \tag{7.8}$$

$$\mathbf{H} = \frac{1}{Z_{22}} \begin{bmatrix} \Delta_Z & Z_{12} \\ -Z_{21} & 1 \end{bmatrix} = \frac{1}{j\omega L_2} \begin{bmatrix} \omega^2(M^2 - L_1 L_2) & j\omega M \\ -j\omega M & 1 \end{bmatrix} = \begin{bmatrix} 0 & \sqrt{\frac{L_1}{L_2}} \\ -\sqrt{\frac{L_1}{L_2}} & \frac{1}{L_2} \end{bmatrix} \tag{7.9}$$

$$\mathbf{H} \approx \begin{bmatrix} 0 & \sqrt{\frac{L_1}{L_2}} \\ -\sqrt{\frac{L_1}{L_2}} & 0 \end{bmatrix} = \begin{bmatrix} 0 & \frac{N_1}{N_2} \\ -\frac{N_1}{N_2} & 0 \end{bmatrix} = \begin{bmatrix} 0 & n \\ -n & 0 \end{bmatrix} \tag{7.10}$$

This indicates that coupled inductors have the ability, to some extent, to perform impedance scalin like transformers do.

In practice, resistive losses in the conductors must be taken into account and the model of Fig. 7.4 is used. Additionally, if an electromagnetic structure designed as a pair of coupled inductors is simulated and results in a 4-port, it can be treated as a 2-port by connecting some terminals to ground and the parameters of the coupled inductors can be extracted with the setup of Fig. 7.5.

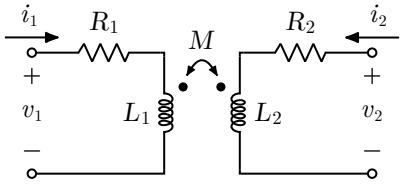


Figure 7.4: Lossy coupled inductors

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & j\omega M \\ j\omega M & R_2 + j\omega L_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{7.11}$$

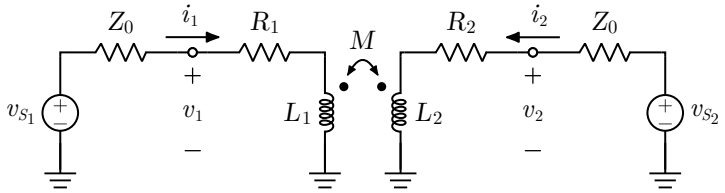


Figure 7.5: Setup for coupled inductors parameters extraction

$$L_1 = \frac{1}{2\pi f}\mathrm{Im}[Z_{11}] \quad \wedge \quad R_1 = \mathrm{Re}[Z_{11}] \quad \wedge \quad Q_1 = \frac{\mathrm{Im}[Z_{11}]}{\mathrm{Re}[Z_{11}]} \tag{7.12}$$

$$L_2 = \frac{1}{2\pi f}\mathrm{Im}[Z_{22}] \quad \wedge \quad R_2 = \mathrm{Re}[Z_{22}] \quad \wedge \quad Q_2 = \frac{\mathrm{Im}[Z_{22}]}{\mathrm{Re}[Z_{22}]} \tag{7.13}$$

$$M = \frac{1}{2\pi f}\mathrm{Im}[Z_{12}] \tag{7.14}$$

Obviously, these parameters change with frequency for the same reasons analyzed in 6.2. Analogous models can be extracted for coupled inductors as the ones for inductors and self resonance need to be avoided for them as well.

In fact, coupled inductors can be more susceptible to self resonance than simple inductors. Achieving good magnetic coupling without ferromagnetic cores, as is with on chip inductors, requires bringing two inductors very close to each other. This creates capacitive signal paths whose impedance becomes lower at higher frequencies and the structure fails to behave as a pair of coupled inductors.

Good coupling is necessary for minimizing losses. The best way to achieve it is with integrated inductors by stacking them one on top of the other made from consecutive metal layers of the stackup, like in Fig. 7.6. The inductors shown have inner diameters of 70 μm and turn width 6μm, which leads to self inductances of 138 pH and 146 pH with a coupling factor of 0.78 at 7.7 GHz.

If tuning of the coupling factor is required two inductors made from the same metal layer can be interleaved, like in Fig. 7.7. The inductors shown have inner diameter of 70 μm, turn width 6μm, and turn spacing of 2.6μm, which leads to both self inductances being 153 pH with a coupling factor of 0.56 at 7.7 GHz. Turn spacing is tunable.

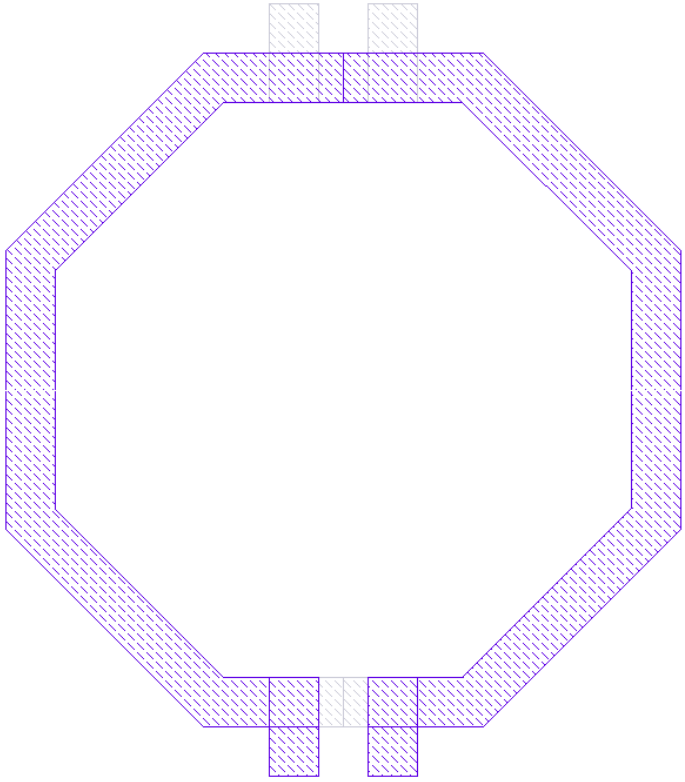


Figure 7.6: Stacked coupled inductors

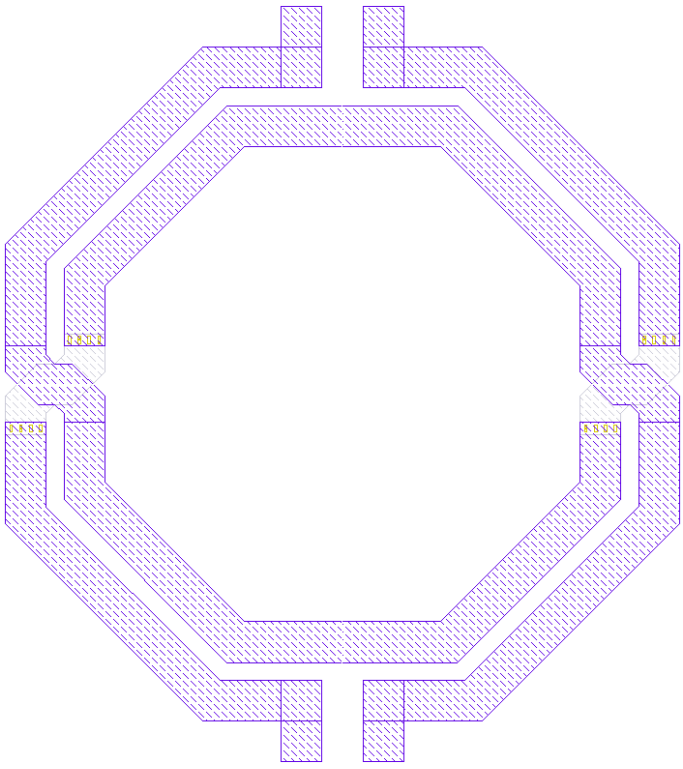


Figure 7.7: Interleaved coupled inductors

7.3 Balancing units

A balancing unit (balun) is an electrical device that allows balanced and unbalanced lines to be interfaced without disturbing the impedance arrangement of either line. It provides common mode noise suppression and possibly impedance matching.

There are many types of baluns with the most common being the classical center tapped transformer type, which utilizes magnetic coupling of inductors and provides galvanic isolation between the two signal interfaces, which allows them to be on different DC levels as well. There are also autotransformer type baluns, transmission line baluns, and hybrid baluns.

In IC design the most common type of balun being used is the center tapped transformer. Transformers are implemented as explained in 7.2, only with an extra connection to the center of the inductor at the balanced side.

7.3.1 Center tapped transformers

A center tapped inductor can be modeled as two coupled inductors. Therefore, transformer center tapped at one winding can be modeled as three coupled inductors. In Fig. 7.8 a center tapped transformer is shown being measured as a 3-port network.

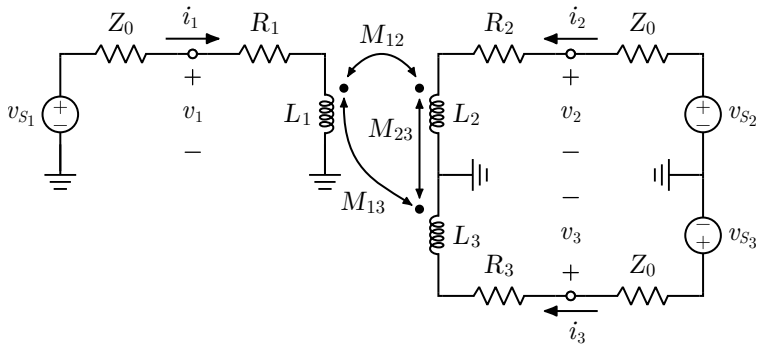


Figure 7.8: A transformer center tapped at the secondary winding as a 3-port

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & j\omega M_{12} & -j\omega M_{13} \\ j\omega M_{12} & R_2 + j\omega L_2 & -j\omega M_{23} \\ -j\omega M_{13} & -j\omega M_{23} & R_3 + j\omega L_3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{7.15}$$

The electromagnetic simulation of a structure designed as a center tapped transformer results in the S-parameters of a 5-port network. Connecting some terminals to ground, like in Fig. 7.8, all the parameters of the inductors can be calculated and undesired asymmetries can be observed, which might require redesigning.

$$L_i = \frac{1}{2\pi f}\mathrm{Im}[Z_{ii}] \quad \wedge \quad R_i = \mathrm{Re}[Z_{ii}] \quad \wedge \quad Q_i = \frac{\mathrm{Im}[Z_{ii}]}{\mathrm{Re}[Z_{ii}]} \tag{7.16}$$

$$M_{ij} = \frac{1}{2\pi f}\mathrm{Im}[Z_{ij}] \quad \wedge \quad k_{ij} = \frac{M_{ij}}{\sqrt{L_i L_j}} \tag{7.17}$$

If symmetry holds, then $v_2 = -v_3$ and $v_{out} = v_2 - v_3$ is free from common mode signals, such as noise and harmonics of even order. Under symmetric termination, the same current flows in and out of the secondary winding and the conditions for symmetry follow.

$$i_2 = -i_3 \quad \wedge \quad R_2 = R_3 \quad \wedge \quad L_2 = L_3 \quad \wedge \quad M_{12} = M_{13} \implies v_2 = -v_3 \tag{7.18}$$

In general, a center tapped transformer can be treated as a 2-port as well, like in Fig. 7.9. However, if it is to be used as a balancing unit, symmetry should be secured first.

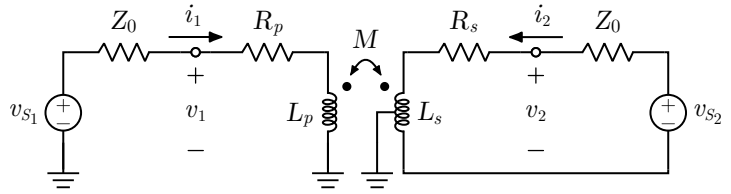


Figure 7.9: A transformer center tapped at the secondary winding as a 2-port

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} R_p + j\omega L_p & j\omega M \\ j\omega M & R_s + j\omega L_s \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{7.19}$$

$$R_p = R_1 \quad \wedge \quad R_s = R_2 + R_3 \tag{7.20}$$

$$L_p = L_1 \quad \wedge \quad L_s = L_2 + L_3 + 2M_{23} \quad \wedge \quad M = M_{12} + M_{13} \tag{7.21}$$

Center tapped transformers can of course be interleaved and stacked. The inductors in Fig. 7.11 are stacked and have inner diameters of 70 μm and turn width 6μm, which leads to self inductances of 145 pH and 537 pH with a coupling factor of 0.75 at 7.7 GHz. The inductors in Fig. 7.11 are interleaved have inner diameter of 70 μm, turn width 6μm, and turn spacing of 2.6μm, which leads to of 191 pH and 504 pH with a coupling factor of 0.62 at 7.7 GHz. Turn spacing is tunable.

Note that in both cases one inductor has one turn and the other has two, which affects coupling and self inductance and is done in an effort to transform a load impedance. In Fig. 7.10 the second turn is completed by moving one metal layer down and then back one metal layer up. Furthermore, the only difference these structures have than the corresponding transformers is the center tap, which can be seen at the center of an inductor connected with a via to one metal layer up.

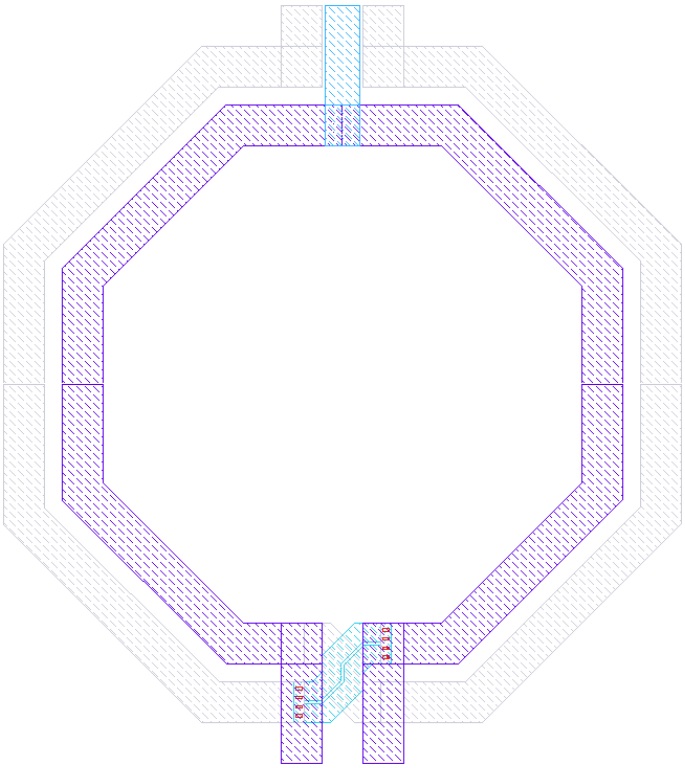


Figure 7.10: Stacked balun transformer

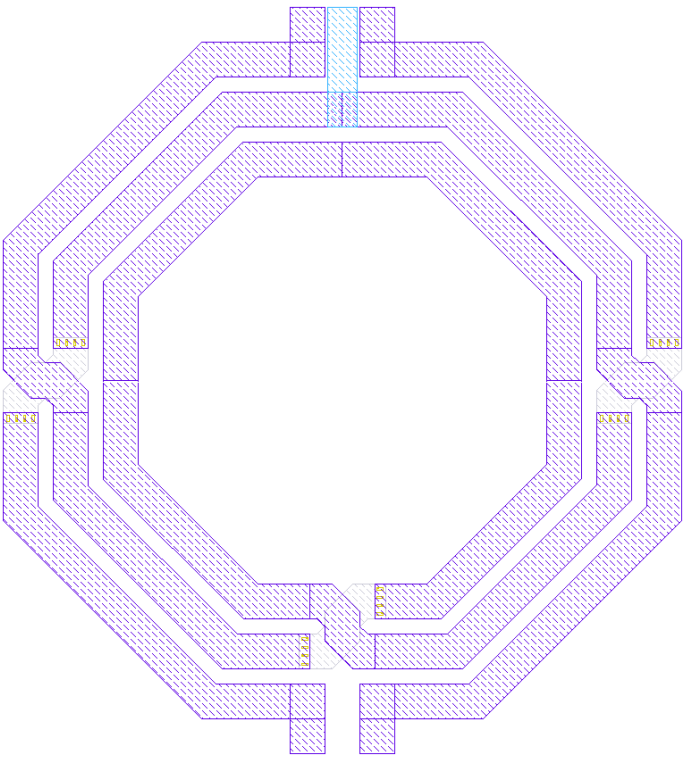


Figure 7.11: Interleaved balun transformer

7.3.2 Balun transformer design

When a single ended signal needs to be converted to differential, such as in an amplifier between stages, a balancing unit is necessary. In IC design, this can be achieved with on chip center tapped transformers. Usually, there is a desired coupling factor and a range of self inductances that are acceptable and geometric parameters of a structure are tuned in order for it to fit the requirements.

In this thesis, custom balun trasformers, such as the one in Fig. 7.12, were utilized. The SKILL script to generate them was kindly provided by Dimitrios Georgakopoulos. The transformer used has an inner diameter of 250 μm and a turn width of 6 μm. This was a tough compromise because large inductances at low frequencies, compared to mm-Wave frequencies, were required and parasitic capacitances between the inductors dominated if the conductors were widened in efforts to trim losses.

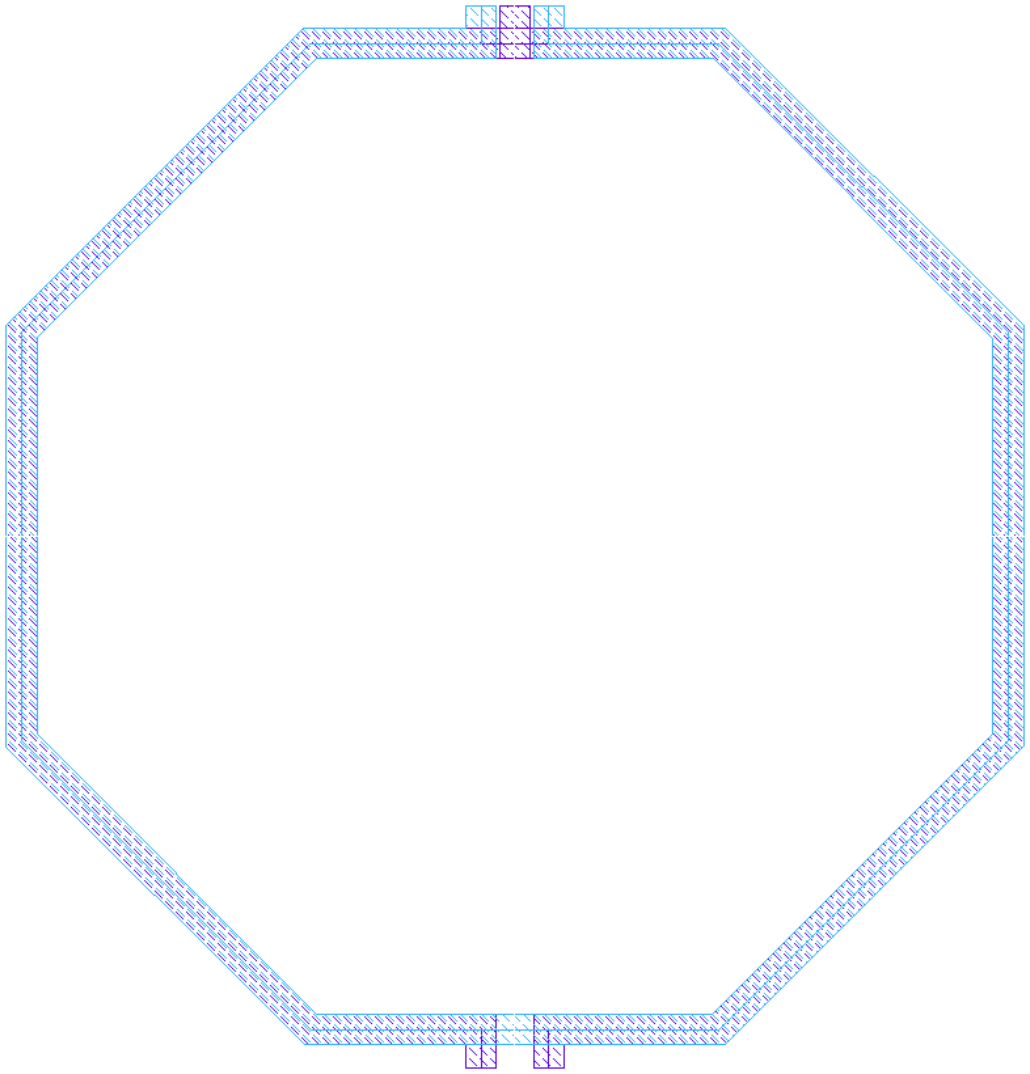


Figure 7.12: Balun transformer

In order to find appropriate geometric parameters for a balun transformer some theoretical calculations can be done, but eventually a structure's behavior needs to be verified with results from electromagnetic simulation. The setup to evaluate a balun transformer was shown in Fig. 7.8.

First of all, the 3-port S-parameters must be evaluated. The transformer needs to exhibit low losses and small amplitude imbalance at the operating frequency range, as shown in Fig. 7.16. Since power from the first port is being split and delivered hopefully symmetrically to the other two ports, these S-parameters are expected to be below −3 dB. Additionally, low phase imbalance is required, as shown in Fig. 7.17.

$$\Delta A_{\mathrm{dB}} = 20 \log \left(\frac{|S_{21}|}{|S_{31}|} \right) \mathrm{dB} \tag{7.22}$$

$$\Delta \phi = [180^\circ - \arg(S_{21}) + \arg(S_{31})] \bmod 360^\circ \tag{7.23}$$

Making a balun that exhibits its minimum losses within the operating frequency range might seem like an attractive idea, however its losses minimize near self resonance, as shown in Fig. 7.13, and it is critical that this frequency region be avoided. This can be verified by extracting inductances shown in Fig. 7.18 and Fig. 7.19. Note that the operating frequency band is from 7 up to 8.4 GHz, while the self resonance frequency is at 12.81 GHz, barely satisfying the rule of thumb that the transformer should not operate above 2/3 of the self resonance frequency.

This highlights the significant difficulty of the trade offs. The need for high inductances and high coupling leads to large diameters of inductors, which makes the structure susceptible to self resonance requiring thinner conductors that exhibit greater losses, demonstrated by poor quality factors in Fig. 7.20. After proper tuning, the transformer can be measured as a 2-port with the setup of Fig. 7.9, and if the results, like in Fig. 7.21, Fig. 7.22, and Fig. 7.23, are satisfactory it can be used as a balun. The coupling factor at the operating frequency is 0.91.

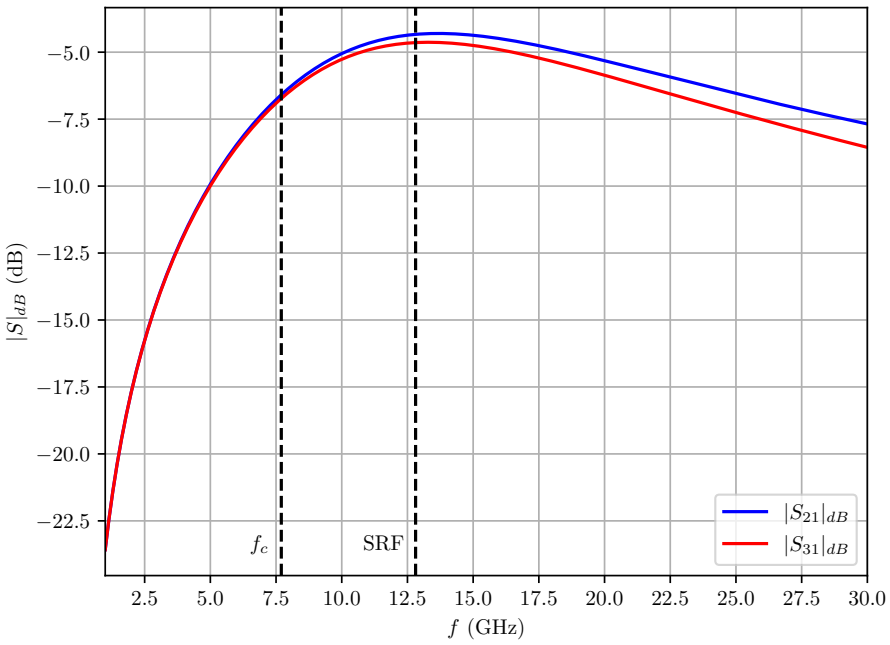


Figure 7.13: Balun transformer S-parameters magnitude

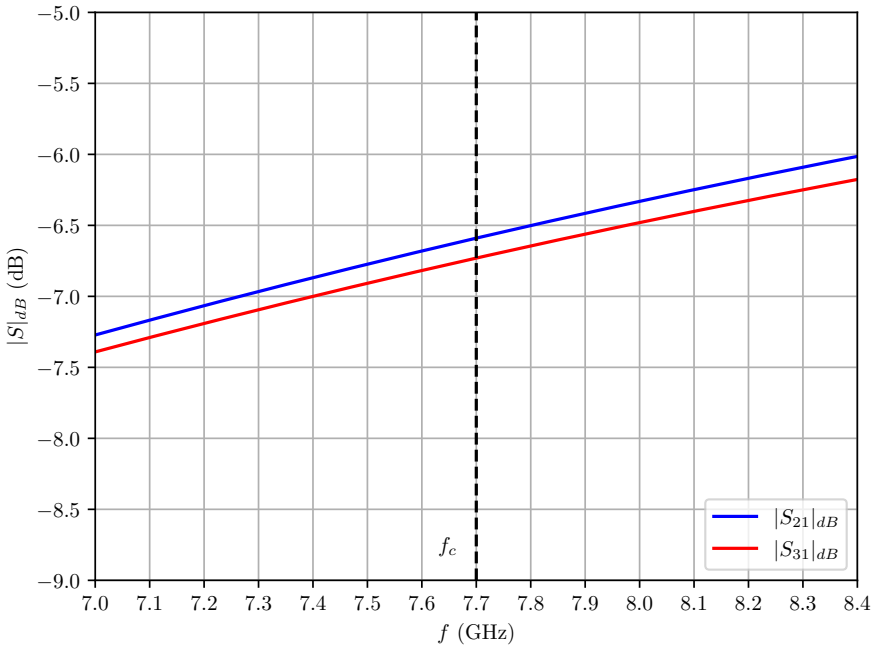


Figure 7.14: Balun transformer S-parameters magnitude (zoomed in)

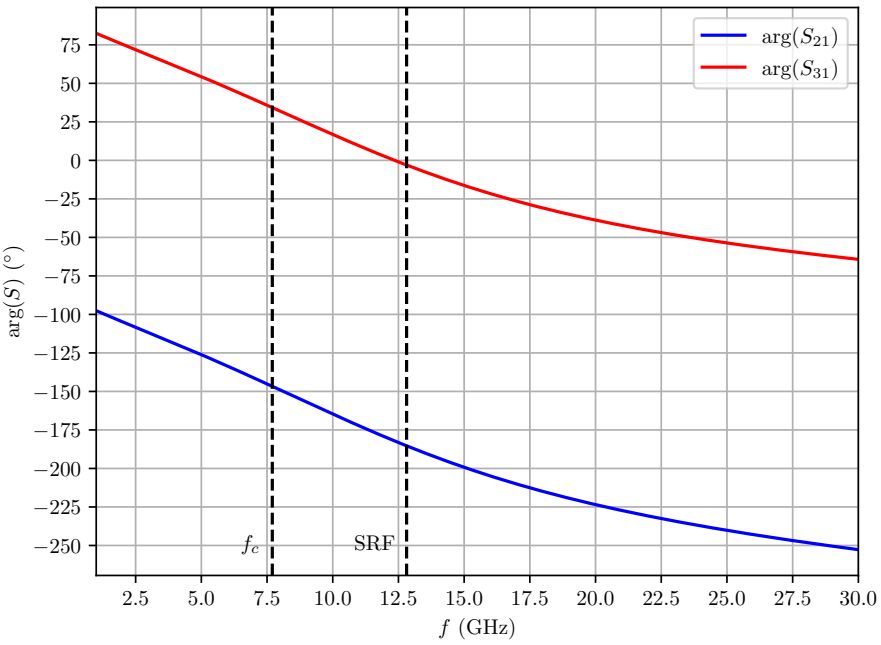


Figure 7.15: Balun transformer S-parameters phase

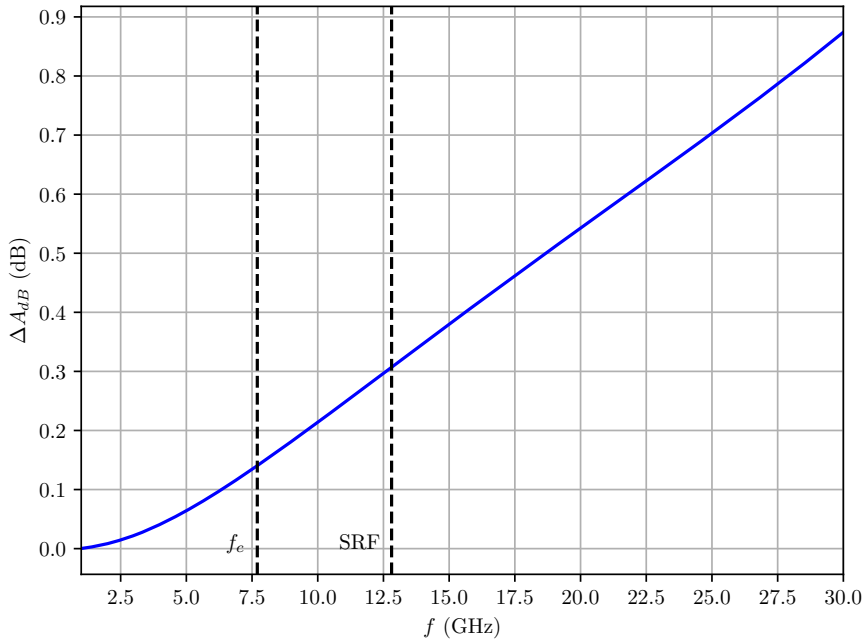


Figure 7.16: Amplitude imbalance

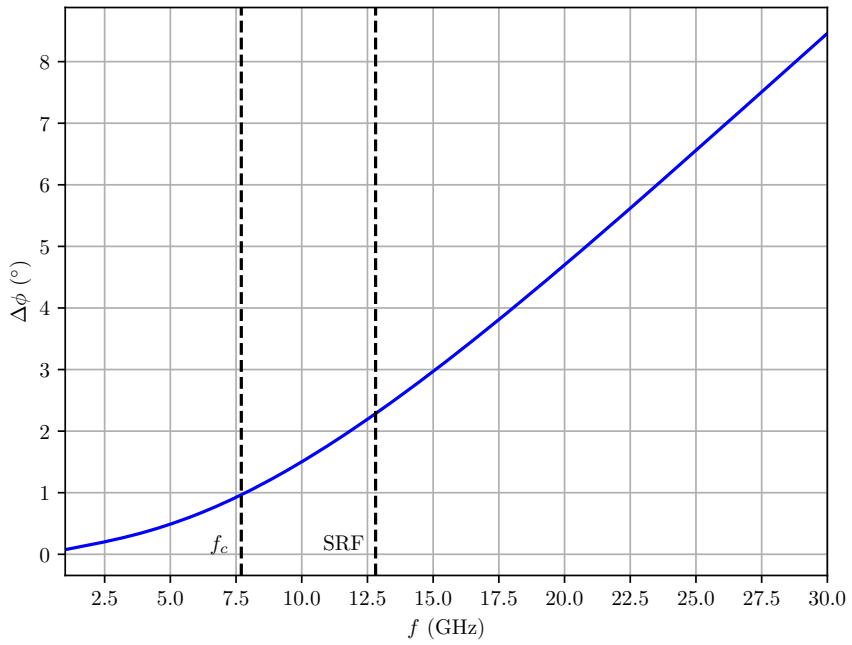


Figure 7.17: Phase imbalance

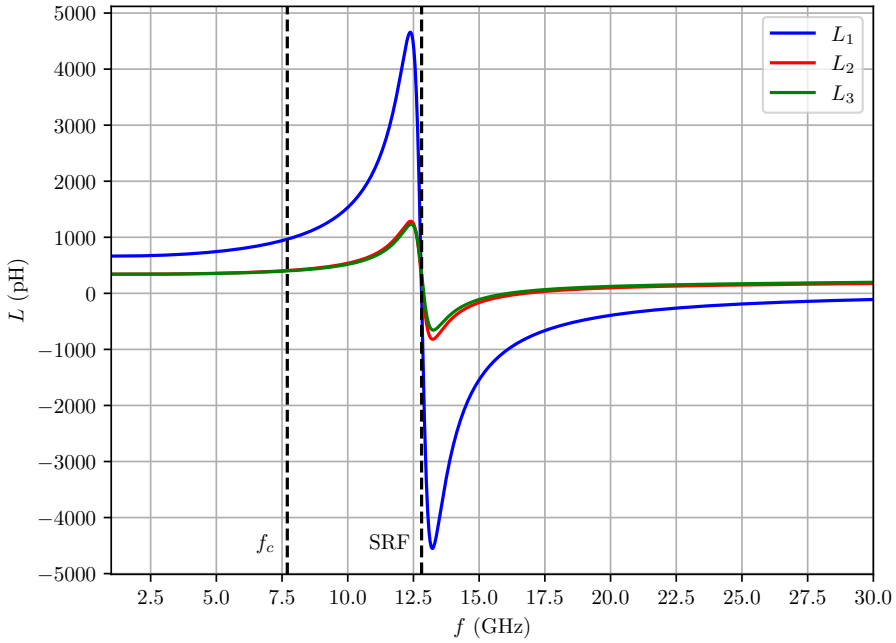


Figure 7.18: Balun transformer self inductances

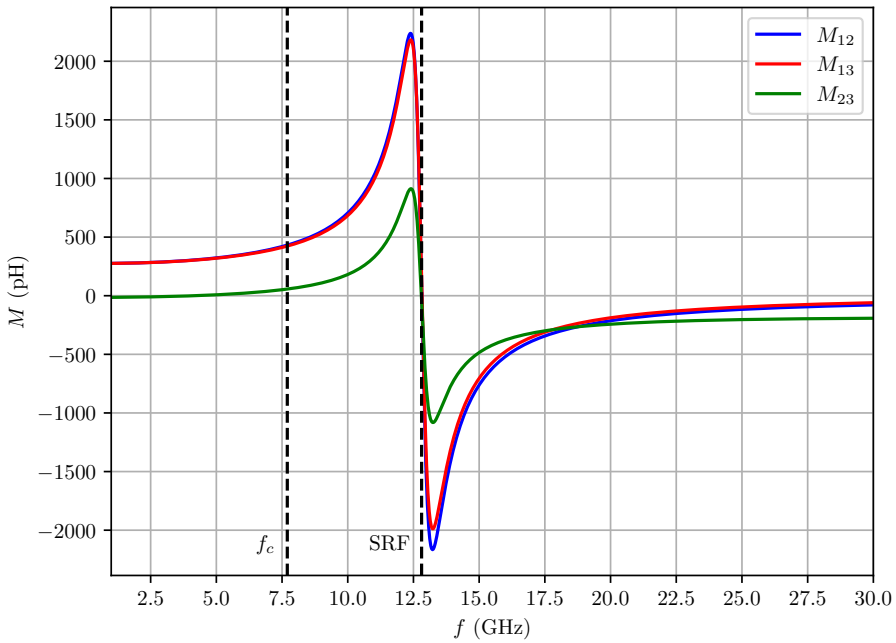


Figure 7.19: Balun transformer mutual inductances

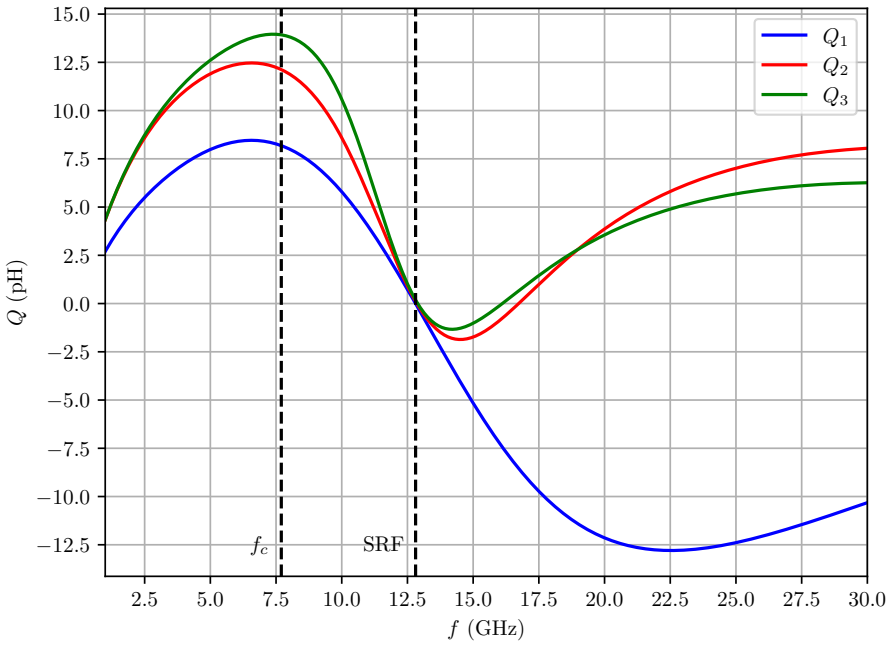


Figure 7.20: Balun transformer quality factors

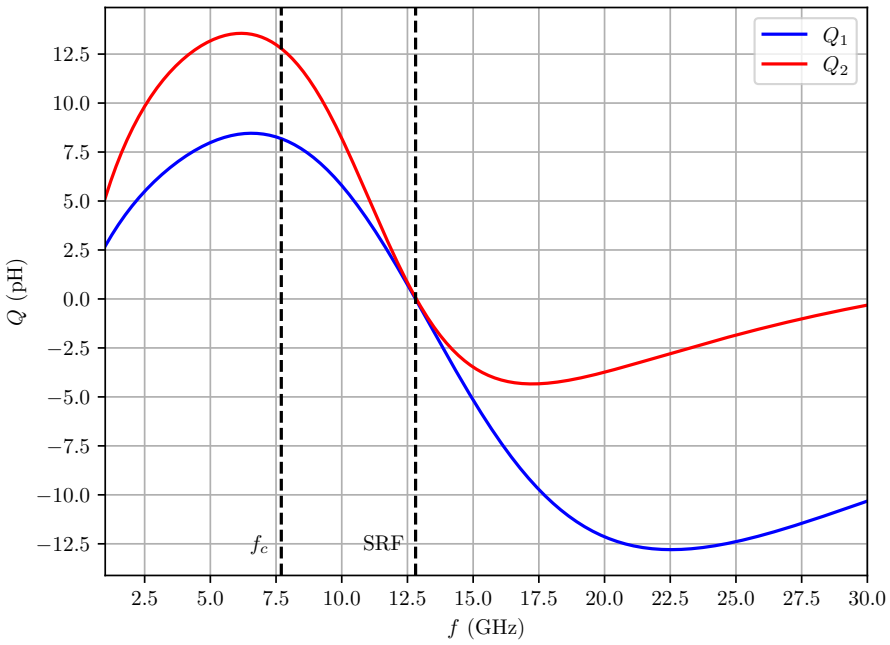


Figure 7.21: Balun transformer as a 2-port quality factors

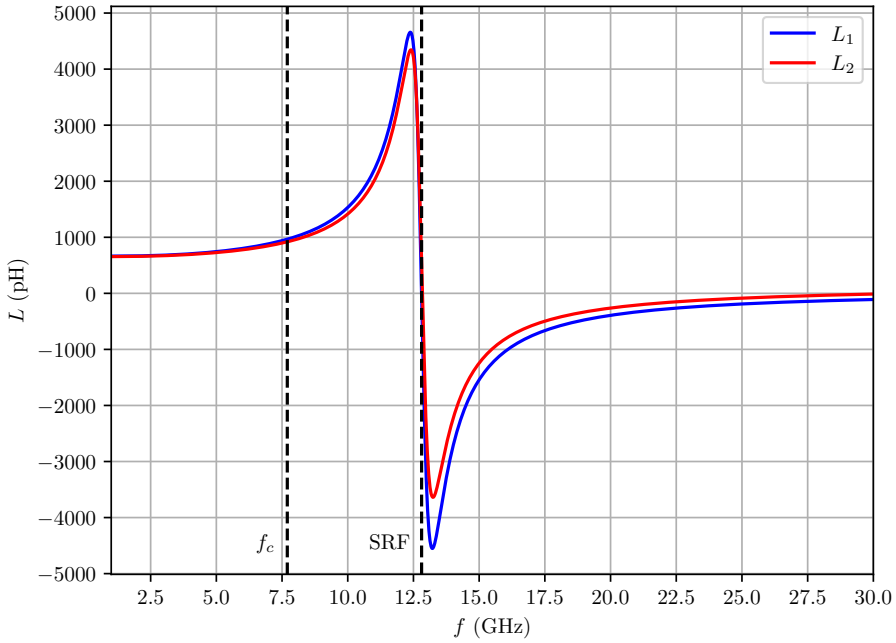


Figure 7.22: Balun transformer as a 2-port self inductances

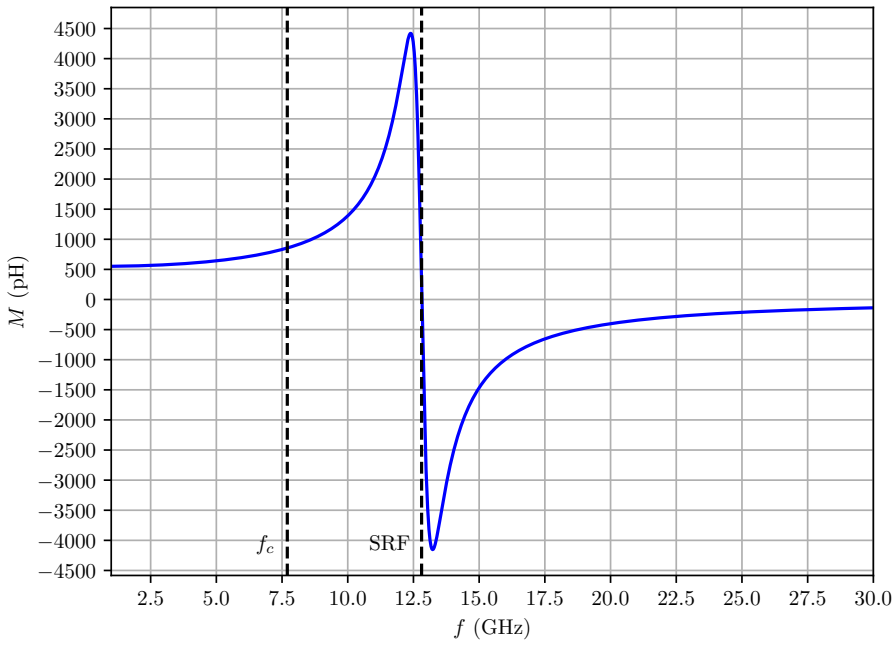


Figure 7.23: Balun transformer as a 2-port mutual inductance

7.4 Impedance matching with coupled inductors

Transformers can aid in impedance matching through the impedance transformation they provide, as explained in 7.1. Even if just conversion from single ended to differential signaling or vice versa is desired, conjugate matching is still required for maximum power transfer. Additionally, a balanced line has a characteristic impedance double that of an unbalanced line, if it consists of two symmetric lines of the same type as the unbalanced line. Therefore, impedance matching is almost always required.

Consider the setup of Fig. 7.24, where there could possibly be center taps as well. The source and load impedances need to be capacitive ($X_S < 0\,,\ X_L < 0$) so that they can be matched with coupled inductors. Resistive losses belonging to the transformer have been absorbed in the source and load impedances. For the case of perfect coupling ($k = 1$) there is a simple closed form solution for the self inductances necessary for conjugate matching.

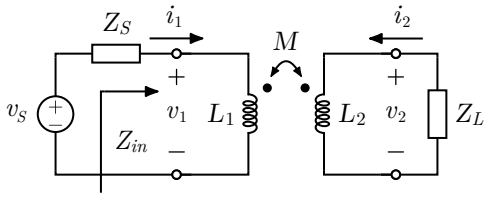


Figure 7.24: Coupled inductors used for impedance matching

$$v_1 = v_S - i_1 Z_S \quad \wedge \quad v_2 = -i_2 Z_L \tag{7.24}$$

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} j\omega L_1 & j\omega\sqrt{L_1 L_2} \\ j\omega\sqrt{L_1 L_2} & j\omega L_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{7.25}$$

$$Z_{in} = \frac{v_1}{i_1} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22} + Z_L} = j\omega L_1 + \frac{\omega^2 L_1 L_2}{R_L + j(X_L + \omega L_2)} \tag{7.26}$$

$$Z_{in} = Z_S^* \iff L_1 = -\frac{R_L(R_S^2 + X_S^2)}{2\pi f(R_S X_L + R_L X_S)} \quad \wedge \quad L_2 = -\frac{R_S(R_L^2 + X_L^2)}{2\pi f(R_S X_L + R_L X_S)} \tag{7.27}$$

The necessity for capacitive source and load impedances is highlighted with these results because self inductances must be positive. Additionally, source and load impedances viewed from the 2-port can be tuned with capacitors if necessary. An example of such a case is when the required self inductances differ slightly from those achieved by the structure.

Note that in practical cases coupling is lower than 1 and many more phenomena, such as parasitic capacitances, may be noticeable even in the operating frequency range, therefore the use of EDA tools is necessary. Closed form solutions for a given coupling factor exist, but they are complicated.

To summarize, the design of transformers for impedance matching and as balancing units basically begins with investigating the performance of structures with electromagnetic simulation, examining the impedances that need to be interfaced, finding the necessary self inductances and tuning both the impedances and the self inductances in order to achieve matching.

Chapter 8

Input/Output parasitcs

Any integrated circuit that needs to interface with off chip equipment inevitably faces very noticeable parasitics that can degrade its performance. Before designing a schematic, especially in the RF front end, such as a low noise amplifier, it is good practice to run some simulations and take into account such parasitics.

The most prominent input/output parasitics result from bond wires and pads. The former result in series inductances and resistances, while the latter in shunt capacitances with leakage resistances. For the design of this thesis, already available data for bond wires were used and S-parameters from PDK pads were extracted with electromagnetic simulation.

8.1 Bond wires

Bond wires connect the chip with the PCB, therefore, in order to include coupling with PCB ground, they can be viewed as a 2-port network. However, the simplest model for a bond wire is the one in Fig. 8.1, like with inductors in 6.2.

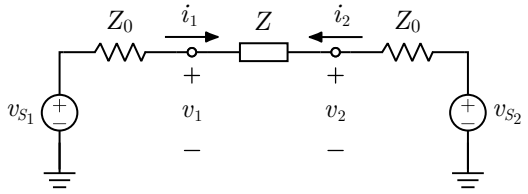


Figure 8.1: A series impedance as a 2-port network

$$\mathbf{Y} = \begin{bmatrix} Y & -Y \\ -Y & Y \end{bmatrix} \tag{8.1}$$

The available bond wire data were for gold bond wires with a diameter of $25\,\mu m$. Gold is less conductive than copper, however it does not suffer from oxidation like copper, except for in very specific environments unrelated to IC packaging. The Z-parameters of the 2-port fit the model of Fig. 8.1 and inductor parameters were extracted.

$$L = \frac{1}{2\pi f}\mathrm{Im}\left[\frac{1}{Y_{11}}\right] \quad \wedge \quad R = \mathrm{Re}\left[\frac{1}{Y_{11}}\right] \quad \wedge \quad Q = \frac{\mathrm{Im}\left[\dfrac{1}{Y_{11}}\right]}{\mathrm{Re}\left[\dfrac{1}{Y_{11}}\right]} \tag{8.2}$$

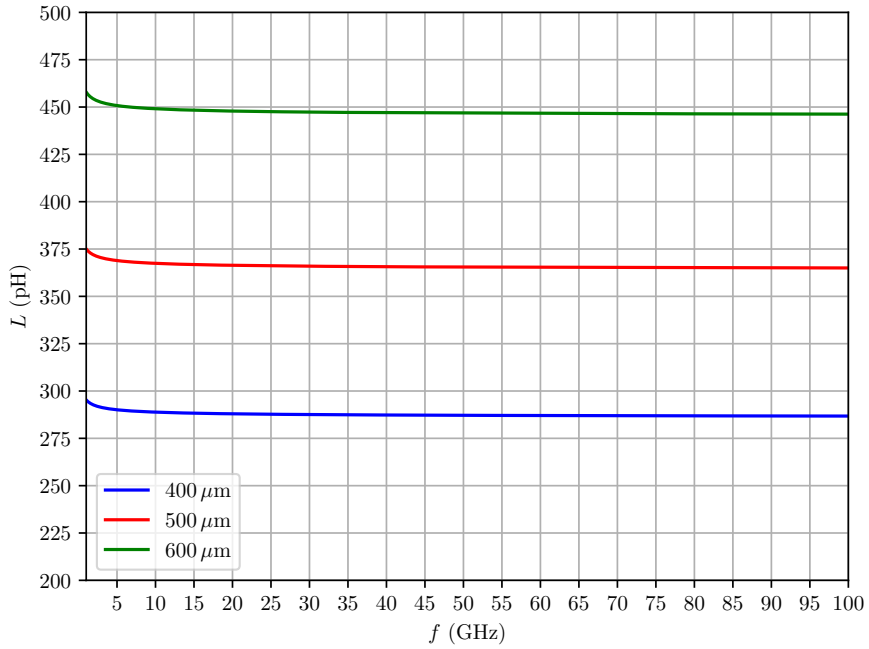


Figure 8.2: Bond wire inductance

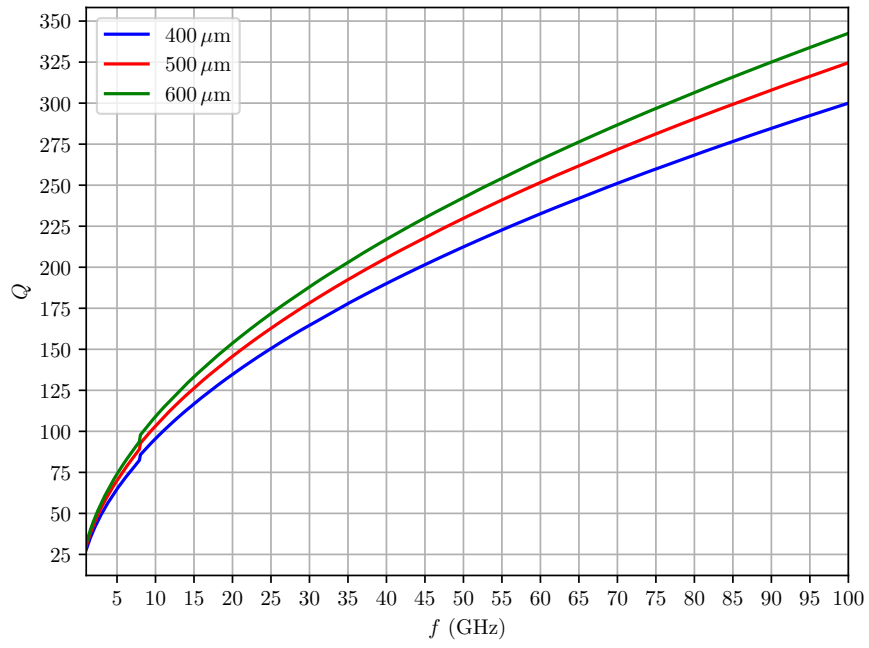


Figure 8.3: Bond wire quality factor

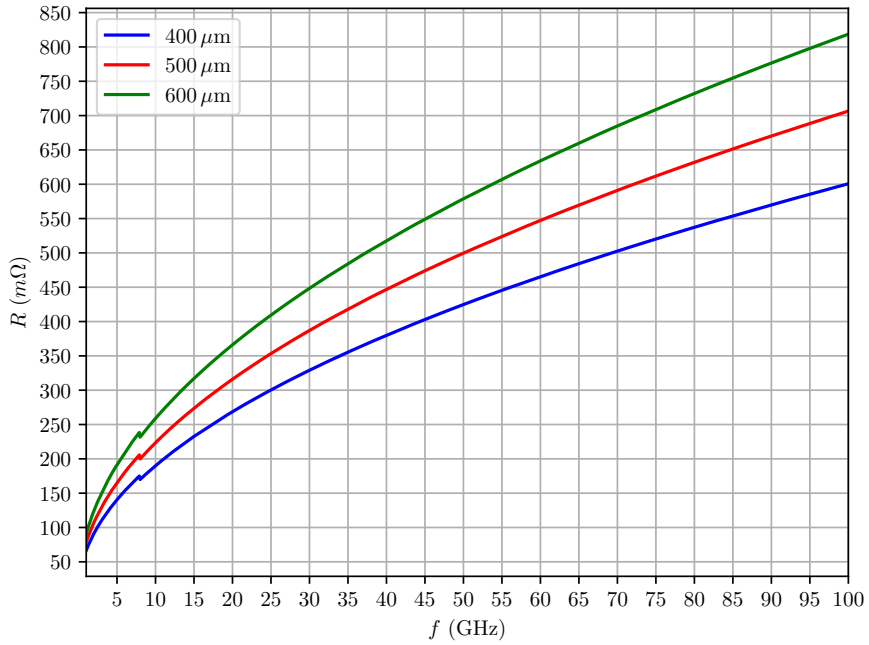


Figure 8.4: Bond wire resistance

The self inductances of bond wires of different lengths can be seen in Fig. 8.2. They amount to self inductance per unit length of about $0.72 - 0.75\,\mathrm{nH/mm}$, which is close to the $1\,\mathrm{nH/mm}$ rule of thumb.

There are other ways to estimate bond wire self inductance as well. It can be treated as a wire of radius r and length l at height h over a ground plane, which has the following external self inductance. This is extracted using the method of images.

$$L = \frac{\mu_0 \mu_r l}{2\pi} \ln\left[\sqrt{\left(\frac{h}{r}\right)^2 - 1} + \frac{h}{r}\right] \approx \frac{\mu_0 \mu_r l}{2\pi} \ln\left(\frac{2h}{r}\right) \quad , \quad a \ll h \tag{8.3}$$

The internal self inductance of the wire is ignored in the model above because at high frequencies it follows an inverse square root law due to skin effect. It vanishes when added to the external self inductance, since the frequencies of interest are quite high. However, the existence of internal wire self inductance can explain the curvature seen in Fig. 8.2 at frequencies up to $5\,\mathrm{GHz}$.

Furthermore, bond wire resistances can be seen in Fig. 8.4. They clearly follow a square root law with respect to frequency, which is expected from the skin effect observed in wires. This results in the quality factor, shown in Fig. 8.3, following a square root law with respect to frequency as well, provided that self inductance remains constant, as it does in this case.

$$Q = \frac{\omega L}{R} \sim \frac{\omega}{\sqrt{\omega}} = \sqrt{\omega} \tag{8.4}$$

8.2 Pads

Since bond wires are used at the interface of a chip with a PCB, they usually have larger dimensions than on chip interconnects. Therefore, on chip pads are required for a bond wire to make a reliable electrical connection.

Pads are basically surfaces made of top level metals of the stackup and their shape depends on the type of connection they support, for instance bond wires, solder balls, probes. For bond wire connections, the PDK for GF22 FD-SOI provides rectangular pads, like the one in Fig. 8.5. The smallest available width and length were used in order to minimize parasitics.

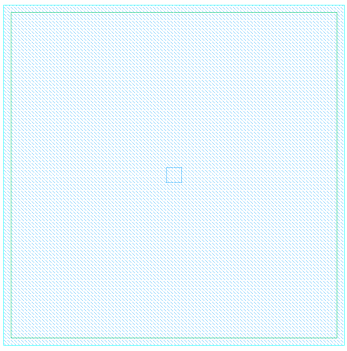


Figure 8.5: PDK provided bond wire pad

After electromagnetic simulation that resulted in S-parameters for the pad, using the model of Fig. 8.6 seemed like a good choice because all Y-parameters were equal. After all, the pad parasitics can be thought of as a capacitance modeling coupling with the substrate and a resistor modeling leakage currents to the substrate.

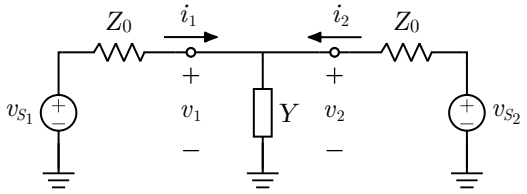


Figure 8.6: A shunt admittance as a 2-port network

$$\mathbf{Z} = \begin{bmatrix} Z & Z \\ Z & Z \end{bmatrix} \tag{8.5}$$

However, attempting to interpret the shunt admittance model as a capacitor with leakage did not yield parameters constant over frequency, as shown in Fig. 8.7 and Fig. 8.8. Thus, it was decided that the pad parasitics should be included by treating the pad as a 2-port network with its S-parameter file from the electromagnetic simulation loaded.

$$Z = \frac{1}{Y} = \frac{1}{G + j\omega C} \tag{8.6}$$

$$C = \frac{1}{2\pi f}\mathrm{Im}\left[\frac{1}{Z_{11}}\right] \quad \wedge \quad G = \mathrm{Re}\left[\frac{1}{Z_{11}}\right] \quad \wedge \quad R = \frac{1}{G} \tag{8.7}$$

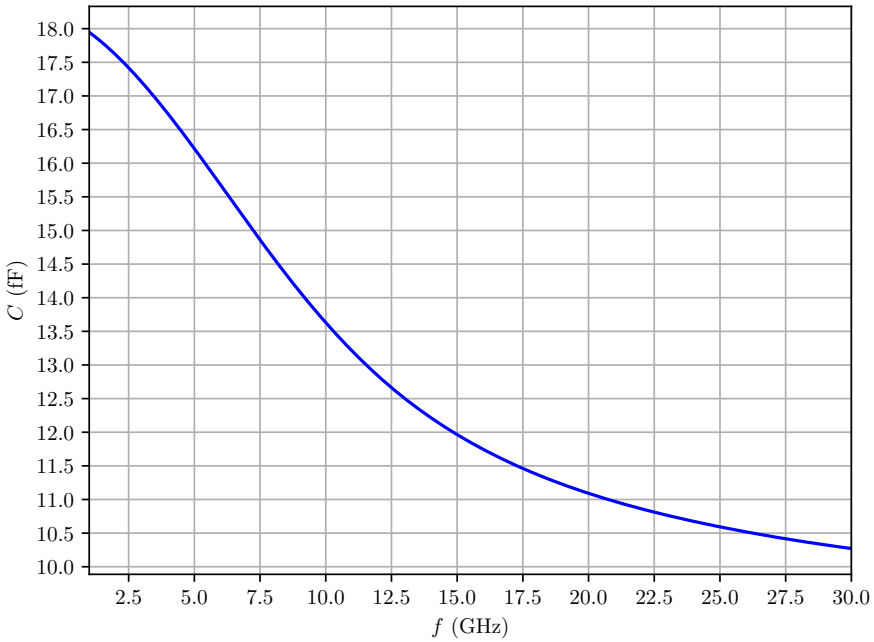


Figure 8.7: Pad to substrate capacitance

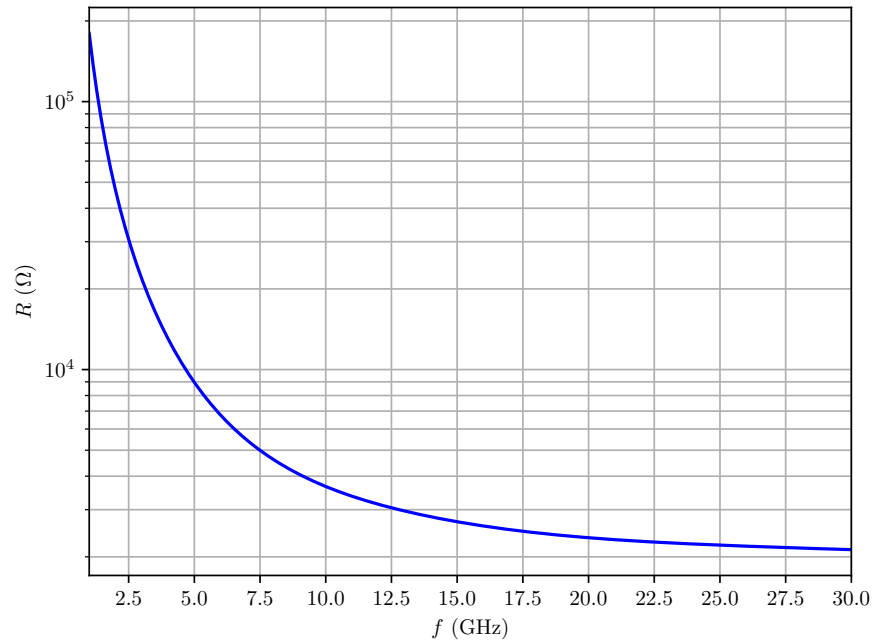


Figure 8.8: Pad to substrate leakage resistance

Chapter 9

LNA schematic design

Theoretical calculations for high frequency design are extremely difficult due to all the parasitics exhbiting very noticeable behaviour. It is impossible to take everything into account and extract accurate formulas for transfer functions or input impedances like in analog design. Therefore, simulations start immediately and with PDK components.

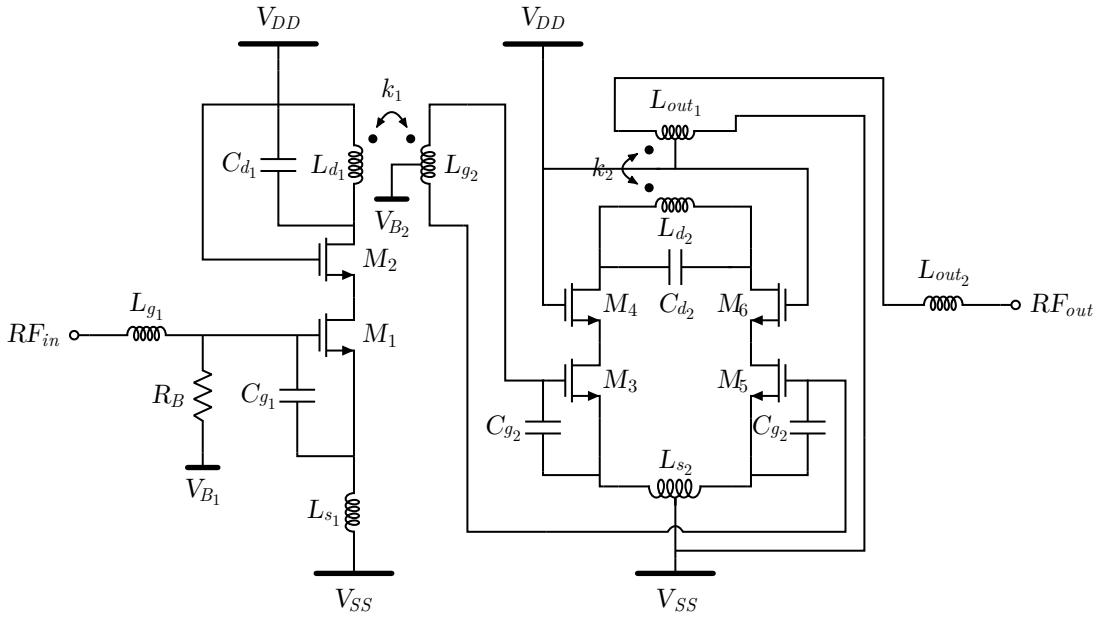


Figure 9.1: The LNA schematic

The schematic of Fig. 9.1 was created in Cadence Virtuoso and design followed from there. The process followed was the one described in 5.5. Because of the range of operating frequencies, the RF library from the GF22 FD-SOI PDK was used. The super low threshold voltage transistors (slvtnfet_rf) were used due to their lower noise and better high frequency performance.

The biasing voltages that resulted from the design process are shown below. For reliability and simulation accuracy reasons, the supply voltage is the PDK specified.

- $V_{DD} = 800\,m\text{V}$
- $V_{B_1} = 400\,m\text{V}$
- $V_{B_2} = 300\,m\text{V}$

9.1 Design of the first stage

The schematic of the first stage in Cadence Virtuoso is shown in Fig. 9.2. Transistors were sized in order to have sufficient gain and biased to achieve their optimal minimum noise figure. Noise matching was taken into account during sizing and it was traded off with input matching. Larger devices exhibit optimum noise impedances of smaller magnitude. The cascode with the extra gate to source capacitance was sized to have $R_{opt} = 50\,\Omega$ and X_{opt} was expected to be tuned by a gate inductor. Input matching is tuned with the gate inductor, the capacitor between the gate and source terminals, and the source inductor.

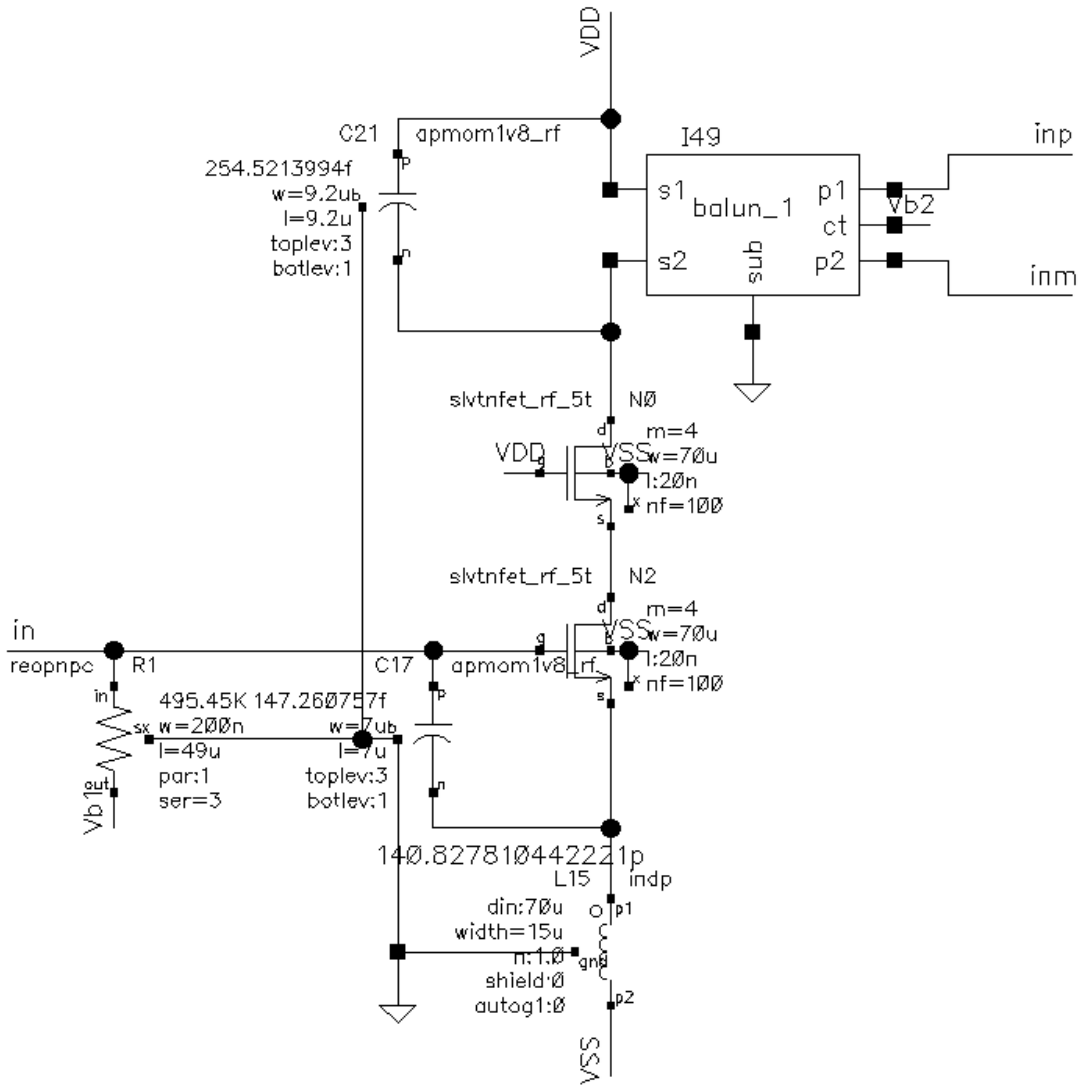


Figure 9.2: Schematic of the first stage in Cadence Virtuoso

The absence of a gate inductor is related to the extreme difficulty of its integration, which led to the decision that an off chip inductor was necessary. The 7.7 GHz frequency of operation is high but large inductances are still required. The poor quality factor of large integrated inductors, especially in deep sub-micron processes, led to unacceptable degradation of minimum noise figure.

9.1.1 The gate inductor

Input matching at 50 Ω is required. The gate inductor tunes out the imaginary part of the input impedance at the operating frequency. However, this must be traded off with tuning out the imaginary part of the optimum noise impedance.

As far as the 2-port's S-parameters are concerned, S_{11} exhibits a dip at the frequency where the imaginary part of the input impedance becomes zero. The steepness of the dip depends on how close the real part of the input impedance is to 50 Ω. In Fig. 9.3, the performance of several types of inductor at input matching is shown.

The ideal inductor yields the expected performance and if a finite quality factor is taken into account, it performs better, due to bringing the real part of the input impedance closer to 50 Ω. Adding shunt capacitors to simulate coupling with ground significantly degrades performance. The PDK model performs very similarly to the EMX model of the inductor. The unshielded inductor is definitely unusable, because it degrades minimum noise figure to unacceptable values. However, the shielded inductors parasitics ruin input matching. Therefore, the decision for an off chip gate inductor was made.

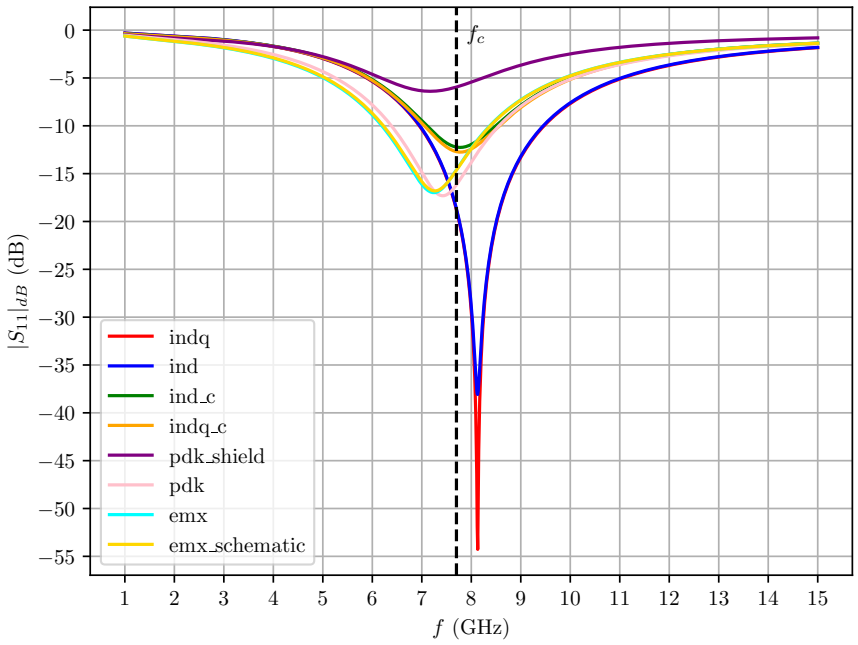


Figure 9.3: Input matching for different typed of gate inductors

- ind, indq: analogLib inductors without and with series resistance
- pdk: inductor model from the 22-FDX PDK
- _c: presence of shunt capacitors
- _shield: shield option enabled
- emx: 2-port S-parameters model from EMX
- emx_schematic: 2-port lumped element model from EMX

9.1.2 The source inductor

The inductive source degeneration is necessary for input matching and improves stability at the cost of reducing gain. By utilizing a simple model shown in Fig. 9.4, the common source stage high frequency input impedance can be found. The capacitance C can contain internal and external capacitances as well as the Miller capacitance.

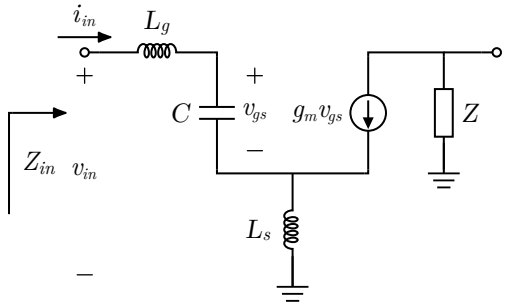


Figure 9.4: A simple model for a common source stage

$$v_{in} = j\omega L_s(g_m v_{gs} + i_{in}) + v_{gs} + j\omega L_g i_{in} \quad \wedge \quad v_{gs} = \frac{i_{in}}{j\omega C} \tag{9.1}$$

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{g_m L_s}{C} + j\left[\omega(L_g + L_s) - \frac{1}{\omega C}\right] \tag{9.2}$$

For this model, closed form solutions for the inductances can be found. However, realistic models are much more complex therefore the expression for Z_{in} is much more useful for just indicating what values of components should be increased or decreased in order to achieve matching. Additionally, the capacitance C can be tuned as well.

$$Z_{in}(j\omega_c) = Z_0 = 50\,\Omega \iff L_s = \frac{Z_0 C}{g_m} \quad \wedge \quad L_g = \frac{1}{\omega_c^2 C} - L_s \tag{9.3}$$

In conclusion it should be noted, that the three components that allow tuning of input and noise matching are the source inductor, the gate inductor, and the gate to source capacitance. The gate to source capacitance can be tuned with device sizing or with external capacitance. The gate and source inductors are tuned by changing geometric aspects of their structure.

Devices should be sized to have high gain and $R_{opt} > 50\,\Omega$. Some of this gain is to be sacrificed for input matching and noise matching by increasing gate to source capacitance with external capacitance and inductive source degeneration. Additionally, inductive source degeneration might need to be increased for stability reasons, further decreasing gain. Tuning out the imaginary part of input impedance and the optimum noise impedance is the last task and only the gate inductor is available for it, thus highlighting the trade off between noise and input matching.

9.2 Design of the second stage

The schematic of the second stage in Cadence Virtuoso is shown in Fig. 9.5. Biasing the second stage is done regarding linearity and not optimal noise performance. This implies large devices and high currents, while keeping the overdrive voltage low.

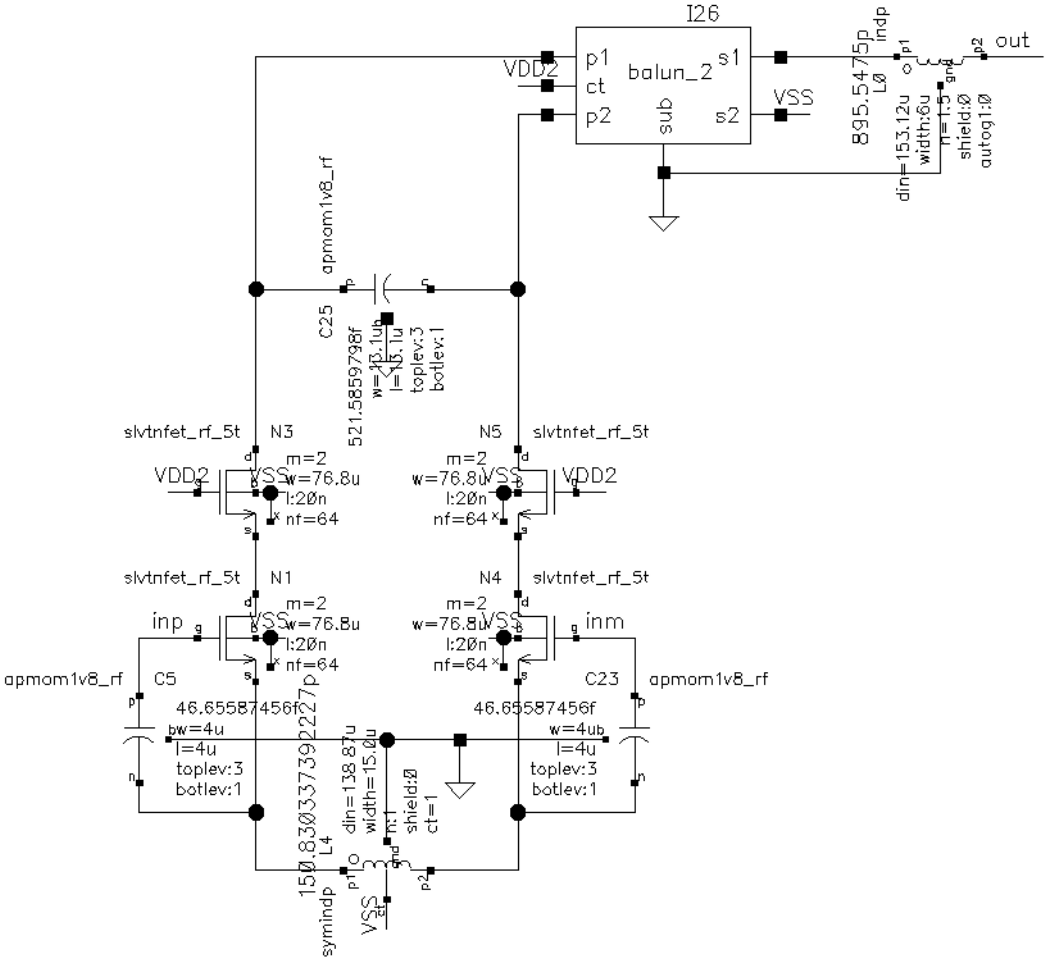


Figure 9.5: Schematic of the second stage in Cadence Virtuoso

At high drain currents the relationship of current with gate to source voltage is much more linear, leading to smaller variations in transconductance during large signal operation. Additionally, low overdrive voltages ensure that the devices stay in saturation and operate more linearly during large signal operation, because large variations in V_{DS} do not necessarily make it lower than V_{OV} and a device remains in saturation as long as $V_{DS} \geq V_{OV} = V_{GS} - V_{t_n}$. Therefore, the gates need to be biased at moderate voltages near the threshold voltage.

The external gate to source capacitances and inductive source degeneration are tuned for stability and input matching. Therefore, the transistors of this stage are biased for sufficient linearity and high gain and some of this gain is traded off for interstage matching and stability. A balun transformer is utilized for output matching and an extra inductor is seen at the output, due to the inductances achieved by the transformer not being enough for matching.

9.3 Balancing units and matching

After adequate performance from both stages has been ensured, matching must follow, especially for the transition from balanced to unbalanced signaling. Balancing units and how they are used in impedance matching were discussed in detail in 7.3. Especially, balun transformer design was discussed in 7.3.2. However, these guidelines serve well up to a point and after that a lot of fine tuning is required.

Essentially, after a point it is more convenient to consider the balun as part of a stage and tune external gate to source capacitances or drain capacitances, in order to achieve matching. Furthermore, as already mentioned, some extra inductance was required at the output. Necessity for very large inductances had posed a problem from very early on, because the transformers offered by the PDK came in limited dimensions, specifically too little diameters.

Consequently, custom balun transformers were generated with SKILL scripts kindly provided by Dimitrios Georgakopoulos. Larger diameters posed challenges as well, due to capacitive parasitics. In an effort to mitigate them, turn width was reduced, effectively sacrificing quality. The same balun transformer was used between stages and at the output and it is shown in Fig. 7.12. It was modeled by electromagnetic simulation and included in schematic simulations as a file of S-parameters from the beginning.

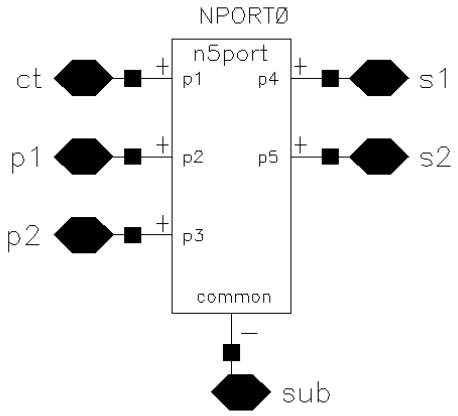


Figure 9.6: A 5-port with the balun transformer's S-parameter file loaded

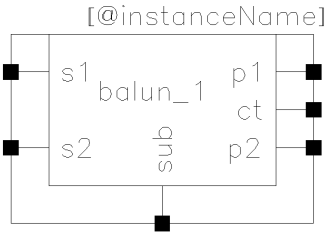


Figure 9.7: The balun transformer's symbol

9.4 I/O parasiticts

The input and output parasitics discussed in 8 were included in the schematic simulations from the beginning. The assumption that there is some control over the length of bond wires during packaging design was made.

9.4.1 Signal path and ground

Bond wires and pads are required at the input and at the output. Six bond wires are used to bring the PCB ground on chip, in order to minimize the effect of their inductance. This inductance degrades performance, especially stability. At high frequencies capacitors can also be used in order to tune out bond wire self inductance while bringing PCB ground on chip, however this was not required here.

The signal path from the antenna to the chip requires a coupling capacitor so that the DC voltage level at the input does not affect the antenna. The value of that capacitor needs to be 20 pF, because at 7.7 GHz its impedance is $X_C \approx -1.03\,\Omega$ and it does not affect the circuit. Such a large capacitor on the signal path could not be included on chip due to noise and parasitics. Also, note the absence of a gate inductor as a supposed 1 nH bond wire inductance was sufficient. This bond wire would have to be tuned and simulated during packaging design.

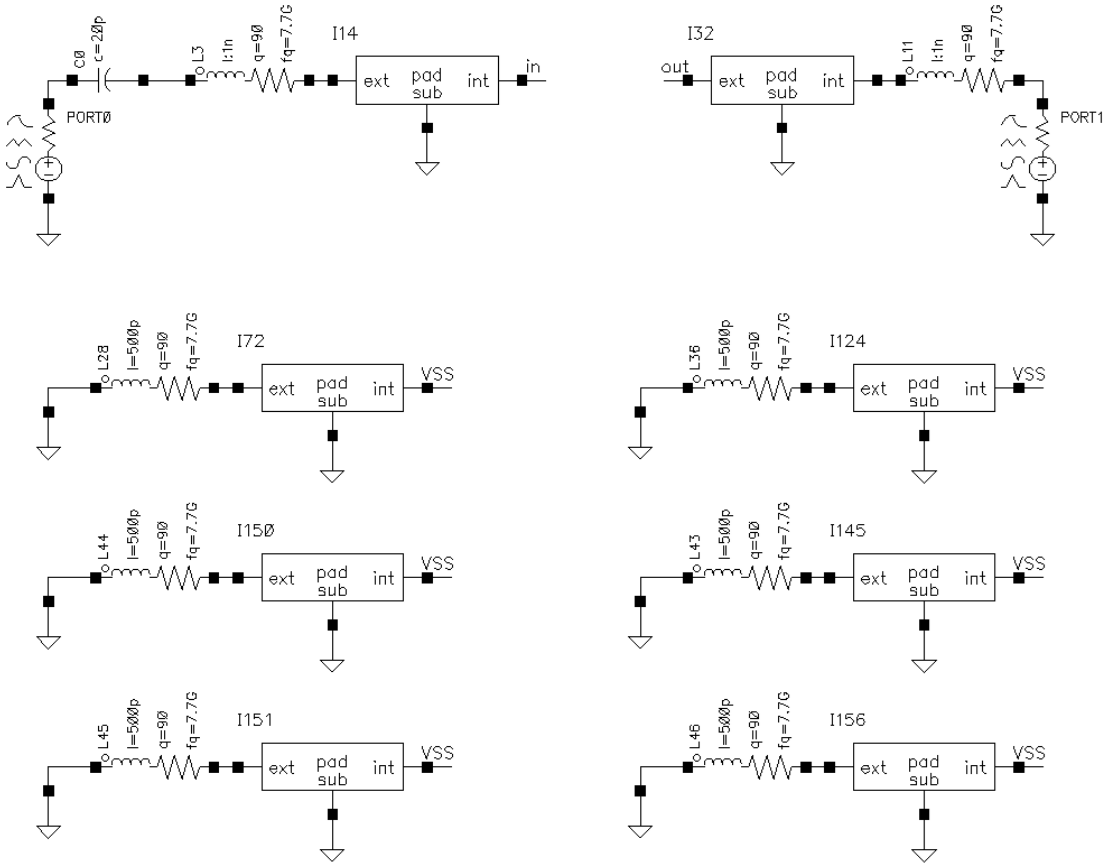


Figure 9.8: Signal path and ground bond wires and pads

9.4.2 Biasing and supply voltages

The biasing and supply voltages for the circuit are generated by external voltage sources and brought on chip with bond wires. This allows for some flexibility in case something fails to work as expected. Each stage has its own supply in order to combat signal paths between stages potentially ruining stability.

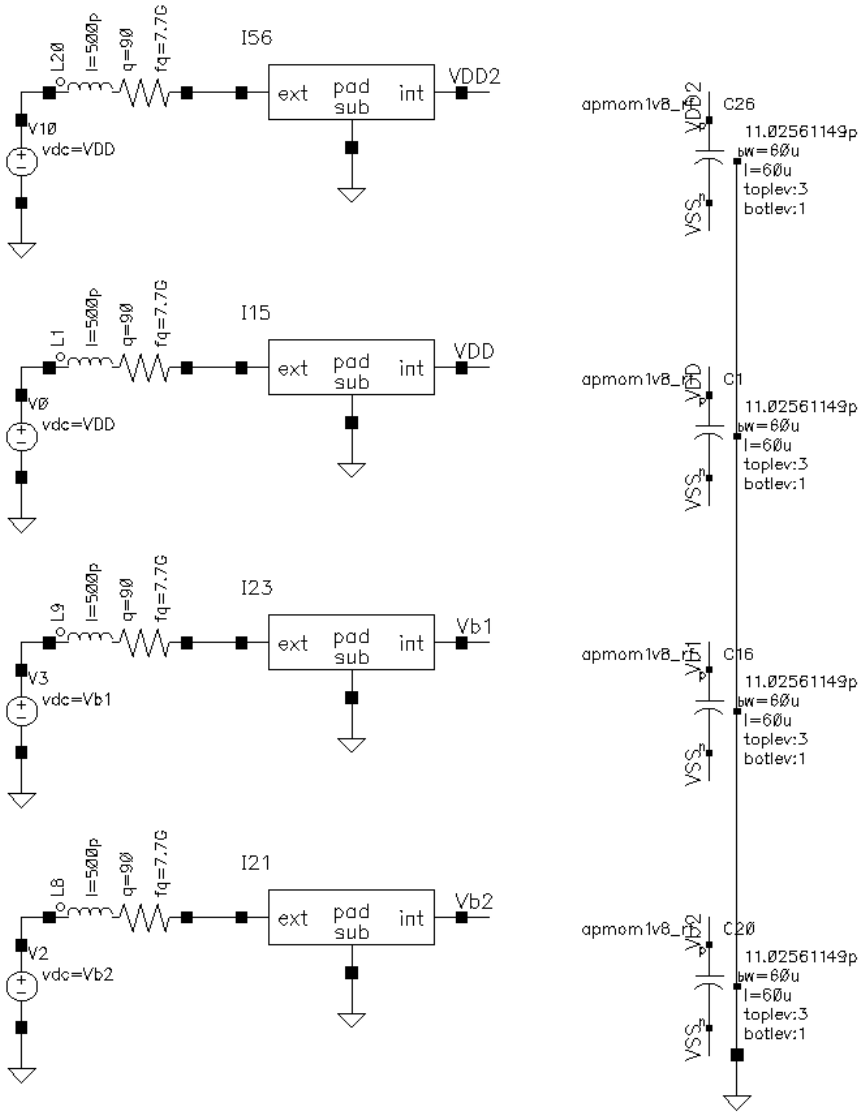


Figure 9.9: Bias bond wires and decoupling capacitors

Additionally, decoupling capacitors are shown here because they are placed immediately after the DC voltage pads. They ensure that V_{DD} and V_{SS} are practically equipotential for AC signals. They improve reverse isolation and stability. Their values were selected by beginning with really large capacitors and making their capacitance smaller up until circuit performance was significantly degraded. Afterwards, a bit larger capacitors were used maintaining adequate performance.

9.5 Simulation results

9.5.1 Nominal case

After iterating through the explained process and tuning everything as required, the following nominal results were achieved. Noise figure and minimum noise figure are shown in Fig. 9.10, where excellent noise matching can be observed, which can be confirmed with the values of the optimum noise impedance in Fig. 9.11.

The S-parameters are shown in Fig. 9.12, where mathing, gain and reverse isolation are observed. The behavior exhibited by S_{11} at frequencies higher than the operating frequency is attributed to the second stage acting as a load to the first stage. Such behavior was not observed and there when the first stage was being designed with the input impedance of the second stage at the operating frequency as a load. At the schematic level, noise matching did not have to be sacrificed for input matching. Every type of gain is presented in Fig. 9.13, confirming maximum power transfer by conjugate matching.

Metric	**Symbol**	**Value**
Noise figure	NF	0.585 dB
Minimum noise figure	NF_{min}	0.579 dB
Optimum noise impedance	Z_{opt}	$(43.06 + j\,0.812)\,\Omega$
Gain	$\lvert S_{21}\rvert_{\mathrm{dB}}$	33.78 dB
Input return loss	$-\lvert S_{11}\rvert_{\mathrm{dB}}$	33.05 dB
Output return loss	$-\lvert S_{22}\rvert_{\mathrm{dB}}$	37.3 dB
Reverse isolation	$-\lvert S_{12}\rvert_{\mathrm{dB}}$	65.49 dB
Input referred 1dB compression point	$\mathrm{IP1dB}_{\mathrm{dBm}}$	−31.15 dBm
Output referred 1dB compression point	$\mathrm{OP1dB}_{\mathrm{dBm}}$	1.63 dBm
Input referred third order intercept point	$\mathrm{IIP3}_{\mathrm{dBm}}$	−7.21 dBm
Output referred third order intercept point	$\mathrm{OIP3}_{\mathrm{dBm}}$	26.64 dBm
Stability metrics	K / B_1	19.25 / 0.9996
Alternative stability metrics	μ / μ'	25.41 / 20.8
Quiescent current	I_Q	39.82 mA
Power consumption	P_{DC}	31.86 mW

Table 9.1: LNA schematic nominal results

Note that input impedance in Fig. 9.14 and output impedance in Fig. 9.15 are calculated with signal excitation at one port and matching at the other.

$$Z_{M_1} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \quad \wedge \quad Z_{M_2} = Z_0 \frac{1 + S_{22}}{1 - S_{22}} \tag{9.4}$$

Stability metrics are presented in Fig. 9.16 and Fig. 9.17 confirms unconditional stability more clearly. Additionally, the K stability factor is presented in Fig. 9.18 along with the B_1 factor in Fig. 9.19 confirming unconditional stability once again. Unconditional stability was also confirmed for frequencies from 100 kHz up to 1 THz, however the diagrams over such a large frequency range are not clear, therefore they are not presented here.

Finally, non linearity metrics are presented. The results of a single tone test are shown in Fig. 9.20, providing the 1 dB compression point, and the results from a multitone test are presented in Fig. 9.21, providing the third order intercept point.

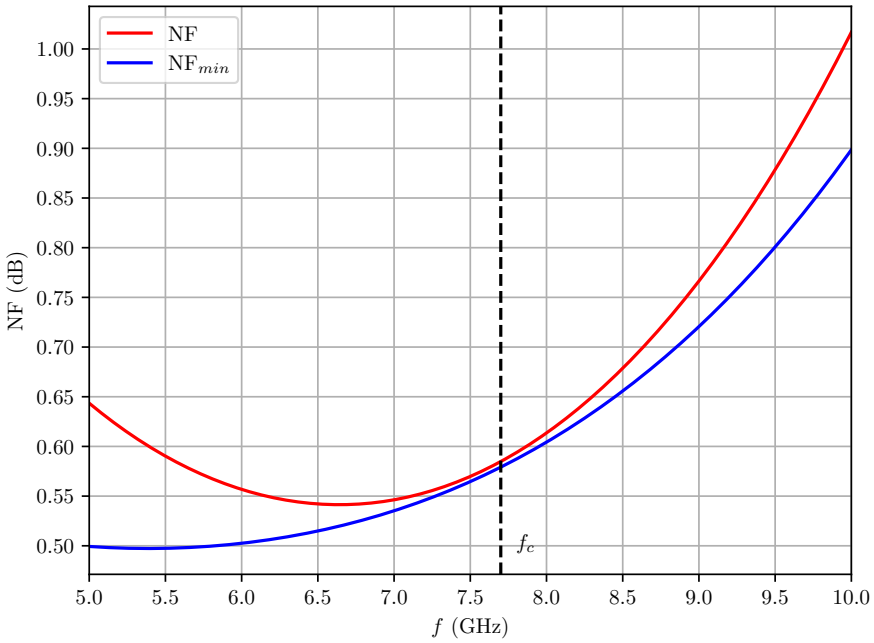


Figure 9.10: LNA schematic noise figure

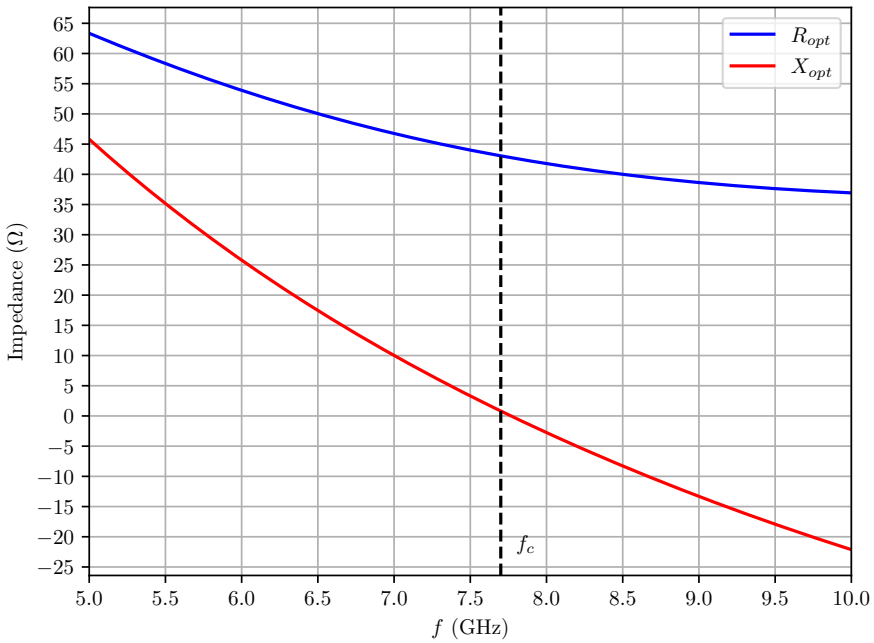


Figure 9.11: LNA schematic optimum noise impedance

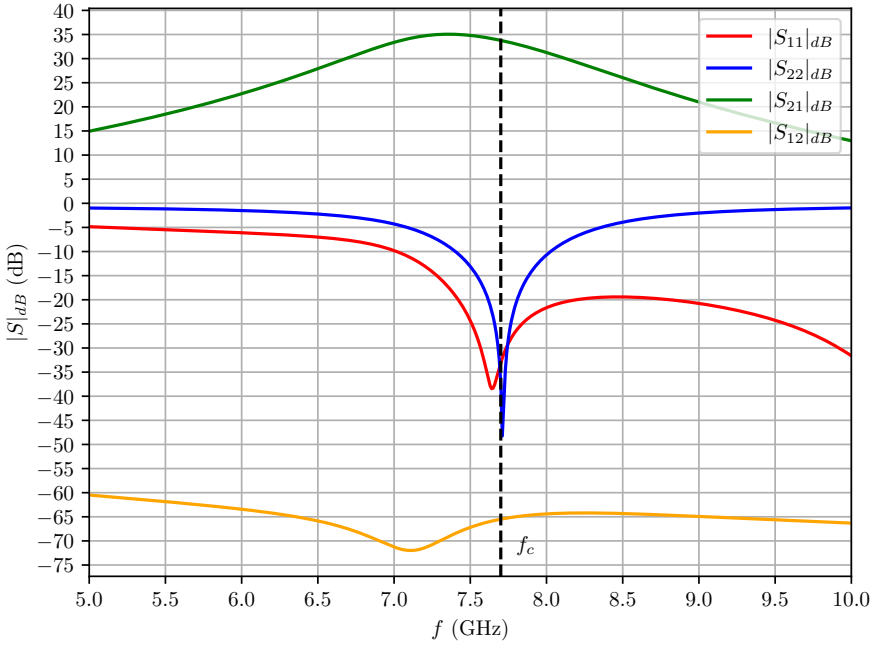


Figure 9.12: LNA schematic S-parameters

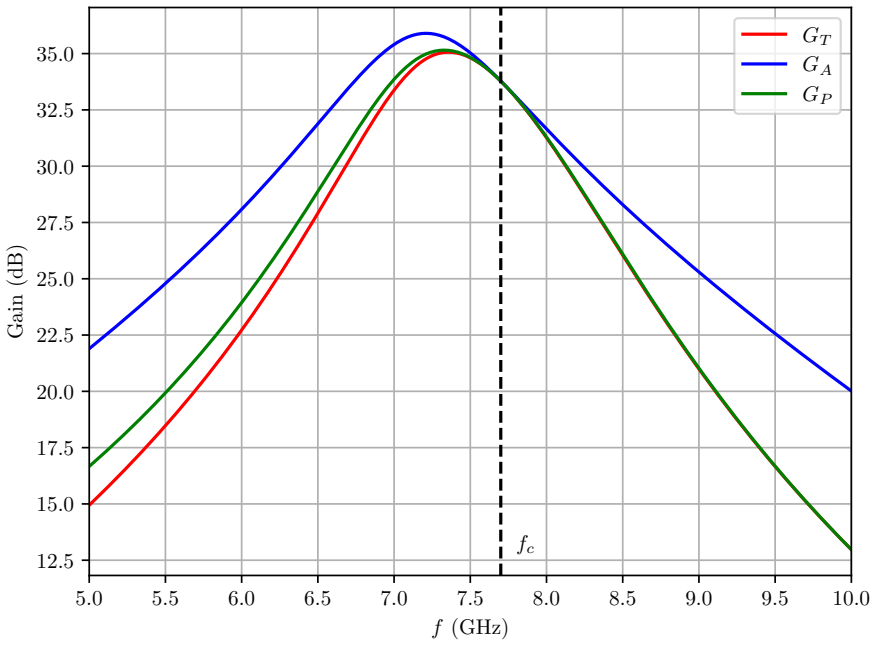


Figure 9.13: LNA schematic gains

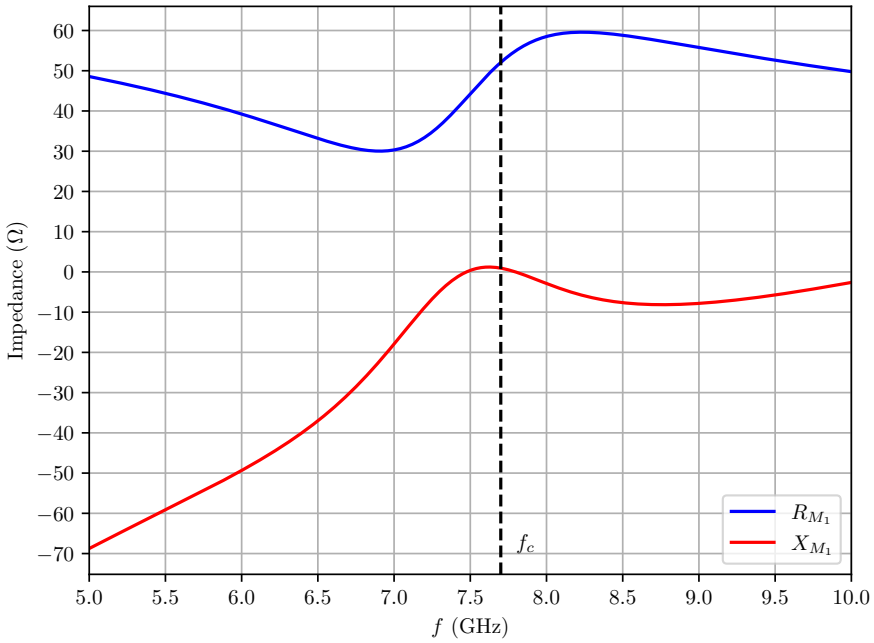


Figure 9.14: LNA schematic input impedance

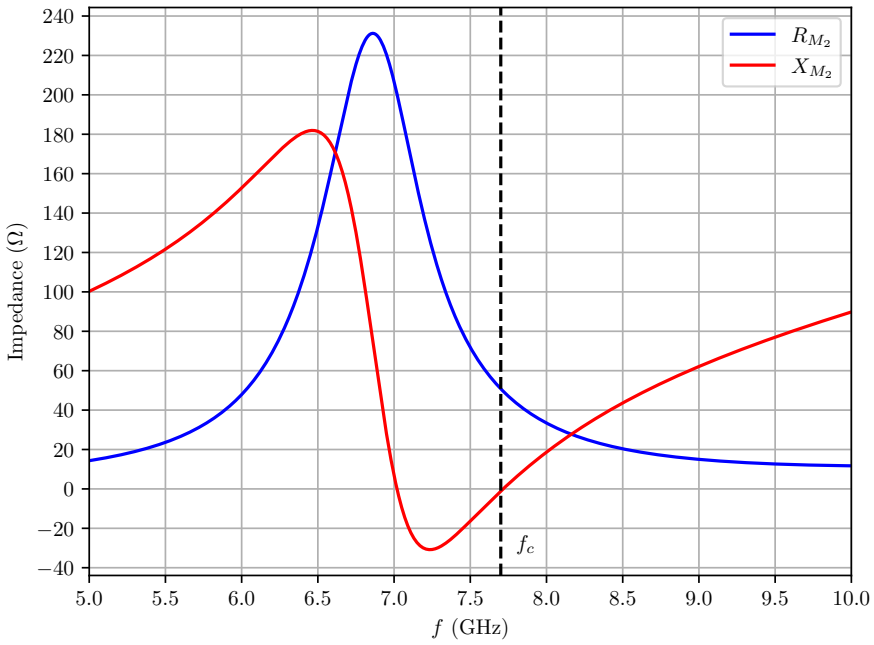


Figure 9.15: LNA schematic output impedance

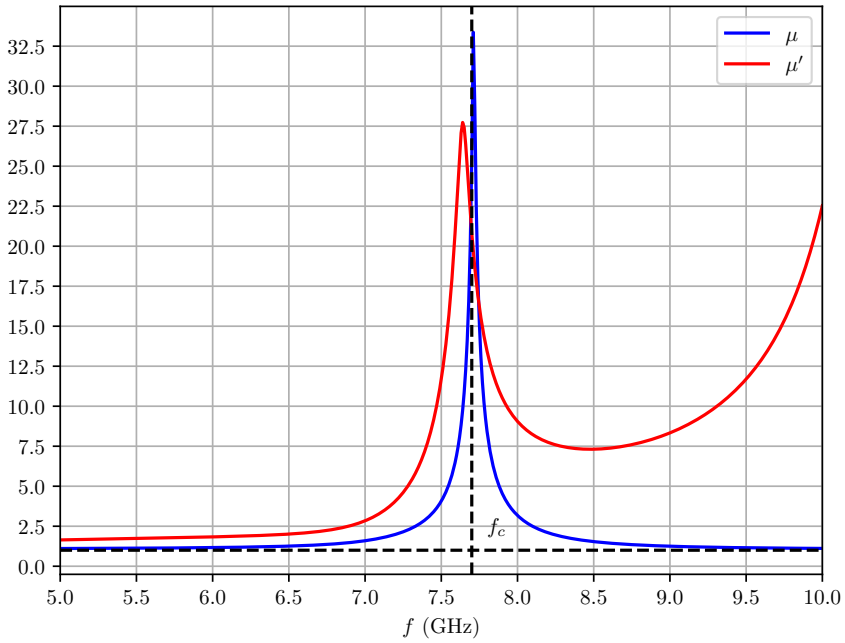


Figure 9.16: LNA schematic stability factors μ and μ'

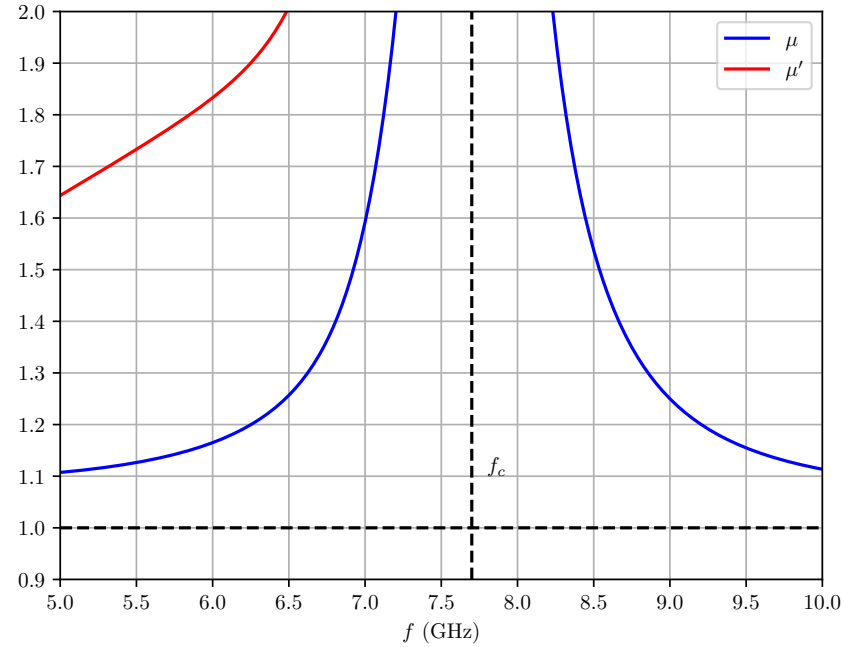


Figure 9.17: LNA schematic stability factors μ and μ' (zoomed in)

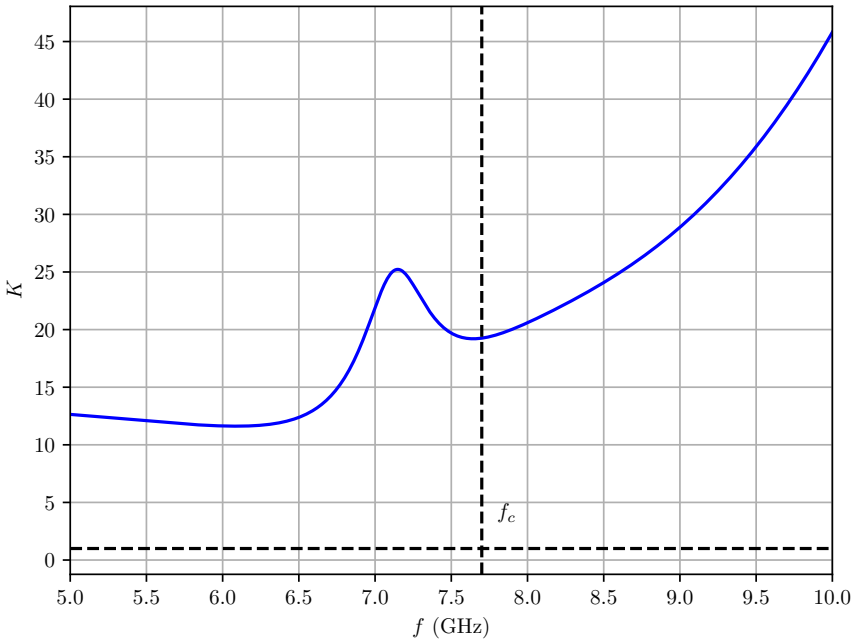


Figure 9.18: LNA schematic stability factor K

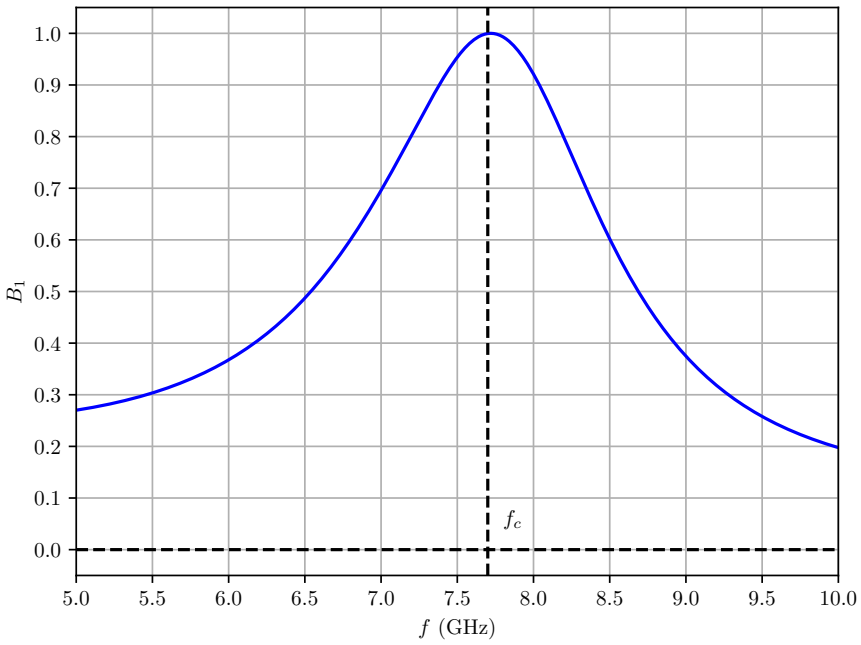


Figure 9.19: LNA schematic stability factor B_1

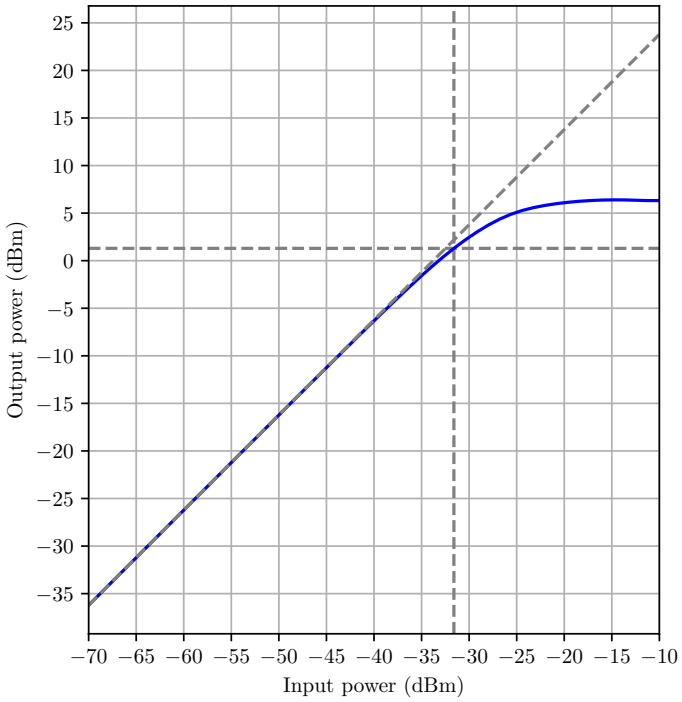


Figure 9.20: LNA schematic output power compression

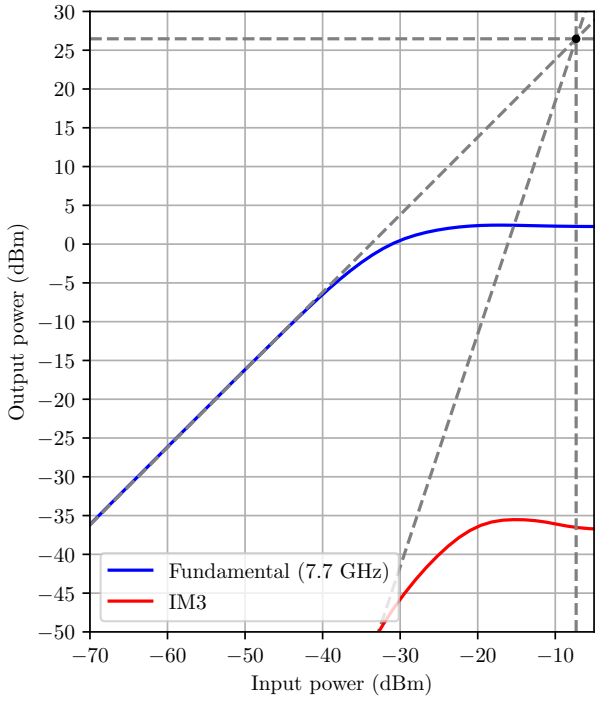


Figure 9.21: LNA schematic third order intercept point

9.5.2 Corner cases

To ensure reliable circuit performance under process, voltage, and temperature (PVT) variations, simulations are carried out across defined corner cases. These corners represent unfortunate manufacturing scenarios, where transistor parameters such as threshold voltage, charge carrier mobility, and oxide thickness may deviate from their nominal values. The corners at which the schematic was simulated entailed typical, fast, and slow transistors (TT, FF, FS, SF, SS), some temperatures, specifically $-40\,^{\circ}\mathrm{C}$, $60\,^{\circ}\mathrm{C}$, and $125\,^{\circ}\mathrm{C}$, and $\pm 10\%$ variations of the supply voltage. The minimum and maximum values across corners for the performance metrics of the schematic are shown in the following table.

Metric	Minimum	Nominal	Maximum
NF	0.375 dB	0.585 dB	1.055 dB
NF_{min}	0.374 dB	0.579 dB	1.012 dB
$\lvert S_{21}\rvert_{\mathrm{dB}}$	22.93 dB	33.78 dB	37.21 dB
$-\lvert S_{11}\rvert_{\mathrm{dB}}$	11.79 dB	33.05 dB	34.52 dB
$-\lvert S_{22}\rvert_{\mathrm{dB}}$	6.4 dB	37.3 dB	37.3 dB
$-\lvert S_{12}\rvert_{\mathrm{dB}}$	62.84 dB	65.49 dB	69 dB
K / B_1	12.23 / 0.791	20.8 / 0.9996	23.78 / 1.007
μ / μ'	1.972 / 3.505	25.41 / 20.8	25.41 / 23.78
I_Q	17 mA	39.82 mA	76.59 mA
P_{DC}	12.24 mW	31.86 mW	67.4 mW

Table 9.2: LNA schematic corner cases simulation results

In general, higher temperatures degrade noise performance, as expected due to higher thermal noise power. Variations of the supply voltage did not significantly degrade performance. The fast-fast and slow-slow corners exhibited the most issues with impedance matching and noise performance. At those corners the electrical parameters of the transistors change and the bias currents become very different. Since a silicon on insulator process is being used, adaptive body biasing techniques could be implemented to counteract that.

All things considered, the schematic operated as a low noise amplifier with low noise figure and high gain at every corner while remaining unconditionally stable.

9.5.3 Monte Carlo simulation

Monte Carlo simulations are used in circuit design to statistically evaluate the impact of manufacturing variations on performance. By randomly varying device parameters such as threshold voltage, charge carrier mobility, or component values according to process-defined distributions, Monte Carlo analysis show how physical variability affects metrics like gain, noise figure, or power consumption. Running hundreds or thousands of simulations provides insight into yield, robustness, and worst case behavior.

A Monte Carlo simulation with 200 samples was performed for the schematic. The results for noise figure are shown in Fig. 9.22, where low variance can be observed. Additionally, all samples performed great in terms of gain, as shown in Fig. 9.23. Finally, Fig. 9.24 and Fig. 9.25 show that unconditional stability at the operating frequency is almost guaranteed, since the distributions of samples are very far from values less than 1.

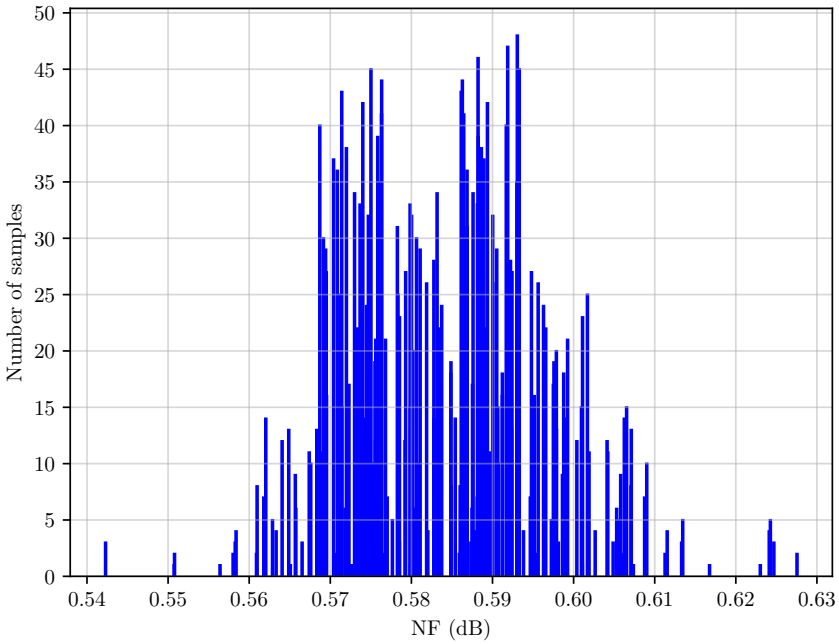


Figure 9.22: Monte Carlo results for schematic noise figure

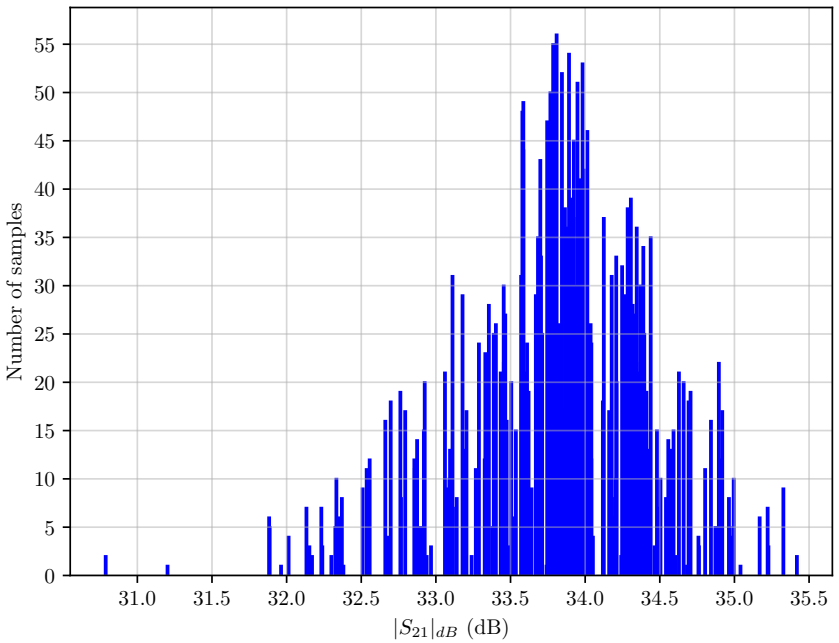


Figure 9.23: Monte Carlo results for schematic gain

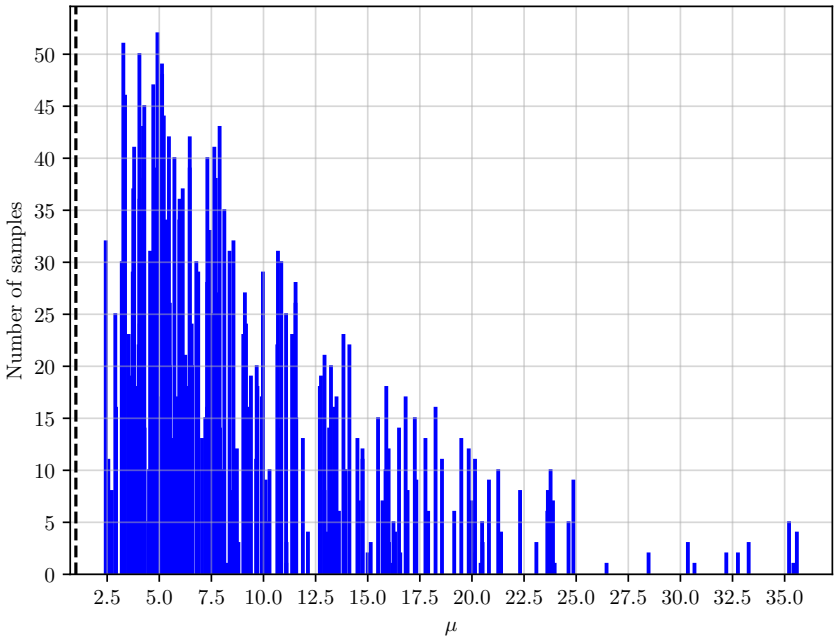


Figure 9.24: Monte Carlo results for schematic stability factor μ

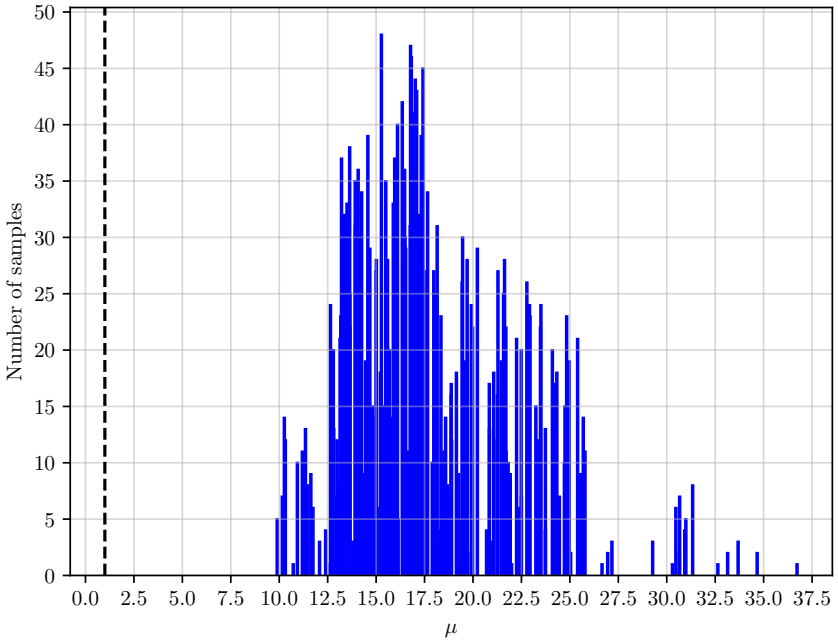


Figure 9.25: Monte Carlo results for schematic stability factor μ'

Chapter 10

LNA layout design

Since schematic design was done with PDK components and structures modeled by electromagnetic simulation, many layout dependent effects had already been accounted for. However, in the GF22 FD-SOI RF library, transistors provide connectivity only up to the first metal layer and their models do not extend beyond that. Additionally, while pads were included in the schematic, interconnects were not.

Consequently, the layout required custom design of the transistor connections to higher metal layers and the routing of interconnects. These elements had to be carefully modeled and certain aspects of the original design were adjusted to mitigate the performance degradation introduced by these physical layout effects. The PDK offers 8 metal layers, which were used for this work.

The layout design process was broken into blocks and stages and design rule checks (DRC) as well as layout schematic verification (LVS) were performed for every block. Additionally, electromagnetic simulation models were created for every block from DC up to 30 GHz. This frequency range was chosen to include third order harmonics which are generated at around 23.1 GHz. At some higher levels of hierarchy small block models were discarded in favor of larger block models including more structures, so that interactions between components could be accounted for.

The layout design stages were the following. Firstly, transistors were connected to higher metals. Secondly, the cascodes were created by routing interconnects between transistors. Afterwards, a rough placement of inductors was required in order to ensure the absence of significant magnetic feedback, which could potentially ruin stability. Finally, long RF interconnects were routed and pads were placed.

Near the end of the layout process but before final verification, the designer must ensure that antenna rules, electrostatic discharge (ESD) protection, and metal fill requirements are properly addressed. For antenna rules, this means checking for violations where long metal interconnects touch transistor gates without an early diffusion connection, and inserting antenna diodes or rerouting as needed. For ESD, the designer must use foundry-approved I/O cells with built-in protection and ensure proper placement of clamps, guard rings, and isolation structures. In addition, metal fill must be added to meet density rules required by the foundry, while ensuring that the added fill does not degrade circuit performance, especially in sensitive RF or analog regions. Since a tapeout was not within the scope of this thesis, this part was omitted.

10.1 Transistor layout

In a low noise amplifier, transistors need to connect to high metal layers because they are designed to be the most suitable for RF interconnects. The two lowest metal layers were used to connect all the fingers together and two gate contacts were made at either side of the transistors. These contacts were connected together with a higher metal layer. Sources and drains were raised to higher metal layers than the two bottom ones and contacts were provided at the three higher metal layers. The transistor used in the first stage is shown in Fig. 10.1, while the one used for the second stage is shown in Fig. 10.2 and their fingers are visible. Note that the two images are not to scale, each image is enlarged to fit the page for better clarity, therefore transistor size comparisons between them cannot be made.

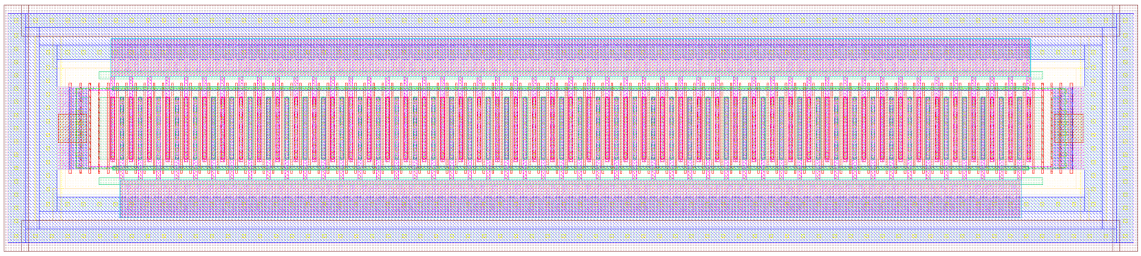


Figure 10.1: Layout of the first stage transistors

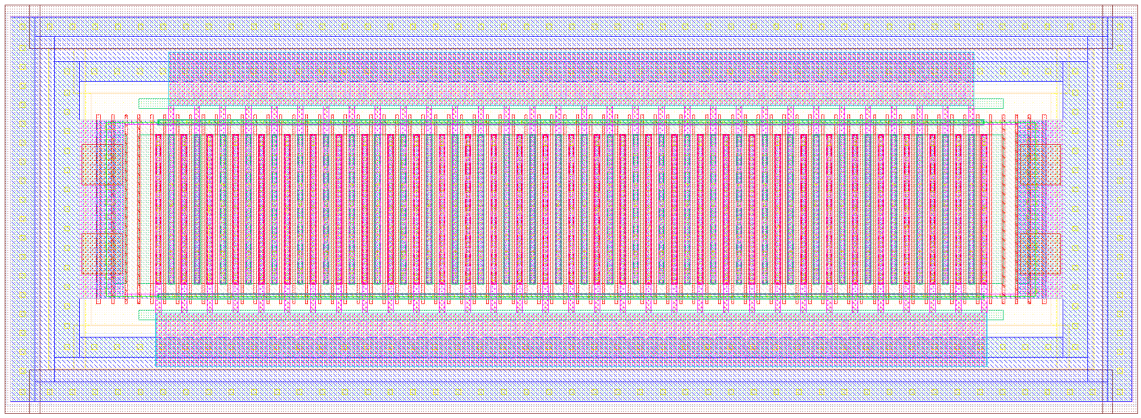


Figure 10.2: Layout of the second stage transistors

10.2 Cascode layout

In order to create cascodes, transistors must be interconnected. Common centroid techniques were avoided due to complex routing. The common source stage was placed at the bottom and the common gate at the top in an effort to minimize and simplify interconnects, which is crucial at high frequencies. The cascode of the first stage is shown in Fig. 10.3, while the cascode of the second stage is shown in Fig. 10.4 and the multiplicity of each transistor is visible. Three metal levels connected with vias were used to interconnect the transistors, in order to minimize losses. Note that the two images are not to scale once again.

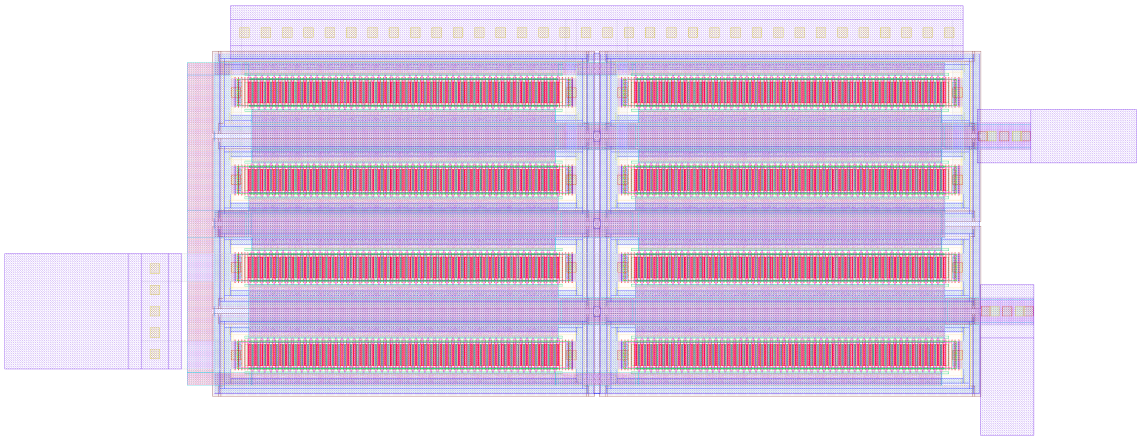


Figure 10.3: Layout of the first stage cascode

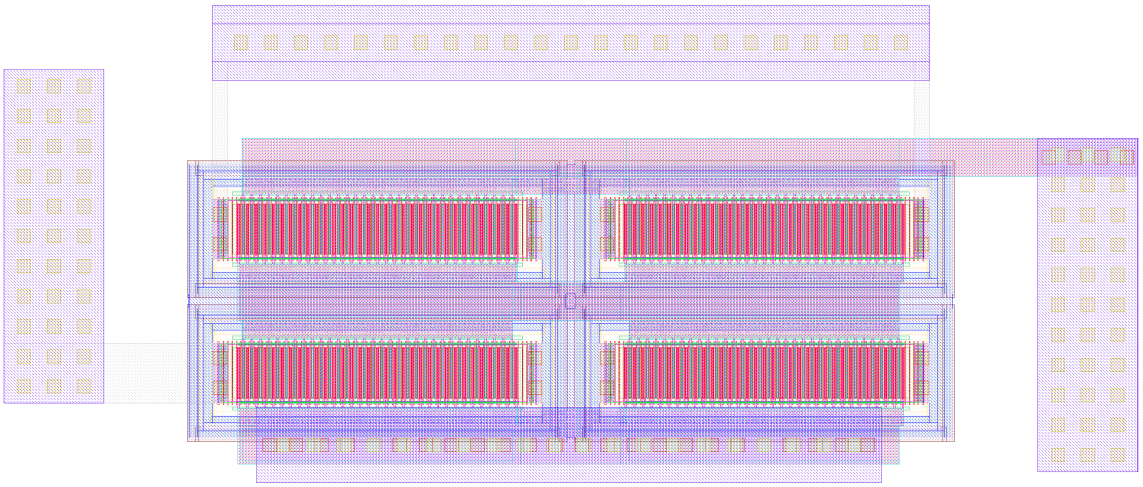


Figure 10.4: Layout of the second stage cascode

10.3 Post-modeling redesign and simulation

After connecting transistors to higher level metals and interconnecting them together to create cascodes, electromagnetic simulations took place in order to extract models. Layout effects altered the performance, therefore redesign was required.

The bond wire self inductance of 1 nH was no longer enough and an off chip gate inductor was placed at the input, as shown in Fig. 10.5. The new design includes cascode models up to the higher level metals, as shown in Fig. 10.6 and Fig. 10.7. Additionally, the inductor at the output was simulated together with the second balun transformer because they are in the same signal path and they are to be placed close to each other. The source degeneration inductor of the second stage has been replaced by two source degeneration inductors for reasons discussed in 10.4. These changes can be seen in Fig. 10.7.

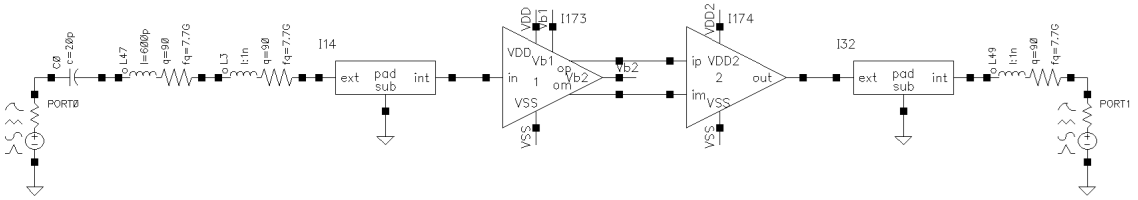


Figure 10.5: The LNA after redesign at a high level of hierarchy

The new design was simulated as was the schematic design and the new results are summarized in the following table. Noise performance was degraded as expected, since interconnects are lossy. However, performance in general was salvaged. The same diagrams showing results like in the schematic case follow.

Metric	Symbol	Value
Noise figure	NF	0.867 dB
Minimum noise figure	NF_{min}	0.811 dB
Optimum noise impedance	Z_{opt}	$(69.82 - j\,14.28)\,\Omega$
Gain	$\lvert S_{21}\rvert_{\mathrm{dB}}$	30.52 dB
Input return loss	$-\lvert S_{11}\rvert_{\mathrm{dB}}$	23.27 dB
Output return loss	$-\lvert S_{22}\rvert_{\mathrm{dB}}$	37.91 dB
Reverse isolation	$-\lvert S_{12}\rvert_{\mathrm{dB}}$	58.12 dB
Input referred 1dB compression point	$\mathrm{IP1dB}_{\mathrm{dBm}}$	−30.13 dBm
Output referred 1dB compression point	$\mathrm{OP1dB}_{\mathrm{dBm}}$	−0.611 dBm
Input referred third order intercept point	$\mathrm{IIP3}_{\mathrm{dBm}}$	−9.407 dBm
Output referred third order intercept point	$\mathrm{OIP3}_{\mathrm{dBm}}$	21.15 dBm
Stability metrics	K / B_1	11.96 / 1.003
Alternative stability metrics	μ / μ'	18.83 / 9.093
Quiescent current	I_Q	29.54 mA
Power consumption	P_{DC}	23.63 mW

Table 10.1: LNA redesign results

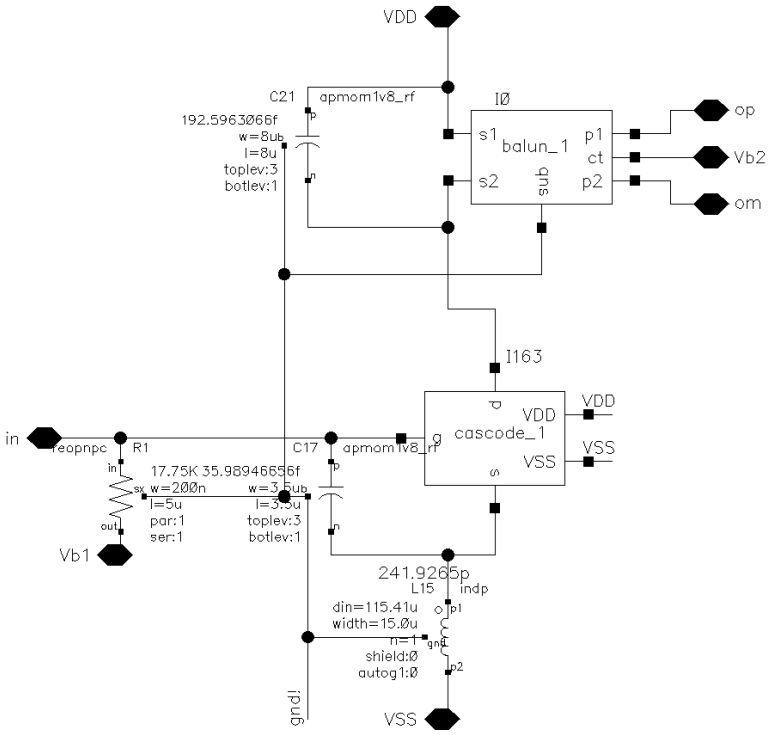


Figure 10.6: The first stage after redesign

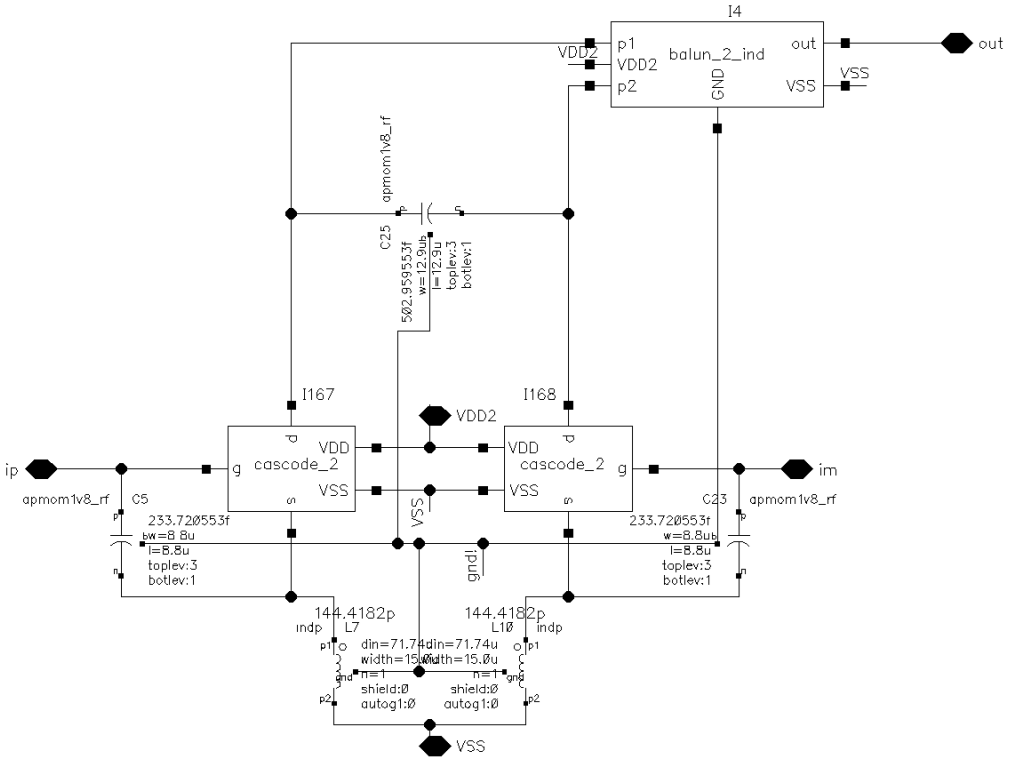


Figure 10.7: The second stage after redesign

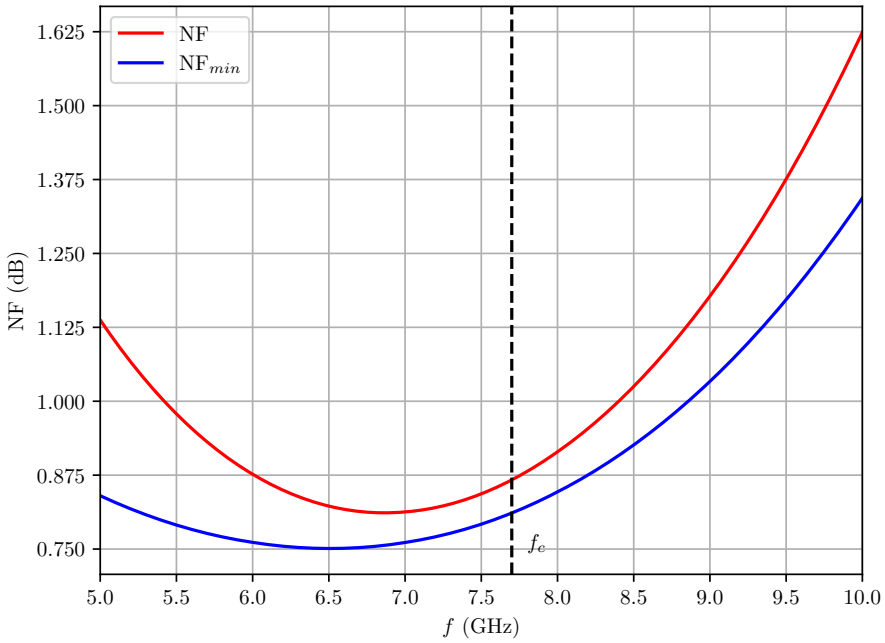


Figure 10.8: LNA redesign noise figure

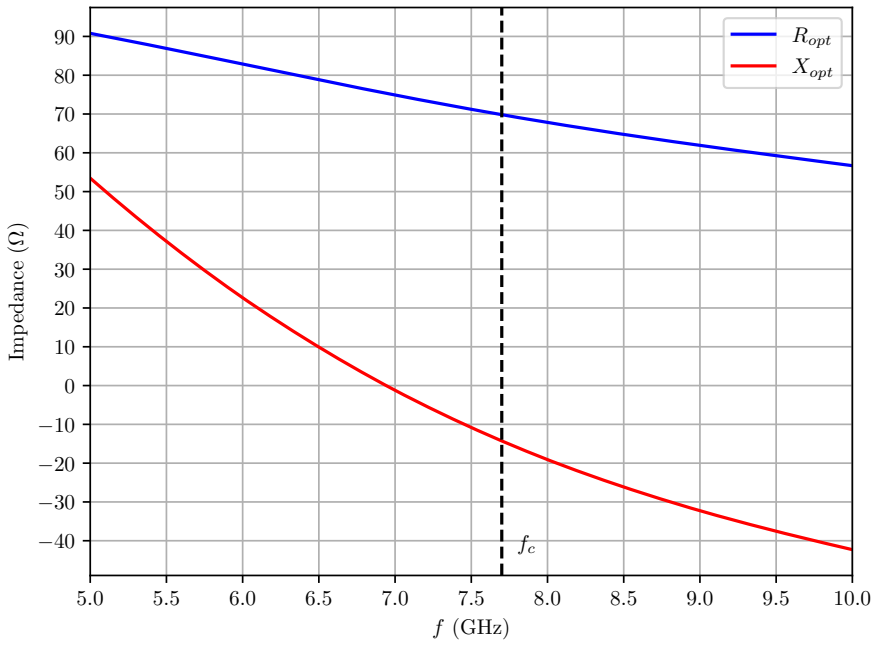


Figure 10.9: LNA redesign optimum noise impedance

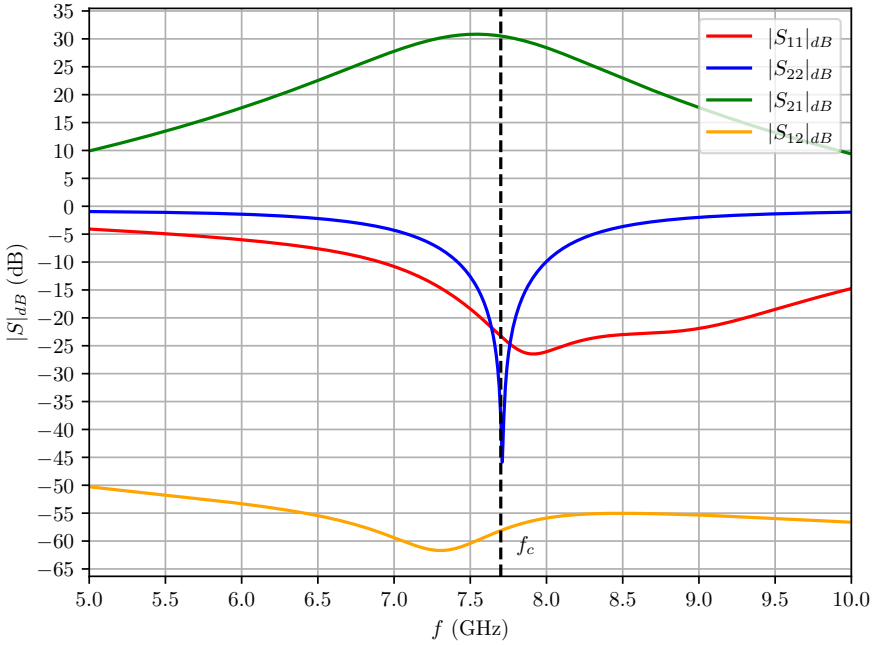


Figure 10.10: LNA redesign S-parameters

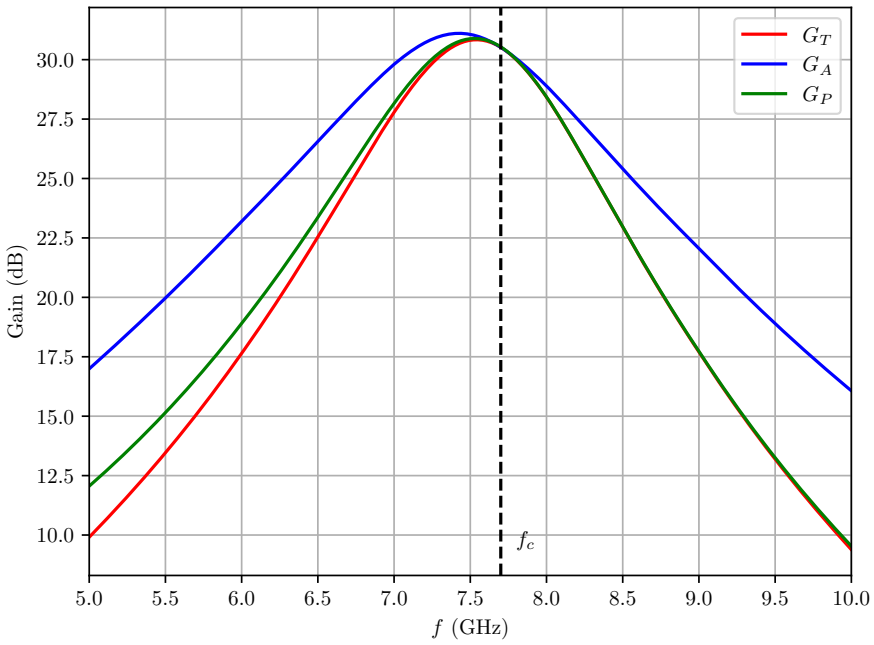


Figure 10.11: LNA redesign gains

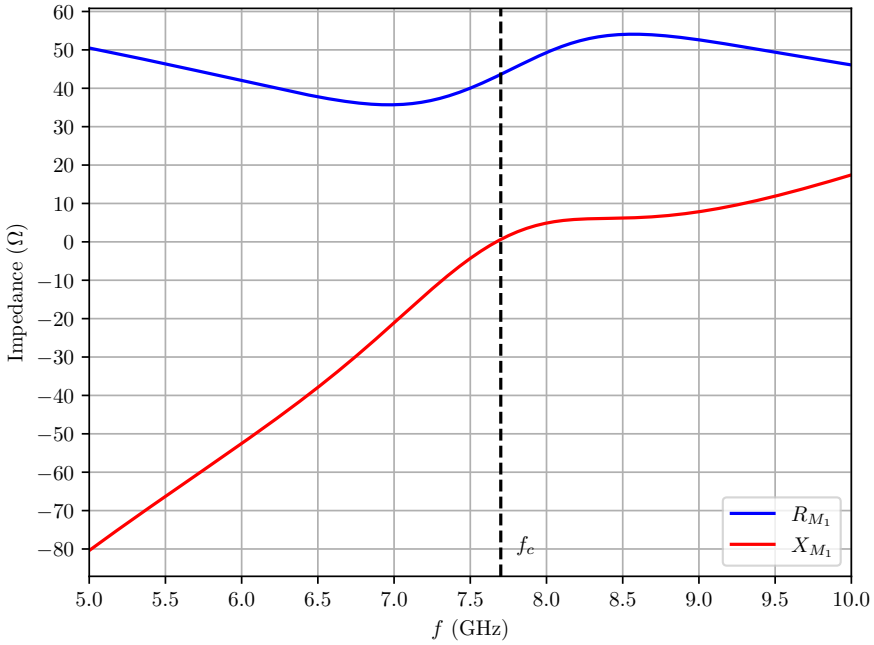


Figure 10.12: LNA redesign input impedance

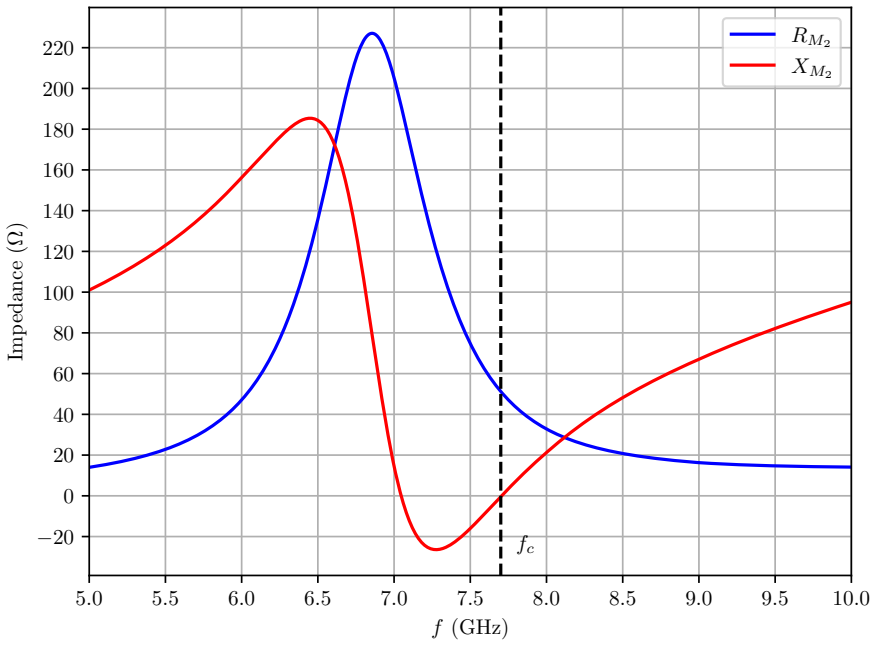


Figure 10.13: LNA redesign output impedance

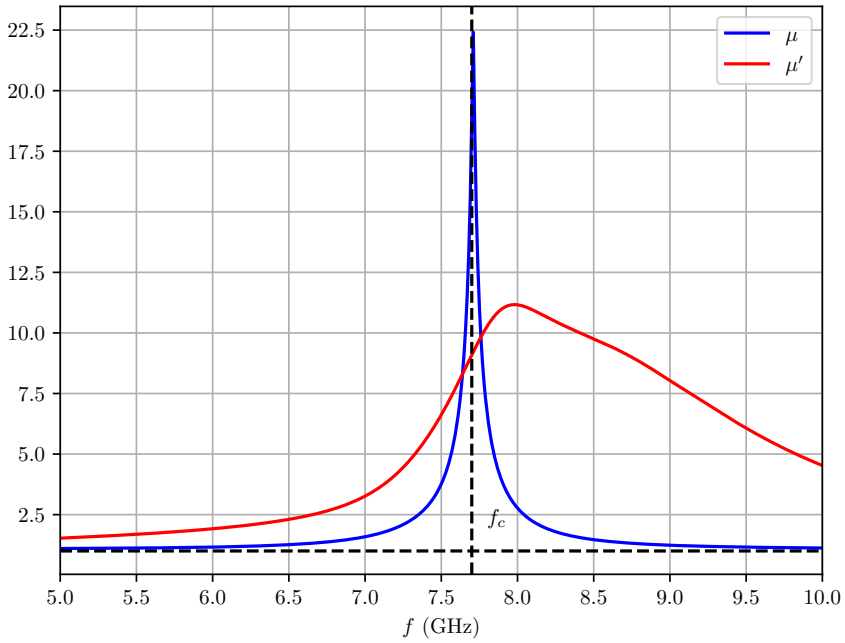


Figure 10.14: LNA redesign stability factors μ and μ'

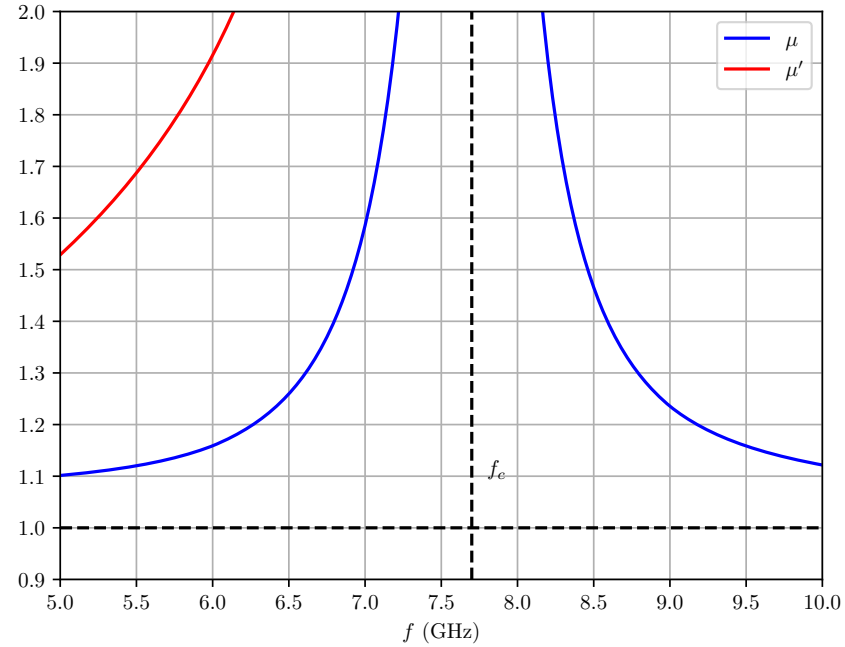


Figure 10.15: LNA redesign stability factors μ and μ' (zoomed in)

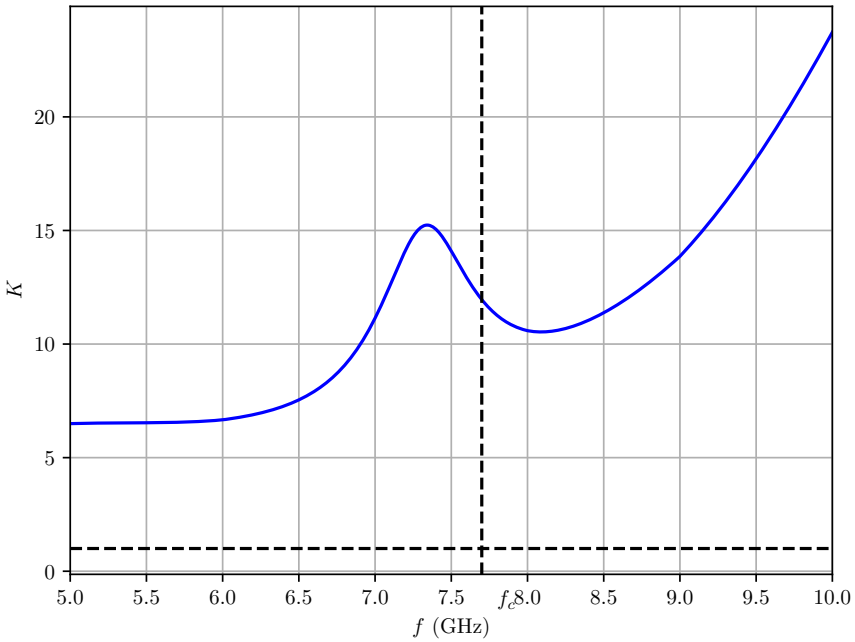


Figure 10.16: LNA redesign stability factor K

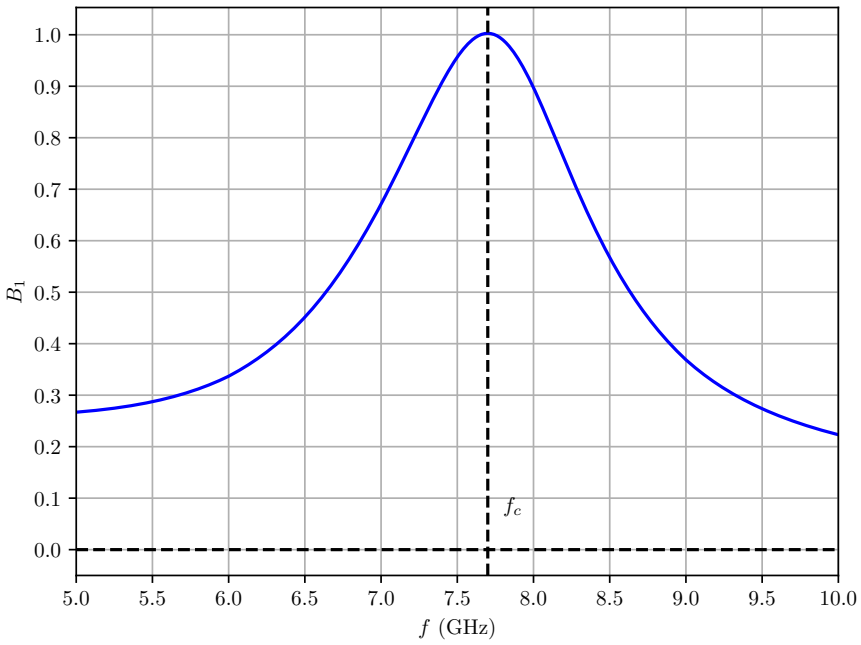


Figure 10.17: LNA redesign stability factor B_1

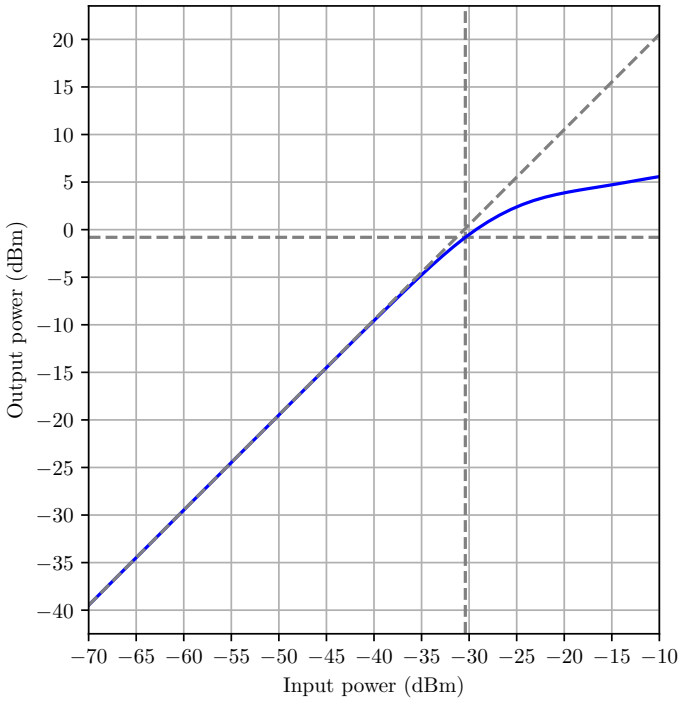


Figure 10.18: LNA redesign output power compression

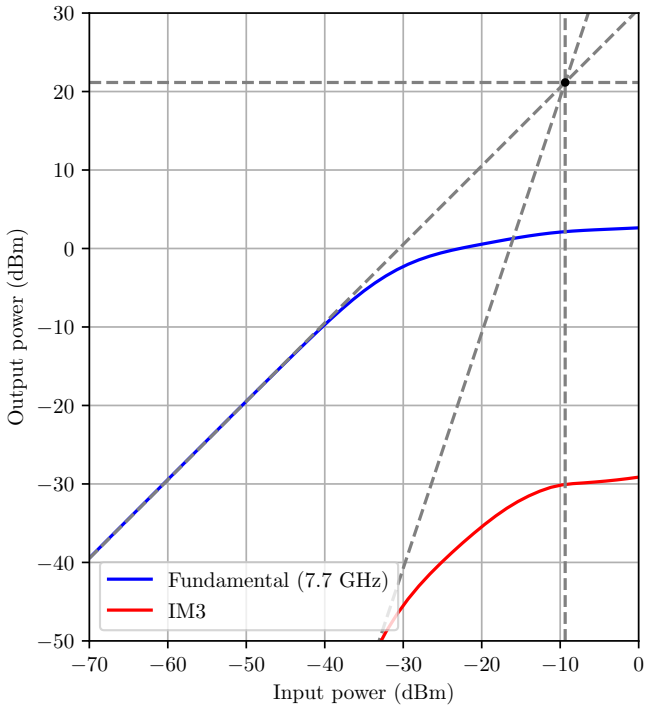


Figure 10.19: LNA redesign third order intercept point

10.4 Inductor placement

Magnetic feedback can potentially ruin stability, therefore it must be avoided. For that reason inductors must be placed with enough distance between them. The rule of thumb is that two inductors must be placed at a distance larger than the outer diameter of the larger one so that the interference between them is negligible. Since inductors cover a rectangular area anyway, due to several extra layers they require or potential guard rings, placing them diagonally is favorable.

However, for the second stage to be symmetric, the two balun transformers had to be placed on the same horizontal and it was critical to maintain enough distance between them. Note that the center tapped source degeneration inductor of the second stage had to be replaced at that point. Maintaining symmetry with a single inductor would require for it to be placed in the middle of the balun transformers driving them further apart and necessitating longer interconnects. Using two inductors allowed for the use of the minimum distance with no interference between the balun transformers, while the two source degeneration inductors were placed in the middle, diagonally to the baluns and as close as possbile without significant interference.

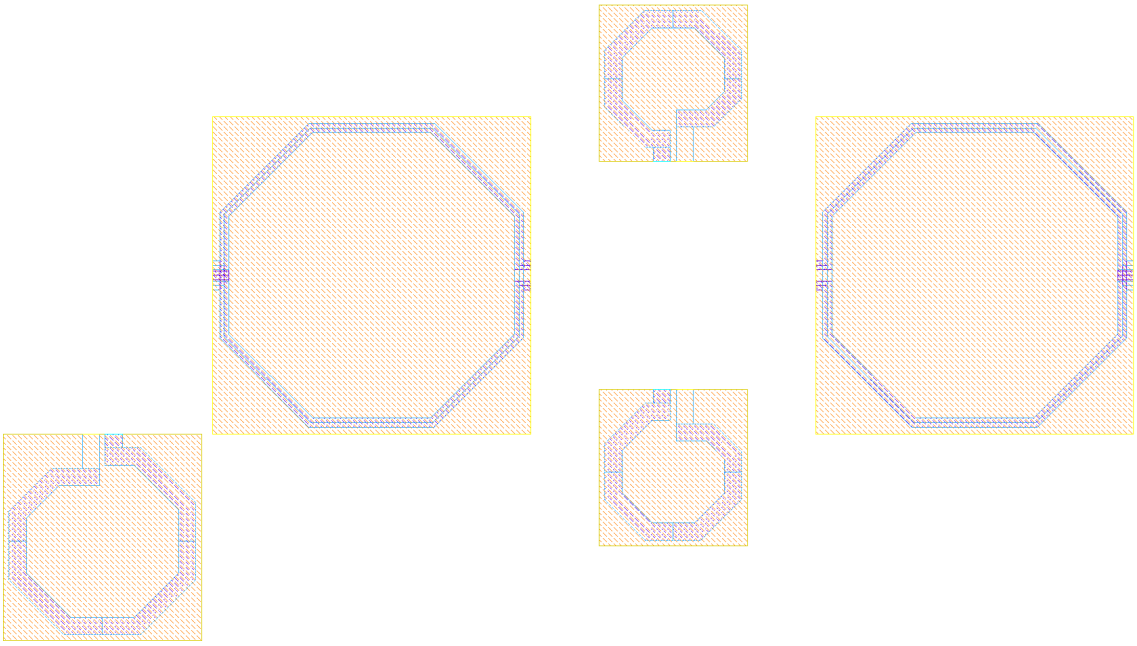


Figure 10.20: Inductor arrangement

The final inductor arrangement is shown in Fig. 10.20. This structure was treated as a 16-port and its S-parameters were extracted in order to confirm minimal interference between inductors. The S-parameters in Fig. 10.21 correspond to signal excitation at the port of a structure closest to its neighboring structure. Only adjacent structures are studied, since if minimal interference is confirmed between them, structures further apart are even less susceptible to it. If an S-parameter S_{ij} is less than $-40\,\mathrm{dB}$, then less than 0.01% of the power inserted at port j emerges at port i.

Also, only one second stage source degeneration inductor was studied, due to symmetry, and the inductor at the output was omitted because only interference was being studied and it is on the same signal path as the second stage balun transformer.

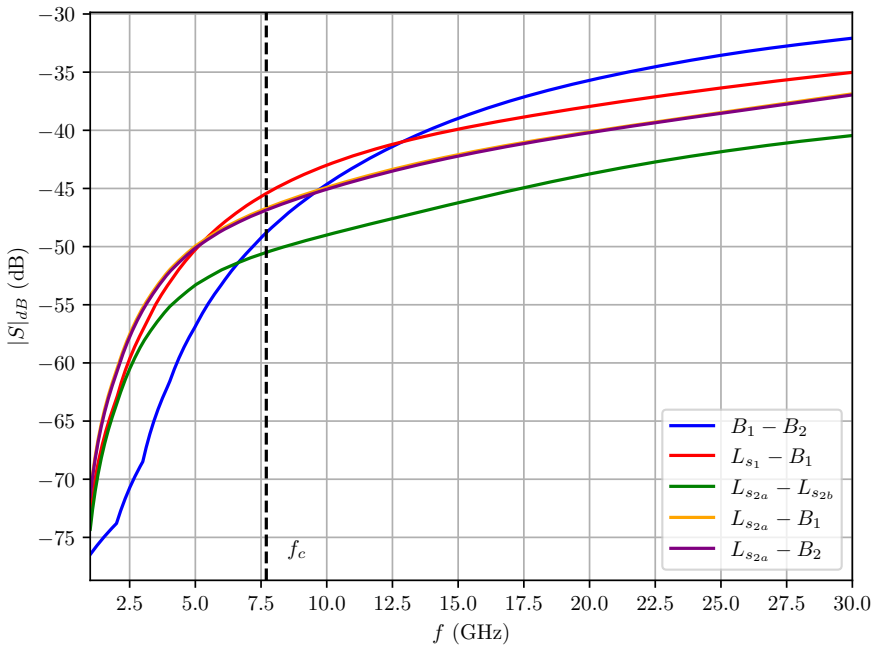


Figure 10.21: Interference between inductors

- $B_1 - B_2$: Interference between the two balun transformers.
- $L_{s_1} - B_1$: Interference between the degeneration inductor of the first stage and the first balun transformer.
- $L_{s_{2a}} - L_{s_{2b}}$: Interference between the two source degeneration inductors of the second stage.
- $L_{s_{2a}} - B_1$: Inteference between one of the source degeneration inductors of the first stage and the first balun transformer.
- $L_{s_{2a}} - B_2$: Interference between one of the source degeneration inductors of the second stage and the first balun transformer.

Simulation revealed more symmetries, which could have been predicted because the source degeneration inductor of the first stage is too far from the source degeneration inductors of the second stage. Therefore, the source degeneration inductors of the second stage interfere in the same way with the two balun transformers.

For a passive linear network containing n nodes and only complex admittances, the admittance matrix can be extracted from S-parameters by considering a port at each node and the network as an n-port. Then the admittance between two different nodes i and j can be found by taking the negative of the admittance matrix element at row i and column j, $-Y_{ij}$.

For results validation, a consistency check was performed by calculating the self inductance between two nodes from the admittance matrix. The expected self inductances were extracted, as shown in Fig. 10.22. Note that the values of these inductors are different than the ones on the schematic because different self inductances had to be used in order to maintain adequate performance after transistor and cascode layout.

$$L_{s_1} = \frac{1}{2\pi f}\mathrm{Im}\left[\frac{1}{-Y_{10,11}}\right] \tag{10.1}$$

$$L_{s_{2a}} = \frac{1}{2\pi f}\mathrm{Im}\left[\frac{1}{-Y_{12,13}}\right] \tag{10.2}$$

$$L_{s_{2b}} = \frac{1}{2\pi f}\mathrm{Im}\left[\frac{1}{-Y_{14,16}}\right] \tag{10.3}$$

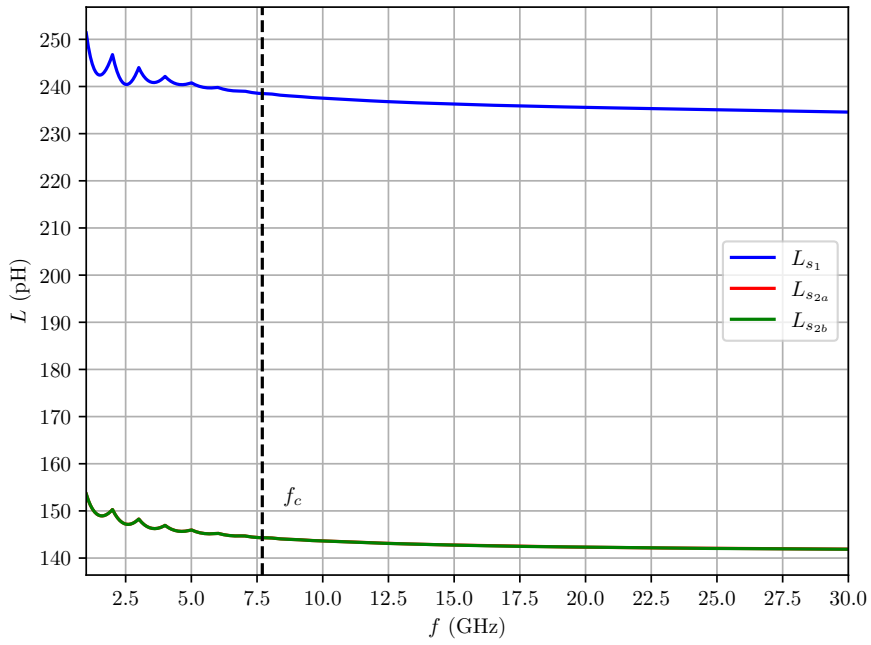


Figure 10.22: Self inductances of the source degeneration inductors extracted from electromagnetic simulation

10.5 Interconnects and final layout

After everything has been brought into contact with high metal layers, interconnects between components are what remains. The interconnects of the two stages were designed and modeled separately.

10.5.1 First stage interconnects

The full layout of the first stage with its interconnects is shown in Fig. 10.23. For a low noise amplifier, anything before the first active stage is critical. The interconnect at the gate was kept very short. The cascode was placed close to the source degeneration inductor in order to minimize the effect of the interconnect between them. Large interconnects were placed for the decoupling capacitors, which are not shown in Fig. 10.23. The interconnects the inductors were electromagnetically simulated together and a model was created.

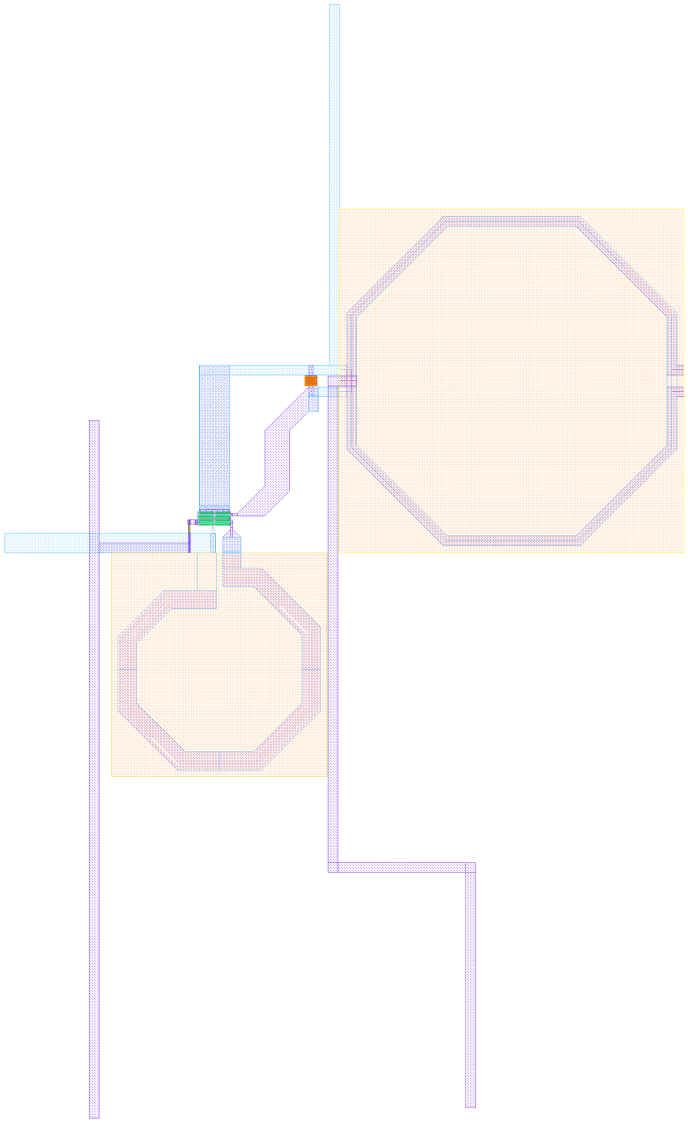


Figure 10.23: Layout of the first stage with its interconnects

10.5.2 Second stage interconnects

The full layout of the second stage with its interconnects is shown in Fig. 10.24. For the second stage, symmetry was crucial and it was preserved fully for the signal paths and to some extent for biasing. The cascodes somewhere between the center and the source degeneration inductors in an effort to minimize interconnect lengths. Large interconnects were placed for the decoupling capacitors, which are not shown in Fig. 10.24. The interconnects and the inductors were electromagnetically simulated together and a model was created.

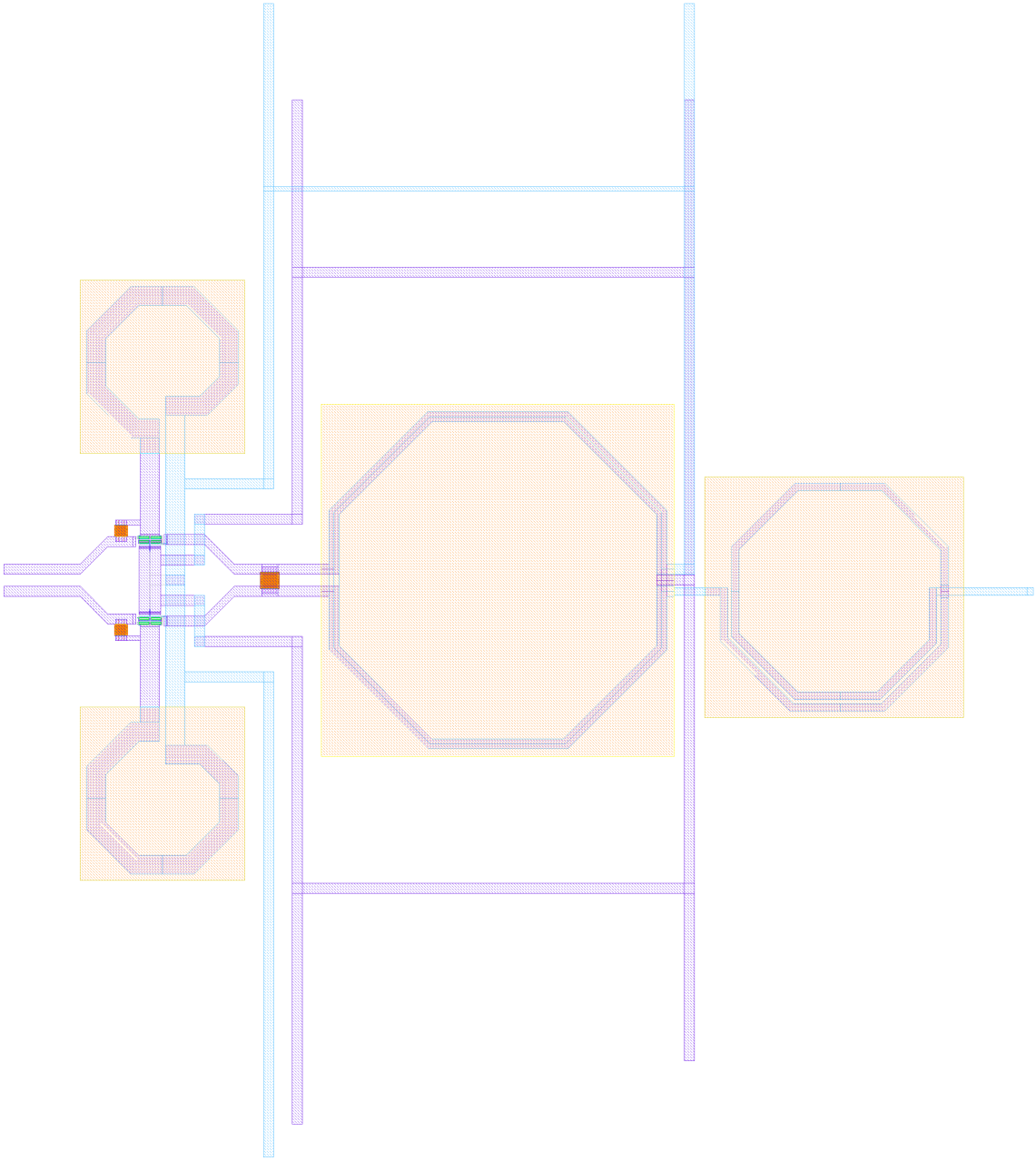


Figure 10.24: Layout of the second stage with its interconnects

10.5.3 LNA final layout

The final layout of the LNA is shown in Fig. 10.25. Coupling capacitors and pads have been included. Note that several small redesign choices had to be made again to maintain adequate performance. The total area of the layout is $1.403\,\text{mm} \times 1.141\,\text{mm} \approx 1.6\,\text{mm}^2$. It is not very compact, but this is the result of keeping inductors at large distances from one another and this was decided to be critical in order to avoid issues with magnetic feedback.

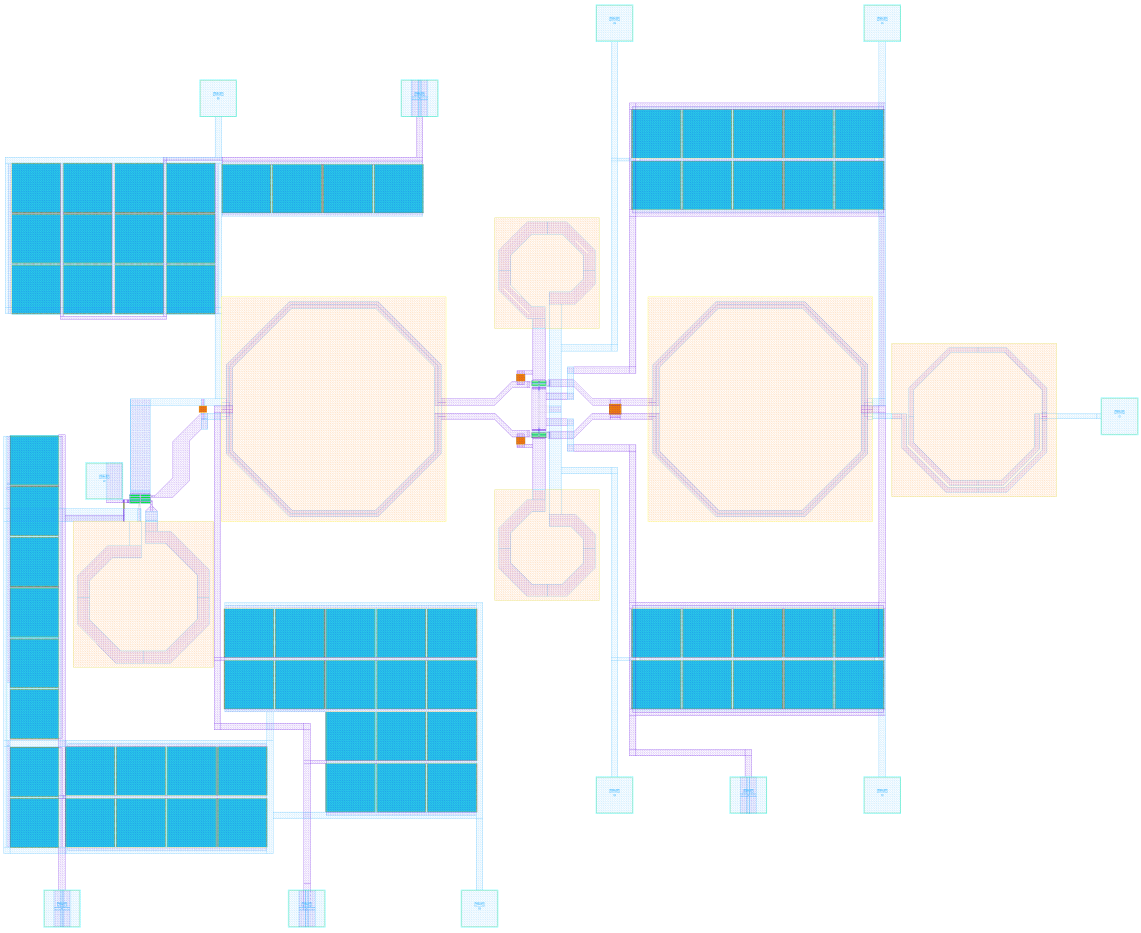


Figure 10.25: Final layout of the LNA

The complete layout did not undergo electromagnetic simulation, due to memory limitations. However, the two stages have been modeled by electromagnetic simulation separately and components were placed at large enough distances for interference to be minimal anyway. Therefore, the complete model for the LNA contains electromagnetic models for both stages and component models from the PDK.

10.6 Post-layout results

After modeling the LNA including its interconnects, some tuning had to take place. The final design is shown at a high level of hierarchy in Fig. 10.26, only to highlight the final value of the gate inductor. In the end, it was assumed that every bond wire has a self inductance of 500 pH. An off chip inductor with self inductance of 1.2 nH is required.

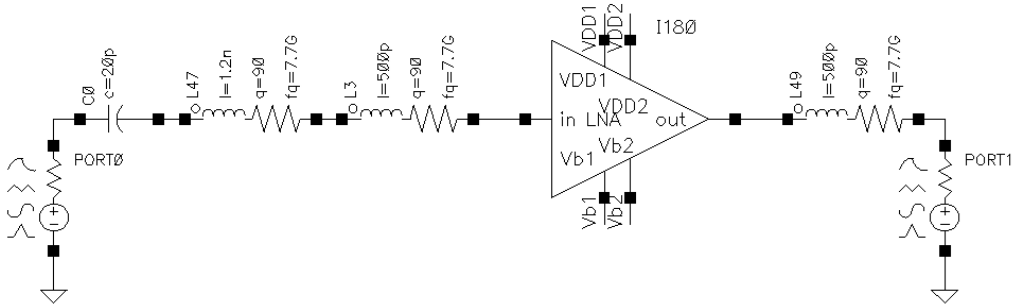


Figure 10.26: The LNA at a high level of hierarchy

10.6.1 Nominal case

The final results of post-layout simulations are shown in the following table and diagrams. Noise performance has been significantly degraded due to interconnects, as expected. They inevitably introduce losses that degrade noise figure. Noise matching and input matching also suffered and compromises were made. In general however, performance was salvaged during tuning. Unconditional stability was confirmed for frequencies from 100 kHz up to 30 GHz, due to the limited range of electromagnetic simulation models.

Metric	**Symbol**	**Value**
Noise figure	NF	1.192 dB
Minimum noise figure	NF_{min}	1.006 dB
Optimum noise impedance	Z_{opt}	$(99.42 - j\,0.61)\,\Omega$
Gain	$\lvert S_{21}\rvert_{\mathrm{dB}}$	22.37 dB
Input return loss	$-\lvert S_{11}\rvert_{\mathrm{dB}}$	16.4 dB
Output return loss	$-\lvert S_{22}\rvert_{\mathrm{dB}}$	22.28 dB
Reverse isolation	$-\lvert S_{12}\rvert_{\mathrm{dB}}$	55.58 dB
Input referred 1dB compression point	$\mathrm{IP1dB}_{\mathrm{dBm}}$	−24.73 dBm
Output referred 1dB compression point	$\mathrm{OP1dB}_{\mathrm{dBm}}$	−3.363 dBm
Input referred third order intercept point	$\mathrm{IIP3}_{\mathrm{dBm}}$	−6.372 dBm
Output referred third order intercept point	$\mathrm{OIP3}_{\mathrm{dBm}}$	16.02 dBm
Stability metrics	K / B_1	22.26 / 1.016
Alternative stability metrics	μ / μ'	10.33 / 5.811
Quiescent current	I_Q	22.72 mA
Power consumption	P_{DC}	18.18 mW

Table 10.2: LNA post-layout nominal results

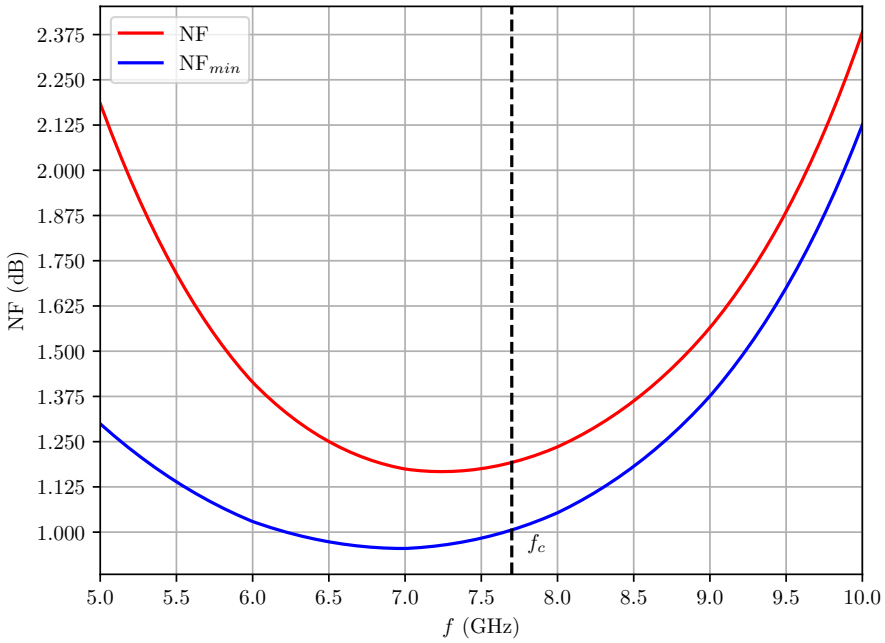


Figure 10.27: LNA post-layout noise figure

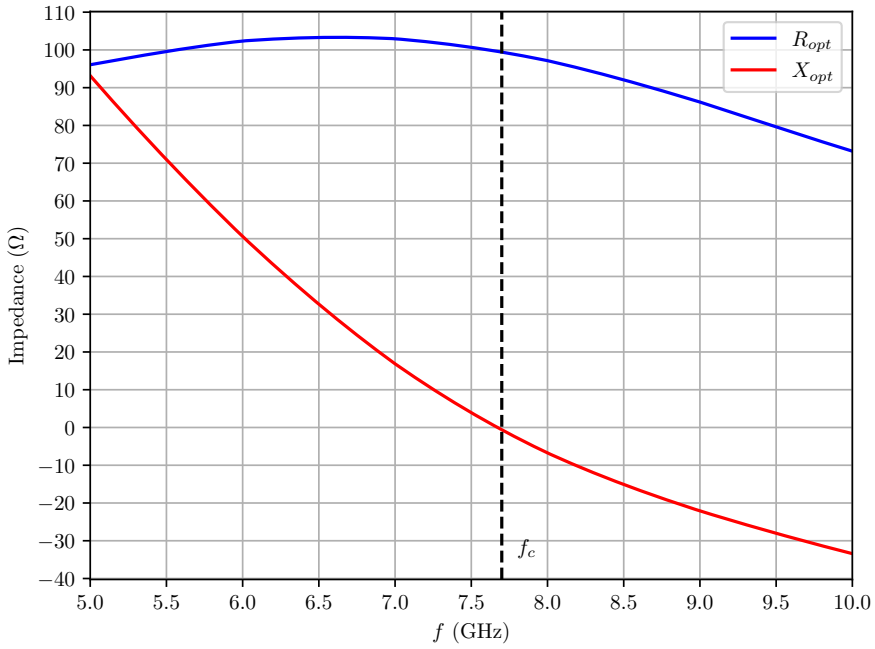


Figure 10.28: LNA post-layout optimum noise impedance

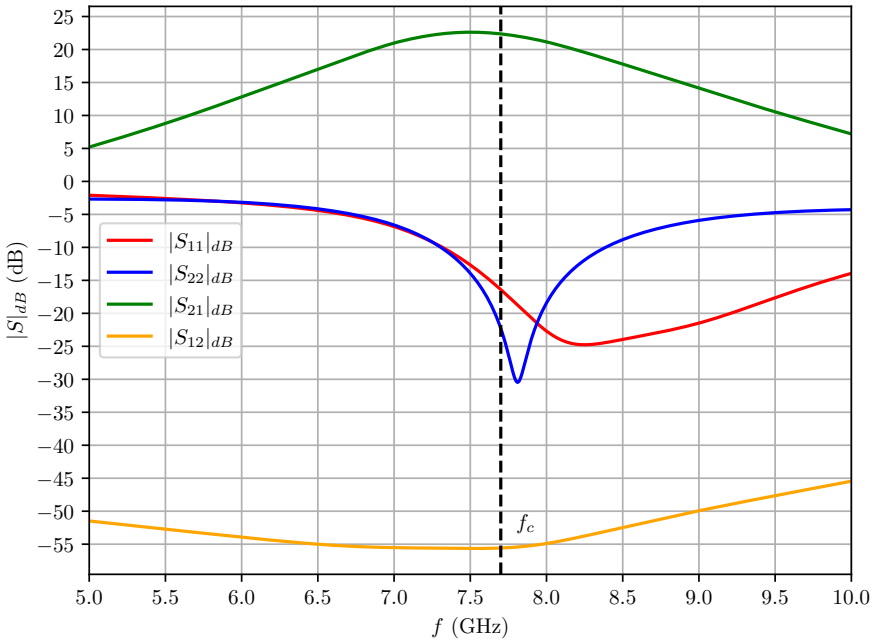


Figure 10.29: LNA post-layout S-parameters

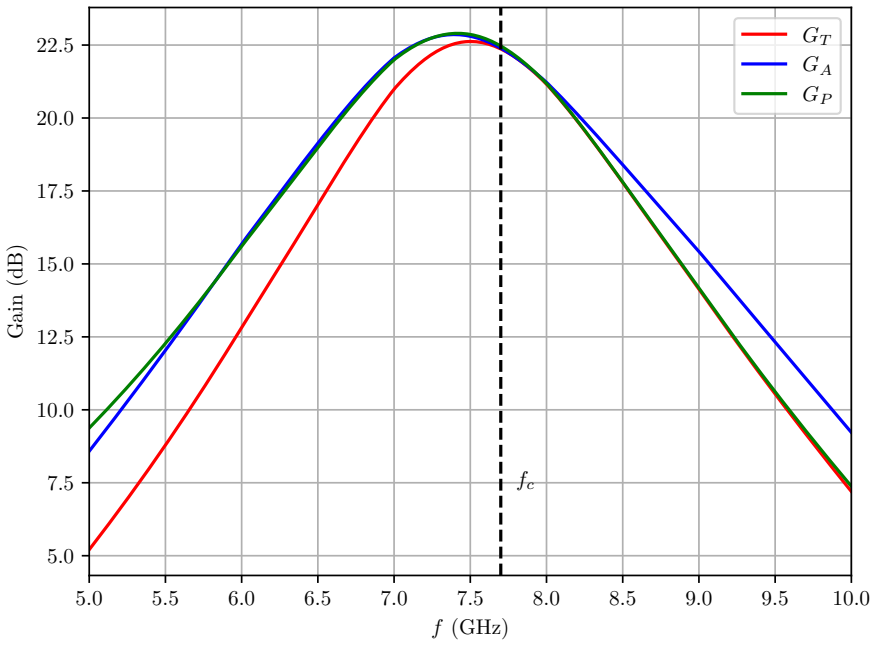


Figure 10.30: LNA post-layout gains

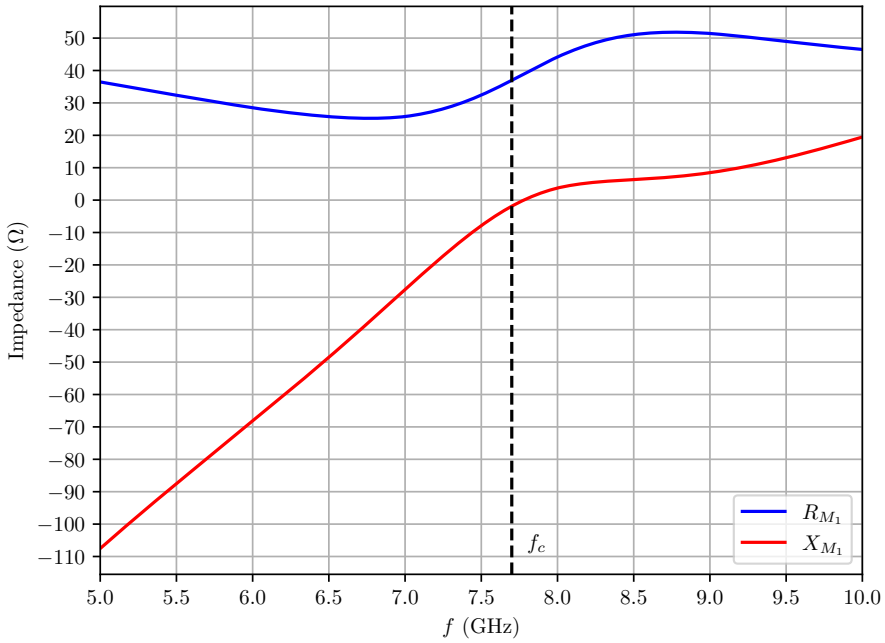


Figure 10.31: LNA post-layout input impedance

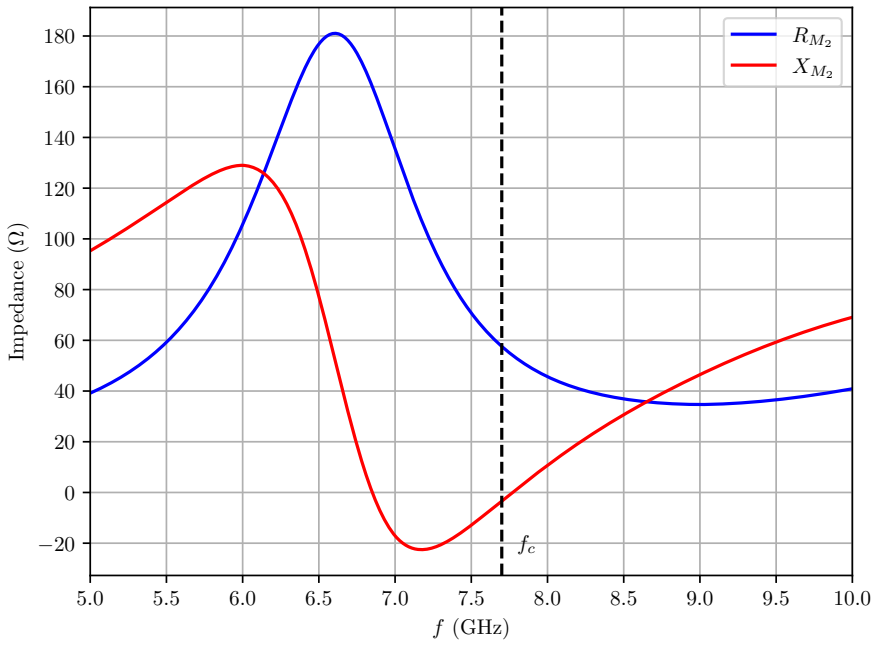


Figure 10.32: LNA post-layout output impedance

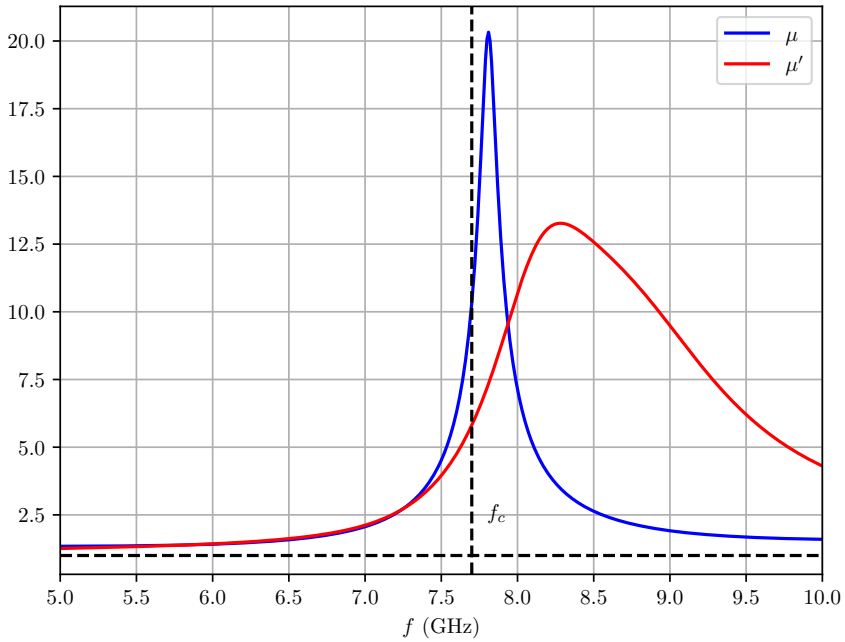


Figure 10.33: LNA post-layout stability factors μ and μ'

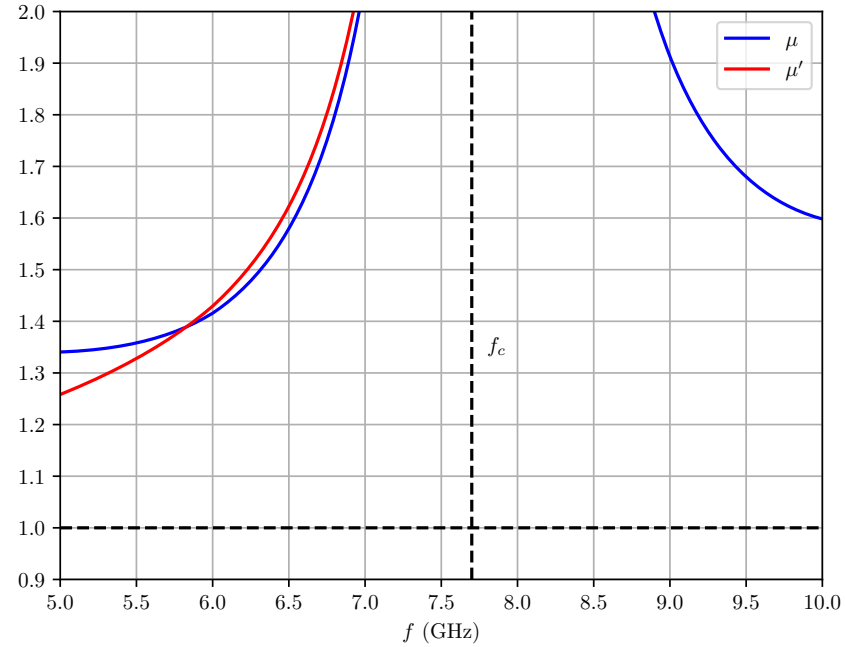


Figure 10.34: LNA post-layout stability factors μ and μ' (zoomed in)

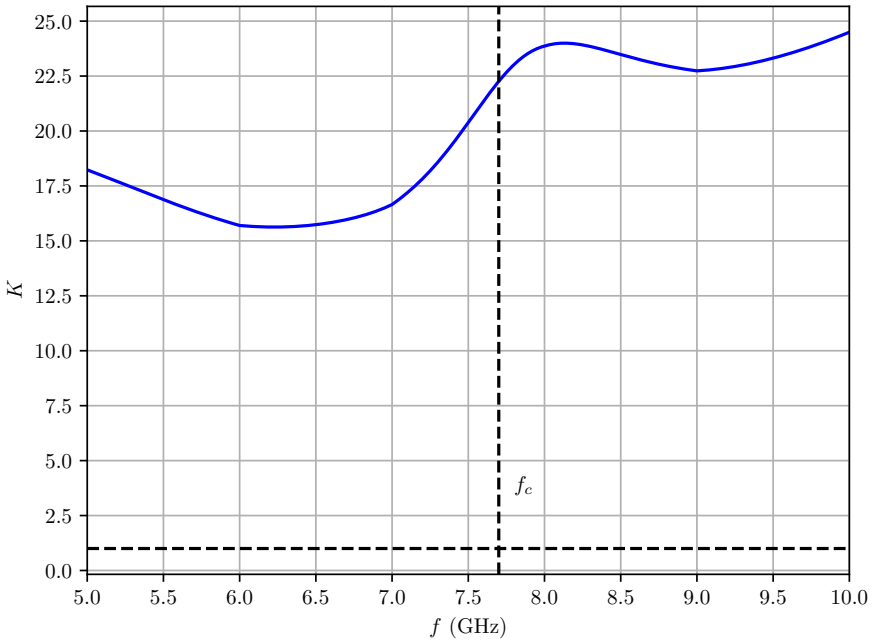


Figure 10.35: LNA post-layout stability factor K

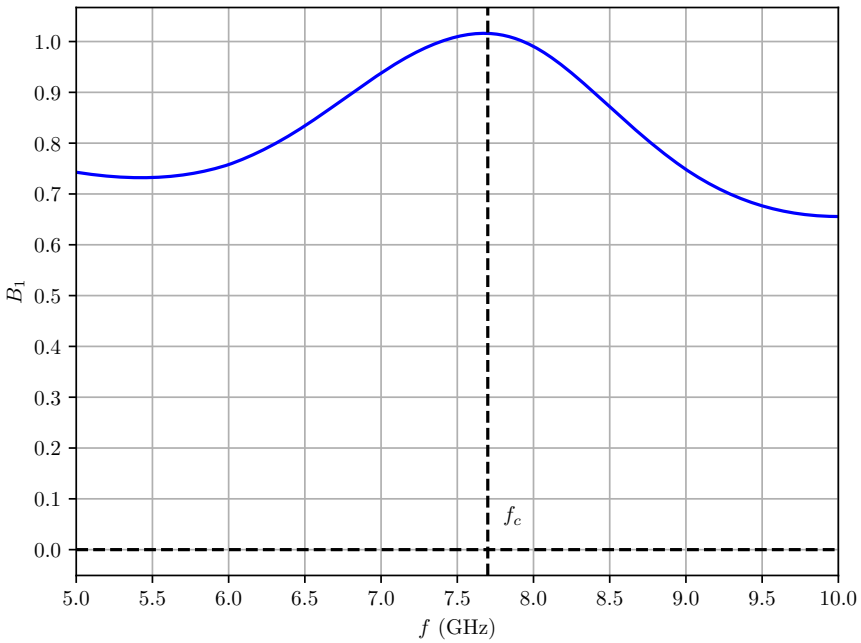


Figure 10.36: LNA post-layout stability factor B_1

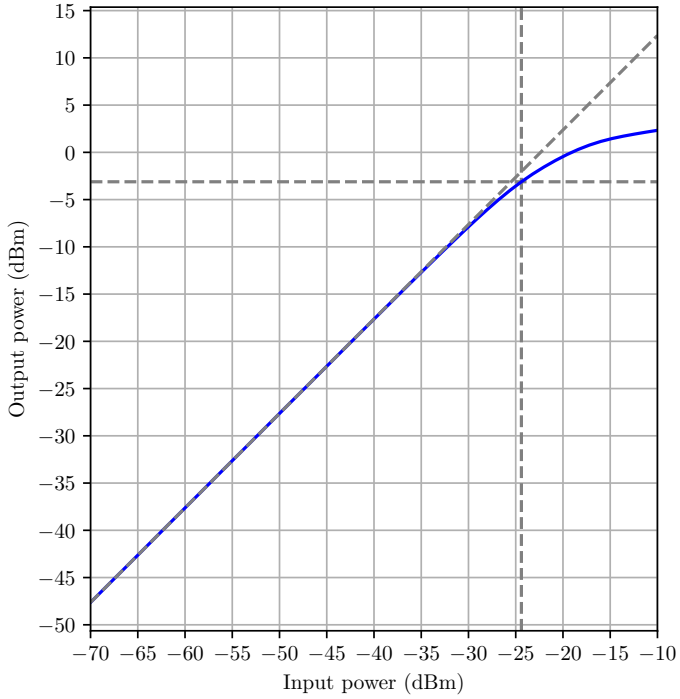


Figure 10.37: LNA post-layout output power compression

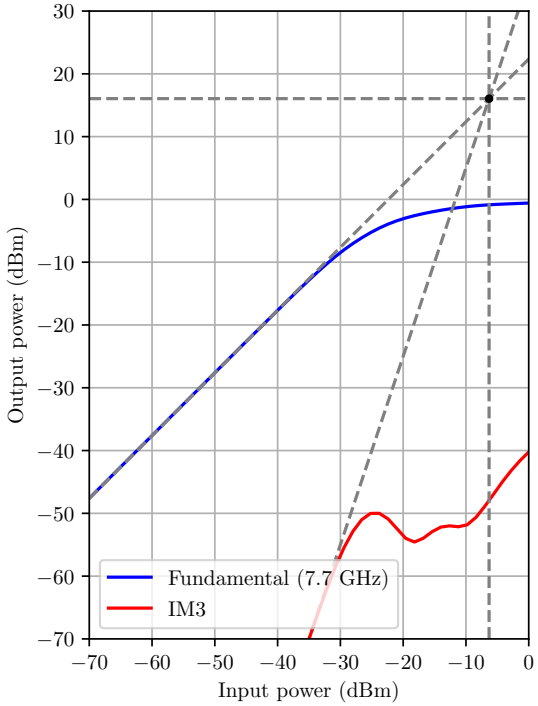


Figure 10.38: LNA post-layout third order intercept point

10.6.2 Corner cases

As with the schematic case, to ensure reliable circuit performance under process, voltage, and temperature (PVT) variations, post-layout simulations are carried out across defined corner cases. The corners at which the post-layout model was simulated entailed typical, fast, and slow transistors (TT, FF, FS, SF, SS), some temperatures, specifically $-40\,^{\circ}\mathrm{C}$, $60\,^{\circ}\mathrm{C}$, and $125\,^{\circ}\mathrm{C}$, and $\pm 10\%$ variations of the supply voltage. The minimum and maximum values across corners for the post-layout performance metrics are shown in the following table.

Metric	Minimum	Nominal	Maximum
NF	0.872 dB	1.192 dB	1.787 dB
NF_{min}	0.719 dB	1.006 dB	1.591 dB
$\lvert S_{21}\rvert_{\mathrm{dB}}$	16.21 dB	23.37 dB	23.38 dB
$-\lvert S_{11}\rvert_{\mathrm{dB}}$	12.87 dB	16.4 dB	24.84 dB
$-\lvert S_{22}\rvert_{\mathrm{dB}}$	10.13 dB	22.28 dB	22.96 dB
$-\lvert S_{12}\rvert_{\mathrm{dB}}$	53.76 dB	55.58 dB	58.07 dB
K / B_1	17.65 / 0.941	22.26 / 1.016	36.52 / 1.021
μ / μ'	2.997 / 4.016	10.33 / 5.811	11.38 / 13.67
I_Q	10.3 mA	22.72 mA	43.08 mA
P_{DC}	7.419 mW	18.18 mW	37.91 mW

Table 10.3: LNA post-layout corner cases simulation results

In general, higher temperatures degrade noise performance once again, as expected due to higher thermal noise power. Variations of the supply voltage did not significantly degrade performance this time as well. At the corners where the electrical parameters of the transistors change and the bias currents become very different problems occurred again. As mentioned before, since a silicon on insulator process is being used, adaptive body biasing techniques could be implemented to counteract that.

All things considered, the post-layout circuit operated as a low noise amplifier, albeit with low gain and relatively high noise figure in some cases. Unconditional stability at the operating frequency was maintained across corners.

10.6.3 Monte Carlo simulation

Monte Carlo simulations are performed post-layout as well in order to statistically evaluate the impact of manufacturing variations on performance.

A Monte Carlo simulation with 200 samples was performed post-layout. The results for noise figure are shown in Fig. 10.39, where low variance can be observed once again. Additionally, the samples performed well regarding gain, as shown in Fig. 10.40. Finally, Fig. 10.41 and Fig. 10.42 show that unconditional stability at the operating frequency is almost guaranteed this time as well, since the distributions of samples are far from values lower than 1.

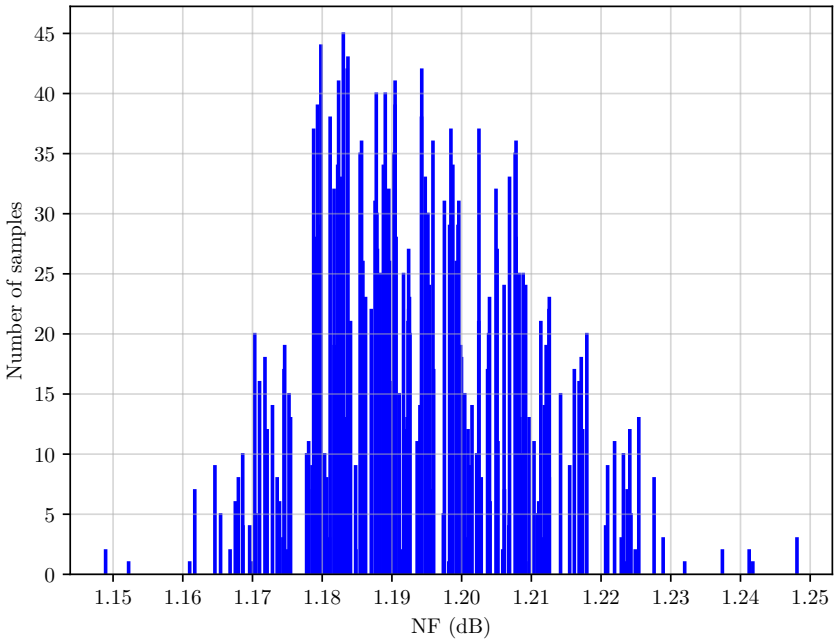


Figure 10.39: Monte Carlo results for post-layout noise figure

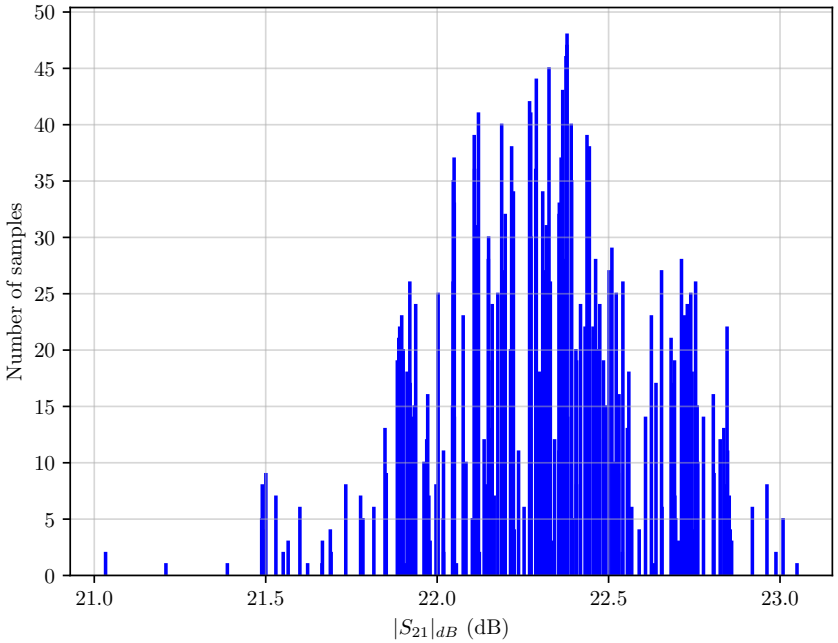


Figure 10.40: Monte Carlo results for post-layout gain

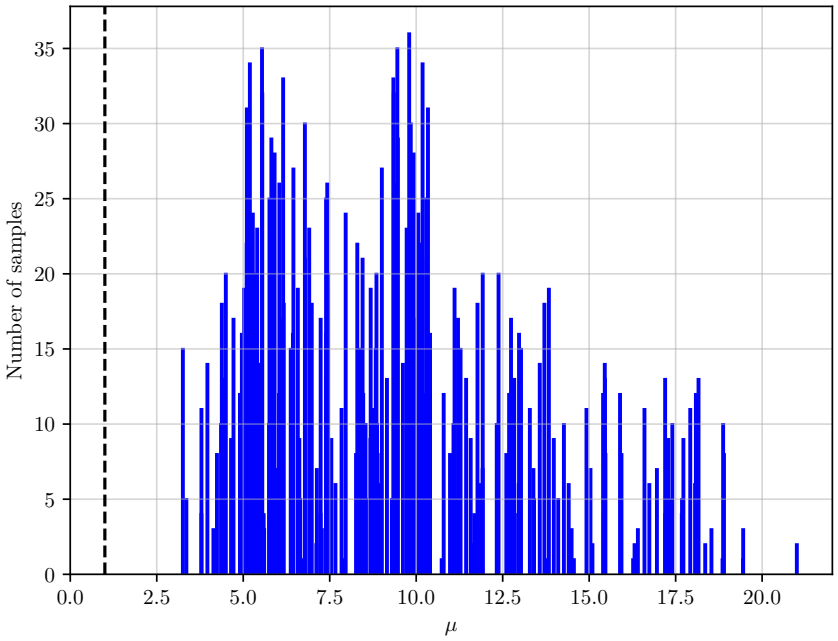


Figure 10.41: Monte Carlo results for post-layout stability factor μ

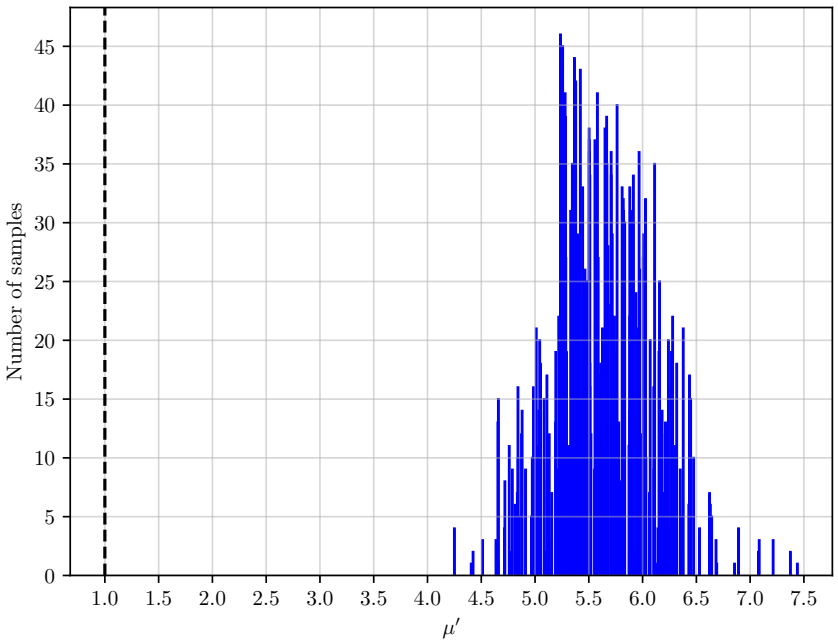


Figure 10.42: Monte Carlo results for post-layout stability factor μ'

Chapter 11

Conclusion and future work

Low noise amplifiers are critical components in RF receiver front-ends, as they directly impact the noise figure of the wireless receiver. Their design is especially vital in modern high frequency applications like in 5G and 6G, where low noise is essential in maintaining signal integrity and reception signals can be very weak.

In this thesis, the design, implementation, and simulation of a low noise amplifier operating in the $7 - 8.4\,\text{GHz}$ frequency band was presented, targeting 5G/6G communication applications using a $22\,nm$ CMOS FD-SOI technology. The design flow was described and very detailed explanations of many steps were given, highlighting critical trade offs. Carefully balancing gain, noise figure, linearity, and power consumption is crucial for a design aiming to meet the stringent requirements of modern high frequency systems. The use of electromagnetic simulations, and post-layout verification is necessary in ensuring accurate modeling of parasitic effects, resulting in a robust and reliable design.

Newer technology nodes might offer many advantages but design becomes more challenging and parasitics dominate as dimensions become smaller. The design of this thesis performed adequately, as shown in the following table. It is by no means a complete industry grade LNA but an educational design in a modern process, regarding RF and analog electronics, and in a frequency range that only recently became available for 6G applications.

Furthermore, the following table highlights the importance of accurate modeling of physical structures in circuit design. While advanced schematics incorporating electromagnetic simulation models and PDK elements provide valuable insights, they often fall short in predicting actual behavior because of how important layout dependent effects are. Even minor interconnect parasitics can significantly impact performance at high frequencies, especially in advanced process nodes. This highlights the necessity of thorough post-layout verification and optimization to ensure design robustness.

Metric	Redesign	Post-Layout
NF	0.867 dB	1.192 dB
NF_{min}	0.811 dB	1.006 dB
Z_{opt}	$(69.82 - j\,14.28)\,\Omega$	$(99.42 - j\,0.61)\,\Omega$
$\lvert S_{21}\rvert_{\mathrm{dB}}$	30.52 dB	22.37 dB
$-\lvert S_{11}\rvert_{\mathrm{dB}}$	23.27 dB	16.4 dB
$-\lvert S_{22}\rvert_{\mathrm{dB}}$	37.91 dB	22.28 dB
$-\lvert S_{12}\rvert_{\mathrm{dB}}$	58.12 dB	55.58 dB
$\mathrm{IP1dB}_{\mathrm{dBm}}$	−30.13 dBm	−24.73 dBm
$\mathrm{OP1dB}_{\mathrm{dBm}}$	−0.611 dBm	−3.363 dBm
$\mathrm{IIP3}_{\mathrm{dBm}}$	−9.407 dBm	−6.372 dBm
$\mathrm{OIP3}_{\mathrm{dBm}}$	21.15 dBm	16.02 dBm
K / B_1	11.96 / 1.003	22.26 / 1.016
μ / μ'	18.83 / 9.093	10.33 / 5.811
I_Q	29.54 mA	22.72 mA
P_{DC}	23.63 mW	18.18 mW

Table 11.1: Results comparison between redesign and post-layout simulations

There is a lot of potential left open for future work. Regarding the circuit, some different approaches can be followed. For example, for the same total gate width, some transistor multiplicities might perform better on the schematic but implementing them in layout is more complex therefore possibly negating their initial advantage. Perhaps inductors can be brought closer in order to mitigate interconnect losses, while still maintaining adequately low levels of interference. Additionally, adaptive biasing circuits can be designed to counteract the biasing issues encountered at corner cases. This can be done with digital-to-analog converters (DACs) and digitally controlled bias circuits that adjust the bias current.

Furthermore, the packaging of the LNA can be designed. This design was a standalone LNA and it was matched to 50 Ω at the input and the output. Bond wires and an off chip gate inductor were modeled by ideal circuit elements, but for this design to be fabricated they would have to be carefully designed with the requirements presented in this thesis. If a tape out was to happen for this design, antenna rules, metal fill rules, and electrostatic discharge protection would have to be addressed as well. An antenna can be designed too, perhaps on the packaging.

To conclude, this thesis aimed to explore the design of low noise amplifiers and to push the capabilities of a modern process to its limits. Hopefully, the insights and methodologies presented in this work will serve as a valuable reference for future students engaging in LNA design and RF circuit development.

Bibliography

[1] M. Gholami and M.-R. Nezhad-Ahmadi, "A wideband combined LNA-filter in 22 nm FDSOI technology for satellite phased arrays," *Microw. Opt. Technol. Lett.*, vol. 66, Sept. 2024.

[2] L.-W. Ouyang, J. C. Mayeda, C. Sweeney, G. Somasundaram, D. Y. C. Lie, and J. Lopez, "A broadband millimeter-wave 5G low noise amplifier design in 22 nm fully-depleted silicon-on-insulator (FD-SOI) CMOS," in *2023 Sixth International Symposium on Computer, Consumer and Control (IS3C)*, IEEE, June 2023.

[3] J. Fu, M. G. Bardeh, J. Paramesh, and K. Entesari, "A Millimeter-Wave concurrent LNA in 22-nm CMOS FDSOI for 5G applications," *IEEE Trans. Microw. Theory Tech.*, vol. 71, pp. 1031–1043, Mar. 2023.

[4] X. Xu, J. Wagner, C. Carta, and F. Ellinger, "A 60 GHz broadband LNA with joined variable gain control and switching in 22 nm FD-SOI," *IEEE Access*, vol. 12, pp. 111627–111637, 2024.

[5] M. Spasaro and D. Zito, "0.52-mw 30-GHz LNA in 22-nm FDSOI CMOS," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 70, pp. 3752–3756, Oct. 2023.

[6] B. Cui and J. R. Long, "A 1.7-dB minimum NF, 22–32-GHz low-noise feedback amplifier with multistage noise matching in 22-nm FD-SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 55, pp. 1239–1248, May 2020.

[7] S. Mousavi, J. Ghasemib, and M. Gholami, "A high gain and forward body biastwo-stage ultra-wideband low noise amplifier with inductive feedback in 180 nm CMOS process," *Int. J. Eng.*, vol. 31, Sept. 2018.

[8] F. Han, X. Liu, C. Wang, X. Li, Q. Qi, X. Li, and Z. Liu, "A multi-band LNA covering 17–38 GHz in 45 nm CMOS SOI," *Electronics (Basel)*, vol. 11, p. 3255, Oct. 2022.

[9] D. K. Shaeffer and T. H. Lee, "A 1.5-v, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 745–759, May 1997.

[10] J. Bergervoet, D. M. W. Leenaerts, G. W. de Jong, E. van der Heijden, J.-W. Lobeek, and A. Simin, "A 1.95 GHz sub-1 db NF, +40 dbm OIP3 WCDMA LNA module," *IEEE J. Solid-State Circuits*, vol. 47, pp. 1672–1680, July 2012.

[11] P.-H. Huang, C.-S. Chiu, G.-W. Huang, K.-M. Chen, and L.-K. Wu, "A low-power low-noise w-band LNA in 90-nm CMOS process with source degeneration technique," *IEEE Microw. Wirel. Technol. Lett.*, vol. 34, pp. 69–71, Jan. 2024.

[12] C. Enz, "Simple expression of the thermal noise excess factor for LNA design," in *2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, IEEE, Oct. 2022.

[13] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Tech.*, vol. 52, pp. 1433–1442, May 2004.

[14] 5G Americas, "Spectrum in North America: The Impact of WRC-23," Aug. 2024.

[15] R. E. Collin, *Foundations for Microwave Engineering*. IEEE Press Series on Electromagnetic Wave Theory, Nashville, TN: John Wiley & Sons, 2 ed., Dec. 2000.

[16] N. K. Oyzounoglou, *Introduction to microwaves*. Athens, Greece: Papasotiriou publications, 2 ed., 1994.

[17] G. Gonzalez, *Microwave transistor amplifiers*. Upper Saddle River, NJ: Pearson, 2 ed., Aug. 1996.

[18] I. A. Roumeliotis and I. L. Tsalamegkas, *Electrmagnetic fields*. Athens, Greece: Tziolas publications, 2 ed., 2024.

[19] D. M. Pozar, *Microwave Engineering*. Chichester, England: John Wiley & Sons, 4 ed., Nov. 2011.

[20] B. Razavi, *RF microelectronics*. Philadelphia, PA: Prentice Hall, 2 ed., Sept. 2011.

[21] S. Voinigescu, *High-frequency integrated circuits*. Cambridge: Cambridge University Press, 2013.

[22] T. H. Lee, *The design of CMOS radio-frequency integrated circuits*. Cambridge, England: Cambridge University Press, 2 ed., June 2012.

[23] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and design of analog integrated circuits*. Hoboken, NJ: Wiley-Blackwell, Jan. 2009.

[24] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Oxford, England: Oxford University Press, 1987.

[25] B. Razavi, *Fundamentals of microelectronics*. Nashville, TN: John Wiley & Sons, Feb. 2008.

[26] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*. CourseSmart, Chichester, England: John Wiley & Sons, Nov. 2011.

[27] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY: McGraw-Hill Professional, Aug. 2000.

[28] Z. Ding, *Modern Digital and Analog Communications Systems*. OXF SER ELEC, New York, NY: Oxford University Press, 4 ed., July 2009.

[29] S. Haykin and M. Moher, *Communication Systems*. Nashville, TN: John Wiley & Sons, Feb. 2009.

[30] P. G. Cottis, *Introduction to telecommunications*. Athens, Greece: Tziolas publications, 2013.