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Design and implementation of a low noise Phase Locked Loop (PLL) for 6-10,5 GHz applications using a 22 nm CMOS FD-SOI technology

DIPLOMA THESIS

of

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Σχεδίαση και υλοποίηση βρόχου κλειδώματος φάσης χαμηλού θορύβου για RF εφαρμογές συχνοτήτων 6-10,5 GHz σε τεχνολογία 22 nm CMOS FD-SOI

ΔΙΠΛΩΜΑΤΙΚΗ ΕΡΓΑΣΙΑ

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Εγκρίθηκε από την τριμελή εξεταστική επιτροπή την 28η Αυγούστου 2025

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Περίληψη

Η παρούσα διπλωματική εργασία παρουσιάζει τη μελέτη και σχεδίαση βρόχου κλειδώματος φάσης χαμηλού θορύβου, ο οποίος λειτουργεί στο εύρος συχνοτήτων 6-10,5 GHz. Ο βρόχος σχεδιάστηκε χρησιμοποιώντας το PDK της τεχνολογίας 22 nm CMOS FD-SOI της GlobalFoundries, η οποία υπόσχεται υψηλή απόδοση με μειωμένη κατανάλωση ισχύος. Η διαδικασία σχεδίασης περιλαμβάνει τη σχεδίαση σε επίπεδο σχηματικού, τη φυσική σχεδίαση (layout) και την επαλήθευση της ορθής λειτουργίας μετά τη φυσική σχεδίαση (post-layout simulations). Οι τελευταίες δύο διαδικασίες εφαρμόστηκαν σε επιλεγμένα κυκλώματα και όχι στον πλήρη βρόχο κλειδώματος φάσης. Η ροή της σχεδίασης τεκμηριώνεται και συνοδεύεται από θεωρητικό υπόβαθρο, αποτελέσματα προσομοιώσεων, καθώς και την ανάλυση των συμβιβασμών (trade-offs) που προέκυψαν στα ενδιάμεσα στάδια, οδηγώντας στο τελικό αποτέλεσμα. Τέλος, η παρούσα εργασία μπορεί να αποτελέσει χρήσιμο βοήθημα όσων επιθυμούν να ασχοληθούν με τη σχεδίαση βρόχων κλειδώματος φάσης.

Λέξεις κλειδιά: Βρόχος Κλειδώματος Φάσης (PLL), Σχεδίαση Ολοκληρωμένων Κυκλωμάτων Ραδιοσυχνοτήτων, CMOS FD-SOI, Ενισχυτές Υψηλών Συχνοτήτων

Abstract

This thesis presents the study and design of a low-noise phase-locked loop (PLL) operating in the frequency range of 6-10.5 GHz.The loop was designed using the PDK of GlobalFoundries 22 nm CMOS FD-SOI technology, which offers high performance with reduced power consumption. The design procedure includes schematic-level design, phyical layout, and post-layout simulations. The latter two processes were applied only to selected subcircuits and not to the complete phase-locked loop. The design flow is documented and supported by the necessary theoretical background, simulation results, and an analysis of the trade-offs encountered in the intermediate stages leading to the final outcome. Finally, this thesis may serve as a useful resource for those interested in the design of phase-locked loops.

Keywords: Phase-Locked Loop (PLL), RF Integrated Circuit Design, CMOS FD-SOI, High-Frequency Amplifiers

Ευχαριστίες

Αρχικά θα ήθελα να ευχαριστήσω τον επιβλέποντα καθηγητή μου Γεώργιο Παναγόπουλο, για την ευκαιρία που μου έδωσε να ασχοληθώ με το παρόν έργο, την καθοδήγηση και την εξαιρετική συνεργασία μας.

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Papagianni Athina
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Κεφάλαιο 1

Εκτεταμένη περίληψη στα Ελληνικά

Η παρούσα διπλωματική εργασία ασχολείται με τον σχεδιασμό, την υλοποίηση και την προσομοίωση ενός βρόχου κλειδώματος φάσης (Phase-Locked Loop-PLL) στο εύρος συχνοτήτων 6-8.5 GHz. Τα PLL αποτελούν θεμελιώδη δομικά στοιχεία στα σύγχρονα ηλεκτρονικά κυκλώματα και στην επεξεργασία σήματος, χάρη στην ικανότητά τους να διατηρούν σταθερή και ακριβή σχέση φάσης μεταξύ δύο περιοδικών σημάτων. Συγκεκριμένα, επιτρέπουν τον συγχρονισμό σήματος, τη σύνθεση συχνοτήτων και την ανάκτηση φάσης σε εφαρμογές τηλεπικοινωνιών, ελέγχου, και επεξεργασίας σήματος. Το εύρος συχνοτήτων που επιλέχθηκε για την παρούσα εργασία προσφέρει δυνατότητες για πολλές εφαρμογές, όπως ραδιοαστρονομία, μικροκυματικές επικοινωνίες, ασύρματα δίκτυα LAN, εξειδικευμένες επικοινωνίες μικρής εμβέλειας (DSRC), σύγχρονα συστήματα ραντάρ, δορυφορικές επικοινωνίες, καλωδιακή και δορυφορική τηλεοπτική μετάδοση, άμεσες δορυφορικές υπηρεσίες (DBS), ερασιτεχνική ραδιοεπικοινωνία και δορυφορική ραδιοφωνία.

Αρχικά, παρουσιάζονται και αναλύονται οι τρεις κύριες κατηγορίες των PLL (Analog PLL, Digital PLL, All-Digital PLL), ενώ στη συνέχεια επεξηγούνται οι διαφορετικές αρχιτεκτονικές των αναλογικών PLL. Τα αναλογικά PLL αποτελούνται από τον ανιχνευτή φάσης, την αντλία φορτίου, το φίλτρο βρόχου, τον ταλαντωτή ελεγχόμενο από τάση και τον διαιρέτη συχνότητας. Καθένα από τα αναφερθέντα υποκυκλώματα μελετάται θεωρητικά και ύστερα σχεδιάζεται σύμφωνα με τους πρακτικούς περιορισμούς που εμφανίζονται στα ολοκληρωμένα κυκλώματα υψηλών συχνοτήτων.

Για τον ανιχνευτή φάσης επιλέχθηκε η κλασική αρχιτεκτονική, η οποία αποτελείται από δύο θετικά ακμοπυροδότητα D flip-flops και από αντιστροφείς διαφορετικής πολλαπλότητας.

Η αντλία φορτίου σχεδιάστηκε προκειμένου να εμφανίζονται μικρότερο mismatch μεταξύ των ρευμάτων I_{up},I_{dn} και μειωμένη ισχύς των spurs σε σχέση με την κλασική τοπολογία. Γι' αυτό επιλέχθηκε resistive based αρχιτεκτονική με ενσωματωμένο offset current για βελτίωση της γραμμικότητας. Το mismatch μετά τον φυσικό σχεδιασμό της αντλίας φορτίου είναι 1.83 μA.

Στον σχεδιασμό του φίλτρου βρόχου δόθηκε ιδιαίτερη έμφαση καθώς η σωστή επιλογή παραμέτρων καθορίζει τη σταθερότητα του συστήματος, τον χρόνο κλειδώματος και την απόρριψη θορύβου.

Ο ταλαντωτής ελεγχόμενος από τάση (VCO) σχεδιάστηκε βασιζόμενος σε έναν LC ταλαντωτή. Προκειμένου να καλυφθεί το εύρος συχνοτήτων 6-8.5GHz, υλοποιήθηκαν 2 VCO καθένας από τους οποίους περιέχει fine grain capacitors bank και coarse grain capacitors bank. Η πρώτη επιτυγχάνει μικρά βήματα, συγκεκριμένα καλύπτει 32 μπάντες, ενώ η δεύτερη

χρησιμοποιείται για μεγαλύτερα βήματα. Κρίσιμο σημείο για την σχεδίαση των VCO ήταν ο θόρυβος φάσης στο 1MHz offset καθώς και η διατήρηση ταλάντωσης κάτω από οποιεσδήποτε συνθήκες.

Τέλος, ο διαιρέτης συχνότητας υλοποιήθηκε από μία αλυσίδα οκτώ D flip-flops.

Τα τελικά αποτελέσματα παρουσιάζονται έπειτα από κατάλληλες προσομοιώσεις. Συγκεκριμένα η τάση ελέγχου V_{ctrl} εμφανίζει σταθερή συμπεριφορά έπειτα από περίπου 26 μs και κυμάτωση της τάξης των 3 mV. Η ανάλυση των σημάτων αναφοράς (V_{ref}) και ανάδρασης (V_{fdbck}) κατέδειξε την ύπαρξη μόνιμου σφάλματος φάσης 39.11°, τιμή αρκετά κοντά στην θεωρητικά αναμενόμενη (36°). Η απόκλιση αυτή αποδίδεται σε καθυστερήσεις διάδοσης των flip-flops και των λογικών πυλών πριν την αντλία φορτίου, ενώ μπορεί να διορθωθεί με την ενσωμάτωση ενός πρόσθετου κυκλώματος μετατόπισης φάσης.

Συνοψίζοντας, τα αποτελέσματα δείχνουν ότι η προτεινόμενη σχεδίαση ανταποκρίνεται στους βασικούς στόχους, παρόλο τους πρακτικούς περιορισμούς, εξασφαλίζοντας σταθερή λειτουργία, γρήγορη επίτευξη κλειδώματος, περιορισμένο σφάλμα φάσης και καθαρή φασματική συμπεριφορά.

Chapter 2

Introduction

2.1 Telecommunication Overview

Telecommunications has come a long way in just a few decades, evolving from early analog communication methods to today's advanced digital networks. Analog systems, which utilized continuous waveforms to transmit information, initially dominated communication technologies. While effective for voice and basic data transmission, these systems were limited by noise susceptibility, bandwidth constraints, and signal degradation over long distances.

The shift to digital communication revolutionized the industry by introducing discrete signal processing techniques, enabling more efficient use of the spectrum and higher data rates. This transition supported the deployment of complex modulation schemes and multiplexing methods, expanding the capacity and reliability of telecommunication networks worldwide.

As demand for faster and more reliable wireless communication has intensified, the use of microwave frequency bands has become increasingly prominent. These frequencies offer a favorable balance between bandwidth availability and propagation characteristics, making them ideal for applications such as satellite communication, radar systems, and emerging wireless standards.

However, operating at these frequencies also introduces new challenges, including higher propagation losses, increased sensitivity to noise and interference, and greater complexity in hardware design and signal processing. Ensuring frequency stability and signal integrity in such environments is fundamental to the success of modern telecommunication systems.

2.2 The necessity of Phase-Locked Loop (PLL)

Phase-locked loops (PLLs) are fundamental building blocks in modern electronics and signal processing due to their ability to maintain a stable and precise phase relationship between two periodic signals. At their core, PLLs are closed-loop negative-feedback control systems designed to synchronize the phase of a controlled oscillator with a reference signal. This allows PLLs to accurately track and measure signal frequencies, extract desired frequency components while rejecting noise, and synthesize new signals based on a reference input.

The versatility of PLLs makes them essential across many scientific and engineering fields. In physics and nanotechnology, they enable precise control in scanning probe mi-

croscopy and stabilize resonators in MEMS and NEMS devices. Beyond these specialized uses, PLLs are vital in electronics, optics, and photonics, where phase coherence and frequency stability are critical.

In communications and signal processing, PLLs range from basic clock signal cleanup to advanced local oscillators in radio systems, offering frequency agility and spectral purity. They also power ultrafast frequency synthesizers in instruments like vector network analyzers, enabling rapid, precise tuning.

Moreover, PLLs are fundamental to modern VLSI designs, ensuring synchronization and timing accuracy in high-speed circuits—a role that grows increasingly important as digital systems become more complex and faster.

In summary, the necessity of PLLs stems from their unique ability to lock and track frequencies with high precision, enabling a wide array of applications across multiple disciplines. Their adaptability and robustness make them essential for advancing technology in communications, instrumentation, nanotechnology, and high-speed electronics.

2.3 Analysis of the 6–10.5 GHz Band

The 6–10.5 GHz frequency range lies within the Super High Frequency (SHF) band, which spans 3 to 30 GHz and corresponds to wavelengths from approximately 100 mm to 10 mm. The SHF band supports a broad variety of applications including radio astronomy, microwave communications, wireless LANs, dedicated short-range communications (DSRC), modern radar systems, satellite communications, cable and satellite television broadcasting, direct broadcast satellite (DBS) services, amateur radio, and satellite radio.

The 6–10.5 GHz frequency range offers significant advantages in bandwidth and resolution but also presents several notable propagation challenges. One primary issue is the increased free-space path loss, which scales approximately with the square of frequency. As a result, signals within this band experience higher attenuation than those at lower frequencies, limiting communication range or necessitating higher transmit power and more sensitive receivers to maintain link quality.

Additionally, the shorter wavelengths at these frequencies reduce the ability of signals to penetrate obstacles such as walls, foliage, and terrain features. This limitation means that reliable communication often requires a clear line-of-sight path, posing challenges in urban and dense environments where obstructions are common.

Parasitic effects within circuit components and environmental factors such as temperature and humidity variations can impact signal integrity, requiring careful hardware design and compensation techniques.

Understanding these propagation challenges is essential for optimizing systems operating in the 6–10.5 GHz band, ensuring that communication and radar applications can perform reliably across a variety of environments.

Chapter 3

Different types of PLL

As already been mentioned a Phase-Locked Loop (PLL) is a feedback control system that generates ana output signal in phase with a reference signal. There are three main categories:

Analog PLL (APPL): An Analog PLL consists of a phase detector, which compares the phase of the input and output signals, a loop filter, which smooths the detector's output to produce a control voltage, and a voltage-controlled oscillator (VCO), which generates an output frequency that changes according to that control voltage. Analog PLLs excel in high-frequency applications because they offer low phase noise and mature, well-understood design principles. However, they are more complex to design, consume more power, and are sensitive to both noise and process variations.

Digital PLL (DPLL): A Digital PLL replaces most analog components with their digital equivalents. Instead of an analog phase detector, it uses a digital one to compare signals; the loop filter is implemented in digital logic or as a digital signal processor (DSP) algorithm; and the oscillator becomes a digitally controlled oscillator (DCO). These changes make digital PLLs more robust against noise and manufacturing variations, and easier to integrate into mixed-signal systems. The trade-off is that at very high frequencies, digital designs can become more complex and may not match the phase noise performance of analog PLLs.

All-Digital PLL (ADPLL): An All-Digital PLL goes one step further by eliminating all analog components. A time-to-digital converter (TDC) replaces the phase detector, the loop filter operates entirely in the digital domain, and the DCO generates the output frequency purely through digital tuning. This approach offers low power consumption, making it ideal for portable devices, and is highly scalable and compatible with modern CMOS processes. It is also fully programmable, allowing designers to reconfigure loop parameters through software. Nonetheless, ADPLLs can face performance limitations at extremely high frequencies and often require precise calibration to achieve optimal results.

Since the focus of this thesis is the design of an analog PLL, the next sections present and discuss different analog PLL architectures, their operating principles, and their relative advantages and disadvantages.

3.1 Charge-Pump PLL (CPPLL)

A Charge-Pump Phase-Locked Loop (CPPLL) is one of the most widely used PLL architectures, combining a phase-frequency detector (PFD), a charge pump (CP), and an analog loop filter in its feedback path to control a voltage-controlled oscillator (VCO).

This configuration enables precise frequency control, high loop stability, and fast lock acquisition, making CPPLLs highly adaptable for both integer and fractional division schemes.

The reference input signal of a CPPLL is typically generated by a highly stable oscillator, most often a crystal oscillator, which provides the frequency f_{osc}. The PFD compares the phase and frequency of this reference signal with the feedback signal obtained from the VCO output after frequency division by an integer N (via the N-divider). This N-divider can also be replaced by a fractional divider to allow finer frequency resolution. By detecting both phase and frequency differences, the PFD produces two digital output pulses whose width and polarity represent the direction and magnitude of the error. These pulses drive the charge pump, which sources or sinks a current proportional to the phase/frequency difference:

1. If the VCO lags the reference, the CP sources current to increase the control voltage.
2. If the VCO leads the reference, the CP sinks current to decrease the control voltage.
3. If the two signals are aligned, no net current is produced.

The loop filter converts the Charge Pump's current pulses into a smooth control voltage. The characteristics of this filter determine key loop parameters such as bandwidth, damping factor, and stability. This voltage is applied to the VCO, a voltage-controlled oscillator whose output frequency varies in proportion to the control voltage. The VCO output f_{out} is then divided down by the N-divider to produce a feedback frequency f_N close to f_{osc}. Through continuous feedback and adjustment, the two frequencies converge, and once f_N=f_{osc}, the loop is said to be locked.

In summary, CPPLLs combine fast locking, low phase noise, and wide frequency programmability, offering advantages over simpler PLL architectures, which makes them widely used in RF synthesizers, communication systems, and test equipment requiring precise frequency control and high performance.

3.2 Sub-Sampling PLL (SSPLL)

A Sub-Sampling PLL (SSPLL) is an analog PLL variant that uses a subsampling phase detector (PD) to directly sample the high-frequency output of the voltage-controlled oscillator (VCO) with the lower frequency reference clock. Unlike traditional PLLs that rely on frequency dividers in the feedback path, the subsampling phase detector samples the VCO output signal at discrete intervals dictated by the reference clock, effectively translating the timing or phase error into a voltage error signal without requiring a frequency divider, as long as the ratio f_{VCO}/f_{ref} is an integer.

At each rising edge of the reference clock, the instantaneous amplitude of the VCO output is captured, producing a sampled signal that represents the phase difference between the VCO and the reference. If the VCO signal is perfectly in phase with the reference clock, these samples remain steady; any phase difference causes the samples to fluctuate, generating a voltage proportional to this phase error.

This sampled error signal is converted into a current by a transconductor and then passed through a loop filter, which smooths the signal by removing noise and high-frequency components, resulting in a control voltage. This control voltage adjusts the frequency of the VCO, causing it to speed up or slow down as needed to reduce the phase difference. Over time, the loop continuously adjusts the VCO frequency until the output signal is phase-locked with the reference clock, achieving synchronization.

However, the periodic sampling operation imposes some challenges. The VCO load

experiences periodic perturbations, modulating its output frequency and generating reference spurs in the PLL output spectrum, known as BFSK (binary frequency shift keying) spurs, which are not filtered out by the loop. Additionally, the subsampling phase detector's narrow detection range increases the risk of false locking, necessitating a separate frequency-locked loop (FLL) to ensure robust initial frequency acquisition.

In conclusion, the Sub-Sampling PLL presents an effective solution for high-frequency synthesis, providing enhanced phase noise performance and a streamlined feedback loop, while requiring careful mitigation of reference spurs and the implementation of reliable frequency acquisition techniques.

3.3 Injection-Locked PLL (ILPLL)

An Injection-Locked Phase-Locked Loop (ILPLL) improves oscillator stability and phase noise by periodically injecting a clean reference signal directly into the voltage-controlled oscillator (VCO). This injection path supplements the traditional feedback loop, forcing the VCO to synchronize its phase and frequency to the reference and effectively "reset" accumulated jitter.

Structurally, an ILPLL consists of the usual PLL components such as the phase detector, loop filter, and VCO, but includes an additional injection path from the reference signal source to the VCO. This injection path features a digital-to-time converter (DTC), typically implemented with voltage-controlled delay lines (VCDLs), which precisely controls the timing of the injection pulses to align them with the VCO oscillation phase. A pulse generator (PG) produces pulses with adjustable width that modulate the amount of injected energy, while control circuits manage synchronization and timing adjustments to prevent mismatches between the PLL clock and the injected signal. This specialized circuitry enables fine-tuning of the injection process to maximize locking efficiency and minimize disturbance.

During operation, the ILPLL injects well-timed pulses from the reference clock into the VCO, correcting phase and frequency errors by "pulling" the VCO phase towards the reference periodically. This process reduces accumulated jitter and lowers both in-band and some out-of-band noise, resulting in improved signal stability and phase noise performance compared to conventional PLLs. The output frequency generally follows $f_{out}=f_{ref}+\Delta f$, where f_{ref} is the reference injection frequency and Δf is a small offset or modulation.

Chapter 4

Design and implementation of a 6-10.5 GHz PLL

The proposed phase-locked loop (PLL) operates in the 6-10.5 GHz frequency range. The architecture follows a conventional integer-N topology, consisting of a phase–frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a frequency divider (N-divider). A resistive-based current replication scheme is implemented in the charge pump to improve current matching and reduce static phase error. The VCO employs an LC-tank architecture, while the frequency divider scales down the high VCO output to a frequency suitable for comparison in the PFD. The loop filter, implemented with two capacitors and one resistor, is designed to ensure loop stability and desired transient response. The following sections detail the design methodology, component-level considerations, and performance trade-offs for each block of the PLL.

4.1 Phase-Frequency Detector (PFD)

The phase-frequency detector (PFD) is responsible for comparing the phase and frequency of the reference signal (f_{ref}) and the feedback signal (f_{fb}) derived from the frequency divider. The PFD generates two control signals, UP and DOWN, which drive the charge pump to either source or sink current into the loop filter. This process adjusts the control voltage of the voltage-controlled oscillator (VCO), thereby reducing the phase and frequency error between the two inputs. A conventional topology based on two edge-triggered D flip-flops and asynchronous reset logic is used in this design due to its robustness, simplicity, and suitability for high-frequency operation.

4.1.1 Architecture

The implemented PFD consists of two edge-triggered D flip-flops, with the first clocked by the reference input f_{ref} and the second by the feedback input f_{fd}. The D inputs of both flip-flops are tied to V_{DD} ensuring that a rising clock edge sets the corresponding Q output high immediately. The Q outputs of the REF and FB flip-flops are each buffered through two stages of CMOS inverters: first by an inverter with $\times 8$ drive strength, followed by an inverter with $\times 32$ drive strength. This two-stage buffering reduces loading on the flip-flops and provides sufficient drive capability for subsequent logic. The buffered signals then form the UP and DOWN pulses, which enable the positive and negative current sources in the charge pump, respectively.

The UP and DOWN signals are fed to a two-input NAND gate, which produces the asynchronous reset signal. The NAND output is routed through a chain of four minimum-sized ($\times 1$) inverters to the reset inputs of both flip-flops. This chain restores logic levels, ensures clean reset transitions, and introduces a controlled delay. The delay is intentionally included to eliminate dead-zone effects by guaranteeing the generation of small UP or DOWN pulses even when the inputs are perfectly phase-aligned.

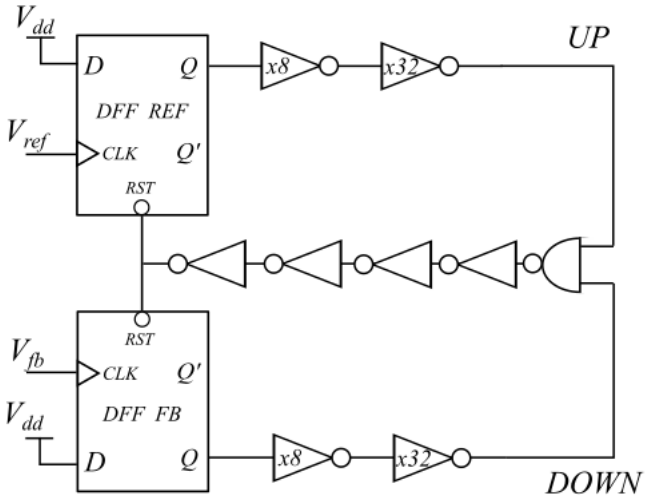


Figure 4.1: Phase-Frequency Detector

4.1.2 Operation

The PFD detects the phase difference between its two inputs and generates an error signal $v_e(t)$ proportional to this difference, expressed as:

$$v_e(t) = K_{\text{PD}} \left[\varphi_{\text{fb}}(t) - \varphi_{\text{ref}}(t)\right] \tag{4.1}$$

where K_{PD} is the phase detector gain in [V/rad].

The PFD can operate under two distinct scenarios:

- **Frequency difference**: When f_{ref} and f_{fb} differ, the PFD generates pulses whose widths change over time, driving the VCO frequency toward the reference. If f_{ref} is higher than f_{fb}, the REF flip-flop's Q output (UP) remains high for most of the cycle, while the FB flip-flop's Q output (DOWN) stays low except during short reset overlaps. This causes the charge pump to source current, increasing the VCO control voltage and raising f_{fb}. Conversely, if f_{fb} is higher than f_{ref}, the DOWN output dominates, sinking current and reducing the VCO frequency.

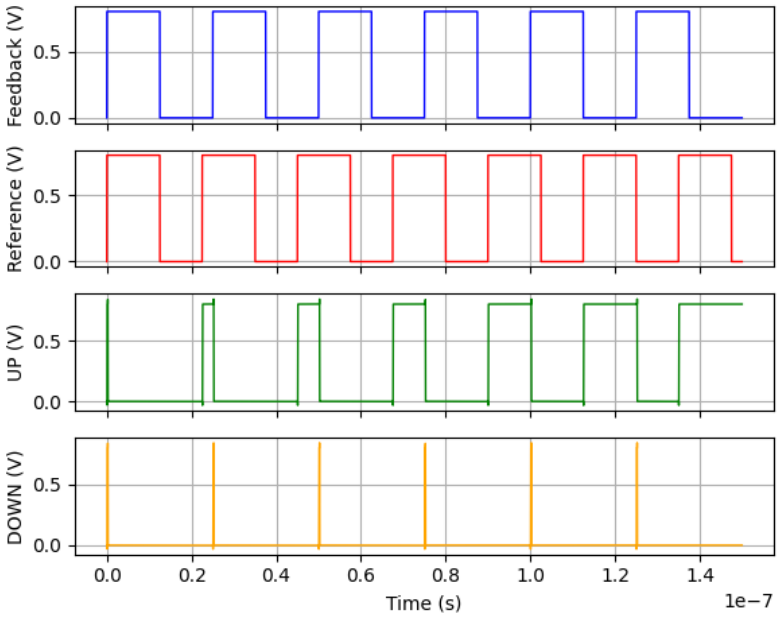


Figure 4.2: Different Frequency Operation

- **Phase difference**: When the input frequencies are equal but there is a phase offset, the PFD outputs a pulse proportional to that offset. If REF leads FB, the UP output remains high for a duration equal to the phase difference until the FB edge arrives, at which point the reset logic clears both outputs. If FB leads REF, the DOWN output behaves in the same way. Due to the finite propagation delay of the NAND gate and the asynchronous reset path, there is a brief interval during which both outputs are high, but this does not disturb loop operation.

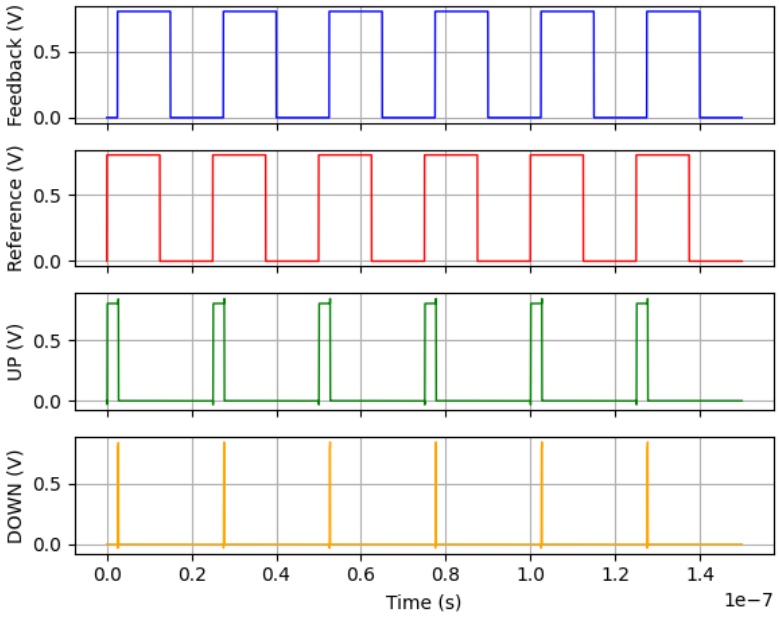


Figure 4.3: Different Phase Operation

To prevent the so-called dead zone—a condition where perfectly aligned edges produce no pulses and allow the VCO to drift—this design incorporates a controlled reset delay. As a result, even when the PLL approaches lock and the time difference between the REF and FB edges becomes very small, the UP and DOWN outputs still produce narrow pulses. At perfect lock, these pulses are minimal but remain present to keep the VCO synchronized with the reference, maintaining continuous control over the loop.

4.2 Charge-Pump (CP)

An ideal charge pump (CP) is a circuit that can either source or sink current. It consists of two ideal current sources, two switches S_1 and S_2, and a load capacitor C_1. The switches are controlled by digital signals UP and DOWN, as illustrated in Figure 4.4. The capacitor C_1 represents the load; in the context of a PLL, this is typically replaced by the loop filter.

The operation of the charge pump can be explained with a simple example. Suppose an UP pulse of width ΔT arrives at switch S_1. When S_1 closes, a constant current I_1 is delivered to the capacitor C_1, charging it. The output voltage increases according to

$$\Delta V_{out} = \frac{I_1 \cdot \Delta T}{C_1}.$$

Similarly, when a DOWN pulse arrives at switch S_2, the capacitor is discharged by the current source, decreasing V_{out} by the same relationship. If both switches are activated simultaneously, the currents cancel and V_{out} ideally remains unchanged.

In a PLL, the charge pump is typically driven by the outputs of a phase-frequency detector (PFD). The PFD generates UP and DOWN pulses depending on the phase or frequency difference between the reference signal and the feedback signal from the VCO. In steady state, when no phase or frequency difference exists, the PFD produces very short synchronized pulses. Ideally, these pulses should not alter the output voltage of the charge pump. In practice, however, small non-idealities lead to a residual voltage ripple at V_{out}, caused by slight charging and discharging events during these pulses.

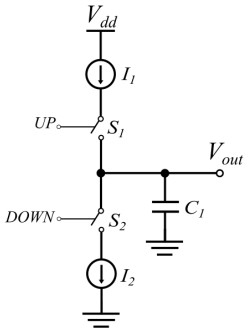


Figure 4.4: Ideal Charge-Pump

4.2.1 Traditional Charge-Pump

A traditional charge pump (CP) implementation is illustrated in Figure 4.5. In this topology, the sourcing current I_{UP} is generated by duplicating the reference current I_{REF} once through the current mirror structure M_{P1}-M_{P3}. The sinking current I_{DN}, in contrast, is obtained by duplicating I_{REF} twice through an additional current mirror stage,

specifically M_{P1}-M_{P2} and M_{N1}-M_{N2}. This asymmetry introduces a higher sensitivity to process variations, which results in current mismatch between I_{UP} and I_{DN}. Such mismatches directly degrade the performance of the PLL, since they contribute to reference spurs at the output.

Furthermore, a simple rail-to-rail operational amplifier is incorporated into the design. Acting as a high-speed buffer, the op-amp provides a large input swing that can track the variations of nodes V_{ctrl} and V_A during the charging and discharging phases. It ensures that node V_A closely follows the control voltage V_{ctrl}, while maintaining a fixed voltage at the drains of the current source transistors. This configuration keeps the transistors in ideal saturation, improves current matching, and makes the operation of the sourcing and sinking branches largely independent of the output voltage.

The main drawback of the traditional charge pump remains the current mismatch caused by process variations and the inherent asymmetry of the mirror stages. In this work, two different techniques are employed to alleviate this limitation:

1. Replacing the traditional topology with a resistive-based charge pump architecture. [1] 2. Introducing an offset current, which counterbalanced the residual mismatch. [2]

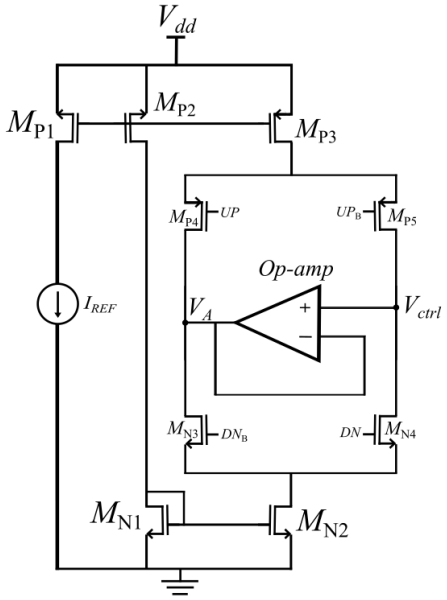


Figure 4.5: Traditional Charge-Pump

4.2.2 Resistive Based Charge-Pump

In the proposed design, the current mirrors typically used for reference current replication are replaced by an operational amplifier and a resistor. A bandgap-derived reference voltage, V_{REF}, is applied in a negative feedback configuration, which stabilizes the reference current according to

$$I_{\mathrm{REF}} = \frac{V_{\mathrm{REF}}}{R_1}.$$

Subsequently, through the action of Op-Amp2 and Op-Amp3, the voltage V_{REF} is replicated across resistors R_2 and R_4, generating the sourcing and sinking currents, I_{UP} and I_{DN}, respectively. Each operational amplifier drives a transistor at its output to ensure voltage stability across the corresponding resistor. Because both I_{UP} and I_{DN} are

derived directly from a single instance of reference current replication, the impact of device mismatch is significantly reduced compared to traditional mirror-based implementations.

The most critical element of this architecture is the design of the operational amplifiers. The central amplifier (OpAmp4), which is responsible for tracking the control voltage V_{ctrl} at node V_A, must be designed to satisfy three essential requirements:

1. High open-loop gain (> 60 dB) to minimize steady-state error.

2. High slew rate and bandwidth to achieve rapid transient response.

3. Rail-to-rail input and output capability to accommodate the full supply voltage range.

The remaining amplifiers (Op-Amp1–3), which are primarily used for biasing, impose less stringent requirements. For these devices, a moderate gain exceeding 40 dB is sufficient to ensure stable operation across the full range of V_{REF}, along with rail-to-rail input and output capability to maintain functionality across the supply voltage.

Similar to conventional charge pump designs, the central op-amp maintains a fixed voltage at the drains of the current-source transistors, thereby keeping them in saturation and improving current matching. However, in this work additional measures are implemented to mitigate switching-related non-idealities. Dummy MOSFETs are employed to suppress the clock feedthrough of the main switching transistors, while the inclusion of series devices reduces reference spurs and alleviates charge-sharing effects.

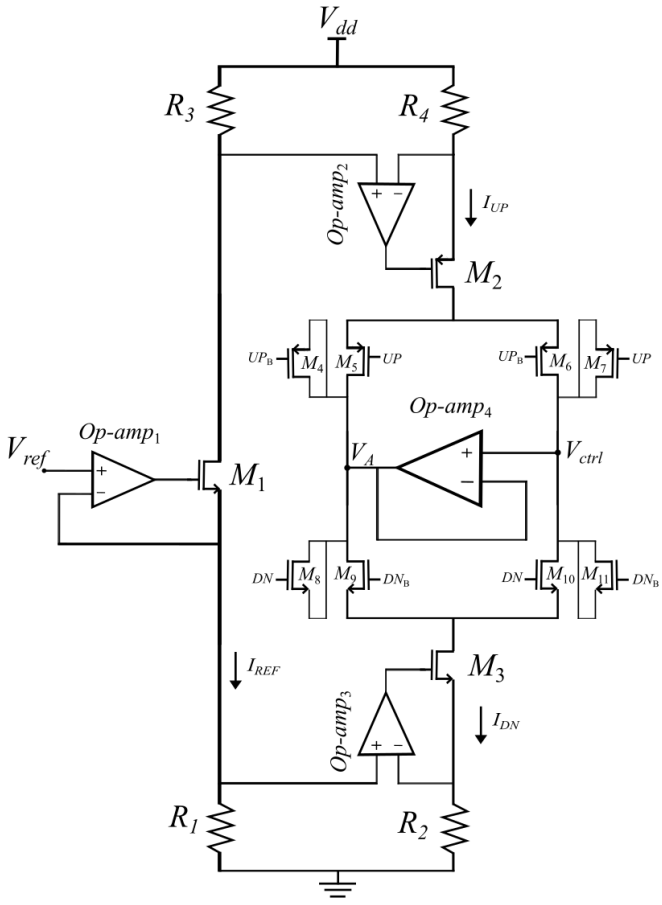


Figure 4.6: Resistive Based Charge-Pump

4.2.3 Operational Amplifiers (OP-Amps)

In order to fully evaluate the suitability of the proposed architecture, it is therefore necessary to analyze the two categories of operational amplifiers separately.

DC biasing Op-Amps

To meet the requirements of DC biasing in op-amps, a rail-to-rail input op-amp architecture was selected. The design begins with a folded cascode stage, implemented using both PMOS and NMOS differential input pairs (M_3,M_4,M_7,M_8). This configuration ensures that at least one input pair always remains in saturation, thereby maintaining first-stage amplification across the entire input common-mode voltage range.

The behavior of the input stage can be summarized in three scenarios:

- Scenario 1: As the input common-mode voltage approaches the positive supply voltage (V_{DD}), the PMOS pair transitions into the triode or even cutoff region, while the NMOS pair remains in saturation.
- Scenario 2: As the input common-mode voltage approaches ground, the NMOS pair enters the triode or cutoff region, while the PMOS pair remains in saturation.
- Scenario 3: For intermediate values of the input common-mode voltage, both the PMOS and NMOS input pairs remain in saturation.

To ensure that all transistors operate in saturation across these scenarios, a wide-swing current mirror (M_{15}–M_{19}) was adopted for the NMOS branch. Given the low supply voltage of 0.8 V, super-low threshold voltage (SLVT) devices were employed, as they provide the minimum required V_{DS} for saturation. Furthermore, the transistor dimensions were carefully chosen to guarantee proper saturation operation, with the final sizing values listed in Table X.

The second stage consists of a common-source amplifier, where transistor M_{21} operates in saturation. The node between transistors M_{14} and M_{17} establishes the dominant pole of the op-amp, which provides frequency compensation and ensures stability. Through parametric analysis, the values of R_1 and C_1 were determined to achieve a phase margin greater than 65°.

Finally, transistors M_1, M_2, M_5, M_6, M_9, and M_{12} are utilized for current mirroring, ensuring accurate biasing throughout the circuit.

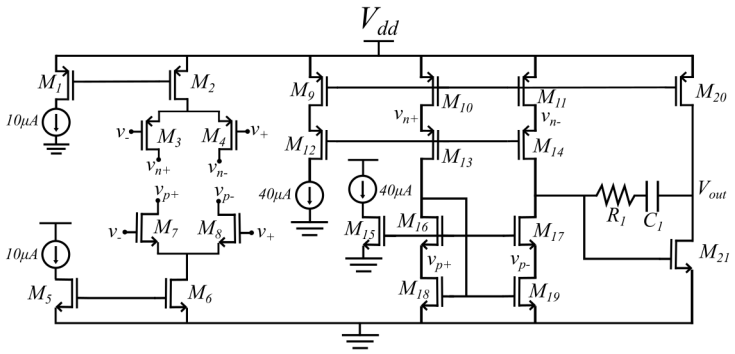


Figure 4.7: DC biasing OP-Amp Architecture

Table 4.1: Device sizing of DC biasing OP-Amp

Device	Width (nm)	Length (nm)	Number of fingers	Multiplier	Type
M_1	640	100	4	4	RVT
M_2	640	100	4	4	RVT
M_3	1280	20	8	2	RVT
M_4	1280	20	8	2	RVT
M_5	640	100	4	4	RVT
M_6	640	100	4	4	RVT
M_7	1280	20	8	2	RVT
M_8	1280	20	8	2	RVT
M_9	3000	40	15	4	SLVT
M_{10}	3000	40	15	4	SLVT
M_{11}	3000	40	15	4	SLVT
M_{12}	3000	40	15	4	SLVT
M_{13}	3000	40	15	4	SLVT
M_{14}	3000	40	15	4	SLVT
M_{15}	400	40	2	1	RVT
M_{16}	600	40	3	3	SLVT
M_{17}	600	40	3	3	SLVT
M_{18}	600	40	3	3	SLVT
M_{19}	600	40	3	3	SLVT
M_{20}	3000	40	15	4	SLVT
M_{21}	800	40	4	2	SLVT
R_1	0.36	3700	-	8	N+ Poly Silicided
C_1	1844	1844	-	-	Apmom1v8

High-Speed Op-Amp

The primary distinction between a high-speed op-amp and the previously discussed DC-biased op-amp lies in the requirements of the output stage. In high-speed designs, the output stage must be capable of sourcing currents up to 500 µA while ensuring that all transistors remain in saturation.

To support this high current, the output transistors are significantly larger than those used in the DC-biased op-amp. This increased sizing allows the transistors to handle larger load currents without leaving saturation. In addition, the larger devices reduce the overdrive voltage, which improves the linearity of the amplifier under high-current conditions, enhancing overall performance.

The final sizing is summarized in Table 4.2.

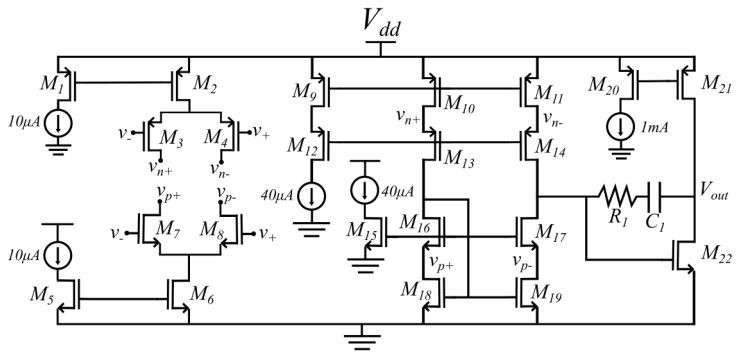


Figure 4.8: High-Speed OP-Amp Architecture

Table 4.2: Device sizing of High-Speed OP-Amp

Device	Width (nm)	Length (nm)	Number of fingers	Multiplier	Type
M_1	640	100	4	4	RVT
M_2	640	100	4	4	RVT
M_3	1280	20	8	2	RVT
M_4	1280	20	8	2	RVT
M_5	640	100	4	4	RVT
M_6	640	100	4	4	RVT
M_7	1280	20	8	2	RVT
M_8	1280	20	8	2	RVT
M_9	3000	40	15	4	SLVT
M_{10}	3000	40	15	4	SLVT
M_{11}	3000	40	15	4	SLVT
M_{12}	3000	40	15	4	SLVT
M_{13}	3000	40	15	4	SLVT
M_{14}	3000	40	15	4	SLVT
M_{15}	400	40	2	1	RVT
M_{16}	600	40	3	3	SLVT
M_{17}	600	40	3	3	SLVT
M_{18}	600	40	3	3	SLVT
M_{19}	600	40	3	3	SLVT
M_{20}	10000	40	20	4	SLVT
M_{21}	10000	40	20	4	SLVT
M_{22}	16000	40	20	4	SLVT
R_1	0.36	3700	-	8	N+ Poly Silicided
C_1	1303	1330	-	-	Apmom1v8

4.2.4 Current Mismatch and Reference Spur Analysis: Comparison of Traditional and Resistive-Based Charge Pumps

The improvements achieved by transitioning from a traditional charge pump (CP) to a resistive-based CP can be analyzed through current mismatch behavior.

In traditional CP architectures, asymmetric current mirroring introduces mismatch between the charging and discharging currents. Specifically, the up current (I_UP) undergoes one stage of mirroring, while the down current (I_DN) is mirrored twice. This can be expressed as:

$$I_{\mathrm{UP}} = \left(1 \pm \frac{2\Delta V_{\mathrm{THP}}}{V_{\mathrm{GSP}} - V_{\mathrm{THP}}}\right) I_{\mathrm{REF}}, \tag{4.2}$$

$$I_{\mathrm{DN}} = \left(1 \pm \frac{2\Delta V_{\mathrm{THP}}}{V_{\mathrm{GSP}} - V_{\mathrm{THP}}}\right)\left(1 \pm \frac{2\Delta V_{\mathrm{THN}}}{V_{\mathrm{GSN}} - V_{\mathrm{THN}}}\right) I_{\mathrm{REF}}, \tag{4.3}$$

Assuming $V_{\mathrm{GSP}} = V_{\mathrm{GSN}} = V_{\mathrm{GS}}$ and $V_{\mathrm{THP}} = V_{\mathrm{THN}} = V_{\mathrm{TH}}$, the resulting current mismatch is:

$$I_{\Delta} = I_{\mathrm{UP}} - I_{\mathrm{DN}} = \left[\left(\frac{2\Delta V_{\mathrm{TH}}}{V_{\mathrm{GS}} - V_{\mathrm{TH}}} \right)^2 + 3 \left(\frac{2\Delta V_{\mathrm{TH}}}{V_{\mathrm{GS}} - V_{\mathrm{TH}}} \right) \right] I_{\mathrm{REF}}, \tag{4.4}$$

In a resistive-based CP, the currents are determined using resistive elements to set the offset:

$$I_{\mathrm{UP}} = I_{\mathrm{REF}} \pm \frac{V_{\mathrm{offset,P}}}{R_1}, \qquad I_{\mathrm{DN}} = I_{\mathrm{REF}} \pm \frac{V_{\mathrm{offset,N}}}{R_2}, \tag{4.5}$$

For symmetric design parameters ($V_{\mathrm{offset,P}} = V_{\mathrm{offset,N}} = V_{\mathrm{offset}}$ and $R_1 = R_2 = R$), the maximum current mismatch becomes:

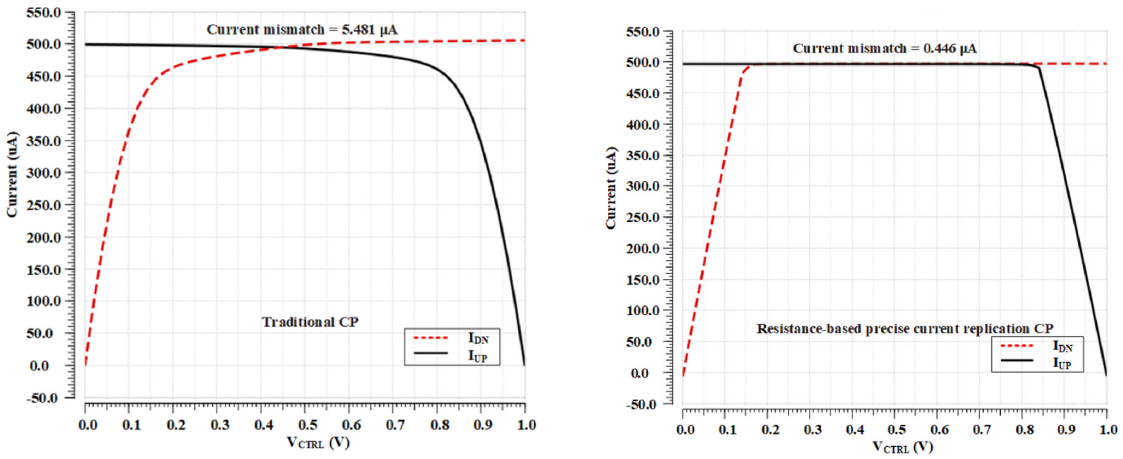
$$I'_{\Delta} = I_{\mathrm{UP}} - I_{\mathrm{DN}} = \frac{2V_{\mathrm{offset}}}{R} = \frac{2V_{\mathrm{offset}}}{V_R} I_{\mathrm{REF}}. \tag{4.6}$$

This analysis demonstrates that:

$$I'_{\Delta} < I_{\Delta}, \tag{4.7}$$

indicating that the resistive-based CP achieves lower current mismatch than the traditional architecture.

The results in [1] quantitatively compare the mismatches of the two architectures and confirm the improvement.



(a) (b)

Figure 4.9: Mismatch comparison: (a) Traditional CP, (b) Resistive-based CP.

Most reference spurs in PLLs are caused by charge and discharge current mismatches in the CP. The resulting phase error can be expressed as:

$$\Phi_{\mathrm{error}} = 2\pi \frac{t_{\mathrm{on}}}{T_{\mathrm{ref}}} \frac{\Delta I_{\Delta}}{I_{\mathrm{CP}}} \tag{4.8}$$

where T_{ref} is the reference period, t_{on} is the PFD turn-on time, I_{CP} is the nominal CP current, and I_{Δ} represents the current mismatch.

For a traditional second-order charge pump PLL, the reference spur magnitude due to this phase error is:

$$P_{\text{spur}} = 20 \log \left(\frac{t_{\text{on}} \, I_{\Delta} \, K_{\text{VCO}}}{4\pi \omega_{\text{ref}} C_2} \cdot \frac{k+1}{k} \right), \tag{4.9}$$

where K_{VCO} is the VCO gain, $k = C_1/C_2$ is the low-pass filter capacitor ratio, and ω_{ref} is the reference angular frequency.

This expression highlights that reducing ΔI_{Δ} is a direct and effective method for suppressing reference spurs in the PLL output.

4.2.5 Offset current

The second linearization technique is to add an offset current. Because of charge-pump current mismatch, the CP characteristic around zero phase error is nonlinear, which increases VCO output spurs. Introducing a small I_{offset} shifts the CP characteristic so that, for small phase errors, the CP operates in a more linear region (Fig. 4.10).

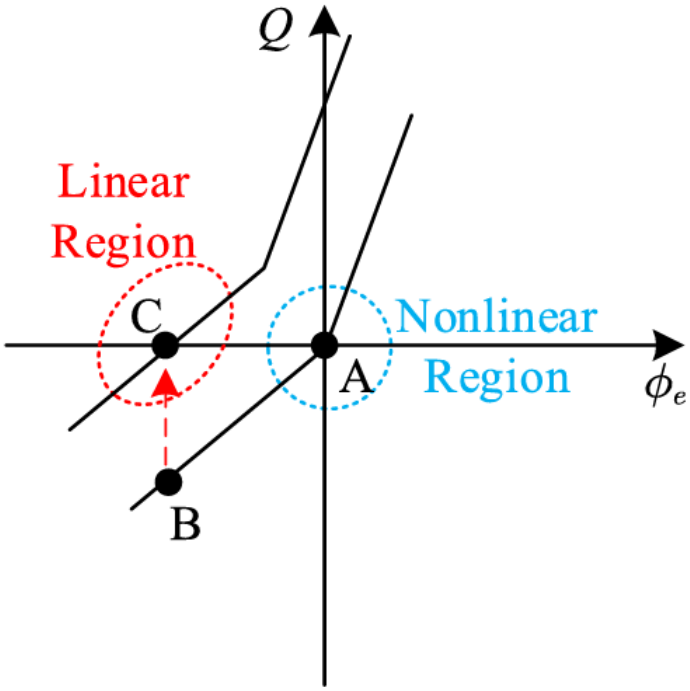


Figure 4.10: PFD-CP characteristic

When the PLL is locked, a small steady-state phase error appears with the feedback clock leading the reference clock. In this condition UP stays low (so I_{UP} is disconnected), while DN produces a pulse and turns on the DN switch so I_{DN} flows. Let t_1 be the interval where DN and FDBCK are both high. During FDBCK high, the offset current I_{offset} is also enabled.

Over one FDBCK period, the charge-pump output current $I_{\text{CP,out}}$ is therefore

$$I_{\text{CP,out}}(t) = \begin{cases} -I_{\text{DN}} + I_{\text{offset}}, & 0 \le t < t_1 \\ I_{\text{offset}}, & t_1 \le t < T/2 \\ 0, & \text{otherwise} \end{cases}$$

This produces ripple on the pre-filtered node V_1 only during the high level of FDBCK; during the low level of FDBCK (and, correspondingly, when CKREF is high), V_1 is essentially flat. Because the switched-capacitor/ sampled LPF (S-LPF) samples V_1 only when FDBCK is low, the sampled control voltage V_{ctrl} remains constant in steady state, which justifies the steady-state assumption.

In the next figure, the corresponding waveforms are presented to provide a clearer understanding of the charge pump operation.

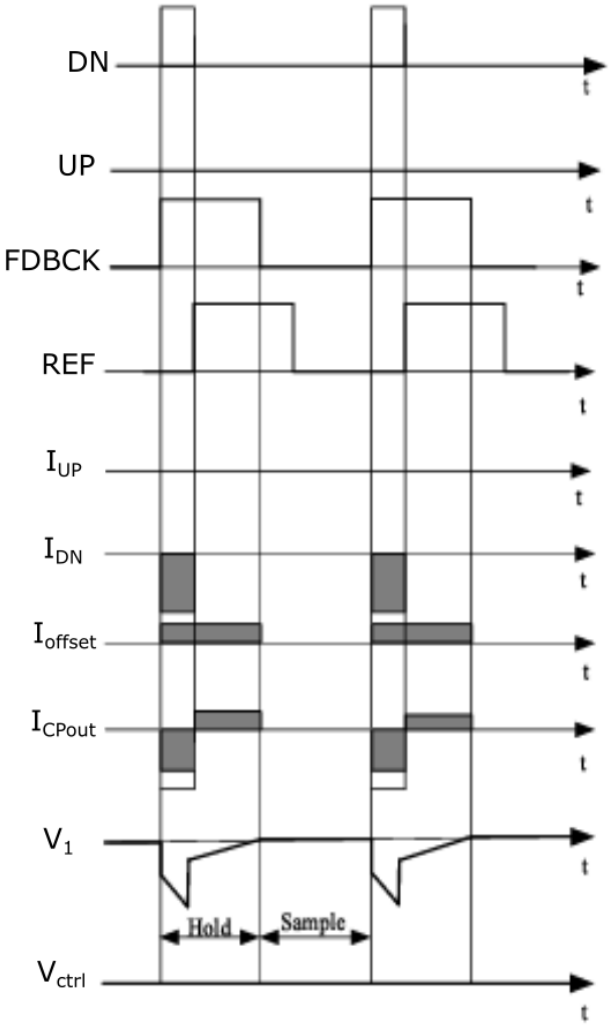


Figure 4.11: Timing waveforms

The final structure of the charge pump is shown in Figure 4.12, followed by the table listing the device dimensions. It should be emphasized that the $FDBCK_A$ and $FDBCK_B$ signals illustrated in this figure are internal control signals of the charge pump. These signals are generated through multiple inversions of the FDBCK signal.

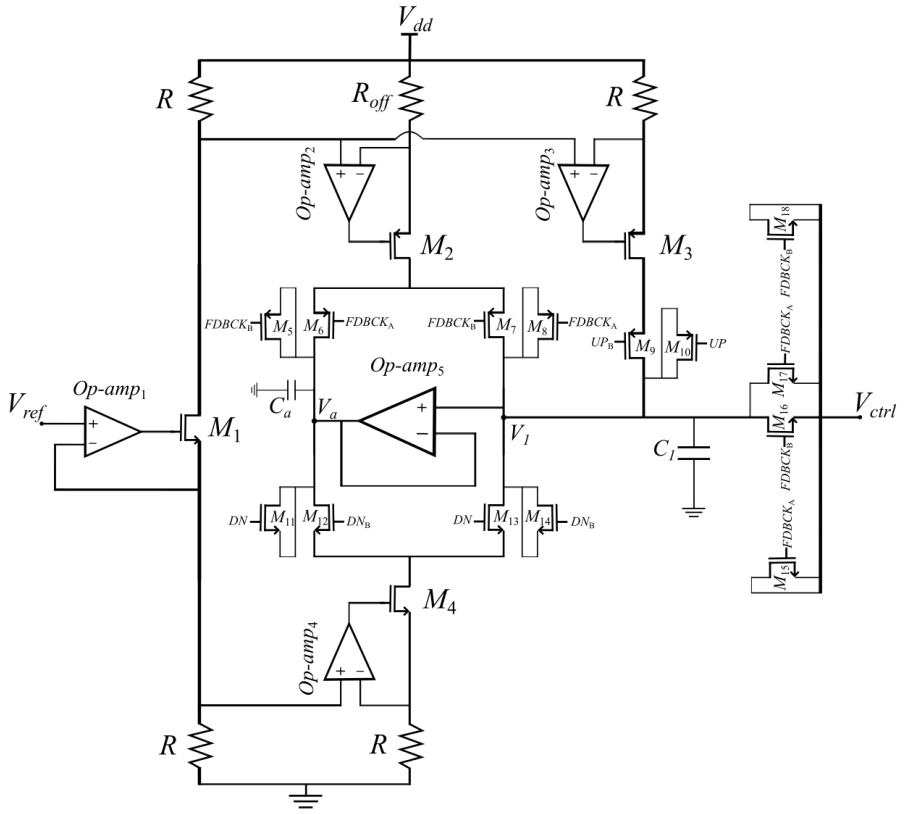


Figure 4.12: Resistive based Charge Pump with offset current

Table 4.3: Device sizing of Charge Pump

Device	**Width (μm)**	**Length (nm)**	**Number of fingers**	**Multiplier**	**Type**
M_1	8	40	20	1	RVT
M_2	8	40	20	4	RVT
M_3	8	40	20	4	RVT
M_4	8	40	20	4	RVT
M_5	30	40	20	4	RVT
M_6	30	40	20	4	RVT
M_7	30	40	20	4	RVT
M_8	30	40	20	4	RVT
M_9	15	40	10	8	RVT
M_{10}	15	40	10	8	RVT
M_{11}	10	40	20	4	RVT
M_{12}	10	40	20	4	RVT
M_{13}	10	40	20	4	RVT
M_{14}	10	40	20	4	RVT
M_{15}	3.75	40	20	2	RVT
M_{16}	3.75	40	20	2	RVT
M_{17}	3.75	40	20	2	RVT
R	0.5	3220	-	1	N+ Poly Silicided
R_{off}	0.5	3220	-	5	N+ Poly Silicided
C_1	22	22	-	4	Apmom1v8
C_a	1303	1330	-	4	Apmom1v8

4.2.6 Layout

This chapter presents the physical layout of the charge pump (CP). The main design goal is to minimize the occupied area while ensuring reliable operation. Particular emphasis is placed on transistor matching, since mismatches can lead to current imbalance and reduced output accuracy. To improve matching, the common-centroid layout technique is employed, which reduces systematic variations caused by process gradients.

Another important factor is the management of parasitic capacitances. Large and irregular coupling capacitances can introduce unwanted delays, charge leakage, and signal distortion, degrading the efficiency of the charge pump.

Signal routing is also a critical aspect. The charge pump requires the transfer of signals over relatively large distances within the integrated circuit. To ensure low-resistance paths and reduce voltage drops, thicker metal layers are extensively used for both long-distance interconnects and for carrying the supply (V_{DD}) and ground (GND) networks.

To support these requirment, the 22 nm CMOS FD-SOI technology provides eight metal layers: M1, M2, C1, C2, C3, IA, OI, and LB. M1 and M2 are the lowest layers, mainly used for short local interconnects, with a minimum width of 40 nm. The intermediate C-layers (C1–C3) are $\tilde{1}.1\times$ the height of M1, offering slightly higher current limits and lower sheet resistance (10 Ω/µm at 44 nm width versus 15.5 Ω/µm for M1).

The IA layer, nine times taller than M1, supports up to 3.1 mA at minimum width (360 nm) and is suitable for higher-power signal routing. The OI layer is thirty-four times the height of M1, with a minimum width of 1.8 µm, a current limit of 71 mA, and an extremely low sheet resistance of 0.027 Ω/µm. These properties make OI ideal for power supply distribution and long interconnects in the PLL design. In contrast, the LB layer, although 2.8 µm thick, has less favorable electrical properties and is therefore not utilized in the layout.

In the following figure, the layout of the charge pump, including the loop filter, is depicted. The total area is calculated as 302.913 μm $\times$ 197.88 μm = 0.05994mm^2. As can be seen, the loop filter capacitor occupies a significantly larger portion of the area compared to the rest of the circuit. The DC biasing op-amps are arranged in an almost square configuration, while the high-speed op-amp is positioned such that, together with the capacitor $C_a = 1.6404pF$, it forms a rectangular structure.

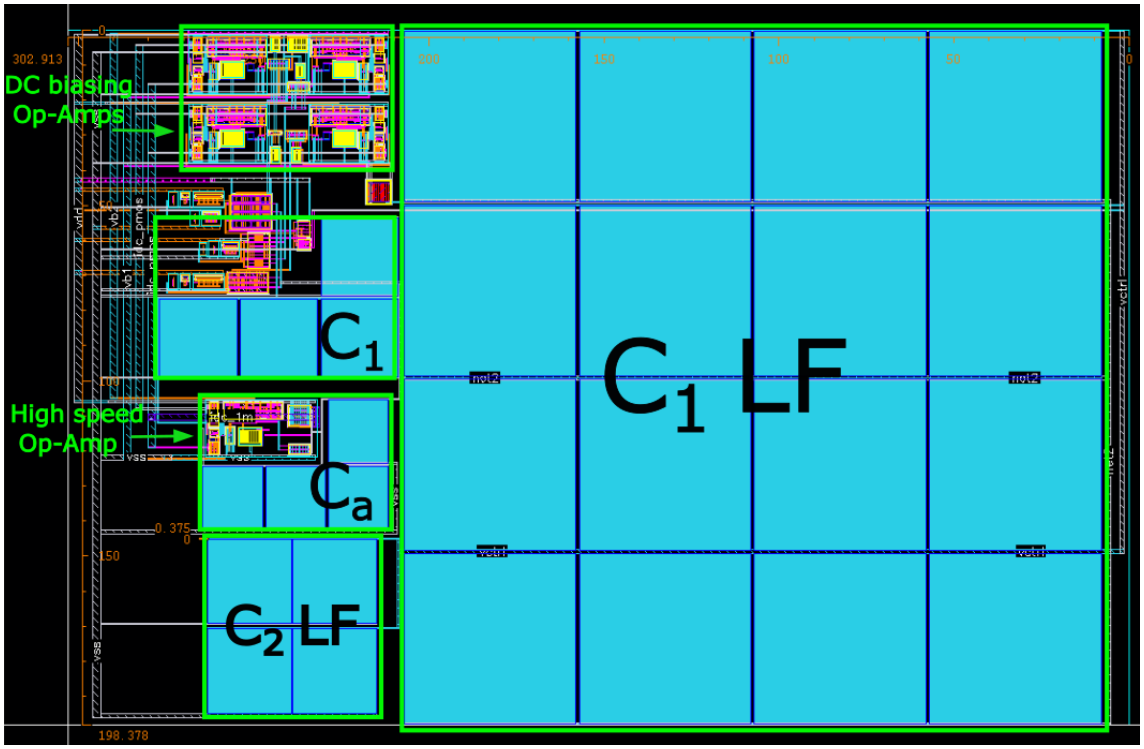


Figure 4.13: Charge Pump and Loop Filter Layout

Op-Amps Layout

The layouts of the operational amplifiers (op-amps) are shown next for clarity. The transistors of the current mirrors are arranged in a common-centroid configuration and enclosed by guard rings to minimize the effects of process variation. For the differential pair, maintaining symmetry after interconnect placement is particularly important to ensure accurate operation. In the folded NMOS branch, the biasing transistor belongs to a different device type and therefore requires a guard ring, since super-low-V_T devices use a triple-well structure, whereas regular devices do not. The remaining PMOS devices share a common guard ring. Beneath them, the resistor and capacitor (implemented using the lowest thin-metal layers) are placed alongside the active common-source NMOS transistor. Dummy devices are also included to enhance matching and mitigate the well proximity effect.

The inter-stage signal paths are routed through different metal layers and are deliberately not stacked vertically, thereby reducing coupling capacitance. Power is supplied through the IA layer, chosen for its ability to handle higher currents with low resistance, making it suitable for both V_{DD} and ground connections.

The main distinction between the DC biasing amplifier and the high-speed, high-current amplifier lies in the PMOS high-current mirror, which is connected via the IA metal layer to the common-source NMOS. While the use of thicker metals improves current-handling capability, it also increases parasitic capacitance. As a result, a smaller compensation capacitor is required to maintain a high phase margin.

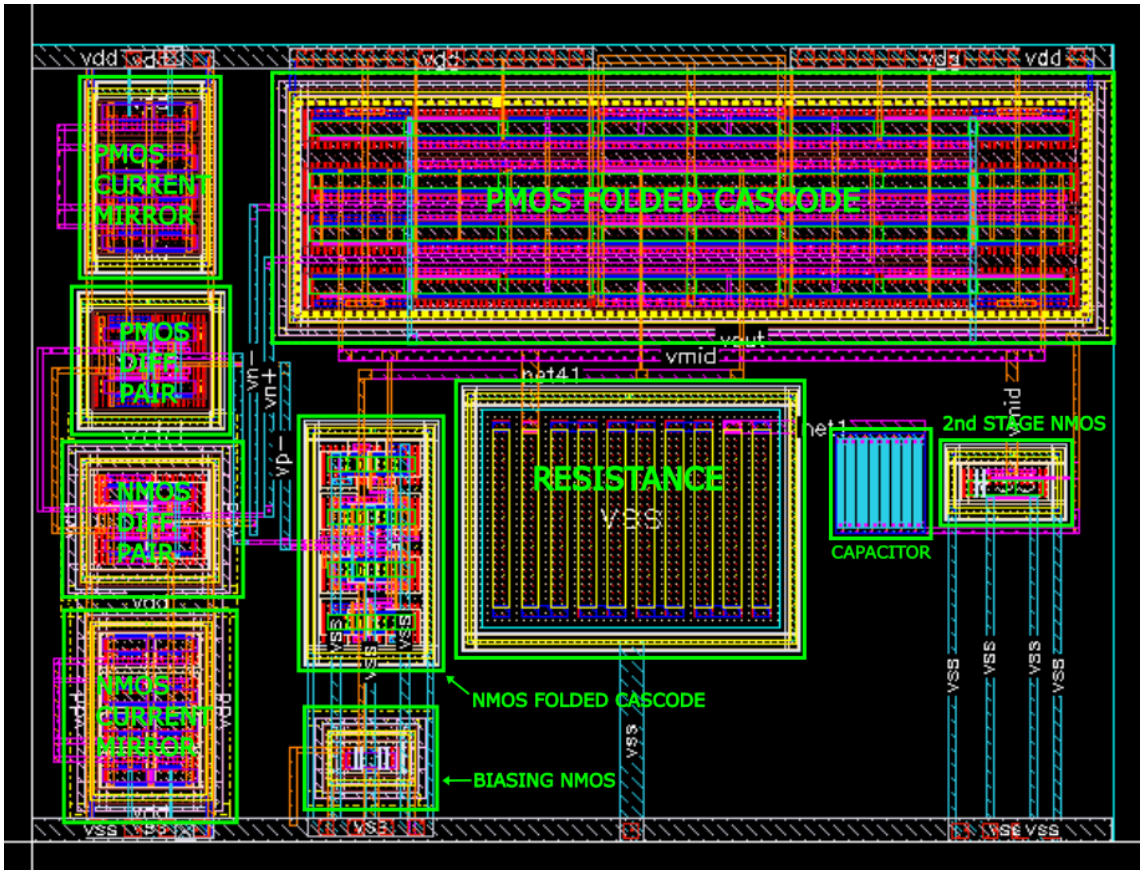


Figure 4.14: DC biasing Op-Amps Layout

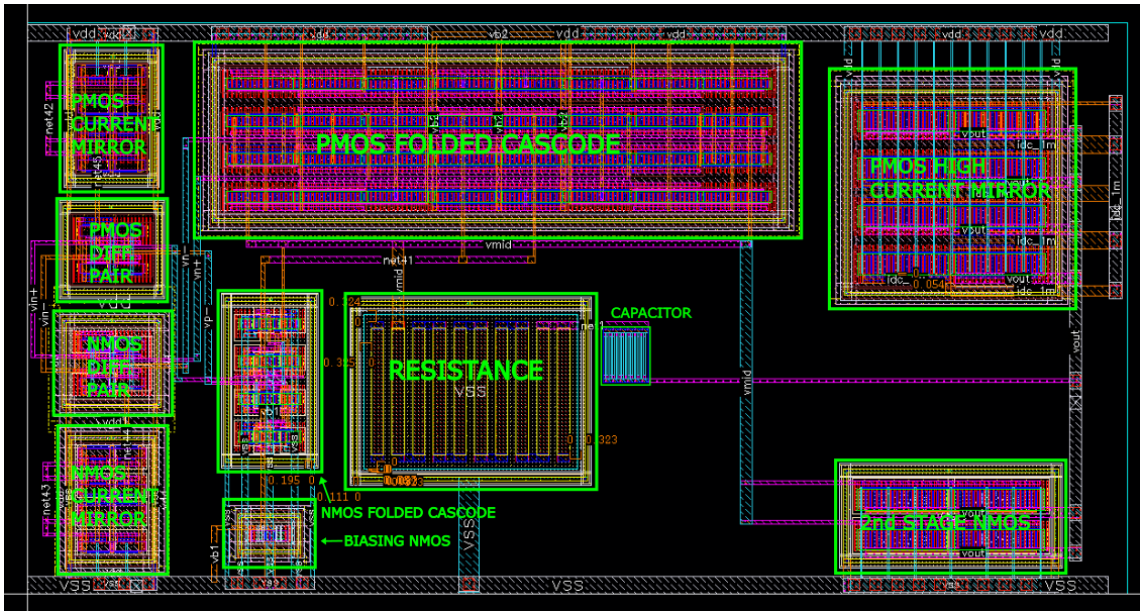


Figure 4.15: High-Speed Op-Amp Layout

4.2.7 Pre Vs Post Layout

The final step of the design and implementation process is the comparison between pre-layout and post-layout results. The first simulation is a transient analysis of the charge pump (CP) with the UP signal held at logic low. The $FDBCK_{ref}$ signal is high for half of the period, while the DN signal remains high for a duration five times shorter, in order to demonstrate a near steady-state condition. Figures 4.16 and 4.17 show the pre-layout and post-layout simulation results, respectively.

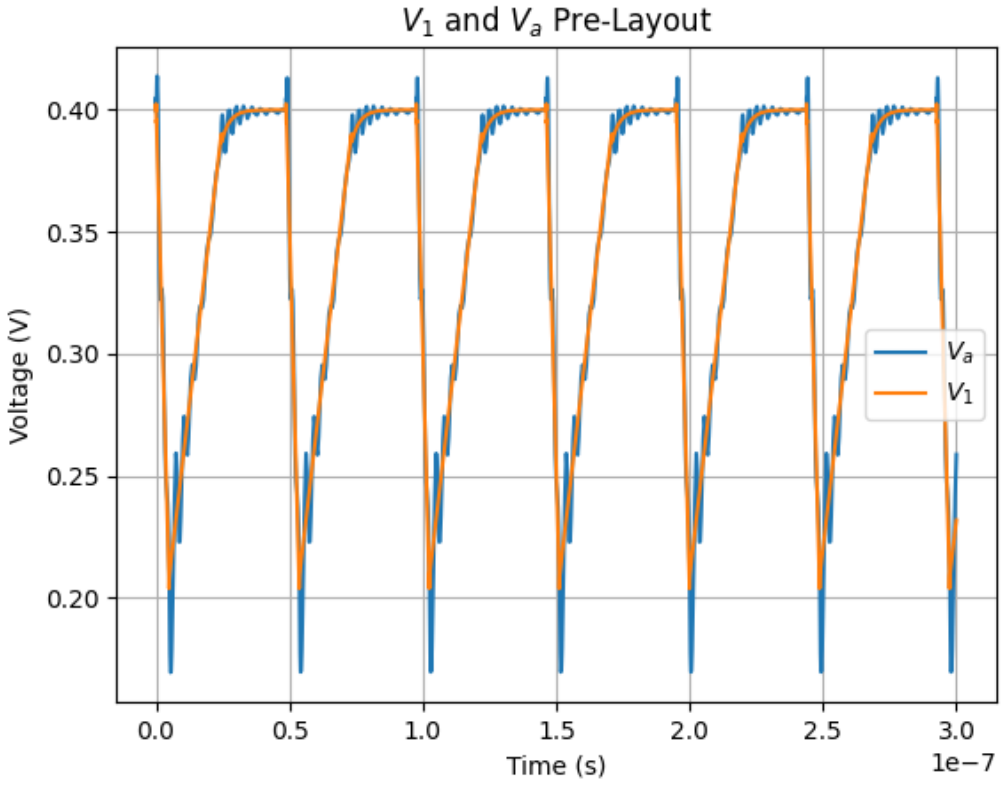


Figure 4.16: V_a and V_a Pre-Layout

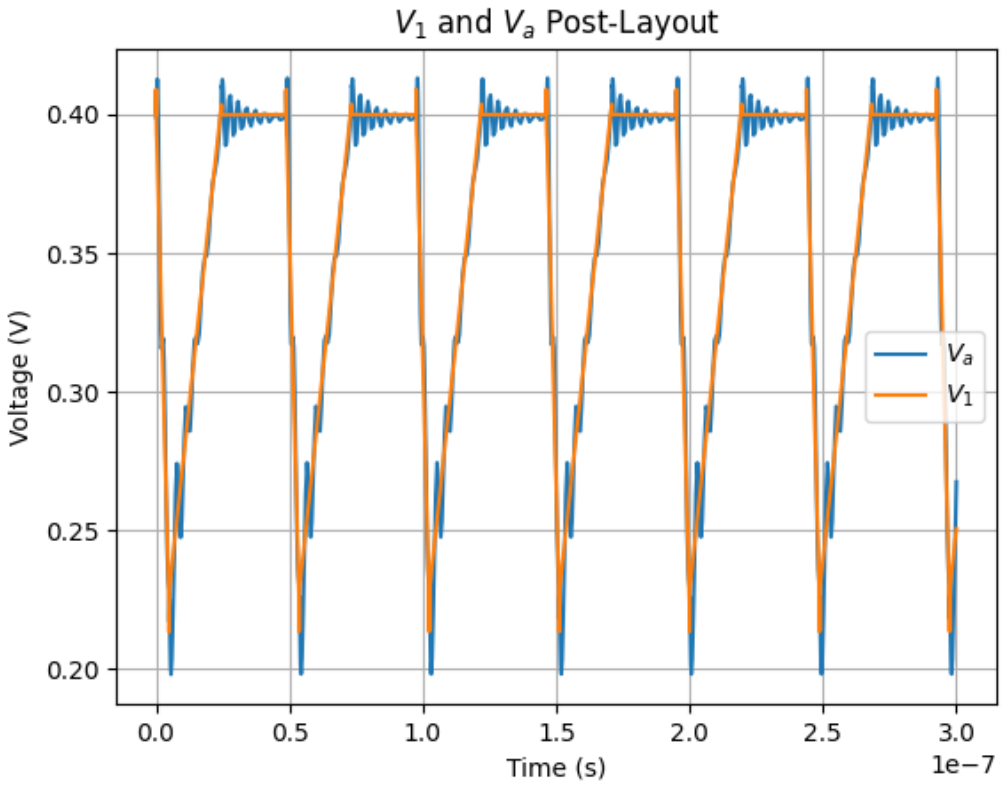


Figure 4.17: V_a and V_a Post-Layout

Next, the mismatch between the UP and DN current sources is evaluated using DC parametric operating-point analysis. Two cases are considered:

1. UP = logic low, DN = logic high
2. UP = logic high, DN = logic low

In both cases, $FBCK_{ref}$ is held at logic high to ensure that the output voltage remains stable and no offset current is delivered to the output capacitors. A large mismatch increases the lock time of the PLL and results in reference spurs of higher magnitude. Figures 4.18 and 4.19 present the pre-layout and post-layout current mismatch, respectively.

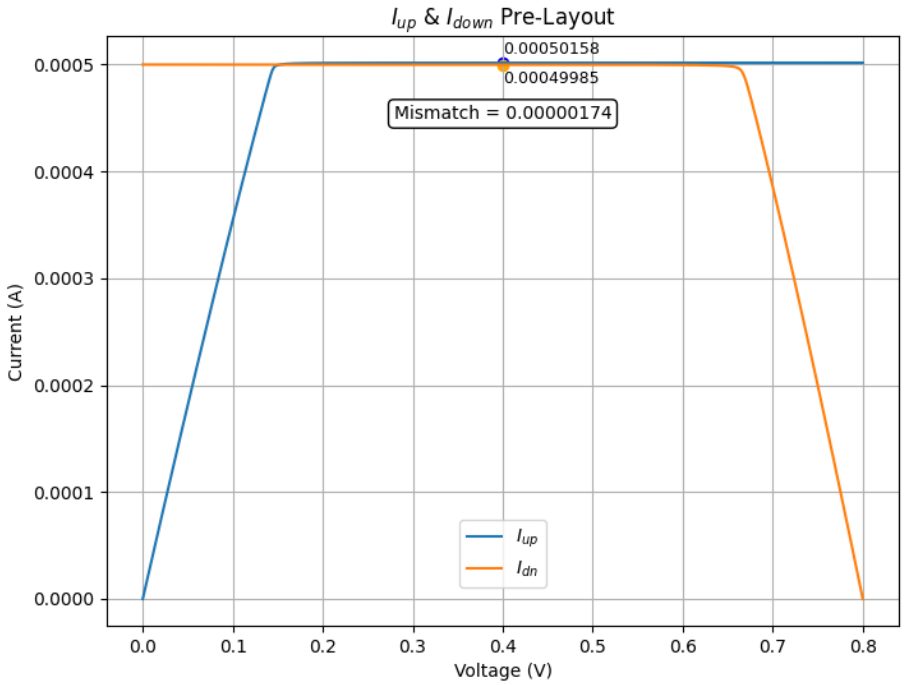


Figure 4.18: Pre-Layout Mismatch

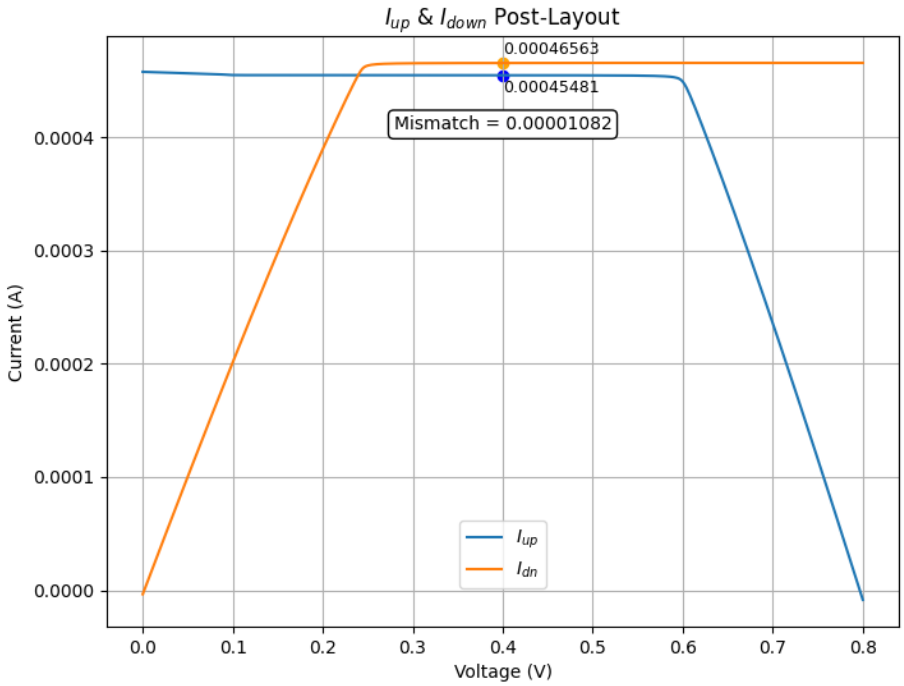


Figure 4.19: Post-Layout Mismatch

In the pre-layout simulation, the mismatch is minimal (1.74 µA), whereas in the post-layout simulation it increases to 10.82 µA. This degradation is mainly caused by voltage drops across vias and interconnect metals connected to the load resistors. To mitigate this issue, the resistor values were adjusted. The original resistance was $R = 194.64\ \Omega$. Since the voltage across a resistor is given by $V = I \cdot R$, the corrected resistor value is calculated as:

$$R_{\text{new}} = R_{\text{old}} \cdot \frac{I_{\text{old}}}{I_{500\mu A}} \tag{4.10}$$

The updated values are:

$$R_{\text{dn}} = 181.26\ \Omega, R_{\text{up}} = 177.05\ \Omega \tag{4.11}$$

After this correction, the mismatch is reduced to 1.83 µA which is comparable to that of the pre-layout design.

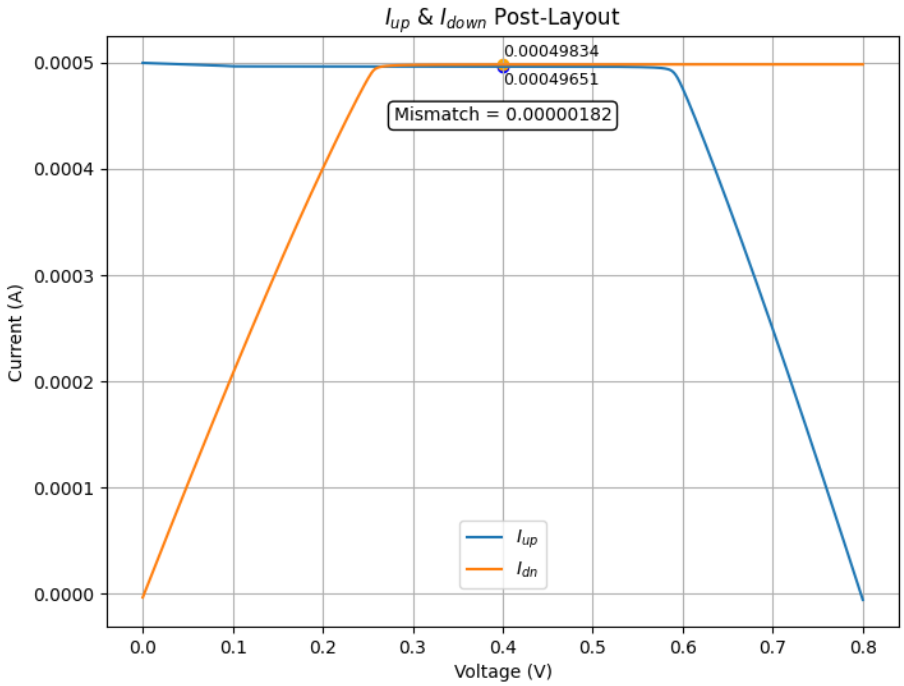


Figure 4.20: Imporved Post-Layout Mismatch

4.3 Loop Filter

The loop filter plays a crucial role in stabilizing the phase-locked loop (PLL) by converting the pulsed current from the charge pump into a smooth control voltage (V_{ctrl}) and by shaping the loop's frequency response. A well-designed filter ensures that V_{ctrl} settles to its intended steady-state value, eliminating residual phase error and maintaining lock.

A second-order loop filter, as shown in Figure 4.21, is widely used because it offers a good balance between noise suppression and loop stability. By integrating low-frequency error components and attenuating high-frequency disturbances, it controls the trade-off between acquisition speed, phase margin, and jitter performance.

In PLL designs, the loop filter must also account for parasitic capacitances and the load presented by the VCO. These effects influence the filter's ability to reject spurious signals and maintain stability, making careful selection of component values essential. The following section outlines the step-by-step procedure for determining these component values based on phase margin and desired loop bandwidth.

4.3.1 Loop Filter Design Procedure

The following loop filter design methodology follows the guidelines provided by Renesas [3]. The transfer function of the second order filter is:

$$H(s) = \frac{1 + sR_1C_1}{s\left(C_1 + C_2 + sR_1\frac{C_1C_2}{C_1+C_2}\right)} \tag{4.12}$$

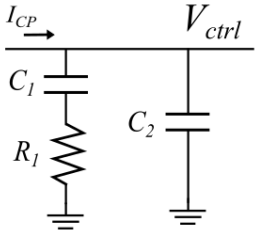


Figure 4.21: Second Order Loop Filter

From the transfer function the zero occurs at:

$$\omega_z = \frac{1}{R_1 C_1} \tag{4.13}$$

and provides phase lead, which helps to increase the phase margin and stabilize the loop. The first pole is located at the origin (ω_{p1}=0) and ensuring that the steady-state phase error is zero. The second pole is at:

$$\omega_{p2} = \frac{C_1 + C_2}{R_1 C_1 C_2} \tag{4.14}$$

This high-frequency pole attenuates control-voltage ripple and suppresses noise beyond the loop bandwidth, but if placed too close to the zero frequency, it can reduce phase margin. In practice, C_2 is chosen much smaller than C_1 so that $\omega_{p2} \gg \omega_z$,preserving the intended lead compensation effect while providing high-frequency noise suppression.

For a PLL to operate reliably, PM must be greater than 50°, ensuring that the loop remains stable. In this work, a phase margin of 65° was chosen as a design target. This value provides a balanced compromise: it offers ample stability margin to prevent oscillations and reduces overshoot and ringing in the transient response, thereby improving lock time consistency and minimizing the impact of disturbances on output jitter. From the phase margin (PM) equation, it is possible to calculate the ratio C_1/C_2:

$$\text{PM} = \arctan\left(\frac{b-1}{2\sqrt{b}}\right) \tag{4.15}$$

where $b = 1 + \frac{C_1}{C_2}$.

By selecting the desired loop bandwidth f_c and using the phase margin equation, the loop filter components can be calculated systematically. The resistor R_1 is determined by:

$$R_1 = \frac{2\pi f_c N}{I_{cp} K_{vco}} \tag{4.16}$$

where N is the divider ratio, I_{cp} is the charge pump current, and K_{vco} is the VCO gain. The capacitor C_1 is computed as:

$$C_1 = \frac{a}{2\pi f_c R_1} \tag{4.17}$$

where $a = \frac{f_c}{f_p}$ is a design constant related to the desired loop response. Finally, the smaller capacitor C_2 is derived from:

$$C_2 = \frac{C_1}{a\beta} \tag{4.18}$$

where $\beta = \frac{f_p}{f_c}$.

By solving the system of equations and refining the design through simulations to minimize voltage ripple, the final values for the loop filter components are determined as follows: The final component values are $C_1 = 205.08\,\text{pF}$, $C_2 = 12.2816\,\text{pF}$, and $R_1 = 59.07\,\text{k}\Omega$. The phase margin was then recalculated to be $63.26°$.

To better understand the frequency response of the loop filter, Figure 4.22 shows the Bode diagram of the open-loop transfer function, with the zero and second pole frequencies clearly marked.

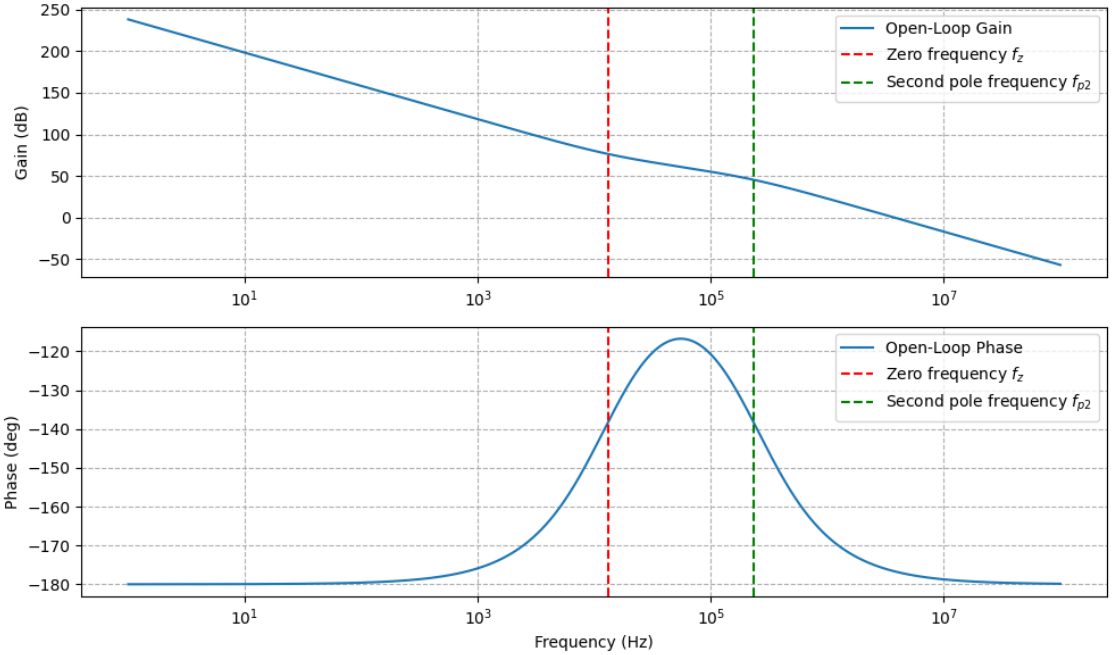


Figure 4.22: Loop Filter Bode Diagram

4.4 Voltage Controlled Oscillatos (VCO)

A voltage-controlled oscillator (VCO) is a key building block in a phase-locked loop (PLL), as it converts a control voltage into an output frequency with high precision. The frequency of the VCO output is directly related to its input voltage, allowing fine control over the oscillation frequency. The proportionality between input voltage and frequency is characterized by the VCO gain, often expressed as $K_{\text{VCO}} = \frac{\Delta f}{\Delta V}$ in units of (Hz/V). In PLL design, the ideal VCO combines a wide tuning range with low power consumption and good spectral purity.

Two types of VCOs are typically used in integrated PLLs: ring oscillators and LC-VCOs. Ring oscillators are the simplest to implement on-chip, consisting of an odd number of cascaded inverting stages connected in a loop. This configuration naturally oscillates and can reach very high frequencies with relatively straightforward design. Ring oscillators are compact and can achieve low-to-moderate power consumption, but they tend to produce square-wave outputs with higher phase noise compared to LC-based designs.

In contrast, LC-VCOs are widely preferred in applications requiring superior phase noise performance and better figure of merit (FOM). An LC-VCO uses a resonant LC tank circuit, where an inductor L is connected in parallel with a capacitor C, oscillating ideally

at:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{4.19}$$

To sustain oscillation, the energy added by a differential cross-coupled transistor pair must exceed the energy dissipated by R_s, the inductor's series loss resistance, which dominates over the capacitor's loss resistance. This active pair generates a negative resistance R_p that cancels the effect of R_s. From Barkhausen's criterion, the oscillation startup condition is satisfied when the magnitude of the negative resistance is greater than or equal to the tank's equivalent resistance, expressed as:

$$g_m R_{p,eq} \geq 1 \quad \Leftrightarrow \quad g_m \geq \frac{2}{R_p} \tag{4.20}$$

,where g_m is the transconductance of each transistor in the cross-coupled pair. An LC-VCO has been chosen as the suitable topology, and its detailed design analysis is presented in the following sections.

4.4.1 Topology Overview

To cover the required PLL frequency range of 6–10.5 GHz, two LC-VCOs are employed. The first operates over 6–8.5 GHz, and the second over 8–10.5 GHz. The architecture of both VCOs is shown in Figure 4.23. In each design, the cross-coupled NMOS transistors are biased via a single current mirror formed by M_3-M_4. The LC tank consists of an inductor, a constant capacitor and a MOS-varactor. Therefore, the tuning network employs a combination of coarse-grain capacitor bank and fine-grain capacitor bank to cover the entire frequency range. The coarse capacitor bank provides discrete frequency steps, offsetting the overall tuning range in larger increments. The fine capacitor bank enables smaller step adjustments, allowing precise alignment of the tuning curve before relying on the varactor for continuous control. In operation, the coarse bank selects the appropriate frequency interval, the fine bank refines the frequency within that interval, and finally, the varactor locks the VCO to the exact desired frequency.

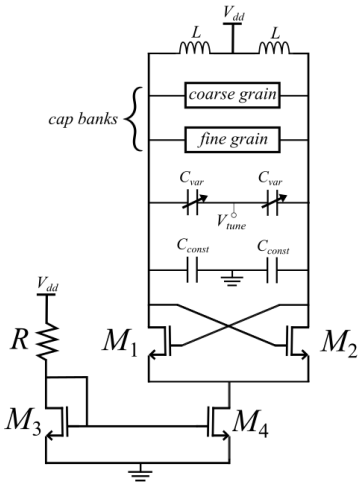


Figure 4.23: Voltage Controlled Oscillator

A MOS varactor is employed as the tunable element. The varactor is directly tuned by an analog control voltage and plays a critical role in defining the frequency response within

the tuning range. A MOS varactor can be realized using a MOSFET with its source and drain terminals short-circuited. The gate is biased at V_{bias}, while the control voltage V_{ctrl} is applied to modulate the gate potential relative to the source V_{gs}. This modulation alters the varactor's capacitance C_{gs}. As illustrated in the characteristic curve 4.24, increasing V_{ctrl} from $V_{ctrl,min}$ to $V_{ctrl,max}$ results in an increase of the capacitance from C_{min} to C_{max}. In the context of a resonant circuit, this capacitance variation causes the oscillation frequency to decrease from f_{max} to f_{min}. The characteristic curve of the MOS varactor shows plateaus at both voltage extremes. These regions correspond to reduced capacitance sensitivity $\frac{dC}{dV}$ making them unsuitable for precise tuning. To ensure predictable behavior, we therefore operate in the central region of the curve, where the $f - V_{ctrl}$ relationship is approximently linear.

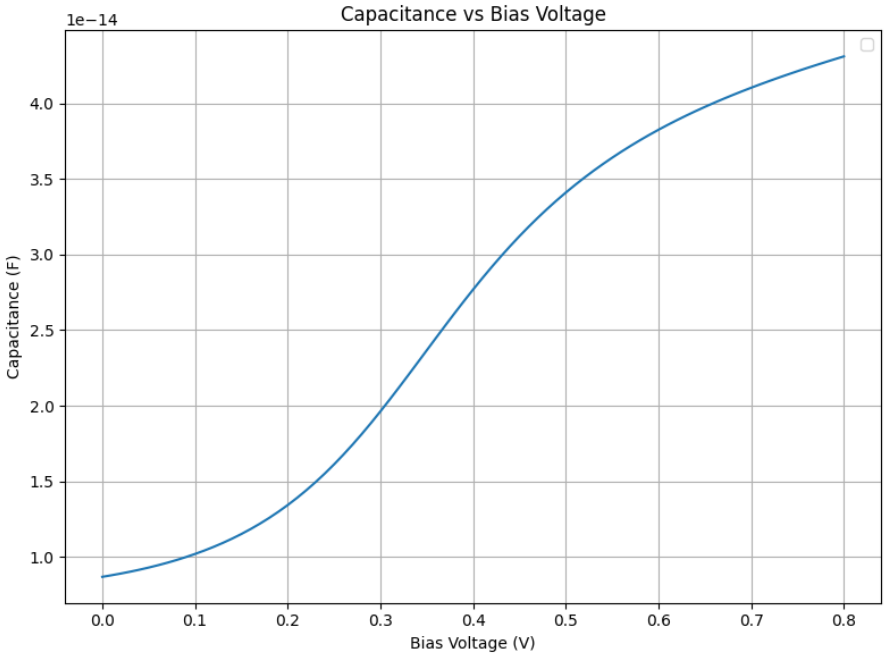


Figure 4.24: MOS Varactor

The MOS varactor inherently provides only a limited tuning range, since its capacitance variation between C_{min} and C_{max} is constrained by device physics. As a result, the corresponding tuning gain K_{VCO} cannot be made arbitrarily large. A high K_{VCO} would lead to excessive sensitivity of the oscillation frequency to control-voltage noise, thereby degrading the phase noise performance of the VCO. To increase the overall frequency coverage while preserving phase noise characteristics, a multiband VCO architecture is adopted. This multiband operation allows the VCO to cover a wide frequency range without requiring an excessively high K_{VCO}, thereby maintaining both wide coverage and good phase-noise performance.

In this approach, multiple overlapping frequency ranges are employed to span the desired tuning spectrum. This is achieved by integrating a digitally controlled fine-grain capacitor bank into the LC resonator. The capacitor bank is designed with 32 overlapping frequency bands, each of which can be selected through digital control signals. The choice of 32 bands was determined through simulation as an optimal solution, ensuring that the tuning gain K_{VCO} remains within a moderate and well-controlled range.

To implement the digitally controlled capacitor bank, MOS switches controlled by digital logic levels ('0' for off and '1' for on) are used to selectively add or remove discrete

capacitance values from the LC tank. In the proposed design, 10 MOS switches and 10 capacitors are implemented in a symmetrical topology with a grounded center node (Figure 4.25).

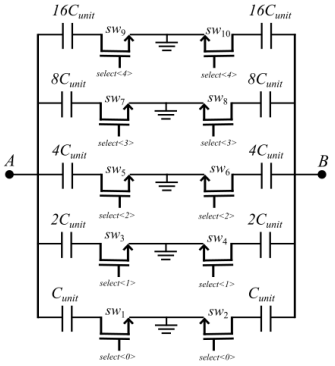


Figure 4.25: Capacitor bank

For instance, if a specific tuning state such as band 27 must be selected, the corresponding digital control word applied to the switches may take the form of 11011, where each bit determines the on/off state of the associated capacitor.The selected switches contribute discrete capacitance values of $16C_{unit}$+$8C_{unit}$+$2C_{unit}$+C_{unit}, leading to a total capacitance addition of $27C_{unit}$.

The coarse-grain capacitor banks share the same basic structure as the fine-grain capacitor bank, consisting of a symmetrical arrangement of switches and capacitors with a grounded center node. These coarse-grain banks are used to achieve large frequency steps. In the VCO operating in the 6-8.5 GHz range, the coarse-grain capacitor bank consists of 6 MOS switches and 6 fixed capacitors, whereas in the VCO operating in the 8-10.5 GHz range, only 4 MOS switches and 4 fixed capacitors are used. This difference in configuration allows each VCO to achieve the desired tuning range while maintaining controlled tuning gain and frequency resolution.

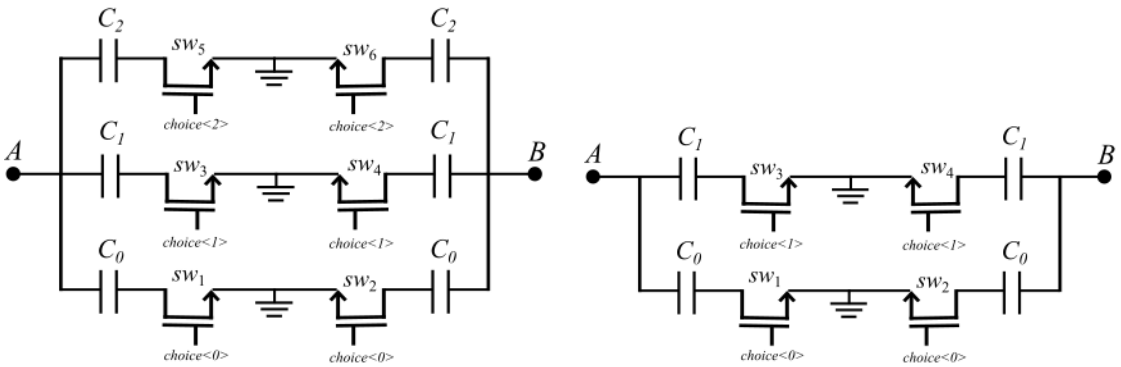


Figure 4.26: Coarse-tuning capacitor banks of two VCOs: (a) first VCO (6–8 GHz), (b) second VCO (8–10 GHz).

4.4.2 Design Procedure

To begin with, the first step in the VCO design is the sizing of the MOSFETs. The cross-coupled NMOS pair is biased using a single current mirror formed by transistors M_3 and M_4. The diode-connected transistor M_3 is biased with a current of 32.41 µA, achieved using a resistor of R = 2.5 kΩ connected to the supply voltage V_{DD} = 0.8 V. M_4 is designed to operate strongly in the triode region to ensure proper current mirroring and stable biasing of the cross-coupled pair. The drain current is I_D = 12.39 mA. Finally, it is important to achieve a large transconductance (g_m), as indicated by equation (3.10), to maximize oscillation amplitude and frequency stability. The calculated transistor sizes for the cross-coupled pair and biasing circuitry are summarized in the following table:

Table 4.4: MOSFETs sizing of both VCOs.

Device	**Width (μm)**	**Length (μm)**	**Number of fingers**	g_m (mA/V)	I_D **(mA)**
M_1	400	0.04	80	133.5	6.198
M_2	400	0.04	80	133.5	6.198
M_3	1.2	1	1	201.8	0.032
M_4	480	1	80	76.8	12.39

In the design of VCO, the inductor and fixed capacitor of the LC resonator are carefully chosen. The quality factor (Q) is a key parameter that influences performance. A higher-Q resonator has a narrower bandwidth, providing better frequency stability since it is less affected by component variations and external factors. However, the reduced bandwidth also limits the oscillator's tuning range. Additionally, high-Q circuits sustain oscillations with minimal energy loss, ensuring efficient and stable operation. Selecting an appropriate Q factor involves balancing frequency stability, tuning range, and energy efficiency.

Taking these considerations into account, the Q factor is selected as 20, which is close to the maximum value supported by the technology (21) at the design frequency of f_0 = 7.25 GHz. The inductor value is set to 100 pH.

The target frequency range of 6–8.5 GHz is divided into three sections, corresponding to the steps controlled by the coarse-grain capacitor bank. Focusing on the first third of the range, the minimum and maximum total capacitance are calculated based on equation (3.9). The total capacitance consists of contributions from the varactor, the transistors, the capacitor banks, parasitic effects, and the fixed capacitor.

By setting the maximum VCO gain K_{VCO} to 40 MHz/V, the required capacitance variation (ΔC_{var}) is determined through varactor sizing, yielding:

$$\Delta C_{var} = 108.85\,\text{fF}.$$

Subsequently, the unit capacitance C_{unit} of the fine-grain capacitor bank is evaluated. From (3.9), the total capacitance difference is found to be:

$$C_{max} - C_{min} = 1.616\,\text{pF},$$

which leads to the relation:

$$31x + \Delta C_{var} = 1.616\,\text{pF}.$$

Solving for x, the smallest unit capacitance is obtained as:

$$C_{unit} = 48.61\,\text{fF}.$$

This implies that the varactor capacitance variation must satisfy:

$$\Delta C_{var} \geq C_{unit},$$

to ensure overlapping between adjacent frequency bands. For a 20% overlap, the required varactor variation is:

$$\Delta C_{var} = 1.2\, C_{unit} = 130.62\,\text{fF}.$$

Since C_{unit} is defined, the fine-tuning capacitor bank can be constructed using binary-weighted elements (powers of two). The same procedure is repeated for the remaining two frequency sections. Finally, the fixed capacitor C_{const} is selected to define the upper frequency limit of the oscillator. Specifically, C_{const} ensures that the tuning starts from 8.5 GHz and extends down to 6 GHz, thus enabling continuous frequency coverage across the desired range. Although at first glance the entire range does not appear fully covered due to the nonlinear decrease of K_{VCO} and parasitic capacitances that were not explicitly included in the above calculations.

After iterative adjustments and simulations, the final design results in four frequency sections, each consisting of 32 bands. The values of the capacitors corresponding to each band and section are summarized in the following table:

Table 4.5: Capacitor sizing of the 6-8.5 GHz VCO.

Device	**Width (μm)**	**Length (μm)**	**Multiplier**	**Overall Value (fF)**
C_{const}	9.35	9.35	8	2364.83
C_{var}	1.6	0.5	1	8.69-43.01
C_{unit}	3.09	3.09	1	30.84
C_{2unit}	3.09	3.09	2	61.68
C_{4unit}	3.09	3.09	4	123.36
C_{8unit}	3.09	3.09	8	246.72
C_{16unit}	3.09	3.09	16	493.44
C_0	12.27	12.27	1	509.46
C_1	23.82	23.82	1	1940.16
C_2	29.3	29.3	1	2939.83

It is also important to consider the sizing of the MOSFET switches used in the capacitor banks. The switches must be designed sufficiently large to ensure reliable operation, i.e., to properly connect and disconnect the capacitors without introducing excessive resistance R_{on} or degrading the tuning linearity.

Table 4.6: MOSFETs switches of the 6–8.5 GHz VCO.

Fine-grain capacitor bank				
Device	**Width (μm)**	**Length (nm)**	**Multiplier**	**Number of fingers**
sw_1	1.4	40	1	2
sw_2	1.4	40	1	2
sw_3	2.8	40	1	4
sw_4	2.8	40	1	4
sw_5	5.6	40	1	8
sw_6	5.6	40	1	8
sw_7	11.2	40	1	16
sw_8	11.2	40	1	16
sw_9	22.4	40	1	32
sw_{10}	22.4	40	1	32
Coarse-grain capacitor bank				
Device	**Width (μm)**	**Length (nm)**	**Multiplier**	**Number of fingers**
sw_1	44.8	40	1	32
sw_2	44.8	40	1	32
sw_3	179.2	40	1	32
sw_4	179.2	40	1	32
sw_5	320	40	1	32
sw_6	320	40	1	32

As a final note, a stability test was performed, with particular focus on the ss_120 corner in Cadence Virtuoso. For sustained oscillation under all conditions, the loop gain must remain higher than unity, satisfying the Barkhausen criterion. In addition, the phase noise (PN) was evaluated, as it is a key performance parameter for oscillators. The target specification requires a phase noise close to –100 dBc/Hz at 1 MHz offset, ensuring acceptable spectral purity and system-level performance.

A summary of the simulation results is provided in Table 4.7, while the corresponding plots are shown in Figures 4.27, 4.28, 4.29 and 4.30.

Table 4.7: Simulation results of the 6-8.5 GHz VCO

Metric	**6–8.5 GHz VCO**
Frequency bandwidth	5.986-8.528 GHz
Tuning voltage range	0-0.8 V
Power consumption	9.912 mW
Phase noise @ 1 MHz	-99.5 dBc/Hz
Maximum K_{VCO}	61.347 MHz/V
Loop gain nominal	2.0341
Minimum loop gain (ss_120)	1.4514

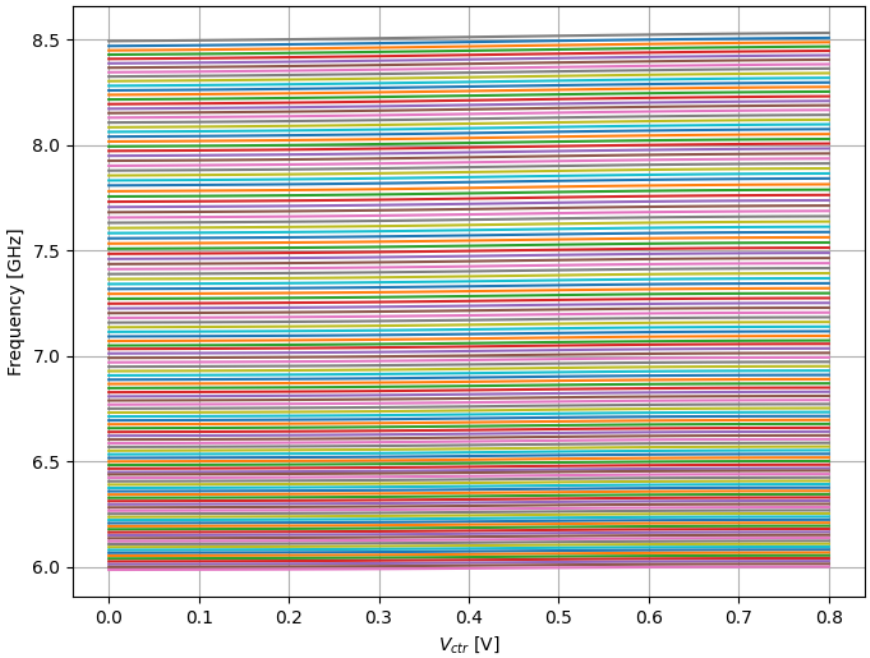


Figure 4.27: Total bands of 6–8.5 GHz VCO

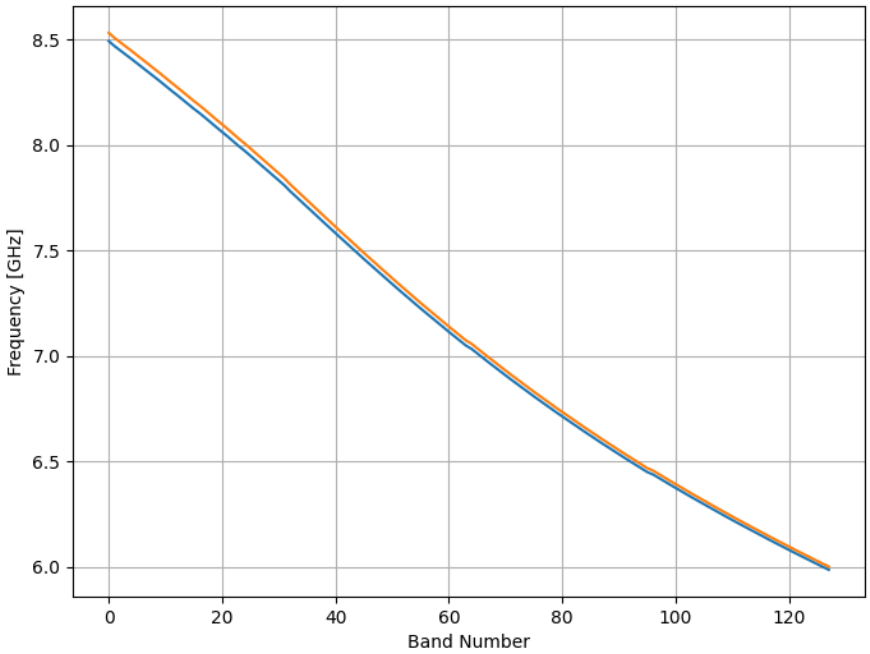


Figure 4.28: Frequency range of 6–8.5 GHz VCO

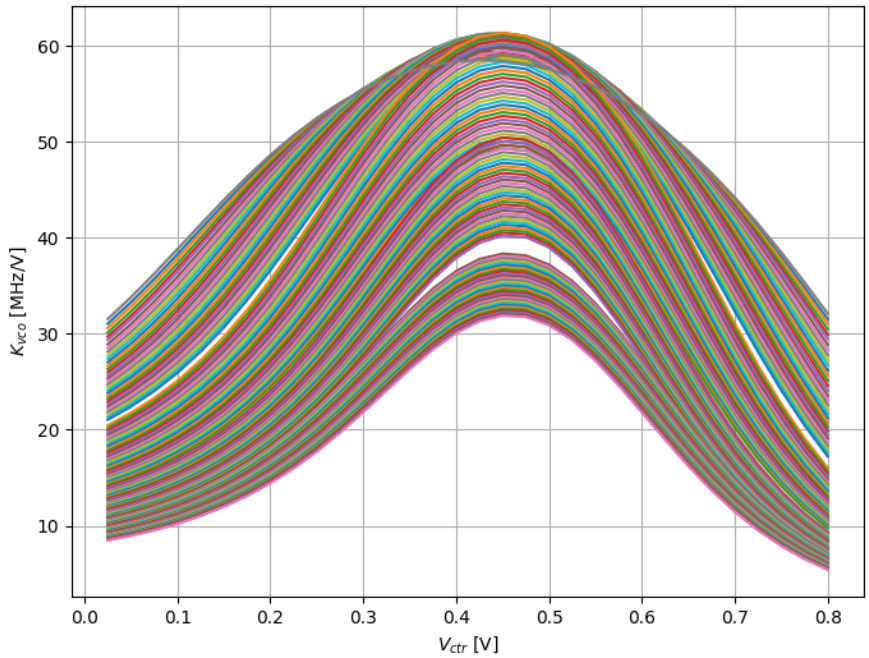


Figure 4.29: K_{VCO} of 6–8.5 GHz VCO

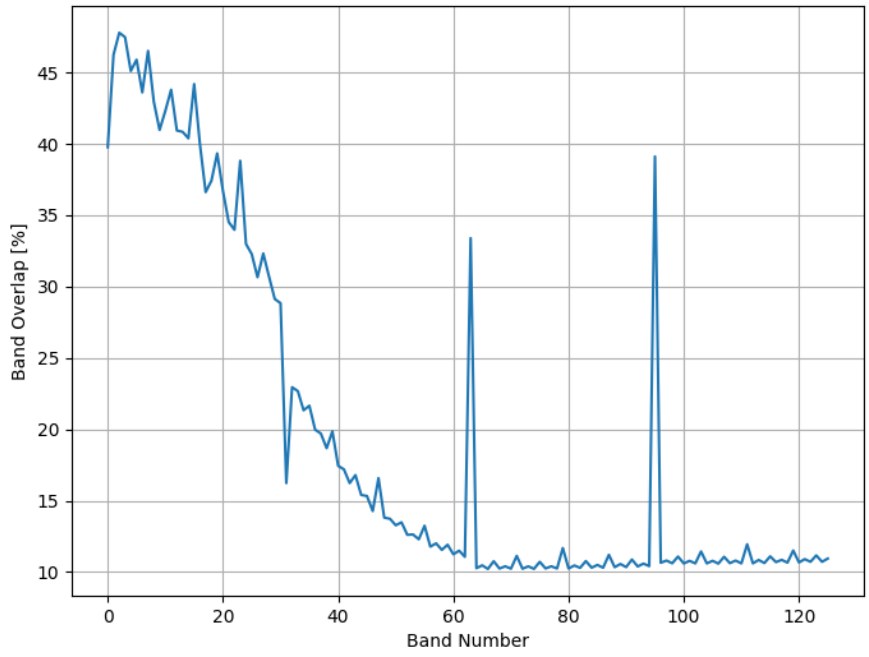


Figure 4.30: Band overlap percetange of 6–8.5 GHz VCO

Following the same design methodology, the procedure is applied to the VCOs operating in the frequency range of 8-10.5GHz The values of the capacitors corresponding to each band and section are summarized in the following table:

Table 4.8: Capacitor sizing of the 8-10.5 GHz VCO.

Device	**Width (μm)**	**Length (μm)**	**Multiplier**	**Overall Value (fF)**
C_{const}	20.47	20.47	8	1426.83
C_{var}	1.1	0.5	1	6.21-29.93
C_{unit}	2.55	2.55	1	20.74
C_{2unit}	2.55	2.55	2	41.48
C_{4unit}	2.55	2.55	4	82.96
C_{8unit}	2.55	2.55	8	165.92
C_{16unit}	2.55	2.55	16	331.84
C_0	14.1	14.1	1	677.06
C_1	19.85	19.85	1	1346.42

Table 4.9: MOSFETs switches of the 8–10.5 GHz VCO.

Fine-grain capacitor bank				
Device	**Width (μm)**	**Length (nm)**	**Multiplier**	**Number of fingers**
sw_1	1.4	40	1	2
sw_2	1.4	40	1	2
sw_3	2.8	40	1	4
sw_4	2.8	40	1	4
sw_5	5.6	40	1	8
sw_6	5.6	40	1	8
sw_7	11.2	40	1	16
sw_8	11.2	40	1	16
sw_9	22.4	40	1	32
sw_{10}	22.4	40	1	32
Coarse-grain capacitor bank				
Device	**Width (μm)**	**Length (nm)**	**Multiplier**	**Number of fingers**
sw_1	44.8	40	1	32
sw_2	44.8	40	1	32
sw_3	89.6	40	1	32
sw_4	89.6	40	1	32

A summary of the simulation results is provided in Table 4.10, while the corresponding plots are shown in Figures 4.31, 4.32, 4.33 and 4.34.

Table 4.10: Simulation results of the 8-10.5 GHz VCO

Metric	**8–10.5 GHz VCO**
Frequency bandwidth	7.87-10.51 GHz
Tuning voltage range	0-0.8 V
Power consumption	9.912 mW
Phase noise @ 1 MHz	-94 dBc/Hz
Maximum K_{VCO}	87.8 MHz/V
Loop gain nominal	2.0251
Minimum loop gain (ss_120)	1.3284

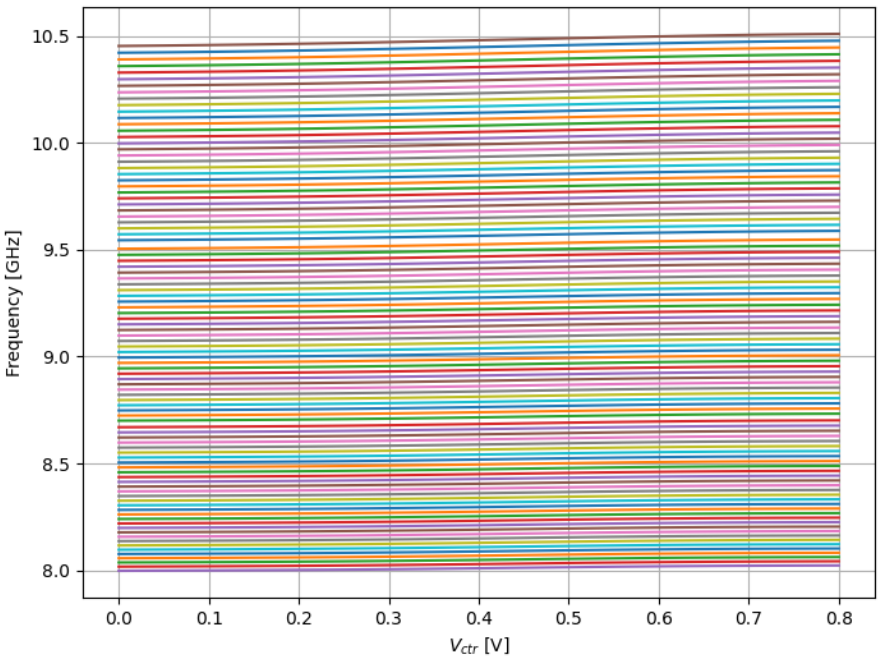


Figure 4.31: Total bands of 8-10.5 GHz VCO

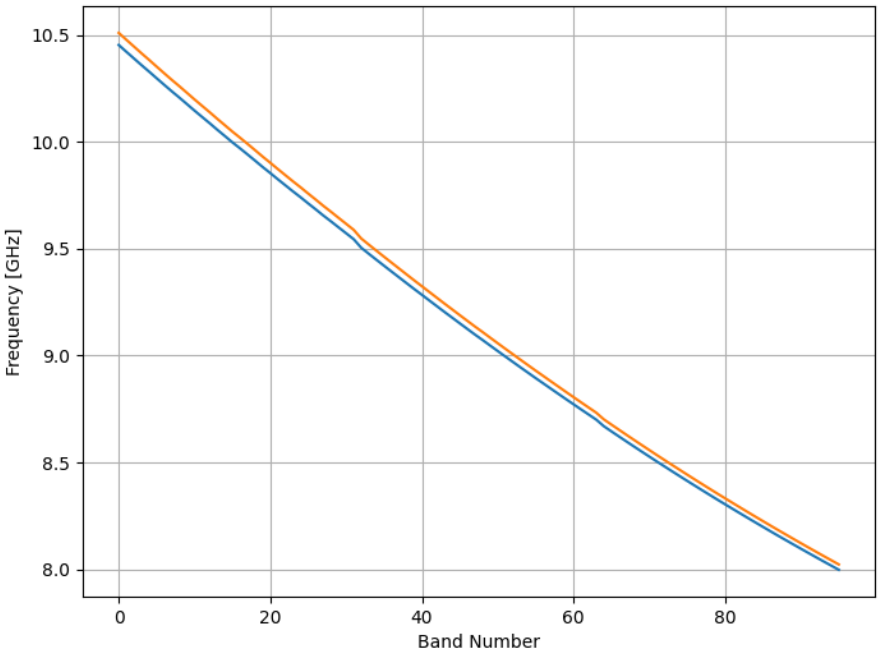


Figure 4.32: Frequency range of 8-10.5 GHz VCO

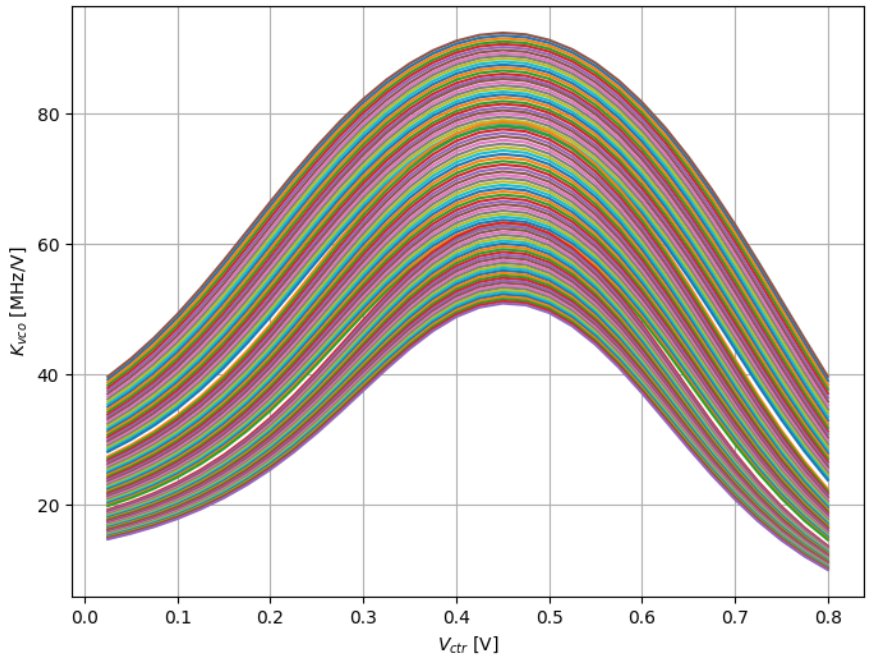


Figure 4.33: K_{VCO} of 8-10.5 GHz VCO

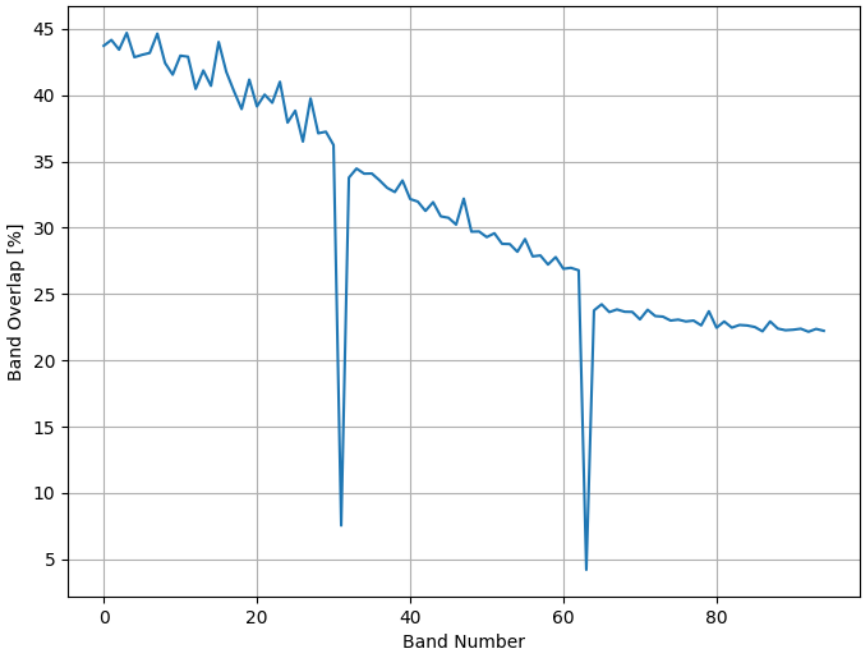


Figure 4.34: Band overlap percentage of 8-10.5 GHz VCO

4.5 RF Amplifier

At the output of the LC-tank voltage-controlled oscillator, an RF amplifier is connected. This stage is critical for the correct operation of the phase-locked loop because it converts the inherently sinusoidal output of the VCO into a clean rectangular waveform suitable for digital processing. Specifically, the frequency divider, implemented as a chain of D flip-flops (see chapter 4.6), requires a well-defined rectangular input to reliably detect rising and falling edges. At high frequencies, a sinusoidal signal crosses the logic threshold only briefly, which can lead to missed transitions and incorrect division. Therefore, the RF amplifier serves as a conversion stage to ensure robust digital operation.

Due to the inductor in the LC tank, the VCO output amplitude may exceed the supply voltage, resulting in a DC offset. To remove this offset, a coupling capacitor is placed at the amplifier input. The core of the amplifier is a CMOS inverter, biased near its point of maximum small-signal gain. At this operating point, the inverter sharpens the sinusoidal waveform around its switching threshold, producing a nearly rectangular output. This behavior is illustrated in the following figure.

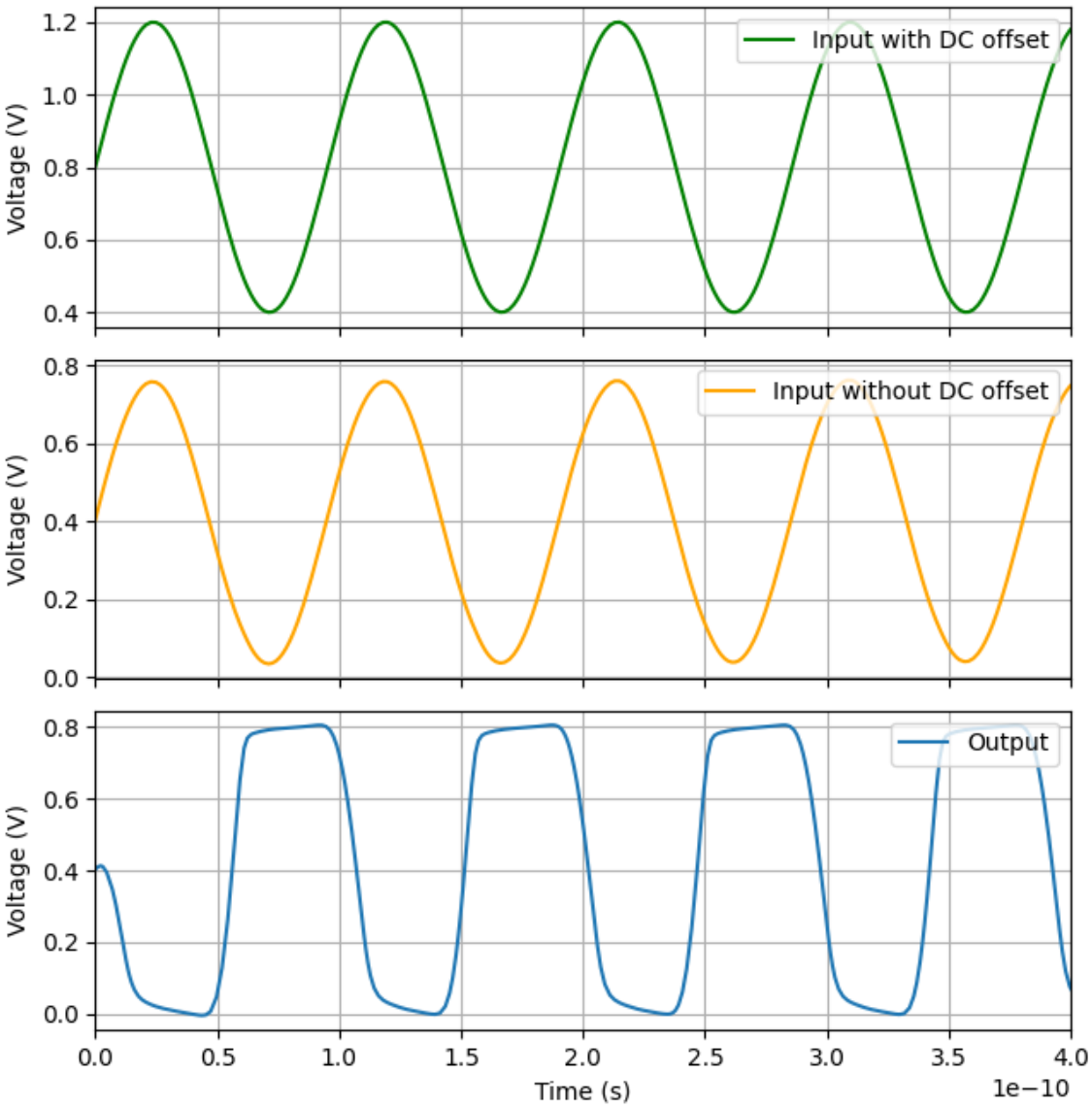


Figure 4.35: RF Amplifier Signal Transformation

A feedback resistor is connected between the inverter's input and output to stabilize the operating point. This resistor allows a small DC current to flow, biasing the inverter close to its optimal switching threshold and ensuring high gain around the zero-crossing of the input sinusoid.

The values of both the coupling capacitor and the feedback resistor are critical for proper operation. The capacitor must be large enough to block the DC offset and filter low-frequency components, but not so large that it lowers the dominant pole frequency below the target range of 6–10.5 GHz, which would reduce the inverter's gain. The resistor must allow a small DC offset between input and output, keeping the inverter biased near its peak gain point, slightly below 400 mV. Proper selection of these components guarantees reliable conversion of the sinusoidal VCO output into a rectangular waveform suitable for the divider stage.

The schematic of the RF amplifier, along with the final component dimensions determined through parametric simulations and the corresponding transient simulation results, is shown below.

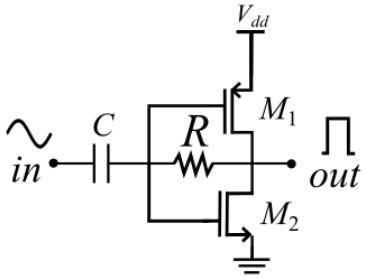


Figure 4.36: RF amplifier schematic

Table 4.11: Capacitor sizing of the 6-8.5 GHz VCO.

Device	Width (μm)	Length (nm)	Number of fingers	Multiplier	Type	Overall Value (fF)
M_1	1.92	20	24	1	LVT	-
M_2	0.64	20	8	1	LVT	-
C	3.15	3150	-	1	Apmom1v8	49.41fF
R	0.5	5300	-	4	High R-N+ Poly	30KΩ

4.6 Divider

In phase-locked loop (PLL) systems, frequency dividers play a crucial role in scaling the output frequency down to the reference frequency for comparison in the phase-frequency detector (PFD). Two common types of dividers used are integer (N) dividers and fractional dividers.

N-dividers divide the input frequency by an integer value N, providing a straightforward and stable division method. They are simple to implement, produce minimal reference spurs, and are commonly used in applications where the output frequency is an integer multiple of the reference.

On the other hand, fractional dividers allow non-integer division ratios by rapidly switching between two adjacent integer division values. This flexibility enables finer frequency resolution and supports fractional frequency synthesis, expanding the PLL's tuning range. However, fractional dividers introduce additional complexity and can generate spurs due to the fractional switching, which may require spur reduction techniques.

In this work, the frequency divider is implemented as an N-divider constructed from a chain of eight D flip-flops (DFFs), effectively realizing a divide-by-256 counter since 2^8=256, as shown in Figure 4.37 . Each flip-flop's D input is connected to its inverted Q output (Q'). The Q output of each flip-flop clocks the next stage, creating a sequential divide-by-two chain. The Q output of the eighth flip-flop provides the divided frequency signal, which serves as the feedback input to the phase-frequency detector (PFD) within the PLL loop.

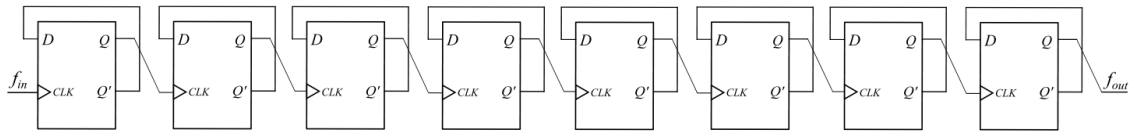


Figure 4.37: Frequency Divider

Chapter 5

Final Results

The final system-level simulation was obtained by integrating all previously designed sub-blocks into a single model. The simulated architecture comprises the phase-frequency detector, charge pump, loop filter, voltage-controlled oscillator (VCO), RF amplifier, and frequency divider, as illustrated in Figure 5.1.

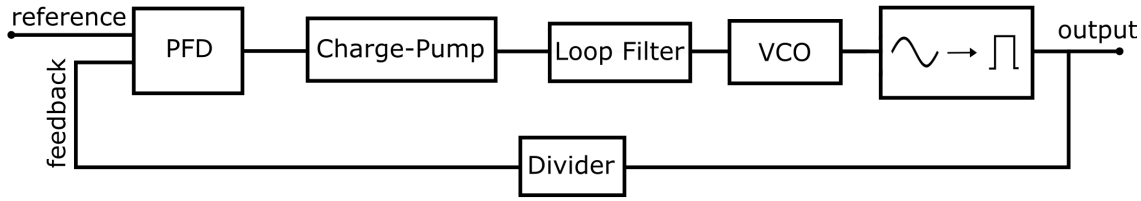


Figure 5.1: System Level Phase-Locked Loop

The reference frequency was configured to 23.5 MHz, resulting in a target output frequency of

$$f_{\text{out}} = f_{\text{ref}} \times 256 = 6.017\,\text{GHz}.$$

For correct locking behavior, the PLL was operated with the first VCO, which covers the frequency range of 6–8.5 GHz. Within this range, the second-to-last band of the 32 available tuning bands was selected. This configuration was required because the implemented PLL lacks an automatic band-selection circuit capable of detecting when the control voltage V_{ctrl} approaches the edge of a band and subsequently switching to an adjacent band.

The transient simulation was performed over a duration of 30 µs in order to capture the complete steady-state behavior of the PLL. This time window was chosen to ensure that all loop dynamics—specifically lock acquisition, stabilization of the control voltage, and suppression of transient effects—were fully observable. Furthermore, the chosen duration provides a sufficient margin for the system to achieve stable steady-state operation.

5.1 Simulation Results

The final transient simulation results are shown below. The critical PLL metric—the control voltage—reaches steady-state (locked condition) at approximately 26 µs, with a voltage ripple of just 2.94 mV (less than 3 mV). Achieving this low ripple required significantly enlarging the loop filter capacitors.

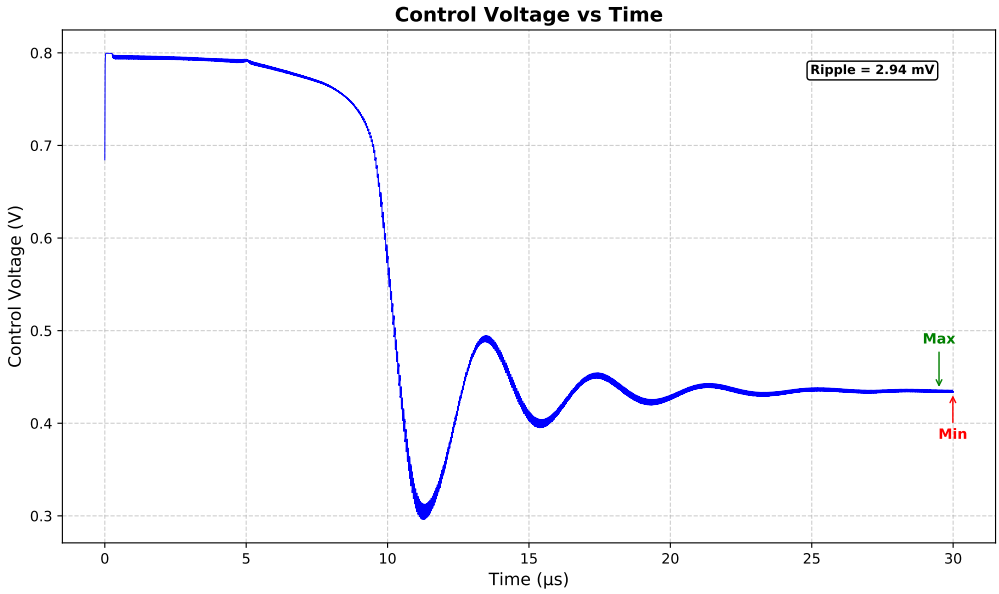


Figure 5.2: Control Voltage u_{ctrl}

Next, the steady-state phase error is assessed. The phase difference between V_{ref} and V_{fdbck} is measured at 39.11°, which aligns closely with the theoretical calculation of $180/5 = 36$. The deviation is likely due to propagation delays in the D flip-flops and logic gates preceding the charge pump. If necessary, a phase-shifter circuit could correct this residual phase error.

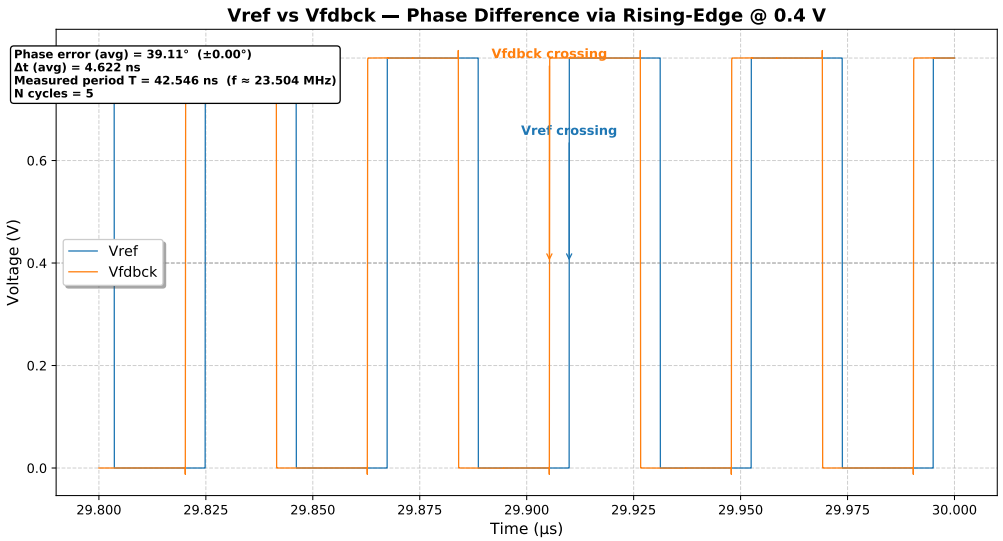


Figure 5.3: V_{ref} and V_{fdbck}

The RF amplifier output waveform is nearly rectangular, which suffices for digital logic: subsequent stages only need a clean rising edge to operate correctly.

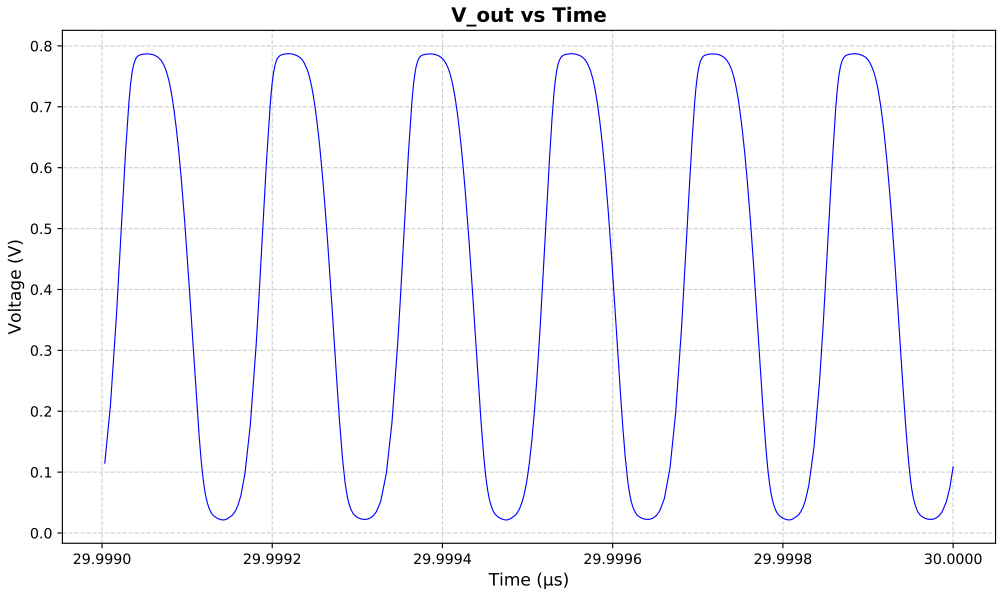


Figure 5.4: V_{ref} and V_{fdbck}

Finally, the output spectrum demonstrates the PLL's spectral purity. The first reference spur (at $2f_{ref}$) is suppressed by at least 31.38 dB below the carrier—well within design targets. However, the second reference spur (at $3f_{ref}$) has relatively lower suppression at only 17.81 dB.

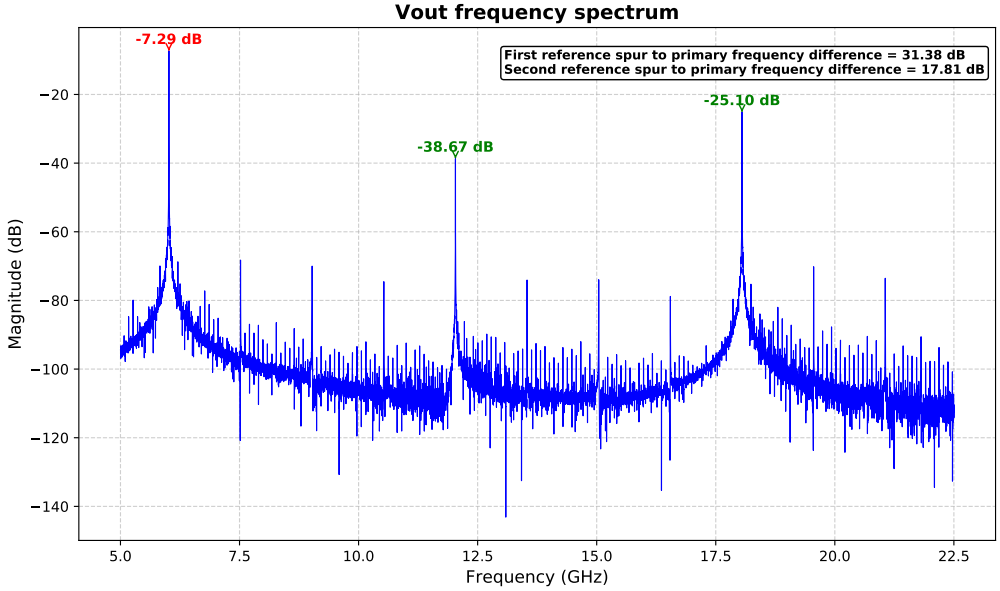


Figure 5.5: Output spectrum of PLL

While adding loop filter components can sometimes further attenuate higher-order spurs, it's important to understand how loop filters affect spurious tones: the filter attenuates disturbances above the loop bandwidth by approximately 40 dB per decade—this

applies to spurs whose frequency falls beyond the loop bandwidth. In other words, increasing attenuation for the $3f_{ref}$ spur would require extending the loop filter's bandwidth or increasing attenuation in that frequency range. However, this comes at the cost of increased phase noise or other trade-offs.

To suppress higher-order spurs more effectively without compromising loop stability or noise performance, more advanced techniques can be considered—such as a sampled-loop filter, oversampling, or other reference-spur reduction architectures. These can significantly reduce spurs without heavily impacting loop dynamics ([4], [5]).

Overall, the PLL meets its primary design goals in terms of stability, lock time, phase error, and spectral quality, validating the robustness of the implemented architecture.

Chapter 6

Conclusion and future work

This thesis has presented the design, implementation, and evaluation of a Phase-Locked Loop (PLL) operating in the 6–8.5 GHz frequency range. The motivation for this work arises from the growing demand for precise frequency synthesis and signal synchronization in modern communication and high-frequency systems. Beginning with the fundamentals of PLLs and progressing toward practical simulation results, this study has addressed both the theoretical foundations and the practical challenges involved in realizing a robust design.

The contributions of this work are multifaceted. A comprehensive examination of the PLL's core building blocks—the phase detector, charge pump, loop filter, voltage-controlled oscillator (VCO), and divider—was carried out with emphasis on their interdependencies. Particular attention was devoted to the loop filter, where capacitor sizing proved to be critical in minimizing ripple on the control voltage. The final design achieved a stable steady-state control voltage with a ripple of approximately 3 mV (measured 2.94 mV) and a lock time of about 26 µs, thereby validating the importance of careful filter design in overall PLL performance.

In addition, the analysis of the reference and feedback signals revealed a steady-state phase error of approximately 39.11°. Although slightly higher than the theoretical 36°, this deviation was consistent across simulations and is attributed to propagation delays in the flip-flops and logic gates preceding the charge pump. The stability of this error suggests that it could be effectively compensated by incorporating a dedicated phase-shifting circuit. Furthermore, the charge pump current behavior confirmed correct operation, with the UP branch momentarily activated each cycle to balance offset currents and maintain loop stability.

The spectral performance of the PLL was also evaluated, and the results demonstrated satisfactory signal purity. Reference spurs at $2f_{\text{ref}}$ were suppressed by more than 31 dB, while those at $3f_{\text{ref}}$ were reduced by 17 dB, values that are acceptable for practical communication applications. Taken together, these results confirm that the PLL architecture developed in this work successfully meets its primary design objectives: stability, fast lock time, controlled phase error, and adequate spectral cleanliness. The system not only demonstrates the feasibility of high-frequency PLL design in the 6–8.5 GHz range but also highlights the practical trade-offs that must be addressed in real-world implementations.

Beyond its technical findings, this thesis also serves as a broader reference for future students and engineers interested in PLL and RF circuit design. The methodology employed—combining theoretical analysis, iterative design through simulation, and careful interpretation of results—offers a structured framework that can be extended to other high-frequency circuit design problems. The insights gained here, particularly regarding

loop filter optimization and phase error analysis, are directly applicable to a wide variety of communication and instrumentation systems.

Although the present design achieves its intended objectives, several opportunities for improvement and extension remain. Possible directions for future work include:

1. **Completion of the physical layout.** The next logical step toward practical implementation is to finalize the full physical layout of the PLL. This includes careful routing of interconnects, minimization of parasitics, and verification through post-layout extraction and simulation. A completed layout would enable fabrication and real silicon testing, thereby validating the design beyond simulation.

2. **Development of an automatic band-selection circuit.** The VCO tuning range in this work is constrained by the control voltage V_{ctrl}. Designing an automatic band-selection mechanism would allow the circuit to detect when V_{ctrl} approaches its limits and automatically switch frequency bands. This would improve reliability across process, voltage, and temperature variations, and extend the usable frequency range.

3. **Integration of an RF switch.** An on-chip RF switch could be added to enable seamless selection between the two VCOs considered in this work [6]. Such integration would not only simplify system-level design but also enhance versatility in multi-band communication systems where dynamic frequency reconfiguration is required.

4. **Incorporation of a programmable prescaler.** Currently, the divider in the feedback path supports only fixed integer division ratios. A programmable prescaler enabling fractional-N division would significantly expand the flexibility of the PLL, allowing finer frequency resolution and enabling its use in applications that demand precise channel spacing [7].

5. **Implementation of a bandgap reference circuit.** The biasing circuitry in this design could be further improved by integrating a bandgap reference. Such a circuit would provide stable and predictable bias currents across variations in temperature and manufacturing process, ensuring more consistent performance of the PLL over a wide operating range [8].

6. **Integration of a phase shifter.** A steady-state phase error of approximately 39.11° was observed in this work, slightly higher than the theoretical prediction. Incorporating a phase shifter into the feedback path could effectively cancel this error, improving synchronization accuracy and reducing spurious tones associated with phase misalignment [9].

7. **Design and integration of a crystal oscillator.** While the present design assumes an external reference, a more self-contained architecture could be achieved by designing and integrating a crystal oscillator. This addition would provide a stable and low-jitter reference source, enabling the PLL to operate as a standalone frequency synthesizer.

8. **Further optimization of the VCO and loop dynamics.** The performance of the VCO remains a key determinant of the overall PLL characteristics. Future efforts could focus on lowering phase noise and improving spectral purity through

careful transistor-level optimization. More advanced techniques, such as sampled-loop filters, oversampling strategies, or adaptive biasing, could also be implemented to suppress higher-order spursbuilding on work such as [5] and [4].

In summary, this thesis has demonstrated the feasibility of designing a high-frequency PLL in the 6–8.5 GHz range and has highlighted both the opportunities and challenges associated with such an endeavor. The results confirm that the design meets its primary objectives while also pointing toward clear directions for future research. By addressing the outlined extensions and optimizations, future work can further improve performance, robustness, and applicability, ultimately contributing to the development of more advanced PLL architectures and continued innovation in RF system design.

Chapter 7

Appendix

7.1 D Flip-Flop (DFF)

A D flip-flop, also known as a "data" or "delay" flip-flop, is a fundamental digital memory element used to store a single bit of data. It has one data input (D), a clock input (CLK), and two outputs: Q and its complement Q'. The D flip-flop operates synchronously, meaning it samples and stores the input value only on a specific clock edge (usually the rising edge). When the clock signal is low, the flip-flop holds its previous state and ignores any changes at the D input. When the clock signal transitions to high, the flip-flop captures the value present at D and updates the Q output accordingly:

- If D = 0, then Q will be set to 0.
- If D = 1, then Q will be set to 1.

The complementary output Q' always holds the inverse of Q: if Q = 1, then Q' = 0, and vice versa.

The behavior of the D flip-flop can be summarized in the truth table below, which shows the relationship between the clock, the D input, and the outputs Q and Q':

Clock	**D**	$\mathbf{Q}_{\text{next}}$	$\mathbf{Q}'_{\text{next}}$
Rising edge	0	0	1
Rising edge	1	1	0
No clock edge	X	Q_{current}	Q'_{current}

Table 7.1: Truth table of the D Flip-Flop

Note that some flip-flops can be asynchronous, responding to inputs without a clock, but the D flip-flop used in PLL circuits is typically synchronous to ensure timing precision.

7.2 NAND Gate

The NAND gate performs the NAND (NOT AND) operation on two or more binary inputs and produces a binary output. It can be thought of as a combination of an AND gate followed by a NOT gate. The output of a NAND gate is low (0) only when all its inputs are high (1); otherwise, the output is high (1).

In Boolean terms, a NAND gate returns:

- 1, if any of the inputs is 0 (or any combination where not all inputs are 1).

- 0, only if all inputs are 1.

Specially, 2-Input NAND Gate has two inputs and one output. With two inputs, there are 2^2=4 possible input combinations. The truth table and logic symbol for the 2-input NAND gate are shown below.

Input A	Input B	Output (A NAND B)
0	0	1
0	1	1
1	0	1
1	1	0

Table 7.2: Truth table of 2-Input NAND Gate

7.3 Inverter

The NOT gate is one of the main building blocks of Digital Logic Circuits. A NOT Gate, also called an inverter, has only one input and one output. The output of the NOT gate is logic 0 when its input is logic 1 and the output is logic 1 when its input is logic 0. Thus, the output is always the complement of its input.

In most modern digital designs, the inverter is implemented using CMOS technology. A CMOS inverter consists of two types of transistors: a PMOS transistor connected to the positive supply voltage (V_{DD}) and an NMOS transistor connected to ground. The input signal controls both transistors simultaneously:

- When the input is low (0), the PMOS transistor turns on (conducts), and the NMOS transistor turns off (non-conducting). This connects the output to V_{DD}, producing a high output (1).
- When the input is high (1), the PMOS transistor turns off, and the NMOS transistor turns on. This connects the output to ground, producing a low output (0).

This complementary action ensures that the inverter consumes very little static power, only drawing significant current during switching transitions.

Drive Strength and Inverter Sizes

Inverters come in different sizes, labeled as ×1, ×2, ×4, ×8, etc. These indicate the drive strength of the inverter — essentially how much current it can provide to charge or discharge the load capacitance quickly:

- A ×1 inverter is the baseline size with minimum drive strength.
- A ×2 inverter is roughly twice as strong, capable of driving twice the load faster.
- Larger sizes like ×4 or ×8 provide even greater drive strength but at the cost of more silicon area and power consumption.

Selecting the appropriate inverter size is a balance between speed, power, and area requirements in the circuit design.

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