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Design and implementation of a low noise Phase Locked Loop (PLL) for 10-15 GHz applications using a 22 nm CMOS FD-SOI

DIPLOMA THESIS

of

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ΕΘΝΙΚΟ ΜΕΤΣΟΒΙΟ ΠΟΛΥΤΕΧΝΕΙΟ
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Σχεδίαση και υλοποίηση βρόχου κλειδώματος φάσης χαμηλού θορύβου για εφαρμογές συχνοτήτων 10-15 GHz σε τεχνολογία 22 nm CMOS FD-SOI

ΔΙΠΛΩΜΑΤΙΚΗ ΕΡΓΑΣΙΑ

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Περίληψη

Η παρούσα διπλωματική εργασία παρουσιάζει τη σχεδίαση και την υλοποίηση ενός βρόχου κλειδώματος φάσης χαμηλού θορύβου που λειτουργεί σε συχνότητες 10-15 GHz. Ο βρόχος σχεδιάστηκε χρησιμοποιώντας το PDK της τεχνολογίας 22nm CMOS FD-SOI της Global Foundries, η οποία υπόσχεται υψηλή απόδοση με μειωμένη κατανάλωση ισχύος. Η διαδικασία σχεδίασης περιλάμβανε την σχεδίαση σε επίπεδο σχηματικού, την μερική φυσική σχεδίαση της διάταξης (layout) και την επαλήθευση ορθής λειτουργίας σε συγκεκριμένα υποκυκλώματα του βρόχου. Η ροή της σχεδίασης παρουσιάζεται και συνοδεύεται από θεωρητικό υπόβαθρο, αποτελέσματα προσομοιώσεων, ενδιάμεσες σχεδιαστικές επιλογές, σχόλια για την απόδοση, με στόχο η παρούσα διπλωματική εργασία να μπορεί να αποτελέσει πολύτιμο βοήθημα για μελλοντικούς φοιτητές που ασχολούνται με τον σχεδιασμό βρόχων κλειδώματος φάσης. Η εργασία γράφτηκε στα Αγγλικά με στόχο να μπορεί να αξιοποιηθεί από μεγαλύτερο κοινό. Εκτεταμένη περίληψή της στα Ελληνικά παρατίθεται στη συνέχεια.

Λέξεις κλειδιά: Βρόχος Κλειδώματος Φάσης (PLL), Σχεδίαση Ολοκληρωμένων Κυκλωμάτων, Ολοκληρωμένα Κυκλώματα CMOS, Ενισχυτές Υψηλών Συχνοτήτων, Θόρυβος Φάσης

Abstract

This thesis presents the design and implementation of a low-noise phase-locked loop (PLL) operating in the 10-15 GHz frequency range. The loop was designed using the PDK of GlobalFoundries' 22nm CMOS FD-SOI technology, which offers high performance with reduced power consumption. The design process included schematic-level design, partial physical layout implementation, and functional verification of specific subcircuits within the loop. The design flow is presented along with the theoretical background, simulation results, intermediate design decisions, and performance commentary, with the aim of making this thesis a valuable resource for future students working on PLL design. The thesis is written in English to make it accessible to a broader audience. An extended summary in Greek follows.

Keywords: Phase-Locked Loop (PLL), Integrated Circuit Design, CMOS Integrated Circuits, High-Frequency Amplifiers, Phase Noise

Ευχαριστίες

Αρχικά, θα ήθελα να ευχαριστήσω τον επιβλέποντα καθηγητή μου, τον κύριο Παναγόπουλο, για την ευκαιρία που μου έδωσε να δουλέψω σε αυτό το έργο καθώς και στην καθοδήγηση και υποστήριξη σε αυτήν την πορεία της εργασίας και γενικότερα στη φοιτητική μου ζωή.

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Κεφάλαιο 1

Εκτεταμένη περίληψη στα Ελληνικά

Η παρούσα διπλωματική εργασία ασχολείται με τον σχεδιασμό, την υλοποίηση και την προσομοίωση ενός βρόχου κλειδώματος φάσης (Phase-Locked Loop - PLL) στη ζώνη συχνοτήτων 10-15 GHz. Τα PLL αποτελούν θεμελιώδη δομικά στοιχεία στα σύγχρονα ηλεκτρονικά συστήματα, καθώς επιτρέπουν τον συγχρονισμό σήματος, τη σύνθεση συχνοτήτων και την ανάκτηση φάσης/χρόνου σε εφαρμογές επικοινωνιών, ελέγχου και επεξεργασίας σήματος. Η επιλογή της συγκεκριμένης ζώνης συχνοτήτων δεν είναι τυχαία: το φάσμα 10-15 GHz χρησιμοποιείται εκτενώς σε δορυφορικές επικοινωνίες (Ku-band), ασύρματα δίκτυα οπισθόζευξης (backhaul) για τα σύγχρονα κυψελωτά συστήματα όπως το 5G, καθώς και σε εφαρμογές τηλεπισκόπησης και βιομηχανικών ραντάρ.

Η εργασία ξεκινά με μία αναλυτική παρουσίαση των βασικών αρχών λειτουργίας των PLL και των κύριων υποσυστημάτων τους: διαιρέτης συχνότητας, ανιχνευτής φάσης, αντλία φορτίου, ταλαντωτής ελεγχόμενος από τάση (VCO) και φίλτρο βρόχου. Ιδιαίτερη έμφαση δόθηκε στον ρόλο του φίλτρου βρόχου, καθώς η σωστή επιλογή παραμέτρων καθορίζει τη σταθερότητα του συστήματος, τον χρόνο κλειδώματος και την απόρριψη θορύβου. Στο πλαίσιο της σχεδίασης μελετήθηκαν οι θεωρητικές αρχές αλλά και οι πρακτικοί περιορισμοί που εμφανίζονται σε ολοκληρωμένα κυκλώματα υψηλών συχνοτήτων.

Ο ανιχνευτής φάσης σχεδιάστηκε με βάση μια κλασική τοπολογία. Ιδιαίτερη έμφαση δόθηκε στις λογικές πύλες που οδηγούν την έξοδό του για καλύτερη οδήγηση σημάτων για την αντλία φορτίου.

Η αντλία φορτίου σχεδιάστηκε με βάση αντιστάσεις και ρεύματα αντιστάθμισης. Παρουσίασε την αναμενόμενη συμπεριφορά: το ρεύμα του κλάδου UP ενεργοποιείται στιγμιαία σε κάθε περίοδο για να διατηρείται σταθερή η τάση ελέγχου, ενώ το υπόλοιπο μισό κύκλου κυριαρχείται από αρνητικό ρεύμα αντιστάθμισης. Το τελικό σήμα εξόδου του VCO ήταν σχεδόν ορθογώνιο, πλήρως επαρκές για τροφοδοσία ψηφιακών κυκλωμάτων, όπου το ζητούμενο είναι καθαρή ακμή ανόδου. Η φασματική ανάλυση της εξόδου επιβεβαίωσε την καθαρότητα του σήματος, με τις ανεπιθύμητες αρμονικές (reference spurs) να κατασταλούν τουλάχιστον κατά 25.6 dB κάτω από τον φορέα, εντός των αποδεκτών ορίων για τις εφαρμογές.

Για τον ταλαντωτή ελεγχόμενο από φάση (VCO) σχεδιάστηκε μετά από ανάλυση θορύβου και επιλογή αριθμού 32άδων μπαντών (band sections). Δόθηκε ιδιαίτερη σημασία στη διαστασιολόγηση των διακοπτών που χρησιμοποιήθηκαν για διατήρηση υψηλού συντελεστή ποιότητας Q. Η επικάλυψη μεταξύ διαδοχικών μπαντών διατηρήθηκε σε ποσοστό μεγαλύτερο του 15% και ο θόρυβος φάσης λιγότερο από -87 dBc/Hz στο 1 MHz offset.

Μέσω εκτεταμένων προσομοιώσεων παρουσιάζονται τα τελικά αποτελέσματα. Το σήμα

ελέγχου (v_{ctrl}) εμφάνισε σταθερή συμπεριφορά με χρόνο κλειδώματος περίπου 17 μs και κυμάτωση της τάξης των 3 μ΄, γεγονός που επετεύχθη με κατάλληλη διόρθωση των παραμέτρων του φίλτρου. Η ανάλυση των σημάτων αναφοράς (V_{ref}) και ανάδρασης ($V_{feedback}$) κατέδειξε την ύπαρξη μόνιμου σφάλματος φάσης περίπου 28.65°, το οποίο παρότι υπερβαίνει την θεωρητική τιμή 25.71°, αποδείχθηκε σταθερό και επαναλαμβανόμενο μεταξύ διαφορετικών προσομοιώσεων. Η απόκλιση αυτή αποδίδεται σε καθυστερήσεις διάδοσης των flip-flops και των λογικών πυλών πριν την αντλία φορτίου, ενώ μπορεί να διορθωθεί με την ενσωμάτωση ενός πρόσθετου κυκλώματος μετατόπισης φάσης.

Συνολικά, τα αποτελέσματα αποδεικνύουν ότι η σχεδίαση πληροί τους βασικούς στόχους: σταθερότητα, μικρό χρόνο κλειδώματος, περιορισμένο σφάλμα φάσης και καθαρή φασματική απόδοση. Η εργασία επομένως καταδεικνύει τη σκοπιμότητα σχεδίασης PLL στη ζώνη 10-15 GHz, με παράλληλη ανάδειξη των πρακτικών περιορισμών που εμφανίζονται σε συστήματα υψηλών συχνοτήτων. Επιπλέον, η μεθοδολογία που ακολουθήθηκε — θεωρητική ανάλυση, επαναληπτική σχεδίαση μέσω προσομοιώσεων και συστηματική αξιολόγηση αποτελεσμάτων — αποτελεί χρήσιμο πλαίσιο αναφοράς για μελλοντικούς φοιτητές και μηχανικούς που θα ασχοληθούν με σχεδίαση PLL και RF κυκλωμάτων.

Chapter 2

Introduction

2.1 Telecommunication

Communication systems are one of the fundamental pillars of Electrical Engineering, making it possible to convey information at distance with speed, accuracy, and dependability. From the analog telephony era to the era of 5G and beyond, communications as a engineering field have evolved extremely rapidly — speeding up the global interconnectedness that we take for granted in virtually every part of modern life.

Essentially, communication engineering is the process of sending and receiving signals, voice, data, video, or control messages. It encompasses a wide variety of technologies including modulation techniques, signal processing, information theory, antenna design, and digital communication protocols. These all coalesce to provide the wireless networks, fiber-optic networks, satellite connections, and Internet of Things (IoT) that define contemporary technology.

It is the work of electrical engineers to build and maintain the infrastructure that supports global communication in our more digital age. Whether it's developing low-latency networks for self-driving cars, building resilient wireless sensor networks for smart cities, or optimizing data transfer in cloud computing, communication engineering is at the forefront of innovation. It allows businesses to operate across continents, supports life-critical services like emergency services and telemedicine, and allows streaming and sharing of data effortlessly that we often take for granted.

Furthermore, the future of communications continues to challenge engineers with difficult demands: higher data rates, lower power consumption, more spectral efficiency, and higher security. Emerging technologies such as millimeter-wave systems, massive MIMO, quantum communications, and machine learning-based signal processing are reshaping what is achievable — pushing the boundaries of how we communicate.

In short, communication is not a discipline of Electrical Engineering but a fast-moving and essential field that fuels global information exchange. Increased reliance on speedy, secure, and trustworthy communication heightens the need for creative engineering solutions to address the demand.

2.2 The necessity for phase locked loops

Phase-Locked Loops (PLLs) are essential building blocks in modern electronic systems, common to communication, control, and signal processing applications. In principle, PLLs

are feedback control systems that lock the phase and frequency of an output signal onto that of a specified reference signal. Despite their relatively simple conceptual basis—a phase detector, low-pass filter, and voltage-controlled oscillator—their functionality is very powerful and versatile.

The need for PLLs is created by the universal requirement for signal synchronization in both the analog and digital worlds. In communications systems, PLLs facilitate the recovery of clock information from data streams so that data can be recovered and timed correctly. Without PLLs, systems such as Ethernet, USB, and newer wireless standards like LTE and 5G would experience timing mismatches and reduced performance. For instance, in frequency synthesis, PLLs create a large number of frequencies from a stable crystal oscillator reference, which in RF transmitters and receivers allows for channel spacing and tuning flexibility.

PLLs also play a critical role in clock generation and distribution within digital systems. Microprocessors, FPGAs, and SoCs use PLLs to generate high-frequency internal clocks from lower-frequency crystal references. These clocks support billions of operations per second, and their accuracy and stability directly impact the system's performance. Additionally, in phase modulation and demodulation methods (e.g., FM or PSK), PLLs are employed to track and recover the modulated carrier, facilitating precise signal demodulation. Aside from communications, PLLs have important applications in motor control systems, radar systems, and instrumentation. In motor drives, for example, PLLs lock the drive control signals to the rotor position, enhancing efficiency and dynamic performance. In radar systems, PLLs stabilize local oscillators for coherent signal processing, which is essential to obtain accurate range and velocity measurements.

2.3 The 10-15 GHz frequency range and its applications

The 10–15 GHz frequency band, situated in the microwave region of the electromagnetic spectrum, plays a critical role in numerous non-military applications within electrical engineering. Its propagation characteristics and ability to support high-bandwidth communication make it especially valuable in commercial, industrial, and scientific domains. One of the primary uses of this band is in satellite communications, particularly in the Ku-band (12–14 GHz), where it enables direct-to-home (DTH) television, VSAT networks, and in-flight connectivity services. Additionally, this frequency range supports wireless backhaul links for modern cellular networks, including 5G, offering high-capacity, line-of-sight communication between base stations. In the field of remote sensing, systems like Synthetic Aperture Radar (SAR) exploit the 10–12 GHz region (X-band) for high-resolution Earth observation, contributing to environmental monitoring, agriculture, and disaster management. Furthermore, industrial radar sensors operating in this range are employed for level measurement, speed detection, and material characterization. The continued advancement of microwave circuit design, low-noise amplifiers, and compact antenna systems is expanding the scope of 10–15 GHz applications, making this band increasingly important in the design of high-frequency systems in electrical engineering.

Chapter 3

Phase Locked Loop Kinds

A phase-locked loop (PLL) is a control system that generates an output signal whose phase is fixed relative to the phase of an input signal. A PLL can also track an input frequency. Moreover, incorporating a frequency divider in the design, a PLL can generate a stable frequency that is a multiple of the input frequency. There are various kinds of PLLs, each with its own advantages and disadvantages. A basic PLL configuration is shown in Figure 3.1.

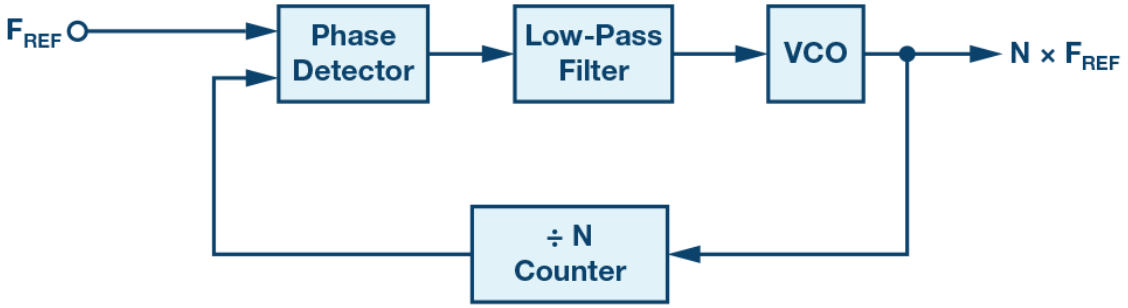

Figure 3.1: Basic PLL configuration

A basic PLL consists of three main components: a phase detector, a low-pass filter, a voltage-controlled oscillator (VCO), and a feedback loop with a divider. The phase detector compares the phase of the input signal with the phase of the output signal from the divider. The low-pass filter smooths the output of the phase detector, and the VCO generates an output signal whose frequency is controlled by the filtered output.

3.1 All Digital Phase Locked Loop (ADPLL)

An all-digital Phase-Locked Loop (ADPLL) is a fully digital implementation of the traditional PLL architecture, replacing analog building blocks with their digital counterparts to improve scalability, programmability, and integration in modern CMOS processes. It typically comprises a Phase-to-Digital Converter (P2D), a digital loop filter, a digitally controlled oscillator (DCO), and a programmable frequency divider. The P2D measures the phase difference between the reference clock and the feedback clock, often using a conventional analog Phase Frequency Detector (PFD) in combination with a Time-to-Digital Converter (TDC) to achieve fine time resolution. The digital loop filter processes the phase

error signal to generate control words for the DCO, which adjusts its output frequency accordingly. It has the advantages of a small area, good portability and no charge pump. However, the system is more complex, and the in-band phase noise is worse than that of the analog PLL.

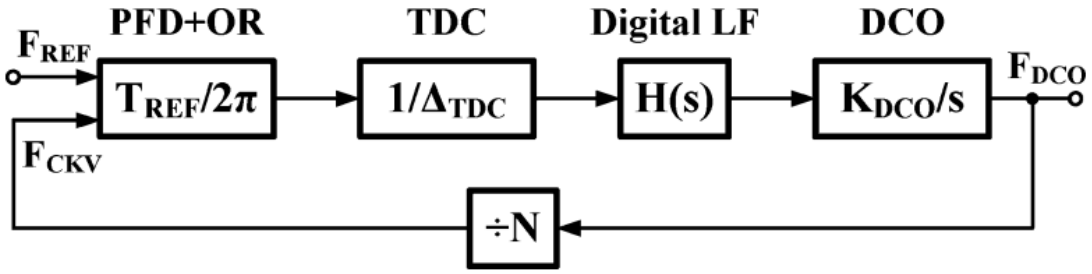

Figure 3.2: All Digital PLL configuration

3.2 Injection Locking Phase Locked Loop (ILPLL)

Injection-Locked Phase-Locked Loops (ILPLLs) are a specialized class of PLLs that exploit the phenomenon of injection locking to achieve frequency and phase synchronization with reduced power consumption and simplified loop architectures. In an ILPLL, the oscillator—often a ring oscillator or LC oscillator—is periodically perturbed by an injected signal at or near its natural frequency. This injected signal forces the oscillator to lock in phase and frequency to the reference, effectively suppressing phase noise and improving spectral purity. Compared to conventional PLLs, ILPLLs can achieve very fast locking times and low clock jitter because the injection process directly influences the oscillator phase without requiring a high loop bandwidth. These properties make ILPLLs particularly attractive for high-frequency and multi-GHz applications, such as clock generation in high-speed serial links, frequency multiplication, and wireless transceivers. However, ILPLLs typically have a narrower locking range than traditional PLLs, higher power consumption and are more sensitive to process, voltage, and temperature variations, which must be carefully considered during design.

3.3 Sub-Sampling Phase Locked Loop (SSPLL)

Sub-Sampling Phase-Locked Loops (SSPLLs) are a high-performance PLL architecture that directly samples the oscillator output using the reference clock, eliminating the need for a frequency divider in the feedback path. By operating the phase detector at the reference frequency instead of the divided VCO frequency, SSPLLs can achieve exceptionally low in-band phase noise and jitter, since the phase detection occurs before noise from the divider is introduced. This approach also allows for very high multiplication factors without degrading the phase noise performance, making SSPLLs ideal for applications such as high-speed data converters, RF transceivers, and high-performance clock generators. The sub-sampling technique inherently provides a wide tuning range and reduced power consumption compared to traditional architectures, although careful design of the sampling phase detector and loop filter is required to mitigate issues such as reference spur

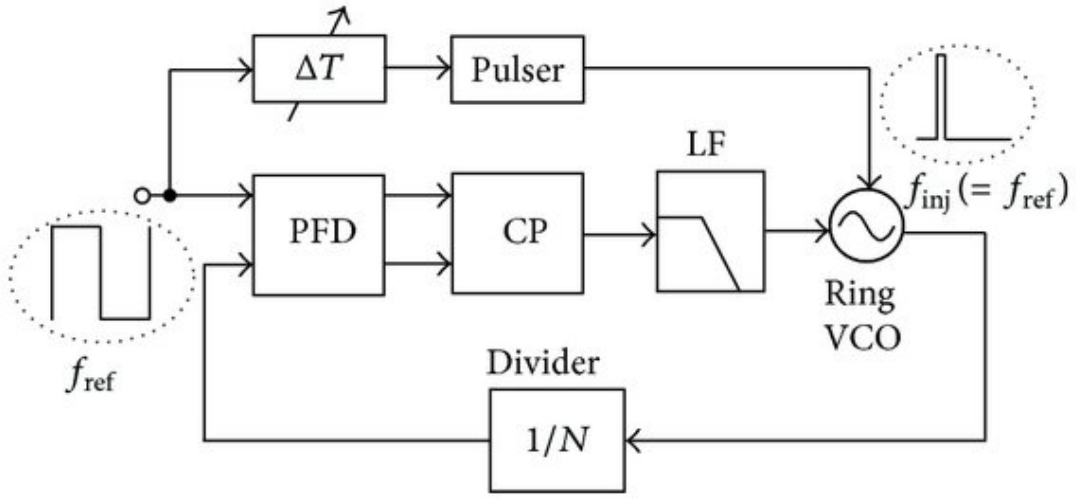

Figure 3.3: Injection Locked PLL configuration

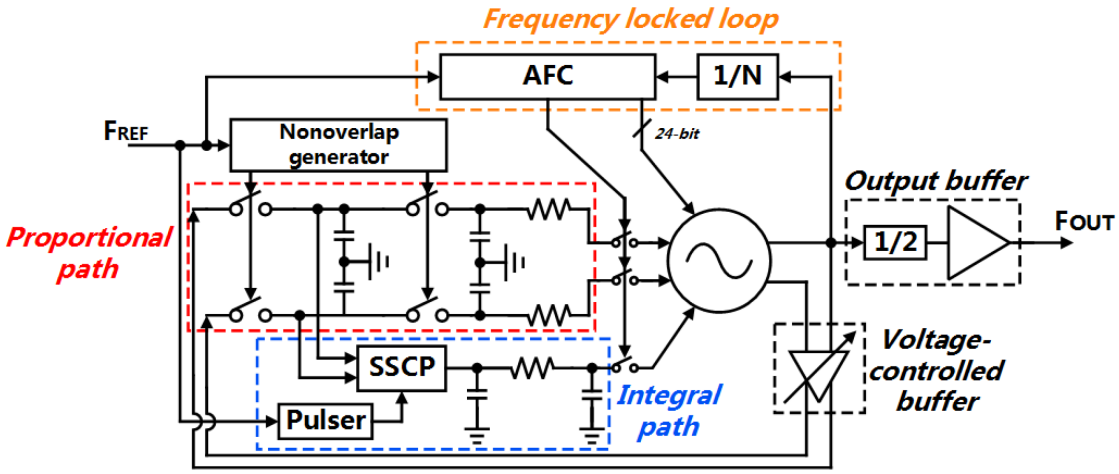

Figure 3.4: Sub-Sampling PLL configuration

generation and sensitivity to supply noise. With SSPLL, the phase noise performance is improved, but an additional frequency-locked loop (FLL) is needed

3.4 Charge Pump Phase Locked Loop (CPPLL)

Charge-Pump Phase-Locked Loops (CPPLLs) are one of the most widely used PLL architectures in modern communication and clock generation systems due to their ability to combine high precision with a relatively simple implementation. In a CPPLL, the phase-frequency detector (PFD) compares the phase and frequency of the reference signal with that of the divided VCO output. The PFD controls a charge pump, which sources or sinks current into a loop filter depending on whether the VCO is leading or lagging in phase or frequency. This current is converted into a control voltage by the loop filter, which then tunes the VCO frequency. The use of a charge pump allows the loop to op-

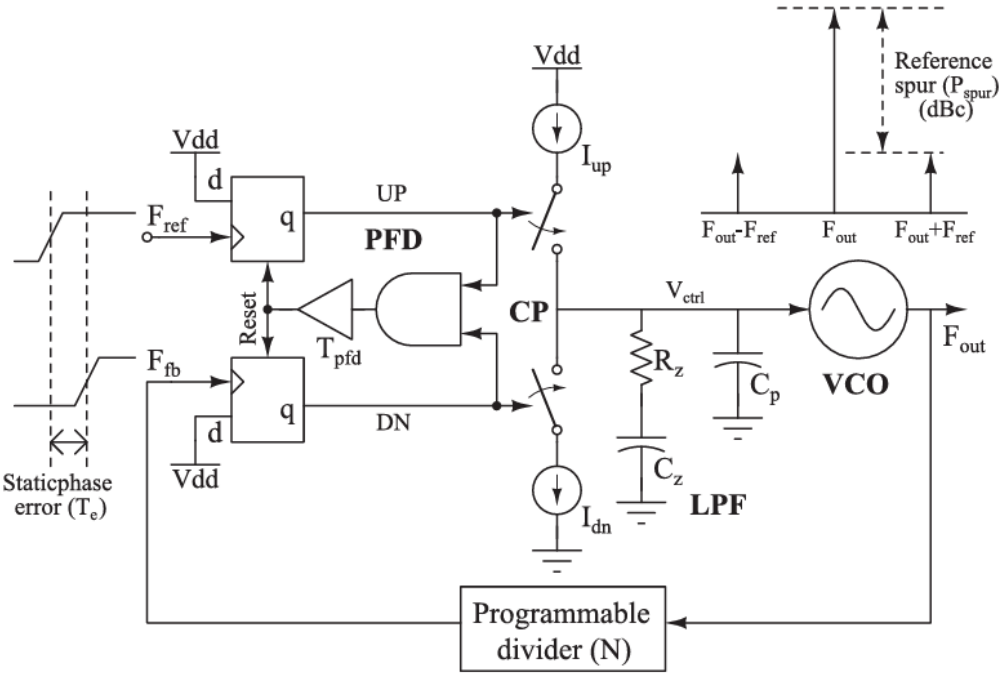

Figure 3.5: Charge Pump PLL configuration

erate with high gain and good linearity, resulting in improved lock time and phase noise performance. CPPLLs are commonly employed in frequency synthesizers, RF transceivers, microprocessors, and other systems where low jitter and high frequency stability are critical. However, careful design is required to minimize non-idealities such as charge pump current mismatch, PFD dead zone, and reference spurs, which can degrade spectral purity.

In this work, a Charge Pump PLL is designed and implemented because of its simplicity, stability, large tuning range and low rms jitter.

A Charge Pump PLL consists of a phase-frequency detector (PFD), a charge pump, a loop filter, a voltage-controlled oscillator (VCO) and a divider. The PFD compares the phase and frequency of the reference signal with that of the divided VCO output. The charge pump sources or sinks current into the loop filter depending on whether the VCO is leading or lagging in phase or frequency. The loop filter converts the current into a control voltage that tunes the VCO frequency.

Chapter 4

Frequency Divider

A frequency divider is a circuit that divides the frequency of an input signal by a specific integer or fractional factor. In phase-locked loop (PLL) systems, both integer and fractional dividers are employed.

Integer dividers are typically implemented using a combination of D-type flip-flops (DFFs) and logic gates (e.g., AND, OR) to achieve the desired division ratio. It is well established that a DFF, with its inverted output Q' short-circuited to its input D, functions as a divide-by-two circuit. By cascading multiple such stages and incorporating appropriate logic gating, any required integer division ratio can be realized.

Fractional dividers, on the other hand, alternate between dividing by k and k+1 in a specific sequence. By controlling the ratio of cycles spent at each division value, it is possible to achieve an average division factor between the two integers. This is generally accomplished using a cycle counter: the divider operates at k for a cycles and at k+1 for N-a cycles, producing an effective division ratio equal to the mean value. [1]

Fractional dividers provide greater flexibility in selecting the division ratio, allowing for trade-offs in loop bandwidth and locking speed. However, they are generally less area-efficient, consume more power, and introduce reference spurs due to abrupt changes in the division ratio.

In this work, an integer divider was selected due to its simplicity and its inherently lower reference spur generation. A division ratio of 512 was chosen based on the reference frequency provided by the crystal oscillator and the desired output frequency range of 10-15 GHz. This was implemented using nine cascaded divide-by-two DFF stages, as illustrated in Figure 4.1. The output of the divider is fed back to the phase-frequency detector (PFD) in the PLL.

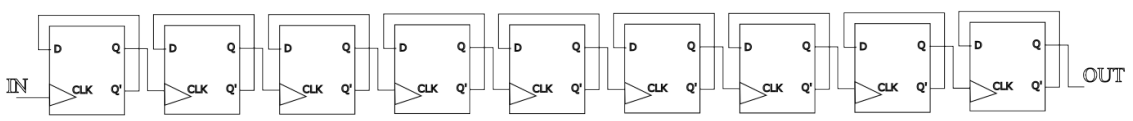

Figure 4.1: Frequency divider configuration

Chapter 5

Phase-Frequency Detector

A Phase Frequency Detector (PFD) is a circuit that compares both the phase and frequency of two input signals and generates outputs proportional to the detected differences. In the context of a PLL, the PFD typically compares the reference signal-most often derived from a crystal oscillator-with the feedback signal obtained after the frequency divider. The PFD output consists of pulses of varying durations, which are subsequently fed to the charge pump to either source or sink current. The most common and conventional PFD architecture employs D flip-flops (DFFs) in combination with logic gates, as illustrated in Figure 5.1.

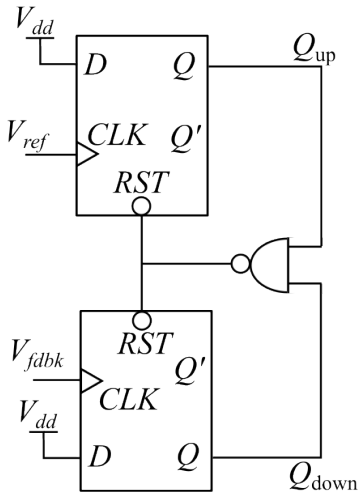

Figure 5.1: Phase-frequency detector configuration

In this implementation, the input **D** of each flip-flop is connected to the supply voltage (V_{DD}), while the clock input is driven by either the reference or the feedback signal. When one of the input signals rises, the corresponding DFF output is set to logic high. When the second signal rises, both DFF outputs become logic high. This causes the NAND gate to output logic low, which in turn resets both DFFs so that their outputs return to logic low.

For example, when both input signals have the same frequency but the reference signal leads in phase, the **UP** output (Q_{up}) will remain high for a time interval equal to the phase difference. Following this, both Q_{up} and Q_{dn} return to logic low due to the reset action. Because of the propagation delay of the NAND gate and the finite reset time of the DFFs,

there is a short interval during which both outputs are high, as depicted in Figure 5.2.

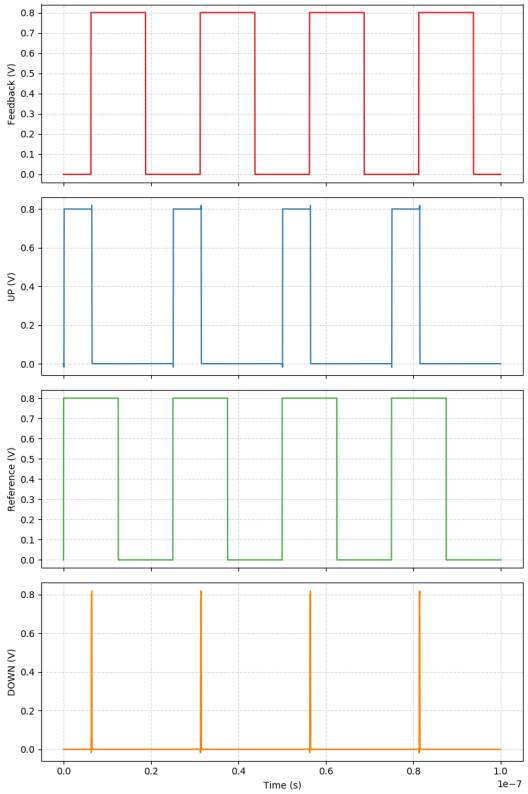

Figure 5.2: PFD output example 1

This phenomenon is referred to as the **dead zone**-a range in which the PFD does not respond to small phase differences. The dead zone should be minimized to reduce the steady-state phase error, but not eliminated entirely. If the generated pulses become too short, the charge pump switches may not turn on fully, which would reduce the effective gain of the PFD and increase jitter [2]. That's the reason in this implementation, inverters are added for a propagation delay. Furthermore, inverters are used to drive the output signals because of the large capacitance of the switches of the charge pump, as shown in Figure 5.3.

Another operating scenario occurs when the two input signals differ in frequency. Without loss of generality, if the reference frequency is higher than the feedback frequency, the width of the Q_{up} pulses will increase over time, while Q_{dn} remains low for the majority of the time, as shown in Figure 5.4.

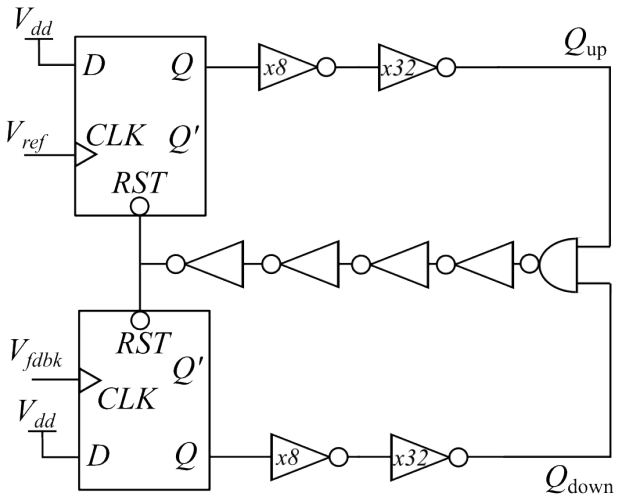

Figure 5.3: PFD design

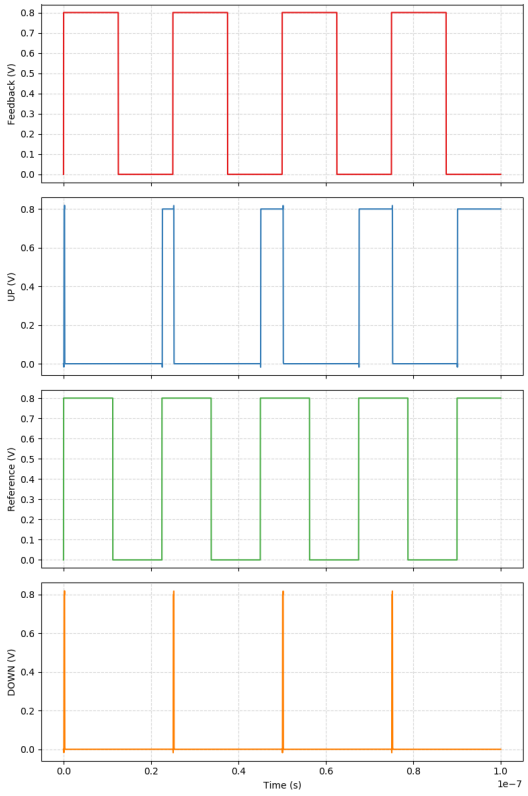

Figure 5.4: PFD output example 2

Chapter 6

Charge Pump

6.1 Basic Charge Pump Operation

A charge pump is a circuit that receives two pulse signals as inputs and, depending on their combination, either sources current, sinks current, or remains idle. It employs two switches and two current sources—one pair corresponding to each pulse (UP and DOWN). A simple implementation of the circuit is shown in Figure 6.1.

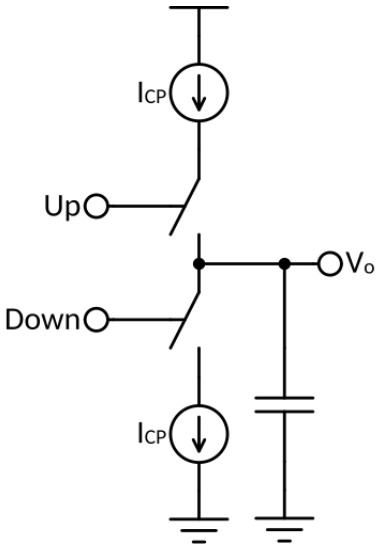

Figure 6.1: Charge pump configuration

The circuit operates according to the following four cases:

1. If the UP pulse is at a logical high level and the DOWN pulse is at a logical low level, only the upper switch is activated, and the charge pump sources current to the output node.
2. If the UP pulse is at a logical low level and the DOWN pulse is at a logical high level, only the lower switch is activated, and the charge pump sinks current from the output node.
3. If both pulses are at a logical low level, no current flows, and the output voltage remains unchanged.

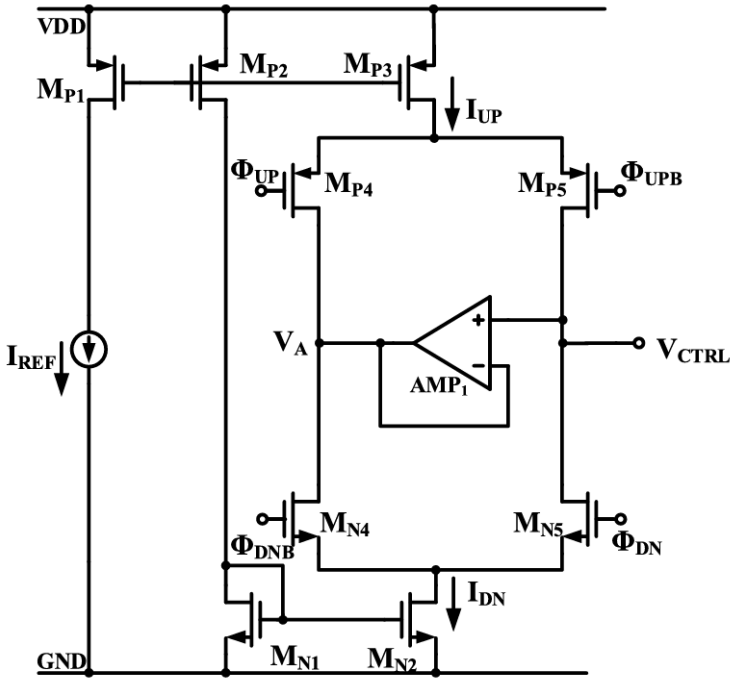

Figure 6.2: Traditional charge pump configuration

4. If both pulses are at a logical high level, current flows directly from the power supply to ground, but the output voltage remains unaffected.

In most implementations, a capacitor is connected from the output to ground immediately after the switches. This capacitor converts the pulsed current into a voltage and also acts as an integrator, helping the loop maintain a stable control voltage in steady state.

6.2 Traditional Charge Pump Architecture

For a more realistic circuit implementation, ideal current sources are replaced with current mirrors. Typically, a PMOS current mirror and an NMOS current mirror are used to replicate the same reference current for the sourcing and sinking branches of the charge pump. This, however, introduces the main design challenge of charge pumps: **current mismatch**. The traditional charge pump architecture is shown in Figure 6.2 [3].

A further refinement to the basic design is the use of an operational amplifier as a voltage follower between the sourcing and sinking branches. This configuration isolates the current sources from each other and ensures that their operation is largely independent of the output voltage. The op-amp maintains a fixed voltage at the drains of the current source transistors, keeping them in ideal saturation and improving current matching. Additionally, the op-amp reduces charge injection and clock feedthrough, thereby lowering output voltage ripple and reference spurs.

In such an implementation, the reference current can be generated by applying a bandgap reference voltage to the PMOS transistor M_{P1}. The resulting current is mirrored to M_{P3} to form the sourcing branch, and also mirrored through M_{N1} and M_{N2} to form the sinking branch. The central op-amp serves as a high-speed buffer, ensuring that V_a follows $V_{control}$ as quickly as required.

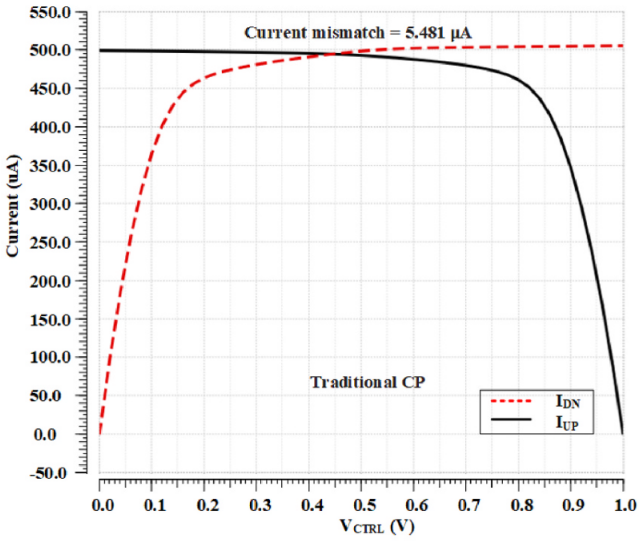

Figure 6.3: Charge pump current mismatch

The primary drawback of this architecture is current mismatch, illustrated in Figure 6.3. The mismatch follows the $I_D - V_{DS}$ characteristic of MOSFETs: when $V_{control}$ deviates from half the supply voltage, the sourcing and sinking currents become unequal, even with all transistors operating in saturation. In extreme cases, mismatch can reach up to 20%, introducing significant asymmetry that prolongs PLL lock time.

6.3 Resistive-Based Charge Pump Architecture

This issue can be mitigated by adopting a resistive-based charge pump architecture, as shown in Figure 6.4. In this design, instead of using current mirrors to enforce equal currents, a resistive reference and op-amp configuration generates the required currents. A bandgap reference voltage—provided by a circuit not implemented in this work—is applied in a negative feedback loop with an op-amp to set a reference current

$$I_{ref} = \frac{V_{ref}}{R_1}.$$

Two additional op-amps replicate the reference voltage across resistors R_4 and R_2 for the sourcing and sinking paths, respectively. Each op-amp, in conjunction with a transistor, ensures voltage stability across its respective resistor. The remainder of the circuit is identical to the traditional charge pump.

The central op-amp in this architecture must have high speed, high slew rate, and high gain (>60 dB) to ensure that V_a follows $V_{control}$ with minimal delay. It must also support rail-to-rail input and output operation to accommodate the full voltage range from ground to the supply voltage. The remaining three op-amps, used for DC biasing, do not require high speed but must be rail-to-rail and have sufficient gain (>40 dB) to maintain stable operation over the range of V_{ref} values.

Finally, transistors placed in series with the switches are employed to reduce reference spurs, mitigate charge sharing, and suppress clock feedthrough effects.

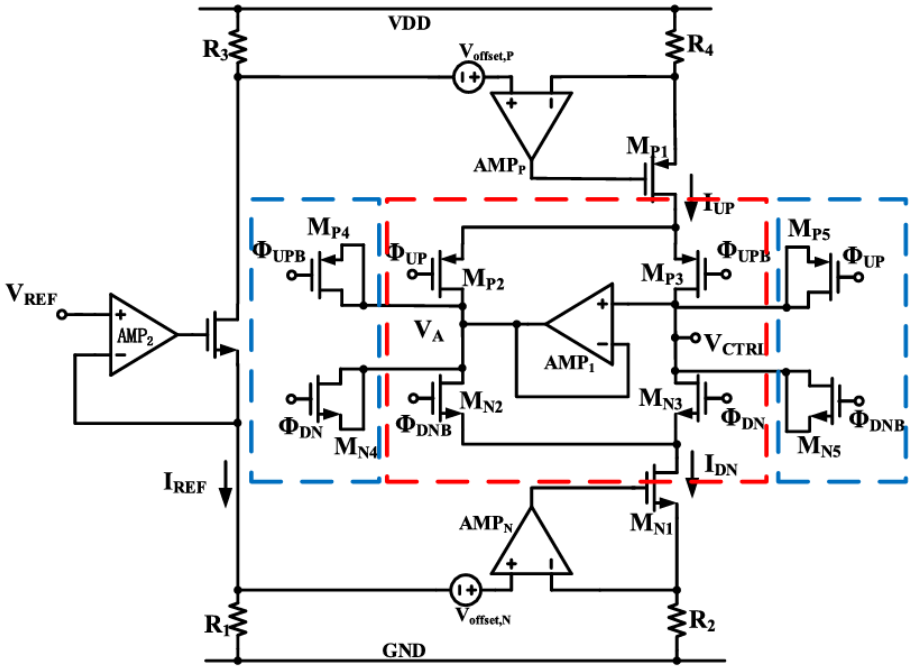

Figure 6.4: Resistive-based charge pump configuration

6.4 Current mismatch and reference spurs analysis

The reference spur in a PLL is strongly influenced by non-idealities of the charge pump (CP), including current mismatch, switching path delay, charge leakage, and other factors. These effects cause fluctuations in the VCO control voltage at the reference frequency, which translate into spurious tones around the VCO output frequency. Among these, the dominant contributor is typically the current mismatch between the charging and discharging paths of the CP. The resulting phase error Φ_{error} due to this mismatch is given by [4]:

$$\Phi_{\text{error}} = 2\pi \frac{t_{\text{on}}}{T_{\text{ref}}} \frac{\Delta I}{I_{\text{CP}}} \tag{6.1}$$

where T_{ref} is the reference signal period, t_{on} is the turn-on time of the PFD, I_{CP} is the nominal CP current, and ΔI is the current mismatch. For a traditional second-order CP-PLL, the reference spur P_{spur} due to this phase error is expressed as [5]:

$$P_{\text{spur}} = 20 \log \left(\frac{t_{\text{on}} \Delta I K_{\text{VCO}}}{4\pi \omega_{\text{ref}} C_2} \cdot \frac{k+1}{k} \right) \tag{6.2}$$

where K_{VCO} is the VCO gain, $k = C_1/C_2$ is the low-pass filter capacitor ratio, and ω_{ref} is the reference angular frequency. Reducing ΔI is therefore a direct means of suppressing the spur.

In the conventional CP architecture (Fig. 6.2), the charging current I_{UP} is obtained by mirroring the reference current I_{REF} once, while the discharging current I_{DN} is obtained via two cascaded current mirrors. This asymmetry makes the design more sensitive to process variations, increasing mismatch. Considering process mismatches, the charging

current can be expressed as [5]:

$$I_{\mathrm{UP}} = \left(1 \pm \frac{2\Delta V_{\mathrm{THP}}}{V_{\mathrm{GSP}} - V_{\mathrm{THP}}}\right) I_{\mathrm{REF}} \tag{6.3}$$

Similarly, the discharging current is:

$$I_{\mathrm{DN}} = \left(1 \pm \frac{2\Delta V_{\mathrm{THP}}}{V_{\mathrm{GSP}} - V_{\mathrm{THP}}}\right)\left(1 \pm \frac{2\Delta V_{\mathrm{THN}}}{V_{\mathrm{GSN}} - V_{\mathrm{THN}}}\right) I_{\mathrm{REF}} \tag{6.4}$$

Assuming $V_{\mathrm{GSP}} = V_{\mathrm{GSN}} = V_{\mathrm{GS}}$ and $V_{\mathrm{THP}} = V_{\mathrm{THN}} = V_{\mathrm{TH}}$, the maximum mismatch becomes:

$$\Delta I = \left[\left(\frac{2\Delta V_{\mathrm{TH}}}{V_{\mathrm{GS}} - V_{\mathrm{TH}}}\right)^2 + 3\left(\frac{2\Delta V_{\mathrm{TH}}}{V_{\mathrm{GS}} - V_{\mathrm{TH}}}\right)\right] I_{\mathrm{REF}} \tag{6.5}$$

The resistance-based precise current replication CP (Fig. 6.4) reduces mismatch by mirroring I_{REF} only once for both I_{UP} and I_{DN}. The charging and discharging currents are:

$$I_{\mathrm{UP}} = I_{\mathrm{REF}} \pm \frac{V_{\mathrm{offset,P}}}{R_1} \tag{6.6}$$

$$I_{\mathrm{DN}} = I_{\mathrm{REF}} \pm \frac{V_{\mathrm{offset,N}}}{R_2} \tag{6.7}$$

If $V_{\mathrm{offset,P}} = V_{\mathrm{offset,N}} = V_{\mathrm{offset}}$ and $R_1 = R_2 = R$, the mismatch becomes:

$$\Delta I' = \frac{2V_{\mathrm{offset}}}{R} = \frac{2V_{\mathrm{offset}}}{V_R} I_{\mathrm{REF}} \tag{6.8}$$

where V_R is the voltage drop across the resistors. Assuming $V_{\mathrm{offset}} \approx \Delta V_{\mathrm{TH}}$ and $V_R = V_{\mathrm{DS}}$, and noting that in saturation $V_{\mathrm{DS}} > V_{\mathrm{GS}} - V_{\mathrm{TH}}$, it follows that:

$$\Delta I' < \Delta I \tag{6.9}$$

Thus, the resistive CP achieves lower mismatch, and consequently better reference spur suppression, especially when combined with low-offset operational amplifiers.

6.5 Phase Noise Analysis

The phase noise of a PLL can be categorized into *out-of-band* and *in-band* components. The out-of-band phase noise is mainly dominated by the intrinsic phase noise of the VCO, while the in-band phase noise originates from noise sources within the loop, primarily from the Phase-Frequency Detector (PFD) and the Charge Pump (CP).

The open-loop transfer function of a second-order charge pump PLL is given by [6]:

$$H_{\mathrm{open}}(s) = \frac{K_{\mathrm{PFD}} I_{\mathrm{CP}} K_{\mathrm{VCO}}}{2\pi N(C_1 + C_2)} \cdot \frac{1 + \frac{s}{\omega_z}}{s^2\left(1 + \frac{s}{\omega_p}\right)}, \tag{6.10}$$

where K_{PFD} is the gain of the PFD, I_{CP} is the charge and discharge current of the CP, N is the frequency division ratio of the divider, and ω_z and ω_p are the loop zero and nonzero pole frequencies, respectively.

When referred to the PLL output, the contribution of the CP to the output phase noise can be expressed as [6]:

$$L_{\mathrm{CP}} = \log_{10}\left(\frac{S_{i,\mathrm{CP,out}}}{2}\right) = \log_{10}\left[\frac{1}{2}\left(\frac{2\pi N}{K_{\mathrm{PFD}} I_{\mathrm{CP}}}\right)^2 S_{i,\mathrm{CP}}\right], \tag{6.11}$$

where $S_{i,\mathrm{CP}}$ denotes the current noise power spectral density of the CP.

From (6.11), it is clear that increasing both K_{PFD} and I_{CP} can effectively suppress the impact of CP noise at the PLL output. So, a design choice was made to have a high CP current equal to 500uA. The 22nm CMOS technology used in this work has large resistances. As a result, a low reference voltage of 0.1V and a resistor of 200Ohm was chosen to achieve this current without using too much area for parallel transistors.

6.6 Operational Amplifiers

6.6.1 DC biasing Operational Amplifiers

As described in Section 6.3, two types of operational amplifiers (op-amps) are employed in the proposed circuit. The DC biasing op-amps are required to exhibit high gain and rail-to-rail input/output capability. To meet these requirements, a conventional rail-to-rail op-amp architecture was implemented, as illustrated in Fig 6.5.

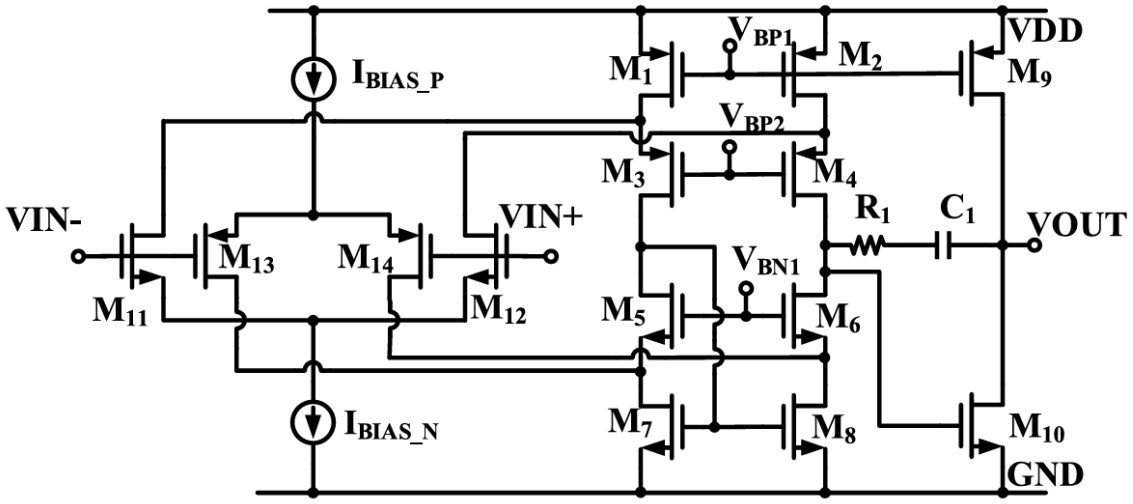

Figure 6.5: Operational amplifier architecture

This topology incorporates both PMOS and NMOS differential input pairs, operating within a folded cascode configuration. The two folded branches function as current steering paths. When the input common-mode voltage approaches the positive supply, the PMOS pair enters triode or cutoff mode, while the NMOS pair remains in saturation. Conversely, when the input common-mode voltage is near ground, the NMOS pair operates in triode or cutoff mode, and the PMOS pair remains in saturation. In the intermediate range, both input pairs operate in saturation. In all cases, at least one pair remains in saturation, ensuring first-stage amplification across the entire input range.

In the lower folded branch, a wide-swing current mirror is adopted due to the low supply voltage of 0.8 V, which must maintain four transistors in saturation simultaneously.

To facilitate this, all transistors in the folded branches are implemented using super-low threshold voltage (`slvt`) devices to minimize the V_{DS} required for saturation. Device dimensions were carefully optimized to guarantee saturation for all four transistors. The final sizing for all active devices is listed in Table 6.1. For the differential pairs, standard `nfet` and `pfet` devices are used, while simple current mirrors are employed for biasing.

The second gain stage employs a common-source configuration. This stage amplifies the signal only when transistor M_{10} operates in saturation, meaning the output voltage must exceed a specific threshold. As such, the output stage is not rail-to-rail, although this does not alter the preceding analysis. The node between M_4 and M_6 corresponds to the dominant pole of the amplifier, necessitating compensation to achieve a sufficiently high phase margin (PM). The values of R_1 and C_1 were determined by parametric analysis to ensure a phase margin exceeding 65°, and were set to 2.437 kΩ and 27.83 fF, respectively.

Table 6.1: Final sizing of the operational amplifier devices.

Device	**Width (μm)**	**Length (nm)**	**Fingers**	**Multiplier**	**Type**
M_1	3	40	15	4	SLVT
M_2	3	40	15	4	SLVT
M_3	3	40	15	4	SLVT
M_4	3	40	15	4	SLVT
M_5	0.6	40	3	3	SLVT
M_6	0.6	40	3	3	SLVT
M_7	0.6	40	3	3	SLVT
M_8	0.6	40	3	3	SLVT
M_9	3	40	15	4	SLVT
M_{10}	1.6	40	8	1	SLVT
M_{11}	1.28	20	8	2	RVT
M_{12}	1.28	20	8	2	RVT
M_{13}	1.28	20	8	2	RVT
M_{14}	1.28	20	8	2	RVT
R_1	0.36	3700	-	8 (series)	N+ Poly Silicided
C_1	2.36	2360	-	1	Apmom1v8

6.6.2 High-Speed Operational Amplifier

The main distinction between the DC biasing operational amplifiers and the high-speed operational amplifier lies in the output stage design. In the high-speed version, the output stage must be capable of sourcing the charge pump output current of 500 μA. To achieve this, the bias current of the last stage is set significantly higher than 500 μA, ensuring that all transistors remain in saturation while delivering the required output current.

To maintain a relatively small V_{GS} and respect the current limits, the transistors in the last stage are sized considerably larger than those in the DC biasing op-amps. This larger sizing reduces the overdrive voltage and improves linearity under high output current conditions. The complete schematic, including all biasing circuitry, is shown in Figure 6.6.

The final sizing for all transistors and passive components is summarized in Table 6.2.

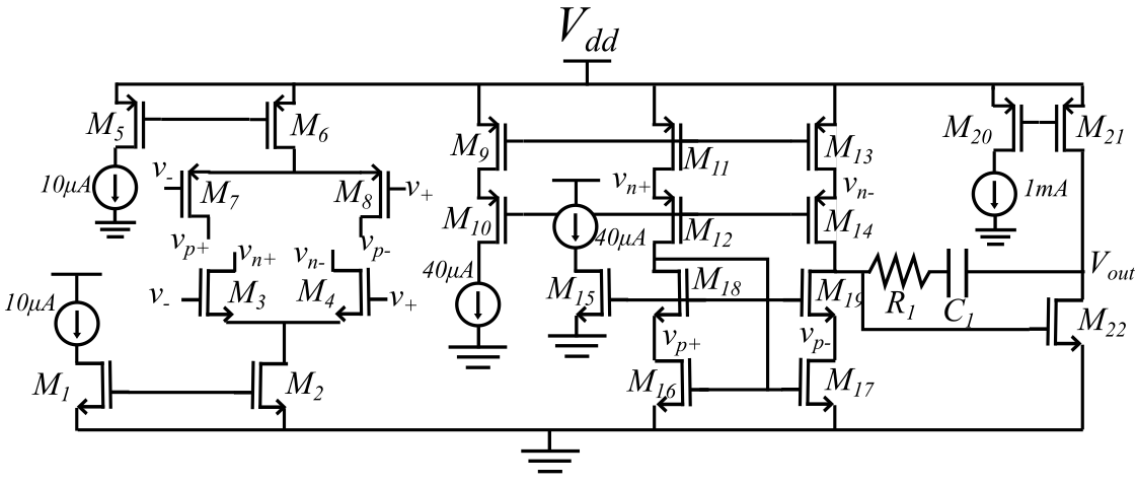

Figure 6.6: High-speed operational amplifier architecture

Table 6.2: Final sizing of the high speed operational amplifier device.

Device	**Width (μm)**	**Length (nm)**	**Fingers**	**Multiplier**	**Type**
M_1	0.16	100	1	16	RVT
M_2	0.16	100	1	16	RVT
M_3	1.28	20	8	2	RVT
M_4	1.28	20	8	2	RVT
M_5	0.16	100	1	16	RVT
M_6	0.16	100	1	16	RVT
M_7	1.28	20	8	2	RVT
M_8	1.28	20	8	2	RVT
M_9	3	40	15	4	SLVT
M_{10}	3	40	15	4	SLVT
M_{11}	3	40	15	4	SLVT
M_{12}	3	40	15	4	SLVT
M_{13}	3	40	15	4	SLVT
M_{14}	3	40	15	4	SLVT
M_{15}	0.4	40	2	1	RVT
M_{16}	0.6	40	3	3	SLVT
M_{17}	0.6	40	3	3	SLVT
M_{18}	0.6	40	3	3	SLVT
M_{19}	0.6	40	3	3	SLVT
M_{20}	10	40	20	4	SLVT
M_{21}	10	40	20	4	SLVT
M_{22}	10	40	20	4	SLVT
R_1	0.36	3700	-	8 (series)	N+ Poly Silicided
C_1	1.32	1320	-	1	Apmom1v8

6.6.3 Layout of the Operational Amplifiers

The 22 nm CMOS FD-SOI technology supports multiple metal stack options. The process used in this work provides eight metal layers: M1, M2, C1, C2, C3, IA, OI, and LB. M1 and M2 are the bottom two layers, typically used for short local interconnects, with a minimum width of 40 nm. The intermediate C layers (C1–C3) are approximately 1.1× the height of M1, offer a slightly improved current limit, and have a lower sheet resistance at minimum width (44 nm), with 10 Ω/μm compared to 15.5 Ω/μm for M1.

The IA layer is nine times the height of M1, supports a current limit of 3.1 mA at minimum width (360 nm), and is used for higher-power signal routing. The OI layer is thirty-four times the height of M1, supports a current limit of 71 mA at minimum width (1.8 μm), and exhibits an extremely low sheet resistance of 0.027 Ω/μm. Due to these properties, OI is primarily used for the power supply and for long interconnects within the complete PLL design. The LB layer is 2.8 μm thick, has less favorable electrical characteristics, and is intended for other purposes, so it is not used in this work.

The layout of the DC biasing op-amp is shown in Figure 6.7. The transistors of each

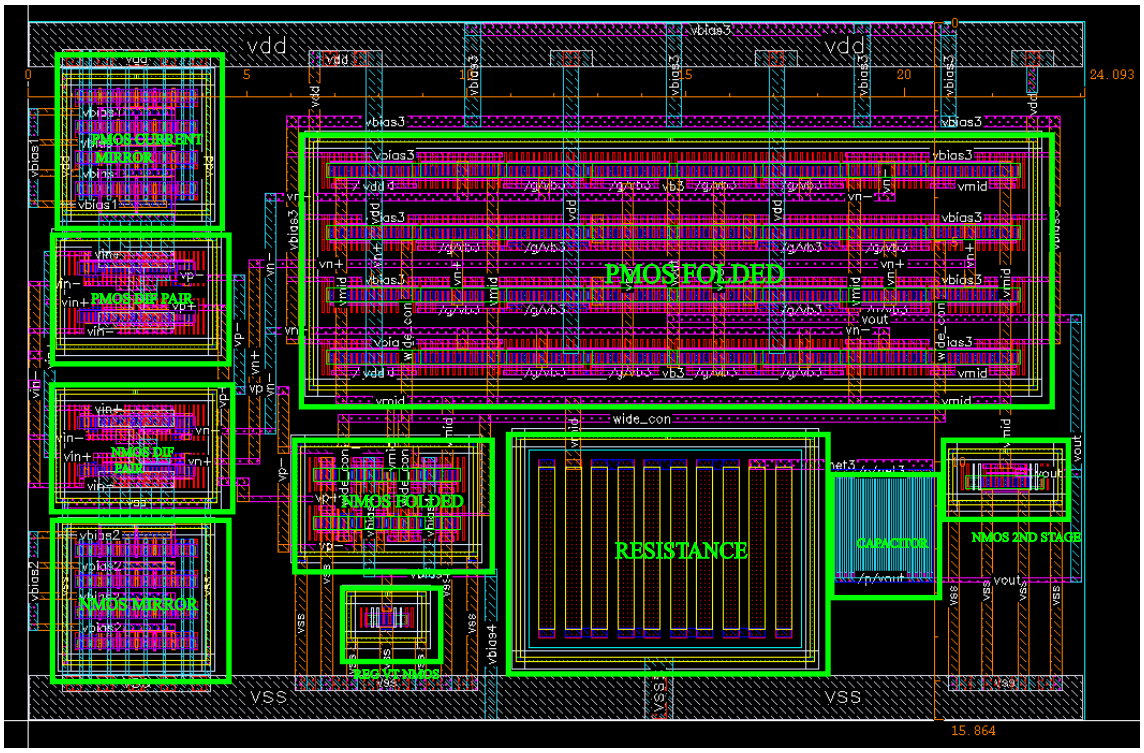

Figure 6.7: Layout of the DC biasing operational amplifier

current mirror are matched using a common-centroid arrangement with identical guard rings to minimize the effect of process variations. The connections to the differential pair are carefully routed to maintain symmetry. The widths and lengths of the metals were adjusted such that the path resistance differences do not exceed 2 Ω.

In the folded NMOS branch, the biasing transistor is of a different type and requires a different guard ring, since the super-low-V_t devices use a triple-well structure while the regular devices do not. The remaining PMOS devices share the same guard ring, and below them are placed the resistor and capacitor (implemented using the bottom five thin metal layers) together with the active common-source NMOS device. The inter-stage signal paths are routed using different metal layers and are not placed directly above each other,

reducing coupling capacitance. Finally, the circuit is powered through the IA layer, chosen for its ability to handle higher currents with low resistance.

The layout of the high-speed, high-power op-amp is shown in Figure 6.8. The transis-

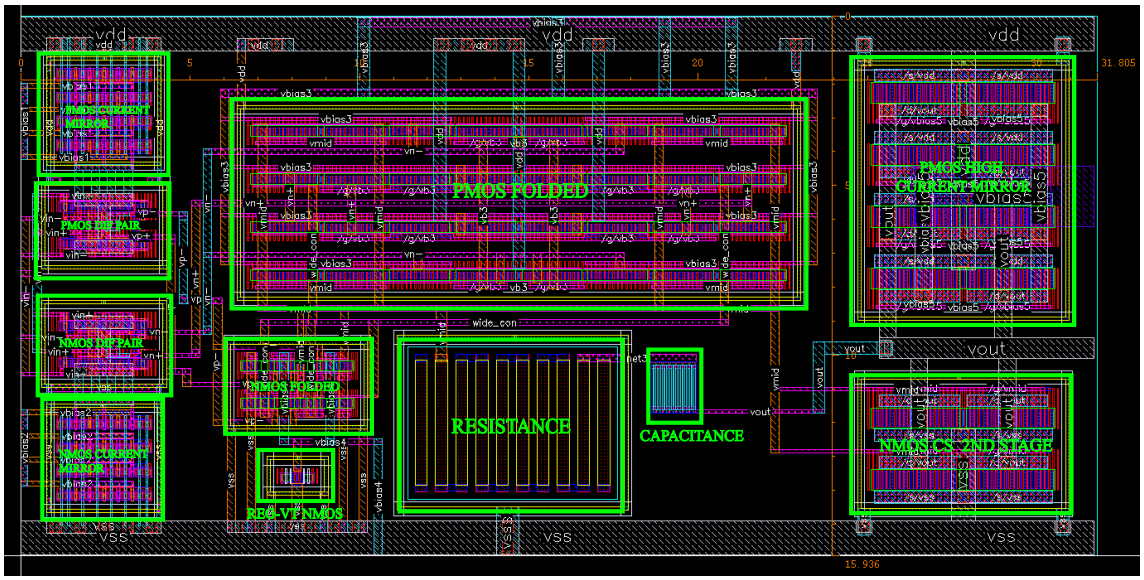

Figure 6.8: Layout of the high-speed operational amplifier

tors of the first stage are connected in exactly the same configuration as in the DC biasing op-amp. Dummy devices are included to improve matching and to mitigate the impact of the well proximity effect.

In the second stage, the PMOS current mirror is biased using the thicker IA and OI metal layers and is connected via the IA layer to the common-source NMOS amplifying transistor located below. The use of these thicker metals improves current-handling capability but increases parasitic capacitance. Consequently, a smaller compensation capacitor is required to achieve a high phase margin.

6.6.4 Pre vs Post Layout Results

The pre-layout simulation results for the DC biasing op-amp show a gain of 59.43 dB, a phase margin of 71.5°, and a Gain Margin of 14.79 dB. The post-layout simulation results yield a gain of 57.47 dB, a phase margin of 59.43°, and a Gain Margin of 13.22 dB as shown in Figure 6.9.

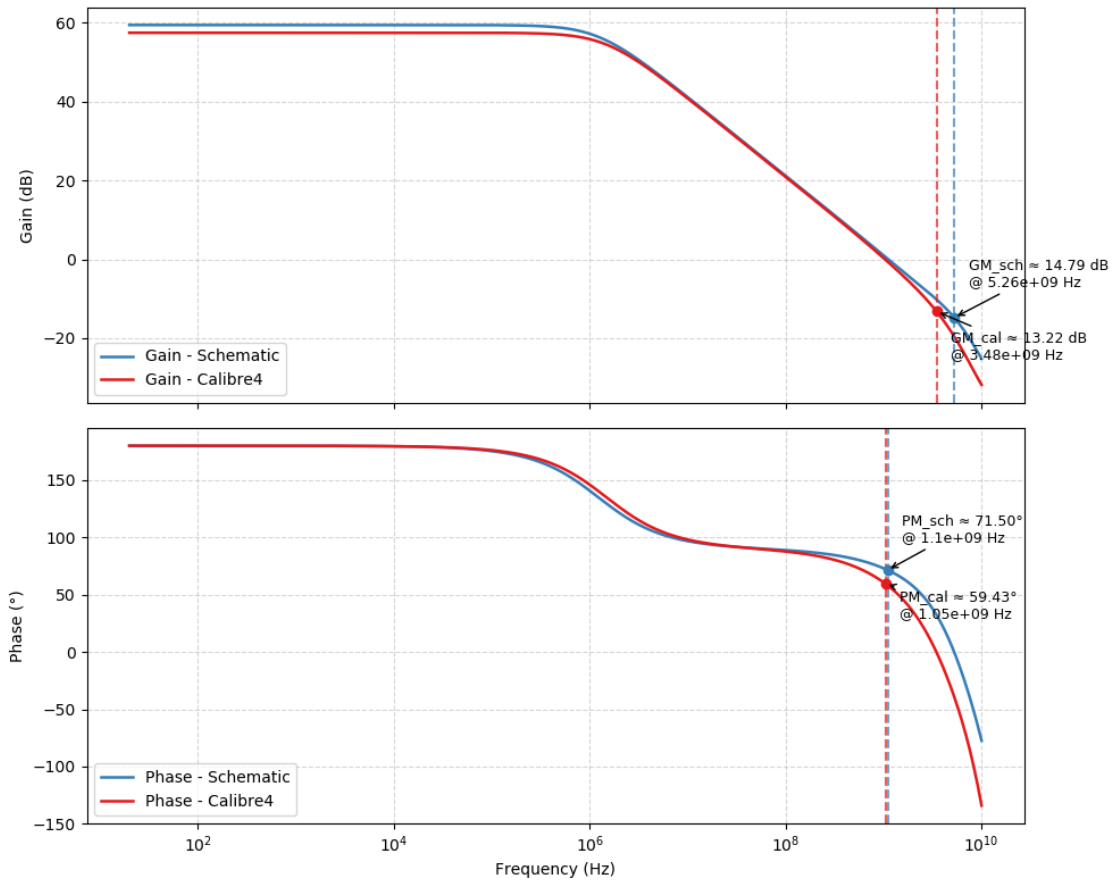

Figure 6.9: DC biasing op-amp bode diagram comparison

The main degradation in the post-layout results is in the phase margin, which is reduced by 12.07°. This is primarily due to the increased parasitic capacitance introduced by the layout, which affects the second most dominant pole of the amplifier, which increased significantly. As a result, to keep the Phase Margin above a safe level a larger compensation capacitor was required, which in turn increased the area of the capacitor. Initially, a smaller capacitor was used in the schematic to achieve a phase margin of 65°, but the post-layout simulation required a larger capacitor to maintain stability.

The pre-layout simulation results for the high-speed op-amp show a gain of 60.8 dB, a phase margin of 73.13°, and a Gain Margin of 14.56 dB. The post-layout simulation results yield a gain of 60.58 dB, a phase margin of 68.01°, and a Gain Margin of 13.03 dB as shown in Figure 6.10.

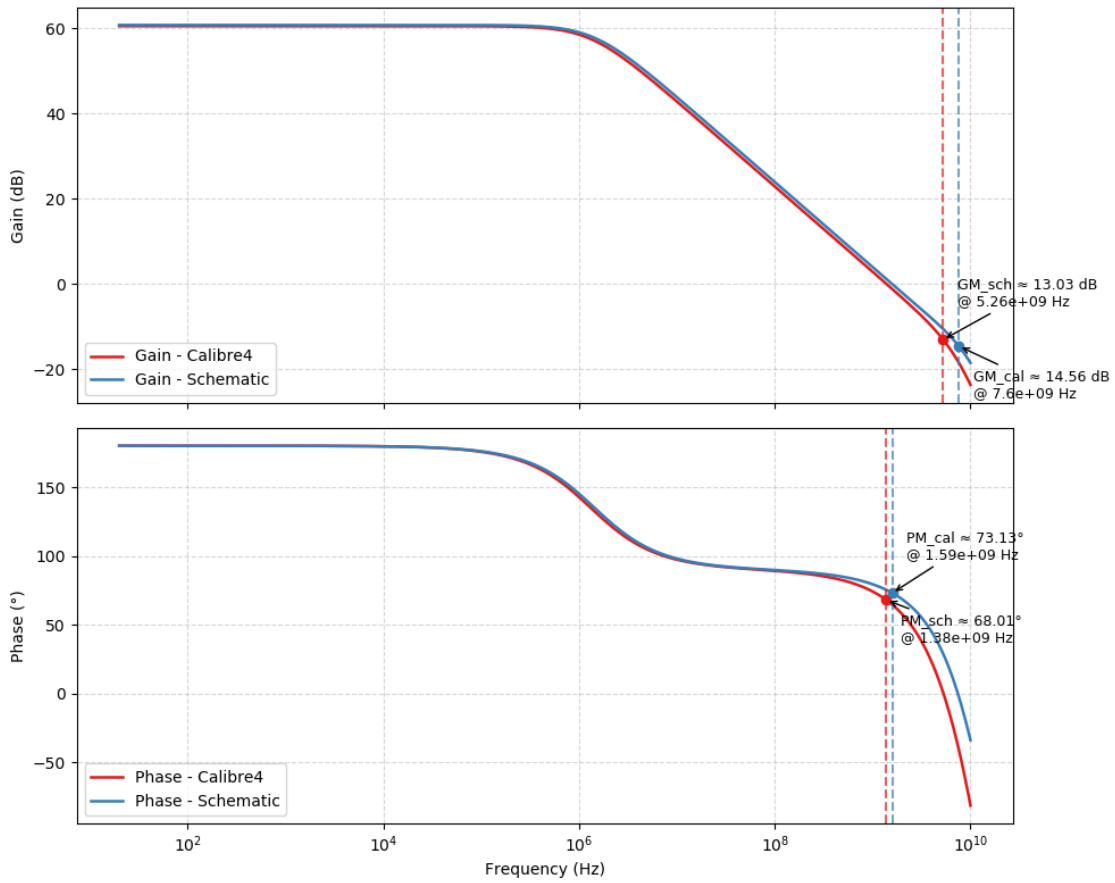

Figure 6.10: High-speed op-amp bode diagram comparison

In this case the most dominant pole was affected by the layout as much as the second one. As a result, the phase margin remained almost the same and no change in the compensation capacitor was required. The Gain Margin was also reduced by 1.53 dB, which is acceptable for this type of op-amp.

6.7 Offset current optimization

A technique analyzed in [7] was implemented in this work. The charge pump of the CPPLL operates in the near-zero phase-error regime in steady state. Because a current mismatch always exists (and can be significant when the output voltage is near the range limits), the near-zero phase-error region is nonlinear. This nonlinearity produces additional reference spurs on the VCO output. To mitigate this, an offset current is introduced. The offset shifts the characteristic curve so that, at small phase errors, the charge pump operates in a more linear region (see Figure 6.11).

The implemented offset charge pump is shown in Figure 6.12. The overall implementation used here is a combination of this offset charge-pump topology and the resistive-based implementation. The complete design is shown in Figure 6.13.

The basic operation is as follows. In steady state there is a specific (small) phase error: the reference clock leads the feedback signal. As a result, an `UP` pulse is generated each period. There is a time interval t_1 during which both `UP` and `CLK` are asserted (logical

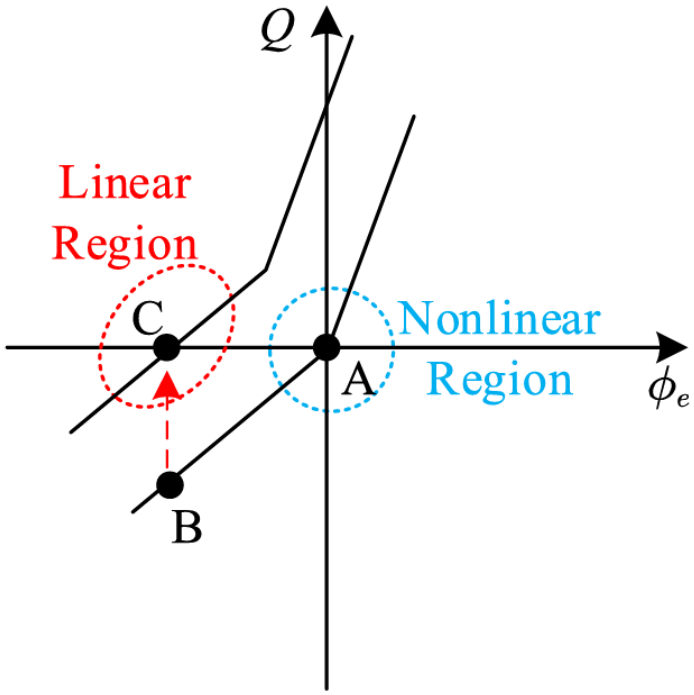

Figure 6.11: Charge pump linear and non linear regions

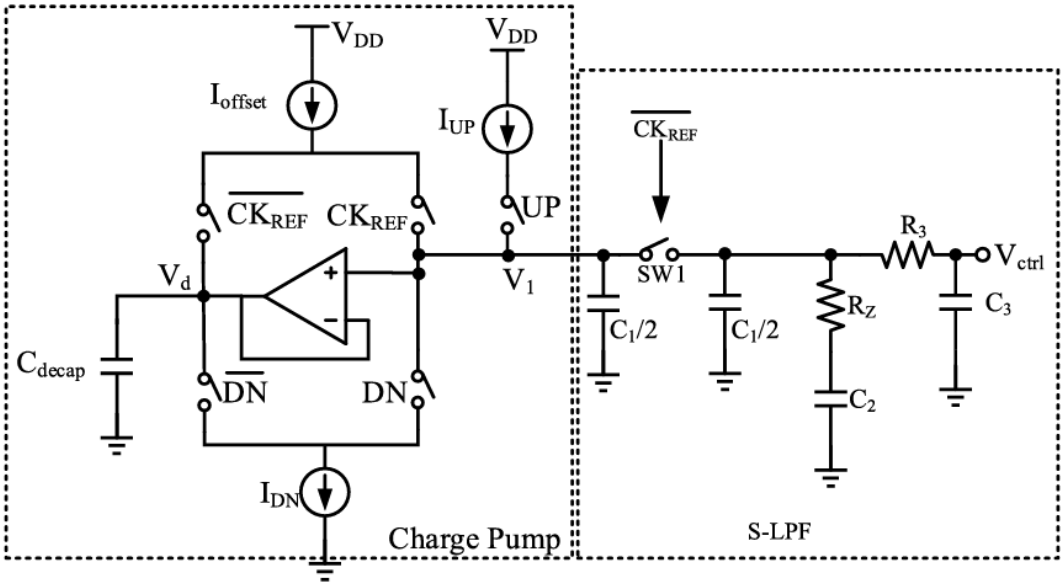

Figure 6.12: Charge pump with offset current

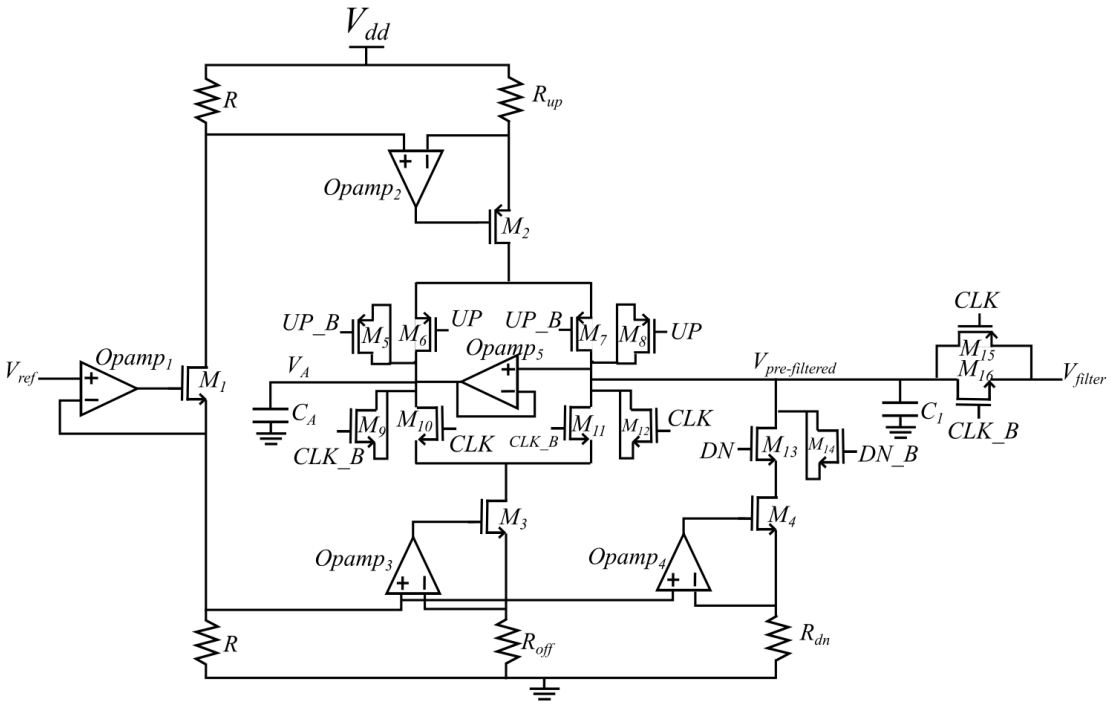

Figure 6.13: Charge pump with offset current and resistive-based architecture

high). During 0 to t_1 the output current is $I_{\mathrm{UP}} - I_{\mathrm{offset}}$. From t_1 to $T/2$ (interval t_2) the output current is $-I_{\mathrm{offset}}$, and for the remainder of the period the output current is zero.

For steady state, the average current over one period must be zero. If we set $I_{\mathrm{offset}} = I_{\mathrm{UP}}/k$, the steady-state phase error h follows from

$$\int_{\mathrm{period}} I_{\mathrm{CP}}(t)\, dt = 0$$

which gives

$$I_{\mathrm{UP}} \cdot h + (-I_{\mathrm{offset}}) \cdot \frac{T}{2} = 0.$$

Substituting $I_{\mathrm{UP}} = k\, I_{\mathrm{offset}}$ yields

$$k\, I_{\mathrm{offset}}\, h - I_{\mathrm{offset}}\, \frac{T}{2} = 0 \quad \Longrightarrow \quad h = \frac{T/2}{k}.$$

This steady-state phase error is the same for every successful lock of the PLL and can be removed easily with a phase shifter. The prefiltered voltage $V_{\mathrm{pre,filtered}}$ is shown in Figure 6.14.

During the other half-period the sampling occurs while the voltage is approximately constant, which justifies the steady-state assumption. The loop filter will be analyzed separately in a later chapter. Final transistor sizes, op-amp parameters and passive component values are listed in Table 6.3.

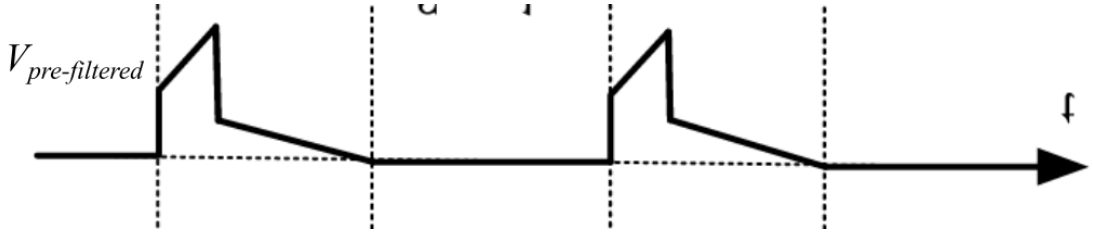

Figure 6.14: Pre-filtered voltage of the charge pump

Table 6.3: Final sizing of the charge pump devices.

Device	**Width (μm)**	**Length (nm)**	**Fingers**	**Multiplier**	**Type**
M_1	4	40	10	2	RVT
M_2	8	40	20	4	RVT
M_3	8	40	20	4	RVT
M_4	32	40	20	1	RVT
M_5	30	40	20	4	RVT
M_6	30	40	20	4	RVT
M_7	30	40	20	4	RVT
M_8	30	40	20	4	RVT
M_9	10	40	20	4	RVT
M_{10}	10	40	20	4	RVT
M_{11}	10	40	20	4	RVT
M_{12}	10	40	20	4	RVT
M_{13}	10	40	20	4	RVT
M_{14}	10	40	20	4	RVT
M_{15}	30	40	20	1	RVT
M_{16}	10	40	10	1	RVT
R	0.5	3220	-	1 (series)	N+ Poly Silicided
R_{off}	0.5	3220	-	7 (series)	N+ Poly Silicided
R_{up}	0.5	3220	-	1 (series)	N+ Poly Silicided
R_{dn}	0.5	3220	-	1 (series)	N+ Poly Silicided
C_1	12.01	12010	-	16	Apmom1v8
C_A	9.035	9035	-	16	Apmom1v8

6.8 Charge Pump Layout

The layout of the charge pump is shown in Figure 6.15. The layout was designed to

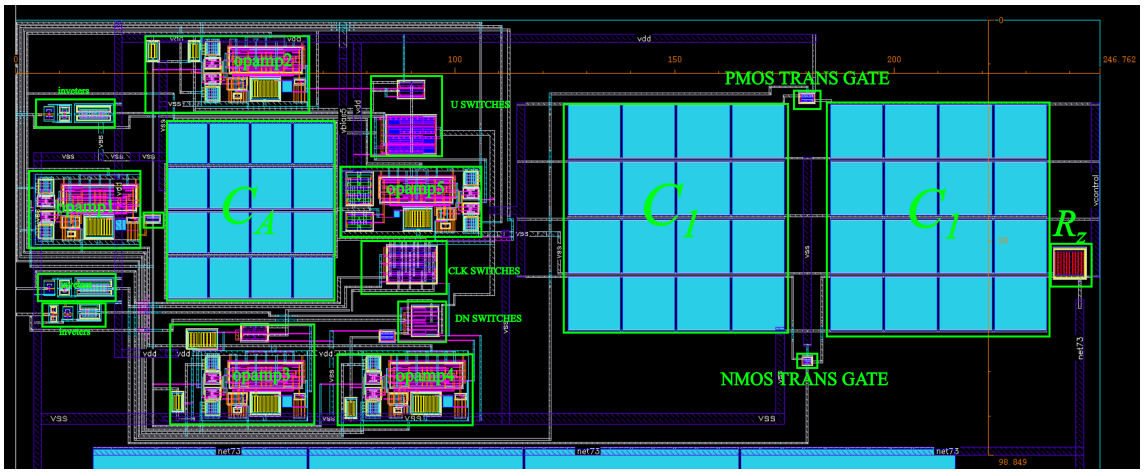

Figure 6.15: Charge pump layout

minimize area while ensuring proper transistor matching and avoiding excessively large coupling capacitances. The NMOS and PMOS transistors in the switches are arranged in a common-centroid configuration to enhance matching performance. Thicker metal layers (IA) are used extensively, while the thickest metal layer (OI) is employed for the power supply lines and long interconnections to the high-power op-amp in order to reduce voltage drop along these paths.

Special attention was given to the routing of the switch gate signals, as only the IA metal layer was available for these paths, requiring careful layout to minimize resistance and parasitic effects.

Finally, a portion of the layout area remains unoccupied due to the differing rectangular geometries of the op-amps and passive components.A more complete layout including the loop filter is shown in Figure 6.16.

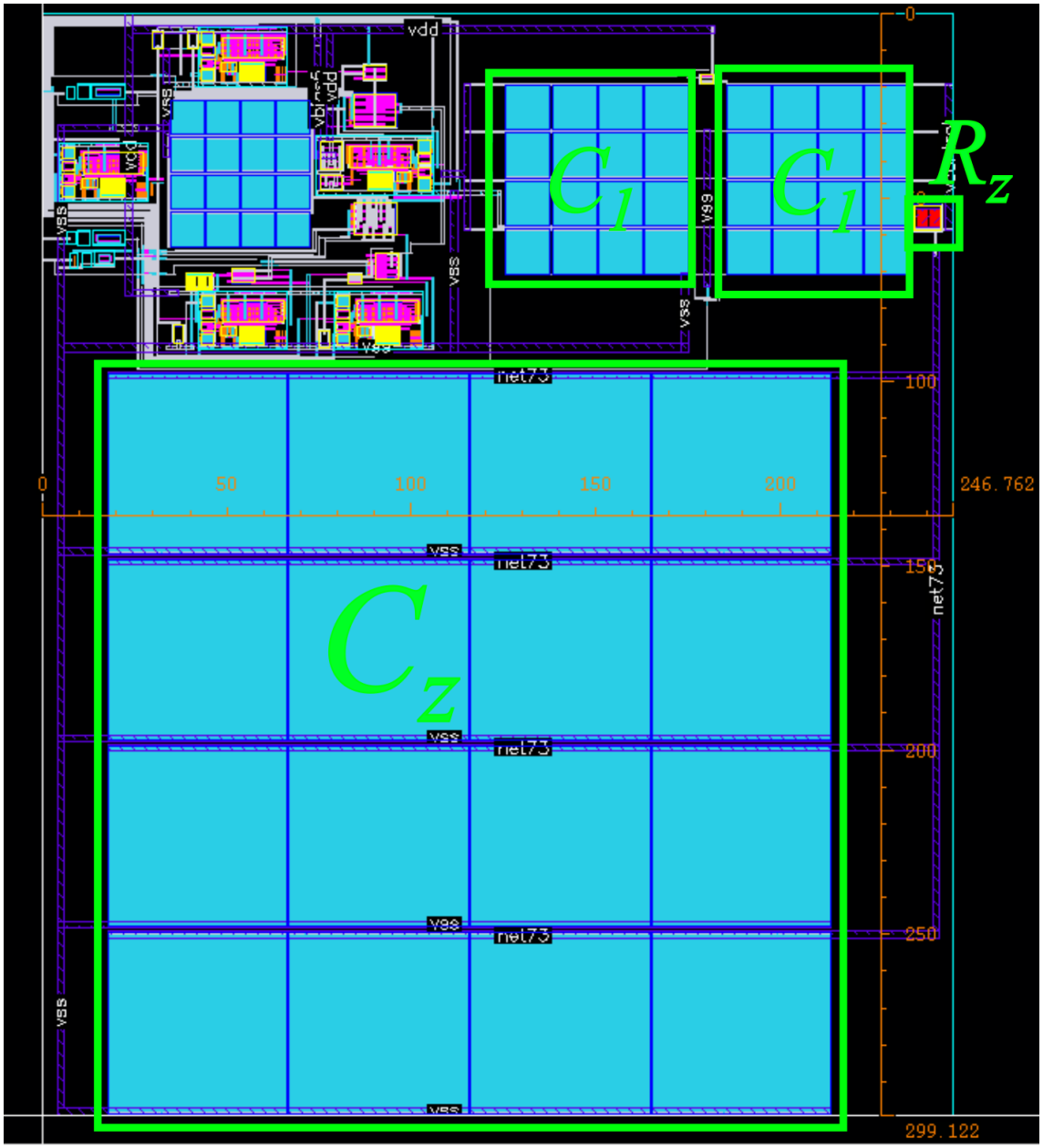

Figure 6.16: Charge pump and loop filter layout

The loop filter capacitor C_Z is extremely large for the circuit and it covers multiple times the area of the rest of the charge pump circuit. That's a big disadvantage of the analog loop filter which will be discussed in the filter chapter.

6.9 Pre vs Post Layout Results

The first simulation is a transient analysis of the charge pump with the DN signal held at logic low. The CLK_{REF} signal is high for half of the period, while the UP signal remains high for a duration seven times shorter, in order to demonstrate an almost steady-state condition. Figures 6.17 and 6.18 show the pre-layout and post-layout simulation results, respectively.

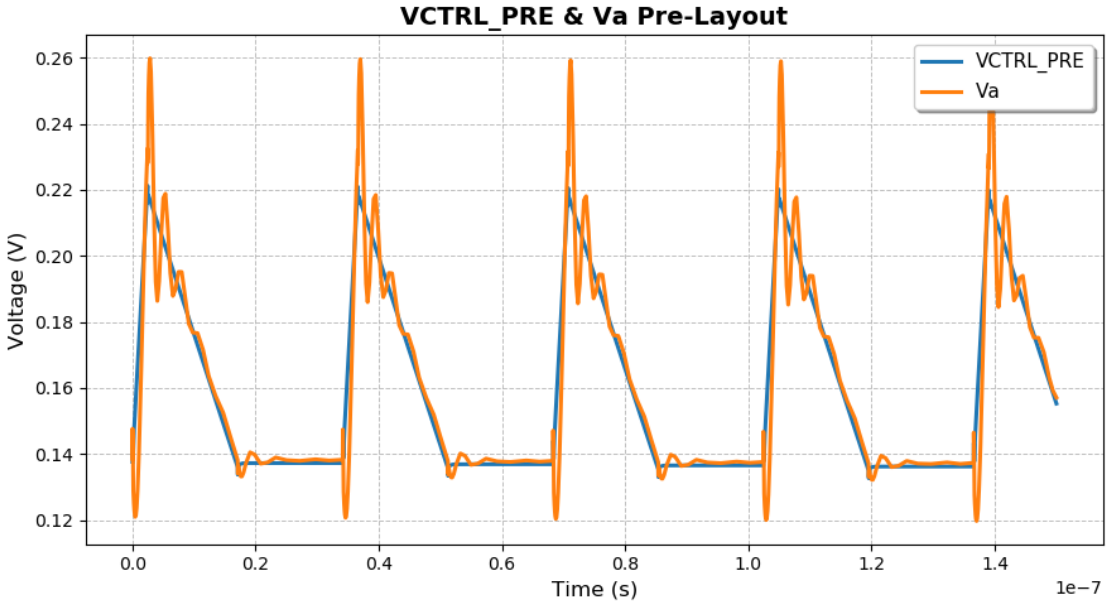

Figure 6.17: Pre-layout transient results of the charge pump

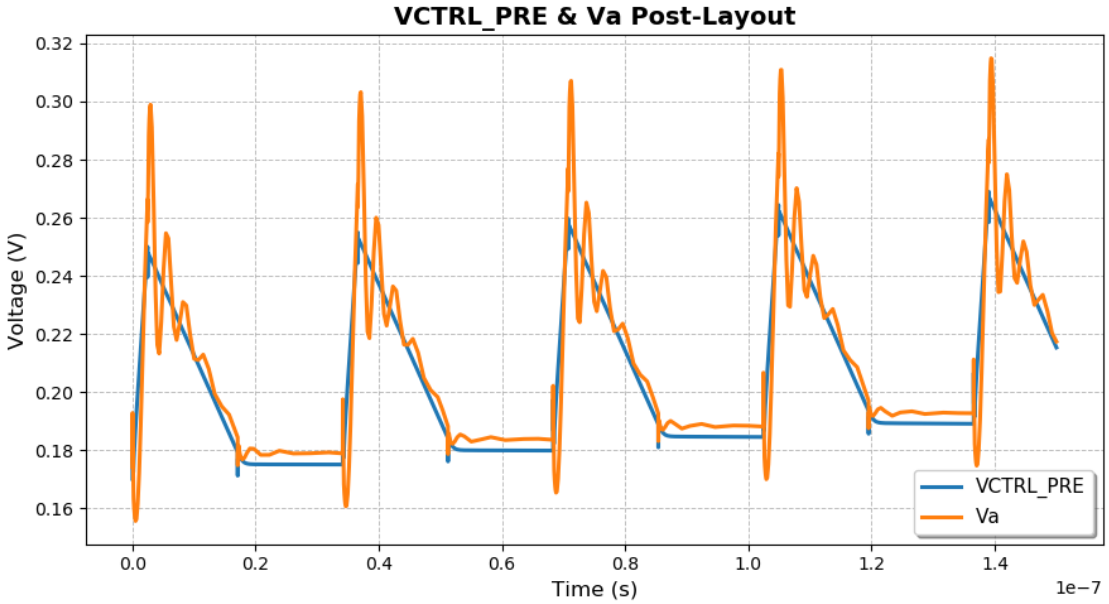

Figure 6.18: Post-layout transient results of the charge pump

In the post-layout simulation, a significant difference is observed: due to increased current mismatch, the output voltage at the sampling instant is no longer in a steady-state condition. The voltage V_a exhibits a similar trend in both cases; however, in the post-layout simulation, a constant voltage offset appears. This offset arises from the non-ideal transfer characteristic of the post-layout op-amp buffer.

Overall, the circuit remains functional, as the steady-state phase error changes in magnitude but remains constant. Such an error can be readily compensated using a phase shifter.

The second simulation is a DC parametric operating-point analysis, performed for two input combinations:

1. UP = logic high, DN = logic low
2. UP = logic low, DN = logic high

In both cases, CLK_{REF} is held at logic low to ensure that the output voltage remains stable and no offset current is delivered to the output capacitors. This simulation evaluates the **current mismatch** between the UP and DN current sources. If the mismatch is large, the PLL requires more time to achieve lock and exhibits reference spurs of higher magnitude. Figures 6.19 and 6.20 show the pre-layout and post-layout current mismatch, respectively.

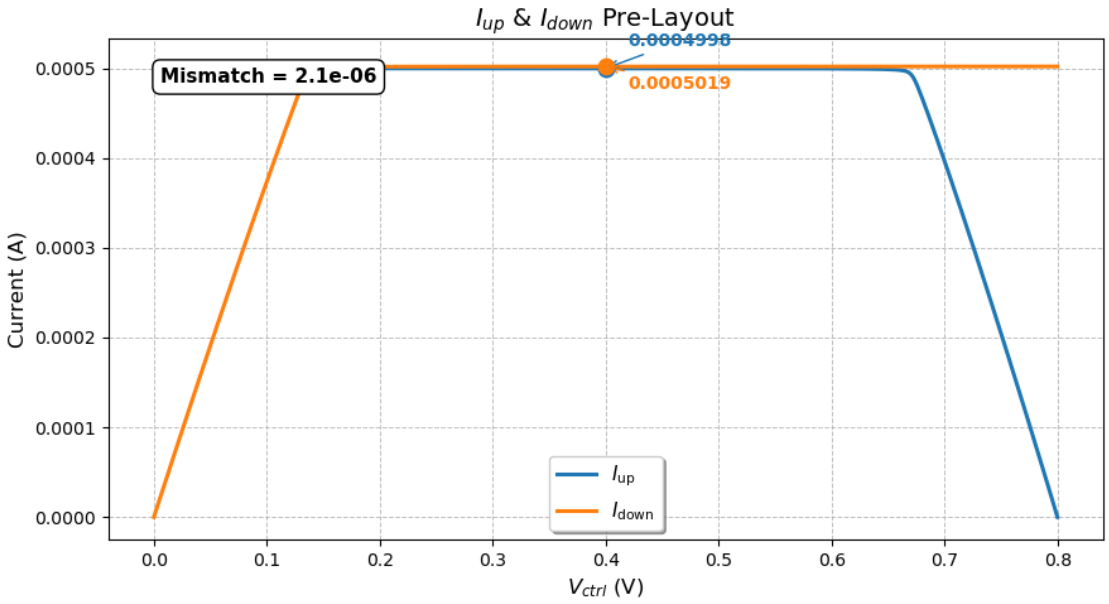

Figure 6.19: Pre-layout DC current mismatch results of the charge pump

In the pre-layout simulation, the mismatch is minimal (2.1 μA), whereas in the post-layout simulation it increases significantly to 49 μA. This degradation is primarily due to voltage drops across vias and interconnect metals leading to the load resistors. To compensate, the resistor values were adjusted. The original resistance was $R_{\text{old}} = 194.64\,\Omega$. Since the voltage across a resistor is given by $V = I \cdot R$, the corrected resistor value can be calculated as:

$$R_{\text{new}} = R_{\text{old}} \cdot \frac{I_{\text{old}}}{I_{\text{target}}}$$

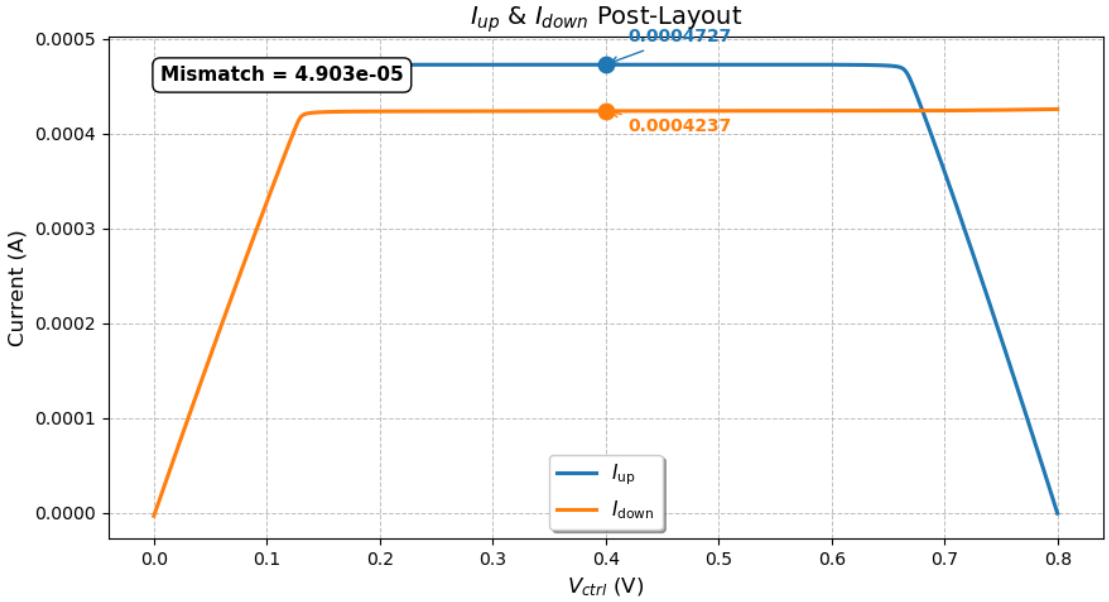

Figure 6.20: Post-layout DC current mismatch results of the charge pump

where, in this case, $I_{\text{target}} = 500\ \mu\text{A}$. Using this expression, the updated values are:

$$R_{\text{UP}} = 184.02\ \Omega, \quad R_{\text{DOWN}} = 164.97\ \Omega.$$

With these corrected values, the post-layout simulation results (shown in Figure 6.21) indicate that the final mismatch is reduced to 1.5 μA, which is comparable to the original pre-layout design.

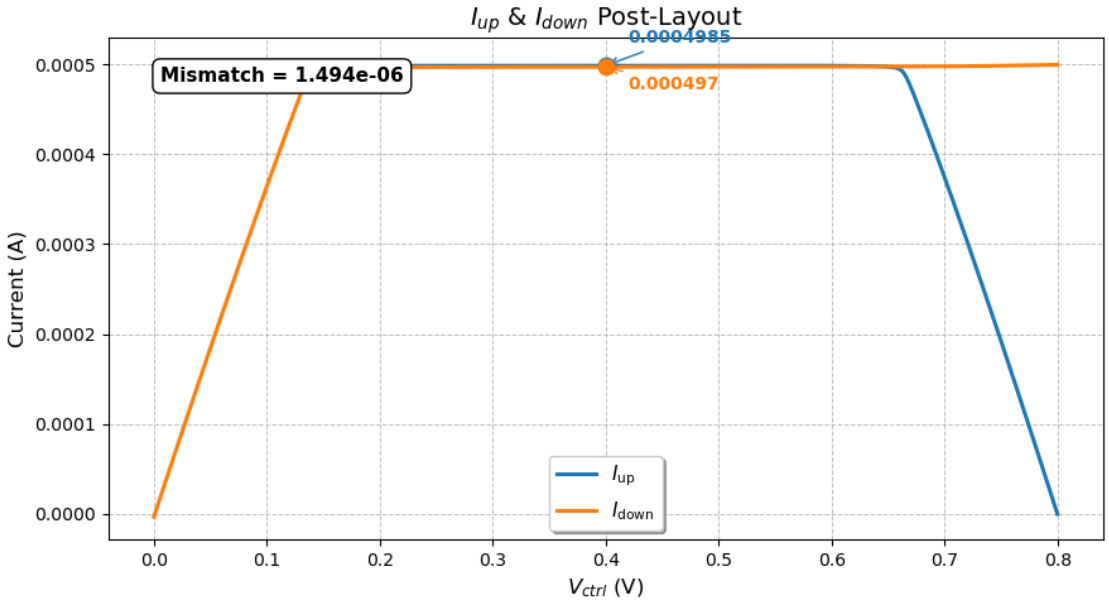

Figure 6.21: Post-layout DC current mismatch updated results

Chapter 7

Voltage-Controlled Oscillator (VCO)

A Voltage-Controlled Oscillator (VCO) is an electronic oscillator whose output frequency is controlled by an input voltage. VCOs are fundamental building blocks in phase-locked loops (PLLs) and frequency synthesizers, as they allow precise frequency tuning via voltage control.

VCOs can be broadly classified according to the waveform they produce:

1. Harmonic (or linear) oscillators - These generate a nearly sinusoidal waveform. In electronics, they typically consist of a resonator and an active device (amplifier) that compensates for the resonator's energy losses while providing isolation from the output load. Common examples include LC oscillators and crystal oscillators.

   LC oscillators use an inductor-capacitor resonant tank to set the oscillation frequency. The active device (e.g., cross-coupled transistors) sustains the oscillation by replacing energy lost in the tank each cycle. The oscillation frequency is given by $f_0 = \frac{1}{2\pi\sqrt{LC}}$, and can be tuned by varying the capacitance, typically using a varactor. LC oscillators generally exhibit low phase noise due to the high quality factor (Q) of the resonant tank.

2. Relaxation oscillators - These produce non-sinusoidal waveforms such as sawtooth or triangular signals. They operate by charging and discharging a capacitor through a resistor or current source, with switching elements determining the oscillation period. They are easy to implement and offer a wide frequency tuning range with minimal external components, but they typically have higher phase noise than harmonic oscillators.

3. Ring oscillators - These produce rectangular (digital) waveforms. They consist of an odd number of inverting stages connected in a feedback loop, satisfying the Barkhausen criteria for oscillation. The oscillation frequency is determined by the total propagation delay of the loop:

   $$f_0 = \frac{1}{2N\tau_d}$$

   where N is the number of stages and τ_d is the delay per stage. The frequency can be tuned by varying the delay, for example, using varactors or by adjusting bias currents. Ring oscillators are compact, require no inductors, and are easy to integrate in CMOS processes, but they generally suffer from higher phase noise compared to LC oscillators due to their lower Q and higher susceptibility to noise.

7.1 Comparison between LC and Ring Oscillators

- Phase noise: LC oscillators usually offer significantly better phase noise performance because the resonant tank filters out high-frequency noise. Ring oscillators have poorer phase noise due to the absence of a high-Q frequency-selective element.
- Tuning range: Ring oscillators can achieve a wide tuning range by varying the delay, whereas LC oscillators have a more limited range set by the tank components.
- Integration and area: Ring oscillators are fully integrable in standard CMOS without the need for large inductors, making them area-efficient. LC oscillators require on-chip inductors or external components, which consume more die area.
- Power consumption: For similar frequency ranges, LC oscillators often consume more power to maintain oscillation and achieve low phase noise, while ring oscillators can operate at lower power but with degraded noise performance.

In this work, an LC oscillator was chosen for a lower out-of-band Phase Noise. The tuning range can be significantly improved by adding capacitor banks and switches and will be analyzed in a following section.

7.2 LC Oscillator analysis

An LC-tank oscillator can be implemented using a pair of transistors in a cross-coupled configuration to provide the negative resistance required to sustain oscillations as shown in Figure 7.1.

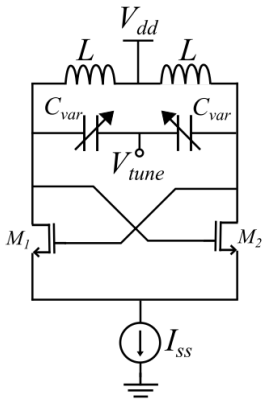

Figure 7.1: Basic LC oscillator topology

The LC tank, composed of an inductor L and a capacitor C, forms a resonant circuit with a natural frequency

$$f_0 = \frac{1}{2\pi\sqrt{LC}}.$$

In the absence of an active device, the finite losses in the tank—represented by its equivalent parallel resistance R_p—cause the oscillations to decay. To counteract this, two transistors are connected so that the gate (or base) of each device is driven by the output of the other. This cross-coupling effectively inverts the signal and feeds it back in phase with the tank voltage at the opposite side, producing a small-signal negative resistance.

From small-signal analysis, the differential pair exhibits an incremental negative resistance of

$$R_{\text{neg}} = -\frac{2}{g_m},$$

where g_m is the transconductance of each transistor [8]. When $|R_{\text{neg}}| \geq R_p$, the negative resistance exactly compensates for the tank's losses, allowing oscillations to build up until limited by the nonlinearities of the transistors. This topology not only satisfies the Barkhausen criteria for startup but also provides symmetrical excitation of the tank, improving waveform purity and reducing even-order distortion. The use of varactors instead of fixed capacitors allows the oscillation frequency to be tuned by varying the control voltage V_{ctrl}, which adjusts the capacitance C in the tank.

7.3 VCO overall design

The overall design of the VCO is shown in Figure 7.2.

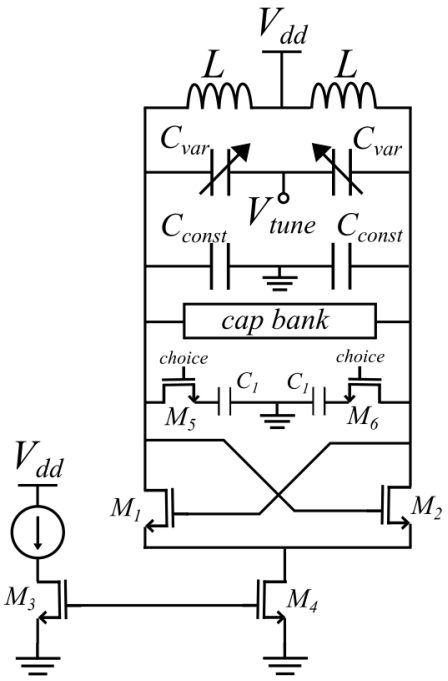

Figure 7.2: Overall VCO design

In this design, the ideal current source is replaced by a simple current mirror. To reduce power consumption, transistor M_4 is designed with a significantly larger W/L ratio so that it can mirror a larger current. Although M_4 operates in the triode region, it is not used for amplification, so this mode of operation does not pose a problem for the intended functionality. A relatively large bias current of 12.53 mA is used to achieve a sufficiently high transconductance (g_m) for transistors M_1 and M_2, thereby ensuring a large loop gain. The loop gain must be considerably greater than unity to guarantee reliable oscillation startup under all process corners and in Monte Carlo simulations.

The AC transconductance of a MOS transistor is given by:

$$g_m = \sqrt{2\mu_n C_{\text{ox}} \frac{W}{L} I_D}.$$

To achieve a high g_m, relatively wide transistors are required in this technology.

For a VCO, an important parameter is K_{VCO}, defined as the slope of the oscillation frequency versus the tuning voltage. As described in [8], the phase noise is proportional to K_{VCO}. Therefore, a large K_{VCO} results in higher phase noise. Using a varactor with an excessively large tuning range increases K_{VCO}, which not only degrades phase noise performance but also makes the PLL more susceptible to noise due to the fine accuracy required in V_{control}. This, in turn, increases the RMS jitter at the output.

A well-known approach to mitigate this problem is the use of multiple **frequency bands**. Each band covers a relatively small frequency range, resulting in a reduced K_{VCO} (and hence lower phase noise), while the combination of multiple bands spans a much wider frequency range.

In this work, the first VCO covers the 10–13 GHz range, and the second VCO covers the 12–15 GHz range. A total of 64 bands is required. The more bands a section has, the less effective K_{VCO} is in each band. For example, if the highest band has 100 MHz/V, the second might have 98 MHz/V, and by the 32nd band, K_{VCO} is approximately halved. Consequently, it is more efficient to use two 32-band sections rather than a single 64-band section. To implement this scheme, the circuit includes a fixed capacitor, a varactor, a capacitor bank for 32-band tuning, and a large switch to select between the two band sections.

The capacitor bank, shown in Figure 7.3, consists of five pairs of MOS switches and

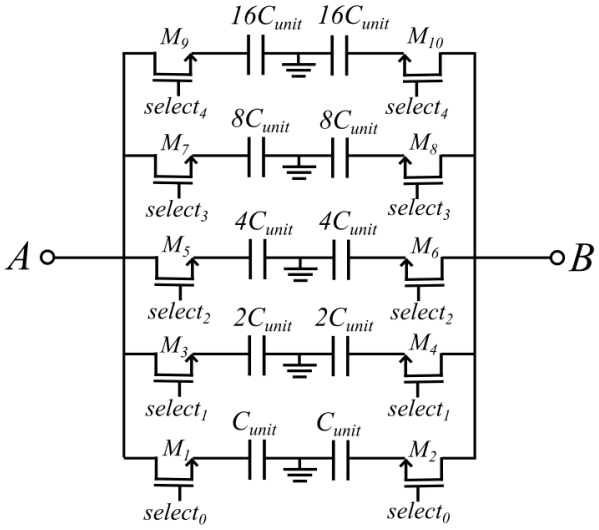

Figure 7.3: Capacitor bank for 32-band tuning

capacitors. The capacitors follow a binary-weighted scheme (powers of two), enabling the selection of any value from 0 to 31 by appropriately opening or closing the switches. For example, to select the 23rd band, switches 1, 3, 5, and 9 would be open, and switch 7 would be closed, resulting in an input capacitance of:

$$C_{\text{unit}} + 2C_{\text{unit}} + 4C_{\text{unit}} + 16C_{\text{unit}} = 23C_{\text{unit}}.$$

The LC tank is designed symmetrically, with a ground connection along the symmetry axis, which yields more consistent results compared to configurations without a central

ground. The inductor is implemented as a series-connected, magnetically coupled structure (similar to a transformer) with a center tap to connect to the power supply.

Another important parameter in VCO design is the **quality factor** (Q). For an RL series circuit, the quality factor is given by

$$Q_L = \frac{L}{R}$$

and for an RC series circuit by

$$Q_C = \frac{1}{RC}.$$

In practice, the resistances in these expressions are not deliberately added components, but rather parasitic resistances originating from the metal interconnects and via paths of the circuit. For inductors, R corresponds to the series resistance of the metal windings. For capacitors, the dominant resistance is the R_{ON} of the MOS switches, which operate in the deep triode region.

To maintain a constant Q factor for each capacitor switching path, R_{ON} must be inversely proportional to the capacitance C of that path. This means that if the capacitance is doubled, R_{ON} should be halved. Achieving this requires doubling the total width of the MOS transistor in the switch. However, to minimize parasitic capacitance, the number of fingers is increased instead of simply widening each finger.

As shown in [8], phase noise is proportional to $1/Q$. Therefore, it is critical to maintain a high Q factor for both the switches and the inductors to keep the phase noise within acceptable limits. In the technology used for this work, the inductors required support up to $Q = 21$, which is sufficient for the intended performance.

Another design consideration is ensuring complete frequency coverage under process, voltage, and temperature (PVT) variations. There must be a deliberate overlap between adjacent frequency bands to guarantee that, even under worst-case conditions, there are no gaps in the frequency range. However, excessive overlap wastes potential tuning range. Based on process variation data for the selected technology, an overlap of approximately 15% was found to be optimal.

To achieve the target frequency range with minimal K_{VCO}, the following iterative design process is used:

1. Select a target K_{VCO}.
2. Starting from the highest frequency band, size the varactor to achieve the desired K_{VCO}.
3. Size the capacitor bank elements so that the overlap between bands remains within the acceptable range (15% in this work).
4. If the required frequency range is not met, increase K_{VCO} by a small margin and repeat the process.

7.4 VCO final sizing and results

The inductor used for both VCOs is a 100 pH inductor with a Q factor of 20, which is sufficient for the intended performance. The varactor is sized to achieve a K_{VCO} of approximately 160 MHz/V, which is suitable for the target frequency range. The current source used for biasing is 100 μA. The sizing of the all transistors is common for both VCOs and is shown in Table 7.1. All transistors are regular V_{th} devices, except for M_5 and M_6, which are Super-Low V_{th} devices to ensure high quality factor for the large capacitor for switching band section.

Table 7.1: Transistor sizing of the VCOs.

Device	**Width (μm)**	**Length (nm)**	**Fingers**	**Multiplier**	**Type**
M_1	400	40	80	1	RVT
M_2	400	40	80	1	RVT
M_3	0.8	1000	1	1	RVT
M_4	128	1000	80	1	RVT
M_5	128	40	32	1	SLVT
M_6	128	40	32	1	SLVT
M_{c1}	0.7	40	2	1	RVT
M_{c2}	0.7	40	2	1	RVT
M_{c3}	1.4	40	4	1	RVT
M_{c4}	1.4	40	4	1	RVT
M_{c5}	2.8	40	8	1	RVT
M_{c6}	2.8	40	8	1	RVT
M_{c7}	5.6	40	16	1	RVT
M_{c8}	5.6	40	16	1	RVT
M_{c9}	11.2	40	32	1	RVT
M_{c10}	11.2	40	32	1	RVT

7.4.1 10-13 GHz VCO

The capacitors' sizes for the 10-13 GHz VCO are shown in Table 7.2.

Table 7.2: Capacitor sizing of the 10-13 GHz VCO.

Device	**Width (μm)**	**Length (μm)**	**Multiplier**	**Overall Value (fF)**
C_1	13.64	13.64	1	565.69
C_{const}	14.15	14.15	1	606.41
C_{var}	1.27	0.4	1	5.952-27.827
C_{unit}	2.675	2.675	1	23.383
C_{2unit}	2.675	2.675	2	46.766
C_{4unit}	2.675	2.675	4	93.532
C_{8unit}	2.675	2.675	8	187.064
C_{16unit}	2.675	2.675	16	374.128

The results of harmonic balance, harmonic balance noise and stability (with differential probe for loop gain) simulations are shown in the table 7.3 and Figures 7.4, 7.5, 7.6 and 7.7.

Table 7.3: Simulation results of the 10-13 GHz VCO.

Parameter	**Value**
Frequency Range	10.0 - 13.0 GHz
Tuning Range	3.0 GHz
Tuning Voltage Range	0.0 - 0.8 V
Phase Noise at 1 MHz offset	-88.85 dBc/Hz
Power Consumption	10.1 mW
Loop Gain nominal	2.74
Loop Gain worst case (ss-120)	1.71
Maximum Band K_{VCO}	160 MHz/V

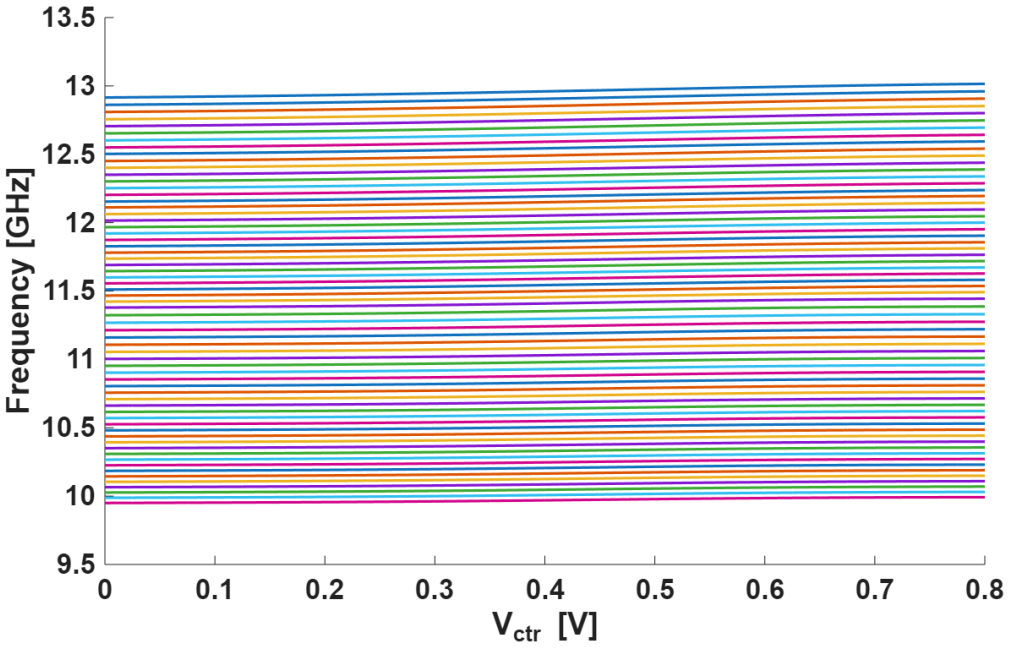

Figure 7.4: Total bands of the 10-13 GHz VCO.

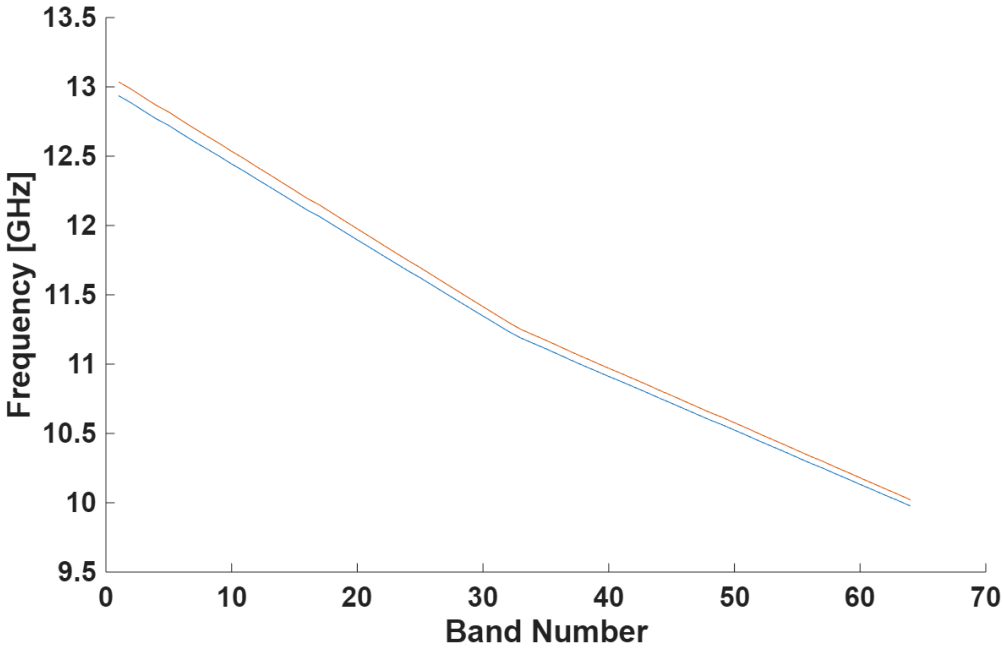

Figure 7.5: Frequency range of the 10-13 GHz VCO.

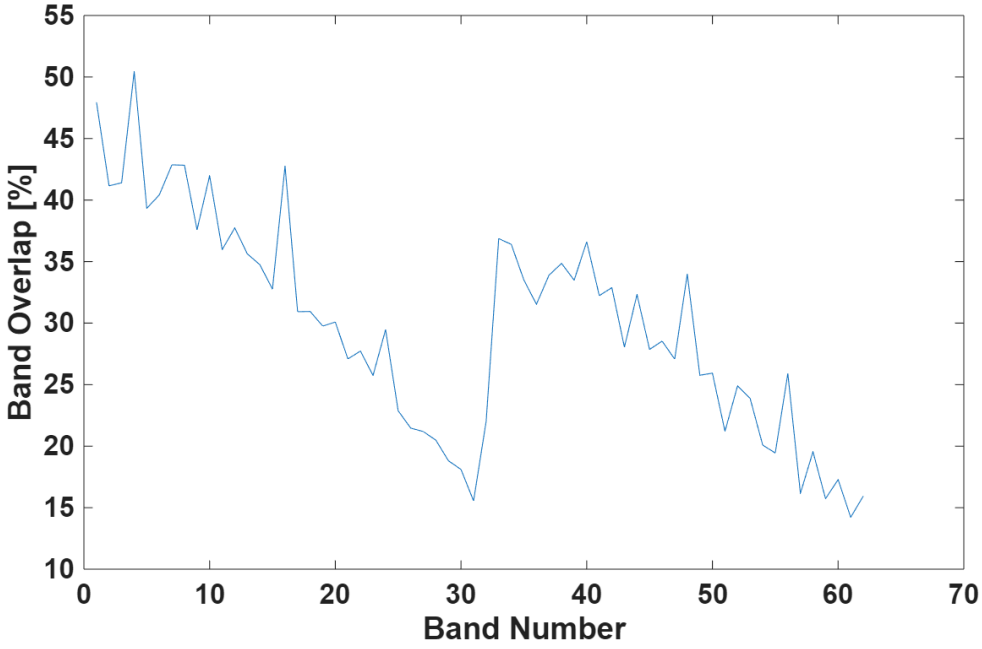

Figure 7.6: Band overlap percentage of the 10-13 GHz VCO.

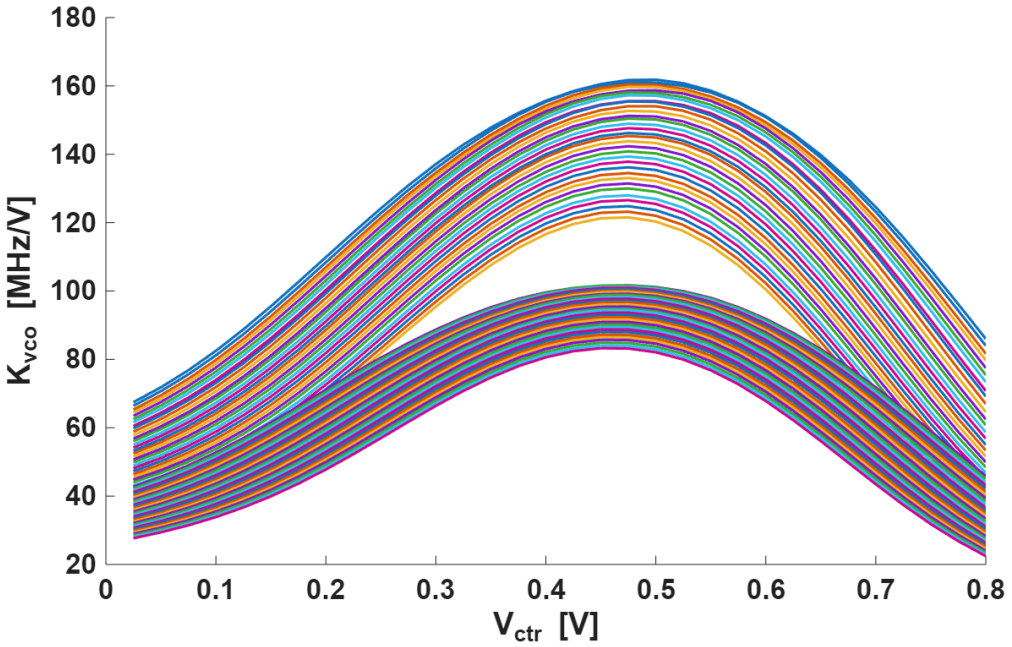

Figure 7.7: K_{VCO} of each band of the 10-13 GHz VCO.

7.4.2 12-15 GHz VCO

The capacitors' sizes for the 12-15 GHz VCO are shown in Table 7.4.

Table 7.4: Capacitor sizing of the 12-15 GHz VCO.

Device	**Width (μm)**	**Length (μm)**	**Multiplier**	**Overall Value (fF)**
C_1	10.91	10.91	1	359.07
C_{const}	9.742	9.742	1	285.66
C_{var}	0.74	0.4	1	3.731-16.548
C_{unit}	2	2	1	12.584
C_{2unit}	2	2	2	25.168
C_{4unit}	2	2	4	50.366
C_{8unit}	2	2	8	100.672
C_{16unit}	2	2	16	201.344

The results of harmonic balance, harmonic balance noise and stability (with differential probe for loop gain) simulations are shown in the table 7.5 and Figures 7.8, 7.9, 7.10 and 7.11.

Table 7.5: Simulation results of the 12-15 GHz VCO.

Parameter	**Value**
Frequency Range	12.0 - 15.0 GHz
Tuning Range	3.0 GHz
Tuning Voltage Range	0.0 - 0.8 V
Phase Noise at 1 MHz offset	-87.14 dBc/Hz
Power Consumption	10.1 mW
Loop Gain nominal	3.33
Loop Gain worst case (ss-120)	2.64
Maximum Band K_{VCO}	164 MHz/V

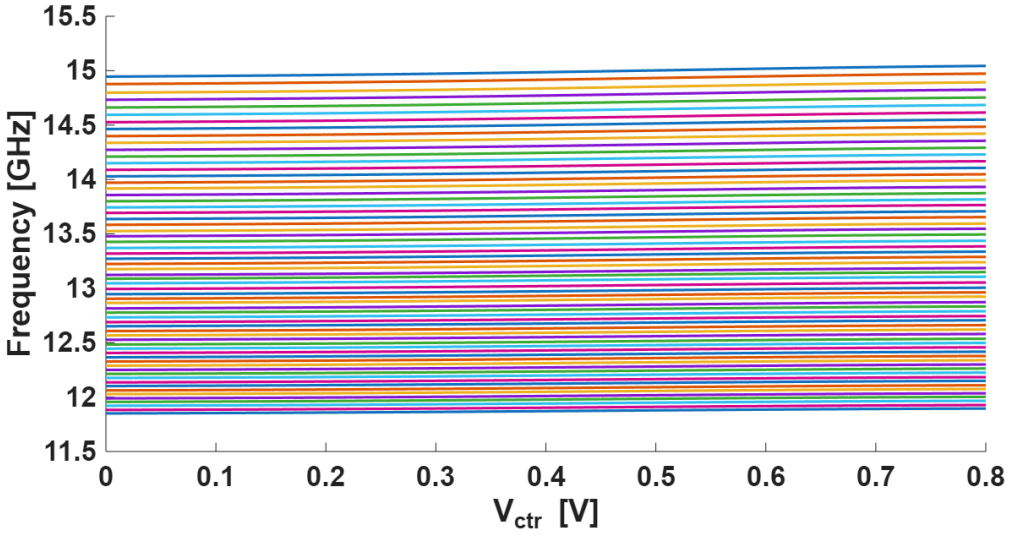

Figure 7.8: Total bands of the 12-15 GHz VCO.

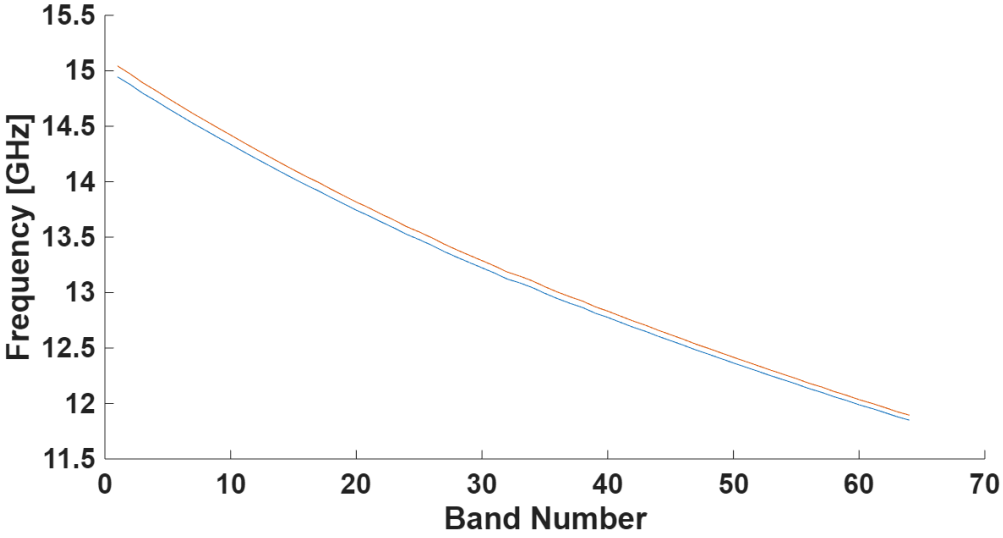

Figure 7.9: Frequency range of the 12-15 GHz VCO.

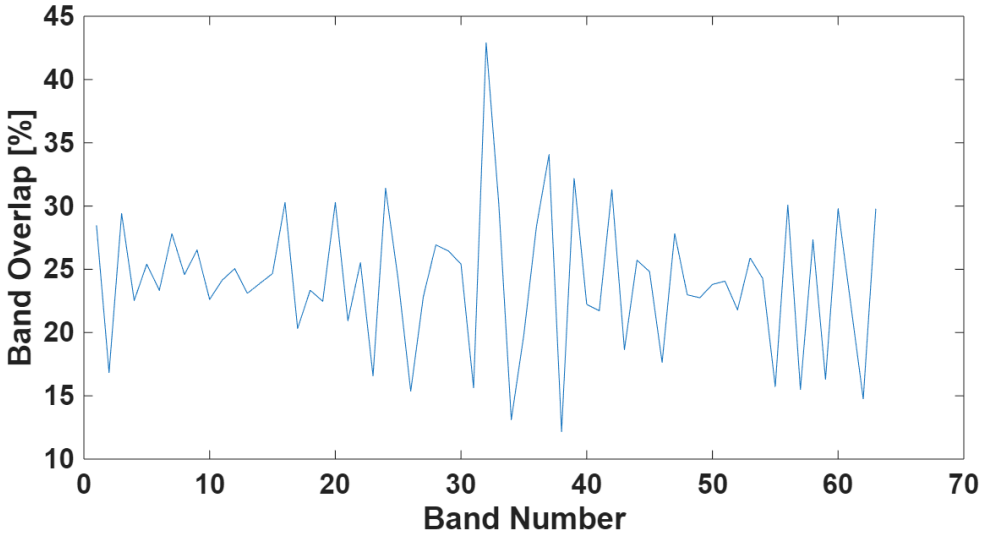

Figure 7.10: Band overlap percentage of the 12-15 GHz VCO.

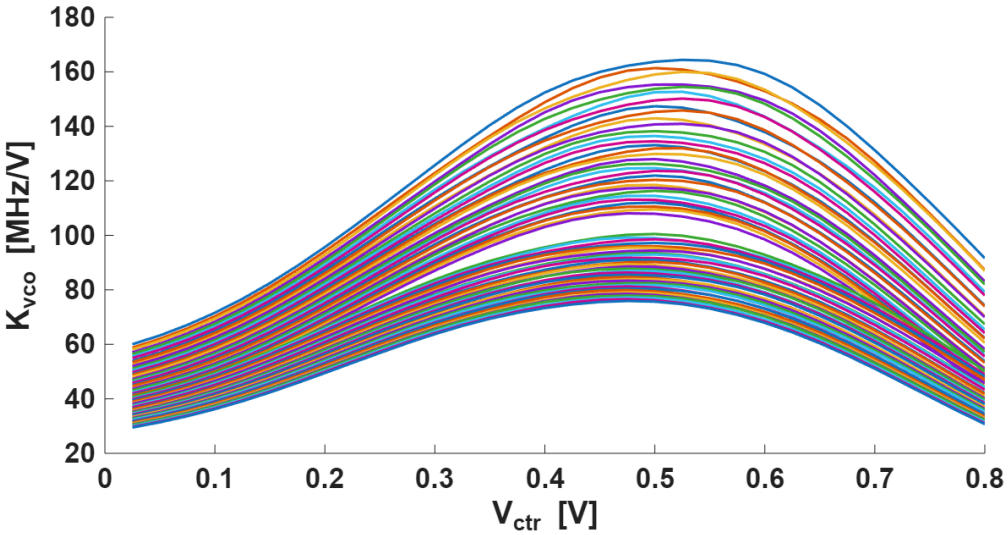

Figure 7.11: K_{VCO} of each band of the 12-15 GHz VCO.

Chapter 8

RF Amplifier Design

An RF amplifier is a circuit that operates at radio frequencies and converts a sinusoidal input signal into a rectangular output signal of the same period. This block is necessary because the LC-tank VCO generates a sinusoidal waveform. Due to the presence of the inductor, the signal amplitude can exceed the supply voltage, resulting in a DC offset. Before feeding this signal to the divider, which is implemented as a chain of D flip-flops (DFFs), it must first be converted into a clean rectangular waveform. Without this conversion, the DFFs may fail to detect rising edges, since a sinusoidal waveform remains above the logic threshold for only a small portion of the period at high output frequencies. Thus, a transformation stage is required. The schematic of the RF amplifier is shown in Figure 8.1.

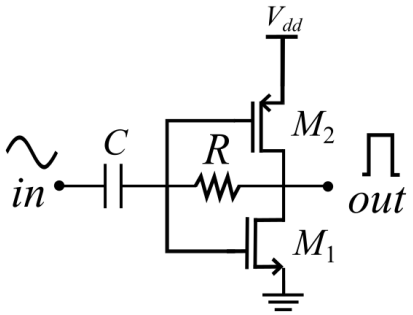

Figure 8.1: Schematic of the RF amplifier circuit.

A coupling capacitor is placed at the input to remove the DC offset of the sinusoidal signal. The core of the circuit is a CMOS inverter biased to operate at its region of maximum small-signal gain. The V_{in}-V_{out} characteristic of the designed inverter, along with its small-signal gain, is shown in Figures 8.2 and 8.3.

By operating near the inverter's maximum gain point, the sinusoidal input is sharply amplified around the switching threshold, resulting in a more rectangular output waveform. To stabilize the operating point, a resistor is connected between the inverter's input and output. This feedback path allows a small current to flow, biasing the inverter close to its optimal DC operating point and ensuring high gain around the zero-crossing of the sinusoid.

The sizing of the capacitor and resistor is critical. The capacitor must be large enough to block the DC offset and filter low-frequency components, but not so large that it pushes the circuit's dominant pole too low in frequency, which would cause the inverter's gain to degrade within the target VCO frequency range (10-15 GHz). The resistor value is equally

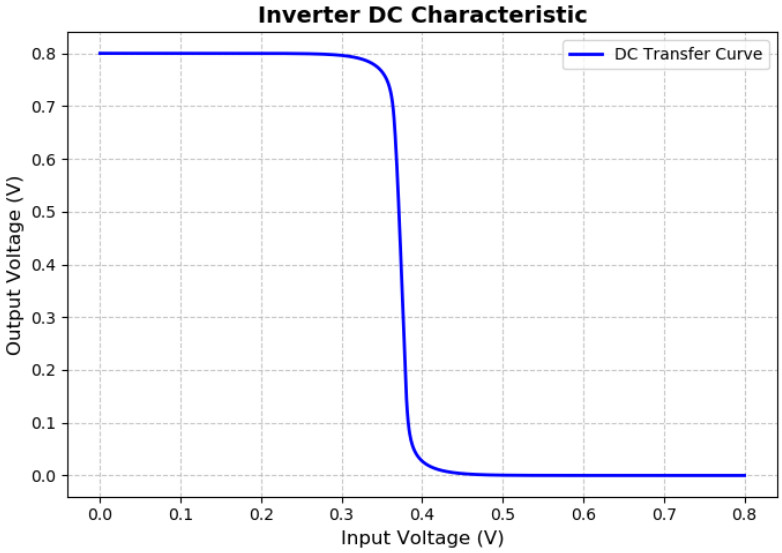

Figure 8.2: Inverter V_{in}-V_{out} characteristic

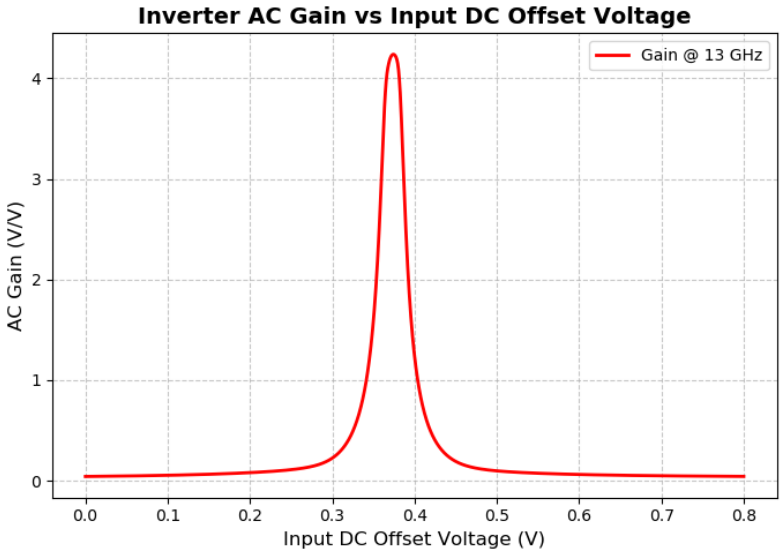

Figure 8.3: Inverter small-signal gain

important: since the peak gain of the inverter occurs slightly below 400 mV, the resistor must be small enough to allow a slight DC offset between the input and output. This ensures proper biasing and keeps the inverter operating at its highest gain point, enabling reliable conversion of the sinusoidal input into a rectangular output.

The final sizing of the RF amplifier components is determined through parametric simulations and is shown in Table 8.1.

Table 8.1: Device sizing of the RF amplifier.

Device	**Width (μm)**	**Length (nm)**	**Fingers**	**Multiplier**	**Type**	**Overall Value**
M_1	1.5	40	15	1	RVT	-
M_2	1.5	40	15	1	RVT	-
C	1.475	1475	-	1	Apmom1v8	10fF
R	0.5	3061	-	4(series)	High-R N+ Poly	18.5kΩ

A realistic transient simulation was performed to verify the correct operation of the circuit. To emulate the actual output of the VCO, a sinusoidal input signal with an amplitude of 800 mV and a DC offset of 800 mV was applied. The results, shown in Figure 8.4, illustrate the input waveform before and after DC offset removal, as well as the corresponding rectangularized output signal.

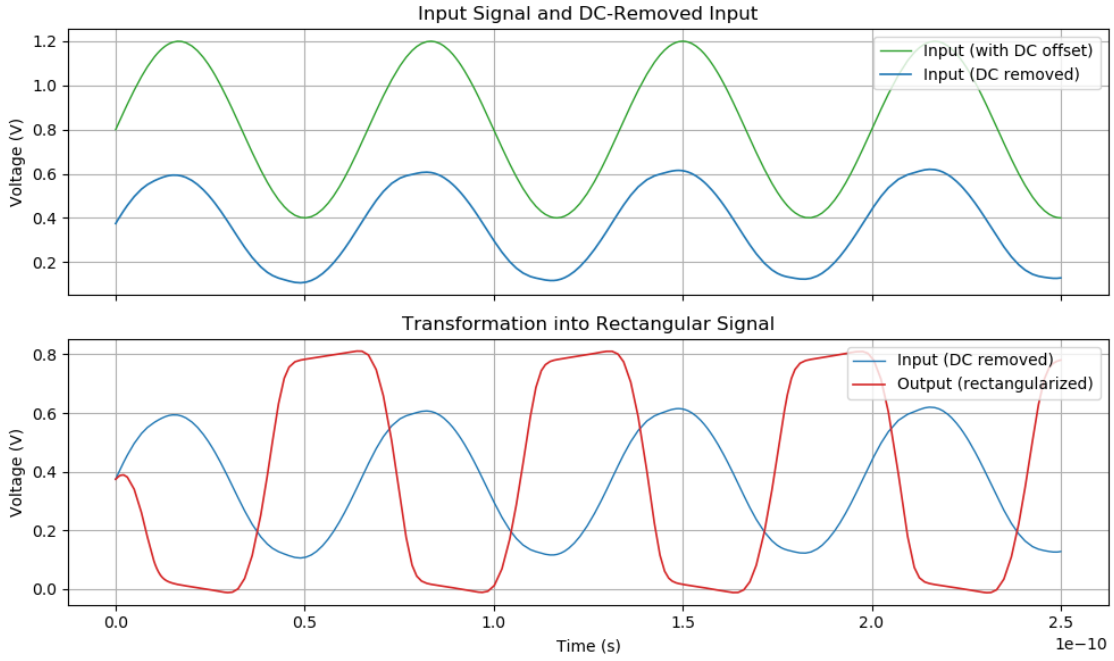

Figure 8.4: Transient simulation of the RF amplifier circuit

Chapter 9

Filter and Loop Analysis

9.1 Role of the Loop Filter in CPPLLs

The loop filter is a critical component in the design and operation of a Phase-Locked Loop (PLL). Its primary role is to process the output of charge pump and generate a control voltage that drives the Voltage-Controlled Oscillator (VCO). Without proper filtering, the control signal would contain high-frequency switching components and noise originating from the PFD and charge pump, which would directly modulate the VCO and degrade the overall system performance.

The loop filter serves several key purposes:

1. **Noise Suppression**: The phase charge pump output typically consists of sharp steps. The loop filter smooths these into a stable control voltage, attenuating unwanted high-frequency components. This significantly reduces phase noise and spurious tones at the PLL output.

2. **Stability of the Control Loop**: A PLL is essentially a feedback system, and like any control loop, its stability depends on the loop dynamics. The loop filter shapes the open-loop transfer function to ensure sufficient phase margin and damping, preventing oscillations or instability.

3. **Bandwidth Control**: The filter defines the loop bandwidth, which determines how quickly the PLL responds to phase or frequency changes. A wider bandwidth improves lock time and jitter tracking but allows more reference noise to pass through. A narrower bandwidth, on the other hand, improves noise performance but increases lock time. The filter therefore provides the flexibility to trade off lock speed against output spectral purity.

4. **Charge Pump Current Matching**: The loop filter also absorbs current mismatches from the charge pump, preventing the build-up of steady-state error at the control voltage. This is crucial for minimizing static phase error.

9.2 2^{nd} Order Loop Filter and its Transfer Function

A second-order loop filter is commonly used in PLL designs due to its balance between complexity and performance. It typically consists of a resistor (R) and two capacitors (C_1 and C_2) arranged in a configuration shown in Figure 9.1.

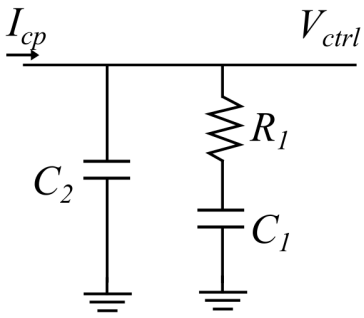

Figure 9.1: Second-Order Loop Filter Configuration

The transfer function of a second-order loop filter can be expressed as:

$$H(s) = \frac{V_{out}(s)}{I_{cp}(s)} = (R_1 + \frac{1}{sC_1})//(\frac{1}{sC_2}) = \frac{sC_1R_1 + 1}{s(sC_1C_2R_1 + C_1 + C_2)} \tag{9.1}$$

In order to make the following analysis easier a simple transformation to the transfer function is made:

$$H(s) = \frac{b}{b+1}\frac{\tau s + 1}{sC_1(\frac{\tau s}{b+1} + 1)} \tag{9.2}$$

where $\tau = R_1C_1$ and $b = \frac{C_1}{C_2}$

The overall PLL linearized block is shown in Figure 9.2.

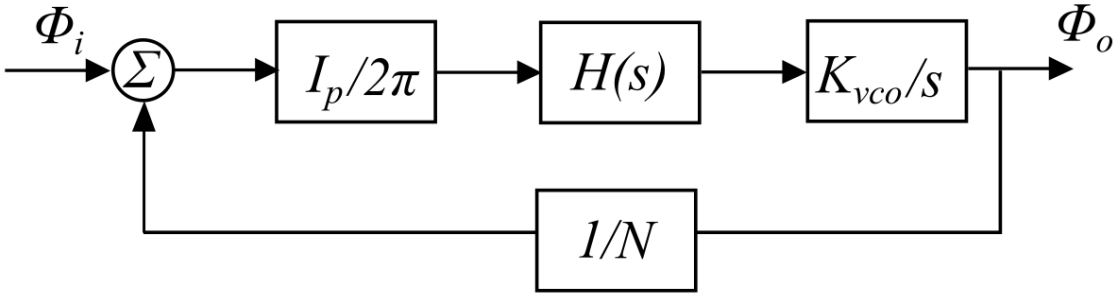

Figure 9.2: Linearized PLL Block Diagram

The transfer function of the PLL can be derived by combining the transfer functions of the PFD, charge pump, loop filter, and VCO. The overall open loop transfer function is given by:

$$H_{PLL}(s) = H_{PFD}(s) \cdot H_{CP}(s) \cdot H_{LF}(s) \cdot H_{VCO}(s) = \frac{\varphi_o}{\varphi_i} = \frac{K_{vco}I_p}{2\pi}\frac{b}{b+1}\frac{\tau s + 1}{s^2C_1(\frac{\tau s}{b+1} + 1)} \tag{9.3}$$

A simple and effective approach and analysis is shown in [9]. The maximum phase margin is:

$$PM_{max} = tan^{-1}(\sqrt{b+1}) - tan^{-1}(\frac{1}{\sqrt{b+1}}) \tag{9.4}$$

To complete the loop analysis it's forced

$$\omega_c = \frac{\sqrt{b+1}}{\tau} \tag{9.5}$$

to be the crossover frequency of the loop and get:

$$\frac{K_{vco}I_p}{2\pi N}\frac{b}{b+1} = \frac{C_1}{\tau^2}\sqrt{b+1} \tag{9.6}$$

A loop filter design recipe can be defined as follows.

1. Find K_{vco} from the VCO simulation.
2. Choose a desired phase margin and find b from 9.4.
3. Choose the loop bandwidth and find τ from 9.5.
4. Select C_1 such that the steady phase v_{ctr} ripple is as desired.
5. Calculate the noise contribution of R_1. If the calculated noise is negligible the design is complete, otherwise go back to step four and increase C_1.

9.3 Filter final sizing and Bode diagrams

The design of the loop filter required an iterative process of tuning and optimization. In particular, the filter capacitors had to be significantly increased to ensure that the control voltage v_{ctrl} exhibited minimal ripple at steady state. A low ripple is essential for maintaining a clean VCO output spectrum, thereby reducing reference spurs near the carrier frequency.

The final values of the filter are shown in the Table 9.1.

Table 9.1: Final device sizing of the loop filter.

Device	**Width (μm)**	**Length (μm)**	**Multiplier**	**Overall Value**	**Type**
C_1	48.73	48.73	16	204.64pF	Apmom1v8
C_2	12.01	12.01	16	12.266pF	Apmom1v8
R_1	0.5	5.21	8(series)	59.051kΩ	High-R N+ Poly

The Bode plots of the loop filter are shown in Figures 9.3 and 9.4. The closed pll loop achieves a cutoff frequency of approximately 55.38 kHz, which satisfies the requirement of keeping the ripple below 1.5 mV. In addition, the phase margin of 63.25° indicates a stable and well-damped design. Overall, this filter implementation ensures robust loop stability, suppresses unwanted noise coupling into the VCO, and directly improves the spectral purity and timing accuracy of the PLL.

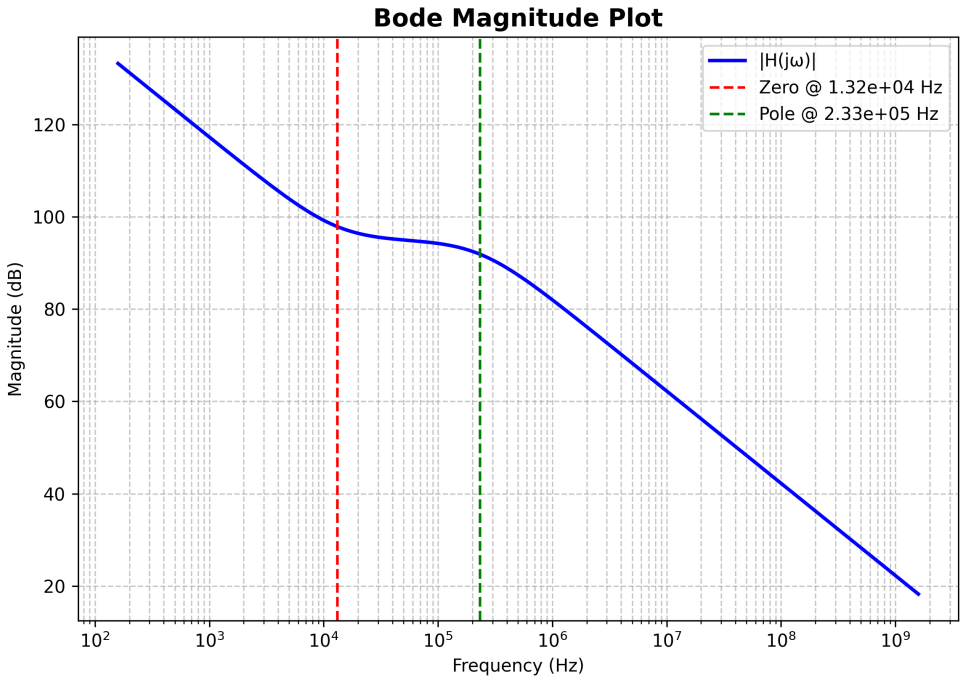

Figure 9.3: Bode magnitude plot of the loop filter

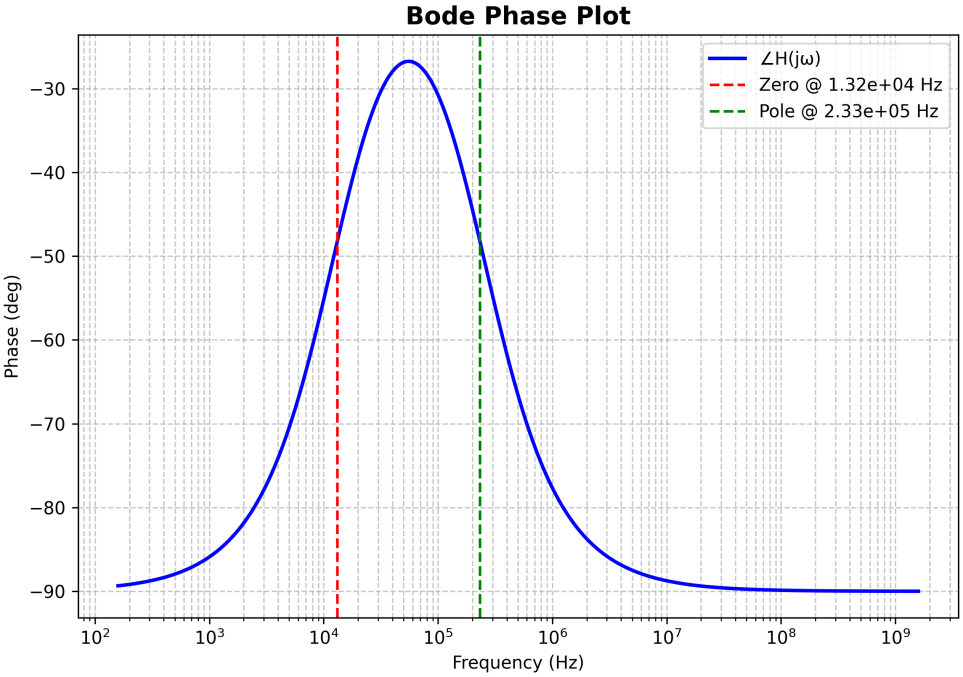

Figure 9.4: Bode phase plot of the loop filter

Chapter 10

Final Simulation Results

10.1 Simulation Setup

The final simulation was obtained by combining all the previous blocks into a single simulation. The setup includes the phase frequency detector, charge pump, filter, voltage controlled oscillator, RF amplifier, and divider as shown in Figure 10.1.

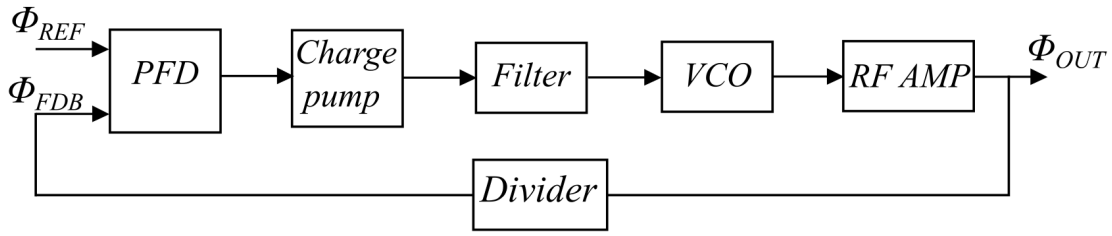

Figure 10.1: Final Simulation Setup

The reference frequency was set to 25.34 MHz, yielding the following target output frequency:

$$f_{out} = f_{ref} \cdot 512 = 12.974 \text{ GHz} \tag{10.1}$$

For proper locking, the PLL operates with the first VCO, which covers the frequency range of 10–13 GHz. In this configuration, the second-to-last band of the 64 available bands was selected. This setup is necessary because the implemented PLL does not include an automatic band-selection circuit to detect when the control voltage v_{ctrl} approaches the limits of a band and switch accordingly.

The transient simulation was carried out over a duration of 20 µs to capture the steady-state behavior of the PLL. This time window was chosen to ensure that the loop dynamics, including lock acquisition and stabilization of the control voltage, were fully observable and that the system had sufficient margin to reach steady-state operation.

10.2 Simulation Results

The results of the final transient simulation are summarized below.

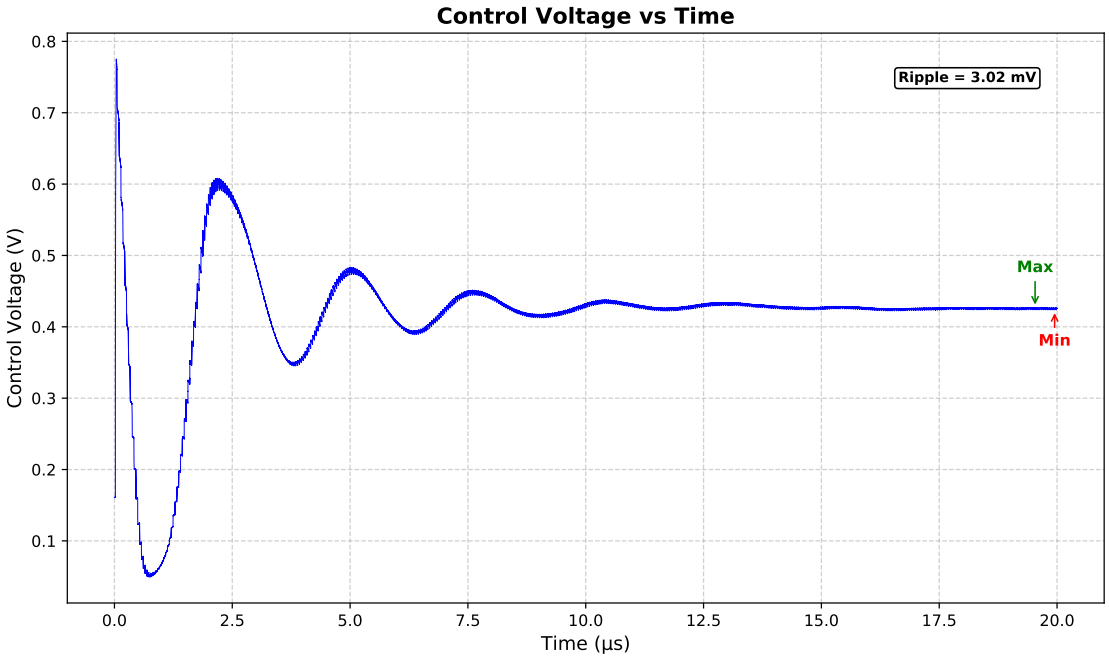

Figure 10.2: Control Voltage v_{ctrl}

The most critical metric of a PLL is the control voltage. The results clearly demonstrate system stability, with a locking time of approximately 17 μs and a steady-state ripple of about $3mV$. To achieve this low ripple, the loop filter capacitors were significantly enlarged, as discussed in Section 9.3.

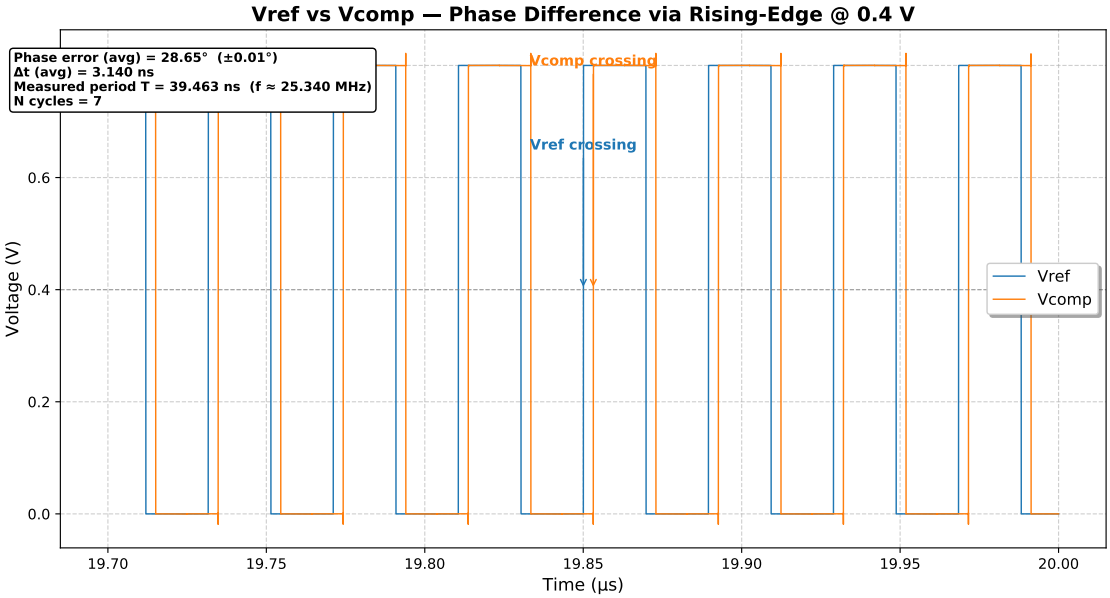

Figure 10.3: Reference Voltage V_{ref} and Feedback Voltage $V_{feedback}$

Next, the comparison between V_{ref} and $V_{feedback}$ highlights the steady-state phase error, which is approximately 28.65°. Given the inherent offset, such a phase error is expected. The theoretical value is $\frac{180°}{7} = 25.71°$, and the additional deviation can be attributed to propagation delays through the DFFs and logic gates preceding the charge pump. Importantly, across multiple simulations, the phase error consistently ranged between 27.8° and 29.1°, demonstrating stability. If required, this residual phase error could be corrected with a phase-shifter circuit.

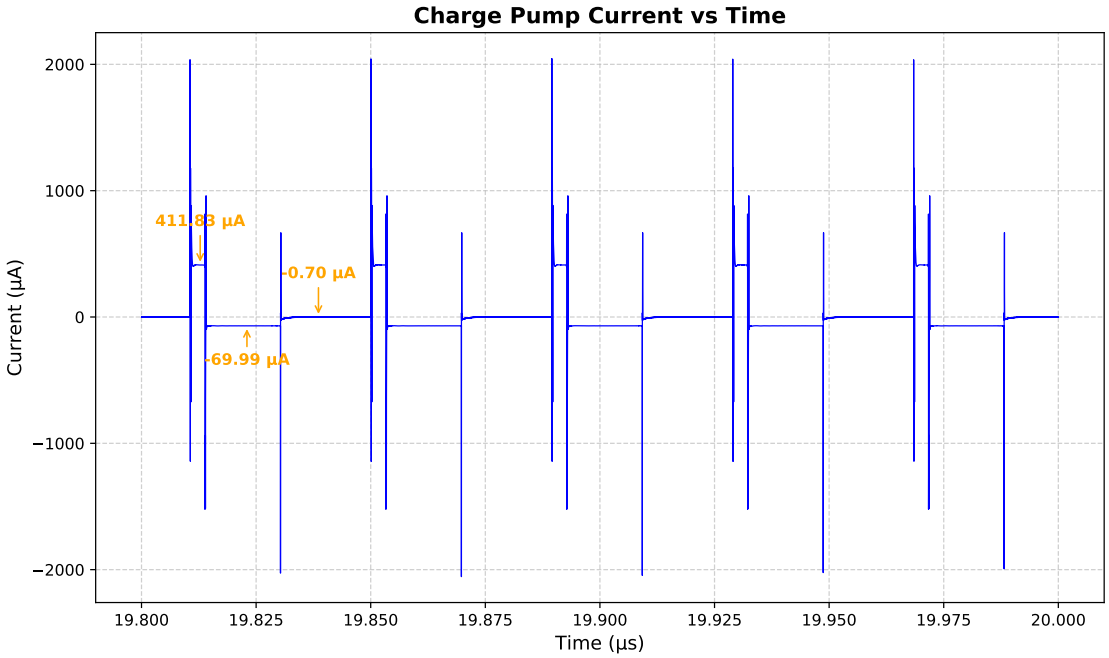

Figure 10.4: Charge Pump Output Current

The output current of the charge pump further validates the behavior of the system. Due to the offset current, the UP branch is briefly activated each period to maintain stability of V_{ctrl}. For the remainder of the cycle, one half-period is dominated by a negative offset current, while the other half-period shows nearly zero current flow.

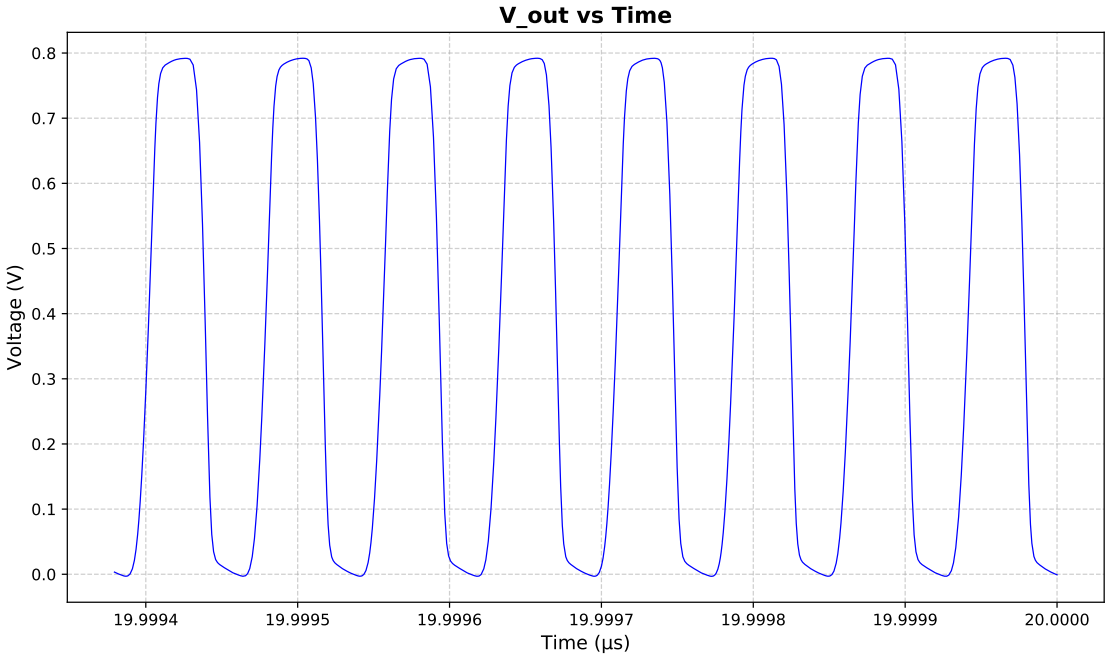

Figure 10.5: VCO Output Waveform

The output of the RF amplifier is also shown. The waveform is nearly rectangular, which is sufficient for digital logic, since subsequent circuits only require a clean rising edge to function correctly.

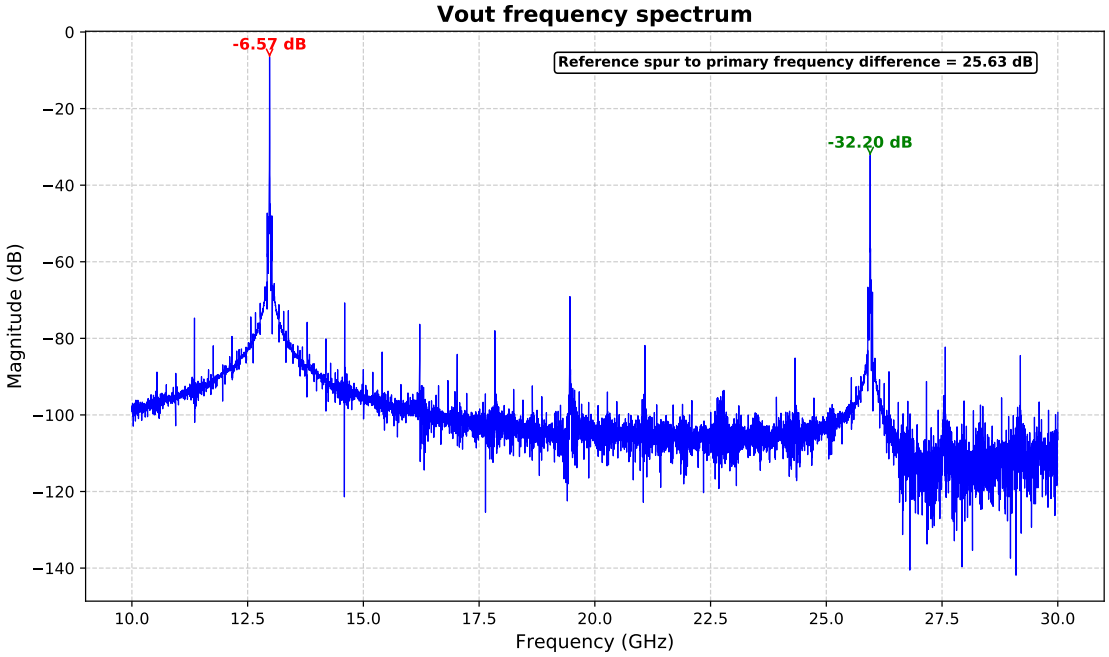

Figure 10.6: Output Spectrum of the PLL

Finally, the output spectrum demonstrates that the PLL delivers a clean signal. Reference spurs are suppressed by at least 25.63 dB relative to the carrier, which is well within

acceptable limits for this design.

Overall, the PLL meets its primary design targets in terms of stability, lock time, phase error, and spectral purity, confirming the validity and robustness of the implemented architecture.

Chapter 11

Conlusion and Future Work

11.1 Conclusion

This thesis has presented the design, implementation, and evaluation of a Phase-Locked Loop (PLL) operating in the 10-15 GHz frequency range. The motivation for this work lies in the increasing demand for precise frequency synthesis and signal synchronization in modern communication and high-frequency systems. From the initial exploration of PLL fundamentals to the practical simulation results, this study has highlighted both the theoretical underpinnings and practical challenges of realizing a robust design.

The key contributions of this work can be summarized as follows. First, a detailed examination of the PLL's building blocks—phase detector, loop filter, charge pump, and voltage-controlled oscillator—was carried out, with emphasis on their interdependencies. Special attention was devoted to the loop filter, whose capacitor sizing was critical for minimizing ripple on the control voltage. The resulting design achieved a stable steady-state control voltage with a ripple of approximately 3 mV and a lock time of about 17 μs, validating the importance of careful filter design in determining overall PLL performance.

Second, the analysis of the reference and feedback signals revealed a steady-state phase error of approximately 28.65°. While higher than the theoretical 25.71°, this deviation was shown to be consistent across simulations and could be attributed to propagation delays in the flip-flops and logic gates preceding the charge pump. This stability suggests that the error can be readily compensated by a dedicated phase-shifting circuit. Third, the behavior of the charge pump current confirmed correct functionality, with the UP branch momentarily activated each cycle to balance offset currents and maintain loop stability. Finally, the spectral analysis of the output demonstrated high signal purity, with reference spurs suppressed by more than 25 dB, an acceptable level for practical communication applications.

Taken together, these results confirm that the PLL architecture developed in this work successfully meets its primary design objectives: stability, rapid lock time, controlled phase error, and spectral cleanliness. The system not only demonstrates the feasibility of high-frequency PLL design in the 10-15 GHz range but also illustrates practical design trade-offs that must be addressed in real-world implementations.

Beyond its technical findings, this thesis also provides broader value as a reference for future students and engineers interested in PLL and RF circuit design. The methodology employed—combining theoretical analysis, iterative design through simulation, and careful interpretation of results—offers a framework that can be adapted to other high-frequency design problems. The lessons learned here, particularly regarding loop filter sizing and error

analysis, are directly applicable to a wide variety of communication and instrumentation systems.

11.2 Future Work

While the present design achieves its intended goals, there remains significant potential for improvement and extension. Several directions for future work are outlined below:

1. Implementation of a phase shifter to eliminate the steady-state phase error, as demonstrated in [10].
2. Development of an automatic band-selection circuit to detect when V_{ctrl} approaches its limits and switch frequency bands accordingly.
3. Integration of an RF switch to enable seamless operation between the two VCOs considered in this work [11].
4. Addition of a programmable prescaler to enable fractional-N division, expanding flexibility beyond fixed integer ratios [12].
5. Further optimization of the VCO to reduce phase noise and improve spectral performance.
6. Implementation of a bandgap reference circuit for improved biasing stability across temperature and process variations. [13]
7. Design and integration of a crystal oscillator to provide a complete, standalone reference source.

In conclusion, this thesis has demonstrated the design of a high-frequency PLL and explored the modern techniques required to push its performance toward practical limits. The insights and methodologies presented here will serve as a valuable foundation for future research and development, enabling more advanced PLL architectures and fostering continued innovation in RF system design.

Bibliography

[1] V. Issakov and S. Trotta, "Low-power dual-modulus frequency divider by 4/5 up to 13-ghz in 0.13µm cmos," *2017 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS)*, 2017.

[2] D. B. Jyuoti Sharma, Tarun Varma, "A brief review of the various phase-frequency detector architectures," *2021 IEEE International Symposium on Smart Electronic Systems (iSES)*, 2021.

[3] D. Qiu, X. Kong, M. Jian, J. Zheng, and C. Guo, "A 1-v 9.6-ghz charge-pump pll with low rms-integrated jitter," *Microelectronics Journal 142 (2023) 106006*, vol. 142, 2023.

[4] J.-S. Lee, M.-S. Keel, S.-I. Lim, and S. Kim, "Charge pump with perfect current matching characteristics in phase-locked loops," *ELECTRONICS LETTERS 9th November 2000*, 2000.

[5] M. M. Elsayed, M. Abdul-Latif, and E. Sánchez-Sinencio, "A spur-frequency-boosting pll with a -74 dbc reference-spur suppression in 90 nm digital cmos," *IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 48, NO. 9, SEPTEMBER 2013*, vol. 48, no. 9, 2013.

[6] X. Gao, E. A. M. Klumperink, P. F. J. Geraedts, and B. Nauta, "Jitter analysis and a benchmarking figure-of-merit for phase-locked loops," *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 56, NO. 2, FEBRUARY 2009*, vol. 56, no. 2, 2009.

[7] J. Wu, M. Hu, X. Wu, Y. Zuo, C. Wan, L. Zheng, and W. Sun, "A low jitter fractional pll with offset current charge pump," *Microelectronics Journal 138 (2023) 105833*, vol. 138, 2023.

[8] B. Razavi, "Voltage controlled oscillators." `https://www.seas.ucla.edu/brweb/teaching/215C_W2013/VCOs1.pdf`, 2013. Accessed: 2025-08-13.

[9] H. R.Rategh, H. Samavati, and T. H.Lee, "A cmos frequency synthesizer with an injection-locked frequency divider for a 5-ghz wireless lan receiver," *IEEE JOURNAL ON SOLID-STATE CIRCUITS, VOL. 35, NO. 5, MAY 2000*, vol. 35, no. 5, 2000.

[10] K.-J. Koh and G. M. Rebeiz, "0.13-µm cmos phase shifters for x-, ku-, and k-band phased arrays," *IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 11, NOVEMBER 2007*, vol. 42, no. 11, 2007.

[11] J. Park and Z. Ma, "15 ghz cmos rf switch employing large-signal impedance matching," *Digest of Papers. 2006 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2006.

[12] P. Larsson, "High-speed architecture for a programmable frequency divider and a dual-modulus prescaler," *IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 31, NO. 5, MAY 1996*, vol. 31, no. 5, 1996.

[13] J. M. Lee, Y. Ji, S. Choi, Y.-C. Cho, S.-J. Jang, and J. S. Choi, "A 29nw bandgap reference circuit," *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015.

[14] R. Manikandan and B. Amrutur, "A zero charge-pump mismatch current tracking loop for reference spur reduction in plls," *Microelectronics Journal 46 (2015) 422-430*, vol. 46, 2015.

[15] A. Redan, M. F. Ibrahim, and F. Farag, "Input-output rail-to-rail cmos ccii for low voltage-low power applications," *Microelectronics Journal 48 (2016) 60-75*, vol. 48, 2016.