National Technical University of Athens
School of Electrical and Computer Engineering
Division of Electric Power

# Current-limiting methods for grid-forming inverters and their effect on transient stability

DIPLOMA THESIS

**ANTONIS MAKRIGIORGIS**

**Supervisor**: Antonios Antonopoulos
Associate Professor, NTUA

Athens, September 2025

National Technical University of Athens
School of Electrical and Computer Engineering
Division of Electric Power

# Current-limiting methods for grid-forming inverters and their effect on transient stability

DIPLOMA THESIS

**ANTONIS MAKRIGIORGIS**

**Supervisor**: Antonios Antonopoulos
Associate Professor, NTUA

Approved by the three-member scientific committee on the 19th of September 2025.

| ..... | ..... | ..... |
|---|---|---|
| Antonios Antonopoulos<br>Associate Professor, NTUA | Vasileios Nikolaidis<br>Assistant Professor, NTUA | Constantinos Vournas<br>Professor Emeritus, NTUA |

Athens, September 2025

.....
**Antonis Makrigiorgis**
Graduate of School of Electrical and Computer Engineering, National Technical University of Athens

# Περίληψη

Η μετάβαση του συστήματος ηλεκτρικής ενέργειας από ένα σύστημα που κυριαρχείται από σύγχρονες μηχανές σε ένα σύστημα που κυριαρχείται από μετατροπείς ηλεκτρονικών ισχύος, έχει επιφέρει σημαντικές τεχνικές και λειτουργικές προκλήσεις. Οι αντιστροφείς διαμόρφωσης δικτύου θεωρούνται μια υποσχόμενη λύση για την ενίσχυση της ευστάθειας των μελλοντικών συστημάτων ηλεκτρικής ενέργειας και για την διευκόλυνση της ενσωμάτωσης των μετατροπέων ηλεκτρονικών ισχύος στο δίκτυο, σε μεγάλη κλίμακα. Σε αντίθεση με τις σύγχρονες γεννήτριες, οι αντιστροφείς διαμόρφωσης δικτύου έχουν περιορισμένη αντοχή σε υπερένταση. Επομένως, οι μέθοδοι περιορισμού του ρεύματος είναι απαραίτητες για την προστασία των στοιχείων του μετατροπέα. Ο σκοπός της παρούσας διπλωματικής εργασίας είναι η κατανόηση των μεθόδων που χρησιμοποιούνται για τον περιορισμό του ρεύματος των αντιστροφέων διαμόρφωσης δικτύου σε διαταραχές, καθώς και η μελέτη της επίδρασης των μεθόδων αυτών στην μεταβατική ευστάθεια.

Αρχικά, παρουσιάζεται μια εκτενής ανασκόπηση των συχνά χρησιμοποιούμενων μεθόδων ελέγχου διαμόρφωσης δικτύου και περιορισμού ρεύματος, η οποία ακολουθείται από την υλοποίηση αρκετών από αυτές τις μεθόδους στο λογισμικό προσομοίωσης PLECS. Στην συνέχεια, πραγματοποιούνται προσομοιώσεις για την επιβεβαίωση της αποτελεσματικής λειτουργίας των υλοποιημένων μεθόδων περιορισμού ρεύματος σε διάφορα σφάλματα, καθώς και για την ανάδειξη διαφορών στην απόκριση τους.

Έπειτα, μελετάται η μεταβατική ευστάθεια των αντιστροφέων διαμόρφωσης δικτύου μέσω καμπυλών ισχύος-γωνίας, οι οποίες προκύπτουν από τα μοντέλα μεγάλου σήματος των χρησιμοποιούμενων μεθόδων περιορισμού ρεύματος. Παρουσιάζεται η θεωρητική πορεία ισχύος-γωνίας για βραχυκυκλώματα και αναλύεται η επίδραση του περιορισμού ρεύματος στην μεταβατική ευστάθεια. Τα μοντέλα μεγάλου σήματος και η θεωρητική ανάλυση επιβεβαιώνονται μέσω προσομοιώσεων.

Τέλος, πραγματοποιούνται προσομοιώσεις πραγματικού χρόνου για την αξιολόγηση της απόδοσης των υλοποιημένων μεθόδων περιορισμού ρεύματος, υπό συνθήκες πραγματικού χρόνου. Τα συστήματα ελέγχου υλοποιούνται σε έναν μικροελεγκτή, ο οποίος αλληλεπιδρά με το υπόλοιπο προσομοιωμένο σύστημα. Τα αποτελέσματα των προσομοιώσεων πραγματικού χρόνου δείχνουν ότι οι υλοποιημένες τεχνικές περιορισμού ρεύματος μπορούν να περιορίσουν αποτελεσματικά το ρεύμα για διαφορετικούς τύπους διαταραχών, υπό συνθήκες πραγματικού χρόνου.

**Λέξεις κλειδιά**: Αντιστροφείς διαμόρφωσης δικτύου, Μέθοδοι περιορισμού ρεύματος, Ελεγκτής στατισμού, Αδρανειακή συμπεριφορά, Μεταβατική ευστάθεια, Προσομοίωση πραγματικού χρόνου

# Abstract

The ongoing transformation of the power system from synchronous machine dominated to power electronic converter dominated, poses major technical and operational challenges. Grid-forming inverters are considered as a promising solution to enhance the stability of future power grids and facilitate the large-scale integration of power electronic converters into the grid. Unlike synchronous generators, the overcurrent capability of grid-forming inverters is limited. Therefore, overcurrent limiting methods are essential to prevent hardware damage of the converter. To that end, the main objective of this thesis is to understand the methods that are used to limit the current of grid-forming inverters during off-nominal conditions and to assess the effect of these methods on the transient stability.

First, a comprehensive review of common grid-forming and current-limiting control methods is presented, followed by the implementation of several of these methods in the PLECS simulation software. Then, time-domain simulations are carried out to validate the effectiveness of the implemented current-limiting methods under various types of disturbances and to highlight differences in their responses.

Next, the transient stability of grid-forming inverters is studied, through power-angle characteristics derived from the large-signal models of the employed current-limiting methods. The theoretical power-angle trajectory for short circuits is presented and the effect of current limitation on the transient stability margin is illustrated. The large-signal models and the theoretical analysis are validated through time-domain simulations.

Finally, hardware-in-the-loop real-time simulations are performed to assess the performance of the implemented current-limiting methods, under real-time conditions. The control systems are implemented on a microcontroller, which interacts with the rest of the simulated system. The results of the real-time simulations indicate that the implemented current-limiting techniques can effectively restrict the current for different types of disturbances, under real-time conditions.

**Keywords**: Grid-forming inverters, Current-limiting methods, Droop control, Inertial effect, Transient stability, Real-time simulation

# Acknowledgments

First and foremost, I am sincerely grateful to my supervisor, Prof. Antonios Antonopoulos, for his trust, guidance and invaluable advice on both technical and non-technical questions. His continuous encouragement and effective cooperation played a crucial role in the completion of this thesis.

I would also like to thank Mustafa Ibrahim and Marcio Magalhães de Oliveira for the technical discussions and for giving me the opportunity to visit the Section of System Studies, HVDC & FACTS of AFRY, in Sweden.

Moreover, I would like to thank my lab-mates Alkis and Christos, for creating a pleasant atmosphere in the lab and for the countless coffees we had throughout this thesis.

Last but not least, I would like to sincerely thank Iro for her continuous support, encouragement and patience throughout this work.

# Contents

# Εκτεταμένη Ελληνική Περίληψη

## Κεφάλαιο 1. Εισαγωγή

Τα παραδοσιακά συστήματα ηλεκτρικής ενέργειας (ΣΗΕ) υφίστανται πολύ μεγάλες αλλαγές, λόγω της ανάγκης αντιμετώπισης της υπερθέρμανσης του πλανήτη. Παρατηρείται μια στροφή προς πιο καθαρές μορφές παραγωγής ηλεκτρικής ενέργειας, η οποία οδηγεί στην σταδιακή αντικατάσταση των μεγάλων κεντρικών θερμικών σταθμών παραγωγής με μικρότερης κλίμακας Ανανεώσιμες Πηγές Ενέργειας (ΑΠΕ), όπως ηλιακή και αιολική ενέργεια.

Στα παραδοσιακά ΣΗΕ κυριαρχούσαν οι σύγχρονες γεννήτριες, οι οποίες αναλάμβαναν την ρύθμιση τάσης και συχνότητας. Οι σύγχρονες γεννήτριες συμπεριφέρονται ως πηγές τάσης και έχουν μεγάλη αδράνεια δρομέα. Αυτά τα χαρακτηριστικά είναι αναγκαία για την ευσταθή λειτουργία του ΣΗΕ. Αντίθετα, οι πλειονότητα των ΑΠΕ συνδέονται στο δίκτυο μέσω αντιστροφέων ηλεκτρονικών ισχύος (inverters) και επομένως αναφέρονται με τον όρο “Inverter-Based Resources” (IBRs). Οι αντιστροφείς έχουν μεγάλες διαφορές σε σχέση με τις σύγχρονες γεννήτριες, όχι μόνο ως προς τα τεχνικά τους χαρακτηριστικά, αλλά και στον τρόπο που ανταποκρίνονται σε διαταραχές στο δίκτυο. Σε αντίθεση με τις σύγχρονες γεννήτριες, η λειτουργία των αντιστροφέων καθορίζεται κυρίως από το σύστημα ελέγχου τους. Επομένως, η μετάβαση από ένα ΣΗΕ που κυριαρχείται από σύγχρονες γεννήτριες σε ένα ΣΗΕ που κυριαρχείται από IBRs, έχει φέρει πολλές προκλήσεις, οι οποίες πρέπει να αντιμετωπιστούν για να εξασφαλιστεί η ευστάθεια των μελλοντικών ΣΗΕ.

Οι αντιστροφείς που συνδέονται στο δίκτυο χωρίζονται σε δύο βασικές κατηγορίες, ανάλογα με το σύστημα ελέγχου τους. Οι δύο κατηγορίες είναι οι αντιστροφείς ακολούθησης δικτύου (grid-following inverters) και οι αντιστροφείς διαμόρφωσης δικτύου (grid-forming inverters). Παρόλο που οι grid forming (GFM) και grid following (GFL) αντιστροφείς έχουν παρόμοια τεχνικά χαρακτηριστικά (hardware) και κοινό στόχο την ανταλλαγή ενεργού και άεργου ισχύος με το δίκτυο, διαφέρουν σημαντικά στα συστήματα ελέγχου, στην μοντελοποίηση τους και στην απόκρισή τους σε διαταραχές στο δίκτυο.

Οι GFLIs, οι οποίοι αποτελούν την πλειονότητα των αντιστροφέων συνδεδεμένων στο δίκτυο, συγχρονίζονται με την τάση του δικτύου μέσω μιας μονάδας συγχρονισμού (π.χ PLL) και ανταλλάζουν ενεργό και άεργο ισχύ με το δίκτυο ελέγχοντας τις κατάλληλες συνιστώσες ρεύματος. Λόγω αυτής της τεχνικής ελέγχου, οι GFLIs συμπεριφέρονται ως πηγές ρεύματος. Ένα ΣΗΕ που κυριαρχείται από αντιστροφείς δεν μπορεί να λειτουργήσει χρησιμοποιώντας μόνο GFLIs, αφού χρειάζονται μια καλά ορισμένη τάση προκειμένου να συγχρονιστούν με το δίκτυο. Από την άλλη, οι GFMIs ελέγχονται με τέτοιο τρόπο ώστε να συμπεριφέρονται ως πηγές τάσης, με αποτέλεσμα να αποκρίνονται σε διαταραχές στο δίκτυο, παρόμοια με τις σύγχρονες γεννήτριες. Επομένως, οι GFMIs θεωρούνται μια πολύ υποσχόμενη λύση για την ενίσχυση της ευστάθειας των μελλοντικών ΣΗΕ.

Λόγω της συμπεριφοράς των GFMI ως πηγές τάσης, η στιγμιαία αντίδραση τους σε διαταραχές του δικτύου είναι να κρατήσουν την εσωτερική τους τάση σταθερή. Αυτό έχει ως

αποτέλεσμα την στιγμιαία αλλαγή του ρεύματος εξόδου τους. Παρότι η απόκριση αυτή είναι επιθυμητή, είναι προφανές ότι το ρεύμα του αντιστροφέα είναι πολύ ευαίσθητο στις συνθήκες του δικτύου, καθώς δεν ελέγχεται άμεσα. Επομένως, όταν η διαταραχή στο δίκτυο είναι επαρκώς μεγάλη (π.χ ένα τριφασικό βραχυκύκλωμα), αν δεν ληφθούν μέτρα, το ρεύμα θα υπερβεί το ονομαστικό επίπεδο. Αντίθετα με τις σύγχρονες μηχανές, οι οποίες μπορούν να αντέξουν ρεύματα αρκετές φορές μεγαλύτερα από το ονομαστικό για κάποιο χρονικό διάστημα, οι αντιστροφείς έχουν πολύ μικρές αντοχές σε υπερεντάσεις. Συνεπώς, προκειμένου οι GFMI να παραμένουν συνδεδεμένοι και να υποστηρίζουν το δίκτυο σε τέτοιες διαταραχές, πρέπει να υλοποιηθούν τεχνικές περιορισμού του ρεύματος τους.

Τα τελευταία χρόνια έχουν αναπτυχθεί πολλές μέθοδοι περιορισμού του ρεύματος των GFMI. Όταν ενεργοποιείται ο περιοριστής ρεύματος λόγω κάποιας διαταραχής, ο αντιστροφέας δεν μπορεί να κρατήσει σταθερή την εσωτερική του τάση. Συνεπώς, η δυναμική συμπεριφορά του αντιστροφέα κατά και μετά το σφάλμα καθορίζεται κυρίως από την τεχνική περιορισμού ρεύματος που χρησιμοποιεί. Ως αποτέλεσμα, παρόλο που ο βασικός στόχος των μεθόδων αυτών είναι η προστασία των στοιχείων του αντιστροφέα, επηρεάζουν παράλληλα και ζητήματα που αφορούν το ΣΗΕ, όπως η μεταβατική ευστάθεια, ο συντονισμός των προστασιών κλπ. Για τον λόγο αυτό, μια μέθοδος περιορισμού ρεύματος πρέπει να τηρεί κάποια κριτήρια που αφορούν τον ίδιο τον αντιστροφέα, αλλά και το ΣΗΕ.

# Κεφάλαιο 2. Αντιστροφείς διαμόρφωσης δικτύου και μέθοδοι περιορισμού ρεύματος

***Αντιστροφείς διαμόρφωσης δικτύου***

Η πλειονότητα των grid forming μεθόδων ελέγχου μπορεί να περιγραφεί από ένα γενικό σύστημα ελέγχου. Οι είσοδοι του συστήματος είναι οι μετρήσεις για τα τριφασικά ρεύματα και τις τάσεις και οι τιμές αναφοράς για την ενεργό/άεργο ισχύ, την συχνότητα και το μέτρο της τάσης, ενώ η έξοδος είναι η αναφορά τάσης που τροφοδοτείται για την διαμόρφωση του αντιστροφέα. Το γενικό σύστημα ενός GFMI αποτελείται από διάφορα υποσυστήματα και επίπεδα, τα οποία είναι υπεύθυνα για διαφορετικές λειτουργίες. Για παράδειγμα το εξωτερικό επίπεδο ελέγχου παράγει τα χαρακτηριστικά της αναφοράς πηγής τάσης (μέτρο και γωνία), ενώ ο σκοπός του εσωτερικού επιπέδου είναι η ακολούθηση της αναφοράς αυτής.

Το εξωτερικό επίπεδο περιλαμβάνει τον ελεγκτή ενεργού ισχύος (ή βρόχος συγχρονισμού) και τον ελεγκτή άεργου ισχύος (ή βρόχος διαχείρισης του προφίλ τάσης), οι οποίοι είναι υπεύθυνοι για τον συγχρονισμό του αντιστροφέα με το δίκτυο και τη ρύθμιση τάσης αντίστοιχα. Συγκεκριμένα, ο ελεγκτής ενεργού ισχύος ρυθμίζει την ενεργό ισχύ και παρέχει στην έξοδό του την γωνία/συχνότητα της εσωτερικής τάσης του αντιστροφέα. Από την άλλη, ο βρόχος διαχείρισης του προφίλ τάσης συνδέεται με την άεργο ισχύ, και παρέχει το μέτρο της εσωτερικής τάσης του αντιστροφέα. Το εσωτερικό επίπεδο μπορεί να περιέχει επιπρόσθετους ελεγκτές τάσης και ρεύματος, ή μπορεί να παραληφθεί αφού η έξοδος του εξωτερικού επιπέδου είναι επαρκής για την υλοποίηση της συμπεριφοράς πηγής τάσης.

Υπάρχουν πολλές υλοποιήσεις για κάθε υποσύστημα του γενικού συστήματος ελέγχου και ο συνδυασμός τους οδηγεί σε αρκετές grid forming μεθόδους ελέγχου, οι οποίες διαφέρουν στην υλοποίηση του κάθε υποσυστήματος. Για παράδειγμα, κάποιες μέθοδοι ελέγχου που χρησιμοποιούνται συχνά για τον ελεγκτή ενεργού ισχύος είναι ο ελεγκτής στατισμού χωρίς και με βαθυπερατό φίλτρο και η μέθοδος Εικονικής Σύγχρονης Γεννήτριας. Μάλιστα, οι δύο τελευταίες είναι ισοδύναμες μεταξύ τους. Για τον βρόχο διαχείρισης του προφίλ τάσης μπορεί παρόμοια να χρησιμοποιθεί ελεγκτής στατισμού χωρίς και με βαθυπερατό φίλτρο, καθώς και PI ελεγκτές για το μέτρο της τάσης και για την άεργο ισχύ. Το εσωτερικό επίπεδο (αν

χρησιμοποιηθεί) μπορεί να αποτελείται από ένα ή δυο βρόχους ελέγχου. Για παράδειγμα μια υλοποίηση με έναν βρόχο, ελέγχει το μέτρο της τάσης. Μια πολύ συχνά χρησιμοποιούμενη υλοποίηση με δύο βρόχους περιλαμβάνει έναν ελεγκτή τάσης και έναν ελεγκτή ρεύματος, ενώ μια παρόμοια υλοποίηση αποτελείται από έναν βρόχο εικονικής αγωγιμότητας και έναν ελεγκτή ρεύματος.

***Μέθοδοι περιορισμού ρεύματος***

Για την προστασία των GFMI σε περίπτωση σφαλμάτων, έχουν προταθεί στη βιβλιογραφία διάφορες μέθοδοι περιορισμού ρεύματος, οι οποίες μπορούν να ταξινομηθούν σε άμεσες, έμμεσες ή υβριδικές, ανάλογα με τον τρόπο με τον οποίο επιτυγχάνουν τον περιορισμό του ρεύματος. Συγκεκριμένα, οι άμεσες μέθοδοι περιορίζουν το ρεύμα προσαρμόζοντας κατάλληλα τις τιμές αναφοράς που παρέχονται στον ελεγκτή ρεύματος. Από την άλλη, οι έμμεσες μέθοδοι επιχειρούν να περιορίσουν το ρεύμα μειώνοντας το μέτρο της διαφοράς μεταξύ της εσωτερικής τάσης του αντιστροφέα και της τάσης στο σημείο σύνδεσης του, ή προσαρμόζοντας τις αναφορές ενεργού και άεργου ισχύος, ή αυξάνοντας την ισοδύναμη εμπέδηση εξόδου του αντιστροφέα. Οι υβριδικές μέθοδοι χρησιμοποιούν ένα συνδυασμό άμεσων ή/και έμμεσων τεχνικών περιορισμού ρεύματος.

Οι άμεσες μέθοδοι διαφέρουν μεταξύ τους στον τρόπο με τον οποίο προσαρμόζουν τις αναφορές του ρεύματος. Για παράδειγμα ο περιοριστής μέτρου περιορίζει μόνο το μέτρο της αναφοράς του ρεύματος, χωρίς να αλλάζει τη γωνία του, ενώ ο περιοριστής σε δεδομένη γωνία περιορίζει το μέτρο και θέτει τη γωνία σε μια προκαθορισμένη τιμή. Επίσης υπάρχουν οι μέθοδοι που περιορίζουν το μέτρο του ρεύματος, δίνοντας προτεραιότητα σε κάποια συνιστώσα του (π.χ συνιστώσα d- ή q-άξονα).

Όσον αφορά τις έμμεσες μεθόδους, οι πιο συνηθισμένες είναι οι μέθοδοι εικονικής εμπέδησης (virtual impedance), οι οποίες μεταβάλλουν την αναφορά της τάσης περνώντας το μετρούμενο ρεύμα μέσω μιας εικονικής εμπέδησης και αφαιρώντας όρους που αντιστοιχούν στην πτώση τάσης πάνω στην εμπέδηση αυτή. Επομένως, αυτές οι τεχνικές επιτυγχάνουν τον περιορισμό του ρεύματος αυξάνοντας την ισοδύναμη εμπέδηση εξόδου του αντιστροφέα.

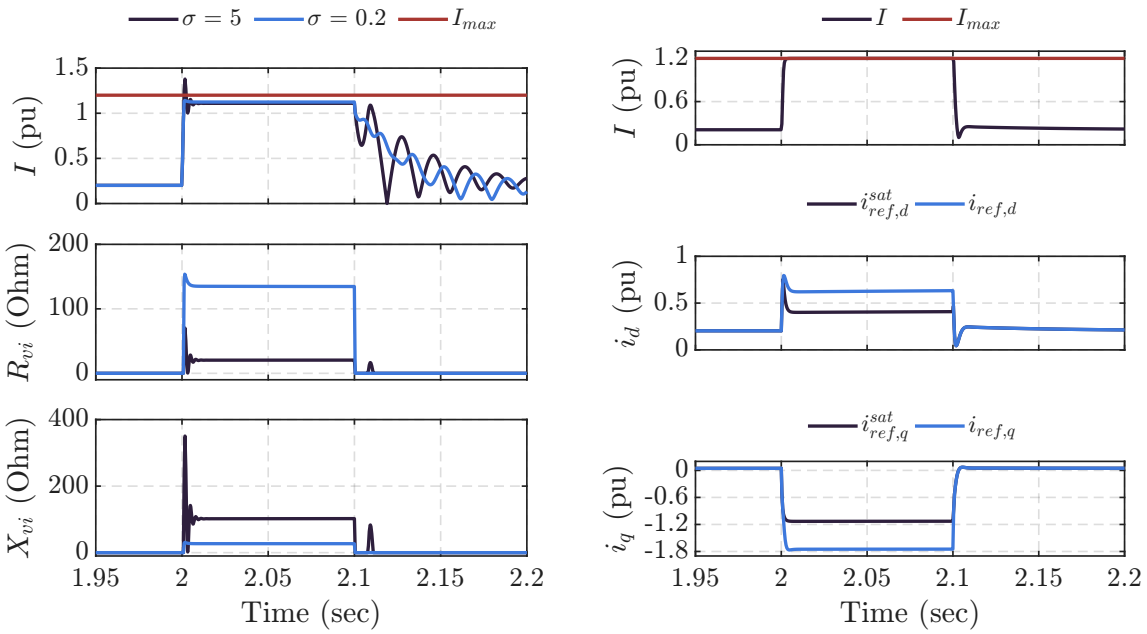
***Υλοποίηση μεθόδων και προσομοιώσεις***

Για την επιβεβαίωση της λειτουργίας των τεχνικών περιορισμού ρεύματος, υλοποιήθηκαν διάφορες μέθοδοι στο πρόγραμμα προσομοίωσης PLECS και πραγματοποιήθηκαν προσομοιώσεις βύθισης τάσης και απότομης αλλαγής της φάσης της τάσης του δικτύου. Το σύστημα που προσομοιώθηκε αποτελείται από έναν GFM αντιστροφέα που συνδέεται στο δίκτυο μέσω ενός επαγωγικού φίλτρου και μιας γραμμής μεταφοράς. Το δίκτυο αναπαρίσταται από μια άπειρη τριφασική πηγή τάσης, ενώ ο αντιστροφέας μοντελοποιείται με το μοντέλο μέσης τιμής. Οι διαταραχές προσομοιώνονται μεταβάλλοντας την τάση του δικτύου.

Αναφορικά με το σύστημα ελέγχου του αντιστροφέα, για τον ελεγκτή ενεργού ισχύος υλοποιήθηκε ο ελεγκτής στατισμού με και χωρίς βαθυπερατό φίλτρο, ενώ για τον βρόχο διαχείρισης του προφίλ τάσης υλοποιήθηκε μόνο ο ελεγκτής στατισμού. Επίσης, υλοποιήθηκαν συστήματα με και χωρίς εσωτερικό επίπεδο ελέγχου. Για τις δομές με εσωτερικό επίπεδο υλοποιήθηκε το σύστημα ελέγχου με δύο βρόχους, το οποίο αποτελείται από βρόχο εικονικής αγωγιμότητας και ελεγκτή ρεύματος. Επιπρόσθετα, από τις άμεσες τεχνικές περιορισμού του ρεύματος υλοποιήθηκε ο περιοριστής μέτρου, ο περιοριστής σε δεδομένη γωνία και οι δύο μέθοδοι που δίνουν προτεραιότητα στην d- και q-συνιστώσα του ρεύματος, ενώ από τις έμμεσες υλοποιήθηκε η μέθοδος εικονικής εμπεδησης. Αναφέρεται επίσης ότι οι άμεσες μέθοδοι εφαρμόστηκαν σε συνδυασμό με την δομή που περιλαμβάνει

εσωτερικό επίπεδο ελέγχου, ενώ η μέθοδος εικονικής εμπέδησης χρησιμοποιήθηκε με την δομή χωρίς εσωτερικό επίπεδο.

Αρχικά, μέσω προσομοιώσεων επιβεβαιώθηκε η ευαισθησία του ρεύματος στις συνθήκες του δικτύου, καθώς και ότι η προσθήκη του βαθυπερατού φίλτρου στον ελεγκτή στατισμού ενεργού ισχύος παρέχει εικονική αδράνεια. Έπειτα, για την επιβεβαίωση της λειτουργίας των τεχνικών περιορισμού ρεύματος προσομοιώθηκαν τα σφάλματα που αναφέρθηκαν πιο πάνω. Στο Σχήμα που ακολουθεί, παρουσιάζονται ενδεικτικά τα αποτελέσματα της προσομοίωσης της βύθισης τάσης του δικτύου για δύο μόνο από τις υλοποιημένες μεθόδους.




Σχήμα: Αποτελέσματα προσομοίωσης για βύθιση τάσης του δικτύου (Αριστερά) Εικονική εμπέδηση; (Δεξιά) Περιοριστής μέτρου

Φαίνεται ότι και οι δύο μέθοδοι περιορίζουν το μέτρο του ρεύματος. Όταν χρησιμοποιείται η μέθοδος της εικονικής εμπέδησης, μπορεί να εμφανιστεί προσωρινή υπερένταση στο αρχικό στάδιο του σφάλματός, ενώ στη συνέχεια δεν αξιοποιείται πλήρως το διαθέσιμο περιθώριο υπερέντασης του αντιστροφέα. Αντίθετα, ο περιοριστής μέτρου περιορίζει το ρεύμα ακριβώς στην μέγιστη επιτρεπτή τιμή, προσαρμόζοντας τις τιμές αναφοράς του ρεύματος.

Συμπερασματικά, τα αποτελέσματα των προσομοιώσεων επιβεβαιώνουν την ικανοποιητική λειτουργία των τεχνικών περιορισμού του ρεύματος που υλοποιήθηκαν.

## Κεφάλαιο 3. Επίδραση των μεθόδων περιορισμού ρεύματος στην μεταβατική ευστάθεια

Παρόμοια με τις σύγχρονες γεννήτριες, η μελέτη της μεταβατικής ευστάθειας για τους GFMIs μπορεί να γίνει μέσω των $P-\delta$ καμπύλων, όπου $\delta$ είναι η διαφορά γωνίας μεταξύ της γωνίας αναφοράς για την εσωτερική τάση του αντιστροφέα και της γωνίας της τάσης του δικτύου. Αυτή η διαφορά γωνίας αναφέρεται ως Εικονική Γωνία Ισχύος. Σε αντίθεση με τις σύγχρονες γεννήτριες, σε μεγάλες διαταραχές είναι πιθανό να ενεργοποιηθεί ο περιοριστής ρεύματος του αντιστροφέα, και συνεπώς η $P-\delta$ καμπύλη του αντιστροφέα καθορίζεται από την μέθοδο περιορισμού ρεύματος που εφαρμόζεται.

Για την μελέτη της μεταβατικής ευστάθειας του αντιστροφέα χρησιμοποιείται ένα

σύστημα στο οποίο ο αντιστροφέας συνδέεται σε έναν άπειρο ζυγό, παρόμοια με το σύστημα που χρησιμοποιήθηκε στο Κεφάλαιο 2. Επίσης, για την απλοποίηση της ανάλυσης, η γραμμή μεταφοράς θεωρείται πλήρως επαγωγική, ενώ αγνοείται η επίδραση του ελεγκτή στατισμού άεργου ισχύος. Επιπρόσθετα, για να μελετηθεί η επίδραση των μεθόδων περιορισμού ρεύματος στην μεταβατική ευστάθεια, στον παρόν Κεφάλαιο αναλύονται ενδεικτικά μόνο οι περιπτώσεις του περιοριστή μέτρου και περιοριστή σε δεδομένη γωνία.

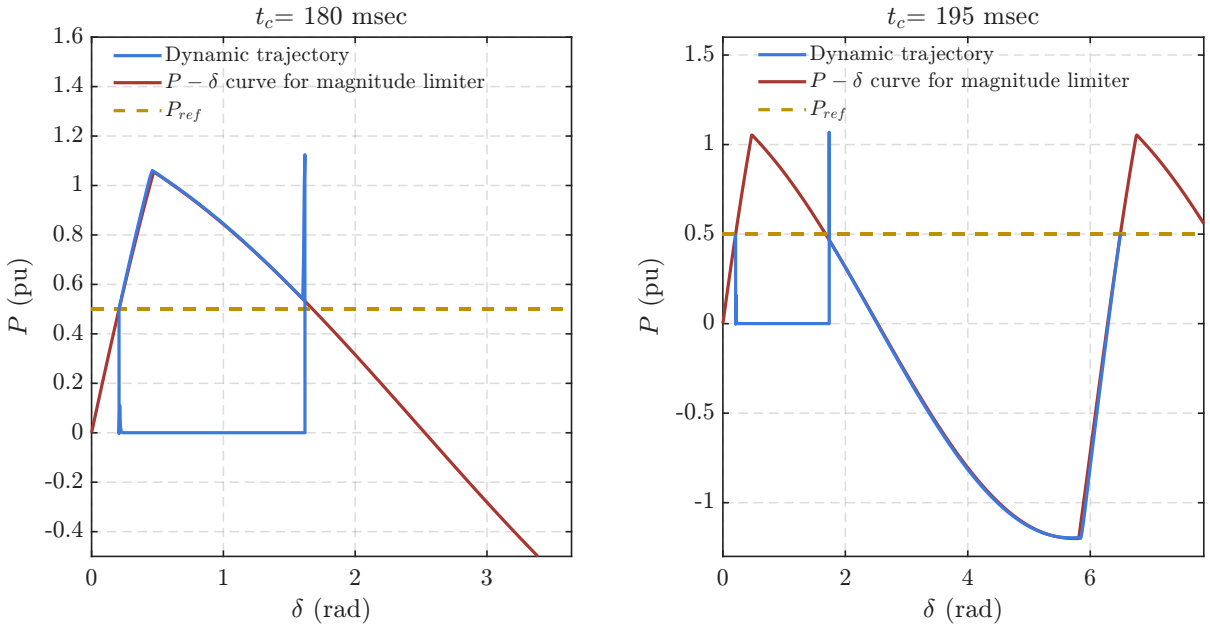
Οι $P-\delta$ καμπύλες εξάγονται μέσω των μοντέλων μεγάλου σήματος για την κάθε μέθοδο που χρησιμοποιήθηκε. Έπειτα, με βάση τις $P-\delta$ καμπύλες μπορεί να εξηγηθεί η πορεία της ενεργού ισχύος κατά και μετά από ένα σφάλμα, όπως ένα βραχυκύκλωμα, ανάλογα με το αν χρησιμοποιείται ελεγκτής στατισμού με ή χωρίς βαθυπερατό φίλτρο για τον ελεγκτή ενεργού ισχύος.

Στην περίπτωση του βραχυκυκλώματος, για να παραμείνει σε συγχρονισμό με το δίκτυο ο αντιστροφέας με τον απλό ελεγκτή στατισμού, αρκεί να εκκαθαριστεί το σφάλμα προτού η εικονική γωνία ισχύος ξεπεράσει την γωνία που αντιστοιχεί στο ασταθές σημείο ισορροπίας της $P-\delta$ καμπύλης μετά το σφάλμα. Αλλιώς, ο συγχρονισμός χάνεται και μετά από περίπου ένα κύκλο ταλάντωσης η εικονική γωνία ισχύος καταλήγει στο νέο σημείο ισορροπίας (αν υπάρχει), επειδή το σύστημα για τον απλό ελεγκτή στατισμού είναι πρώτης τάξης.

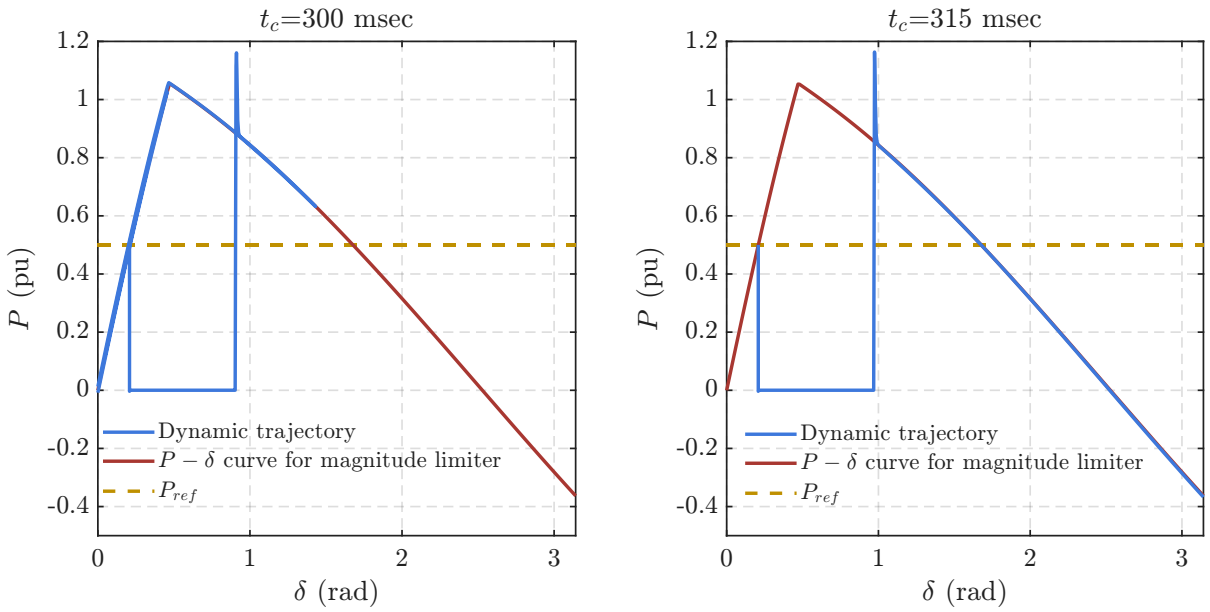
Αντίθετα, η προσθήκη του βαθυπερατού φίλτρου έχει ως αποτέλεσμα την αύξηση της τάξης του συστήματος σε δεύτερης τάξης. Πλέον, ο αντιστροφέας μπορεί να χάσει τον συγχρονισμό με το δίκτυο ακόμα και αν το βραχυκύκλωμα εκκαθαριστεί προτού η εικονική γωνία ισχύος ξεπεράσει την γωνία που αντιστοιχεί στο ασταθές σημείο ισορροπίας. Συγκεκριμένα, κατά τη διάρκεια του βραχυκυκλώματος η συχνότητα του αντιστροφέα επιταχύνεται με αποτέλεσμα το $\Delta\omega$ να γίνεται θετικό και να αυξάνεται η εικονική γωνία ισχύος. Όταν εκκαθαριστεί το σφάλμα, η συχνότητα αρχίζει να επιβραδύνεται αλλά το $\Delta\omega$ παραμένει θετικό, και συνεπώς η εικονική γωνία ισχύος συνεχίζει να αυξάνεται. Αν το $\Delta\omega$ γίνει αρνητικό προτού η εικονική γωνία ισχύος ξεπεράσει την γωνία που αντιστοιχεί στο ασταθές σημείο ισορροπίας, τότε η γωνία ξεκινάει να μειώνεται και καταλήγει στο ευσταθές σημείο ισορροπίας μετά από κάποιες ταλαντώσεις. Από την άλλη, αν η γωνία ξεπεράσει το ασταθές σημείο ισορροπίας προτού το $\Delta\omega$ γίνει αρνητικό, τότε το $\Delta\omega$ ξεκινάει να αυξάνεται ξανά και χάνεται ο συγχρονισμός με το δίκτυο.

Αφού εξηγήθηκε η θεωρητική πορεία της ενεργού ισχύος κατά και μετά το βραχυκύκλωμα, μπορεί να μελετηθεί η επίδραση των μεθόδων περιορισμού ρεύματος στην μεταβατική ευστάθεια. Μέσω των $P-\delta$ καμπύλων που προκύπτουν από τα μοντέλα μεγάλου σήματος των δύο μεθόδων, παρατηρείται ότι σε σχέση με την περίπτωση που δεν εφαρμόζεται περιορισμός ρεύματος, το ασταθές σημείο ισορροπίας μετατοπίζεται πιο κοντά στο ευσταθές και ότι η ικανότητα μεταφοράς ισχύος μειώνεται. Ως αποτέλεσμα, ο περιορισμός του ρεύματος του αντιστροφέα επηρεάζει αρνητικά την μεταβατική ευστάθεια του. Επιπλέον, παρατηρείται ότι για τις συγκεκριμένες παραμέτρους εικονικής αγωγιμότητας που χρησιμοποιήθηκαν, ο περιοριστής μέτρου προσφέρει μεγαλύτερο περιθώριο μεταβατικής ευστάθειας σε σύγκριση με τον περιοριστή σε δεδομένη γωνία (για μηδενική προεπιλεγμένη γωνία). Τέλος, διαπιστώνεται ότι ο υπολογισμός του κρίσιμου χρόνου εκκαθάρισης με την μέθοδο των ίσων εμβαδών οδηγεί σε πιο συντηρητικά αποτελέσματα σε σύγκριση με την αριθμητική ολοκλήρωση των δυναμικών εξισώσεων.

Προκειμένου να επιβεβαιωθούν τα μοντέλα μεγάλου σήματος και η θεωρητική ανάλυση, πραγματοποιούνται προσομοιώσεις διάφορων σφαλμάτων όπως βραχυκύκλωμα, βύθιση τάσης και απότομες αλλαγές φάσης της τάσης του δικτύου. Ενδεικτικά παρακάτω παρουσιάζεται η σύγκριση των θεωρητικών $P-\delta$ καμπυλών με αυτές που προκύπτουν από την προσομοίωση ενός βραχυκυκλώματος, για τον ελεγκτή στατισμού με και χωρίς βαθυπερατό φίλτρο, χρησιμοποιώντας ως μέθοδο περιορισμού τον περιοριστή μέτρου.




Σχήμα: Σύγκριση θεωρητικών $P-\delta$ καμπύλων με αυτές που προκύπτουν από την προσομοίωση ενός βραχυκυκλώματος, για τον ελεγκτή στατισμού, όταν εφαρμόζεται ο περιοριστής μέτρου




Σχήμα: Σύγκριση θεωρητικών $P-\delta$ καμπύλων με αυτές που προκύπτουν από την προσομοίωση ενός βραχυκυκλώματος, για τον ελεγκτή στατισμού με βαθυπερατό φίλτρο, όταν εφαρμόζεται ο περιοριστής μέτρου

# Κεφάλαιο 4. Προσομοίωση πραγματικού χρόνου

Οι προσομοιωτές πραγματικού χρόνου μπορούν να λύνουν τις διαφορικές εξισώσεις που περιγράφουν το σύστημα, σε πραγματικό χρόνο, με την χρήση ψηφιακού υλικού (digital hardware) και παράλληλων υπολογιστικών μεθόδων (parallel computing). Στις offline προσομοιώσεις, η στιγμή κατά την οποία είναι διαθέσιμα τα αποτελέσματα της προσομοίωσης δεν είναι σημαντική. Επομένως, η ταχύτητα με την οποία λύνονται οι εξισώσεις του συστήματος εξαρτάται από τους υπολογιστικούς πόρους και την πολυπλοκότητα του συστήματος. Αντίθετα, σε μια προσομοίωση πραγματικού χρόνου, οι

εξισώσεις του συστήματος για ένα βήμα προσομοίωσης πρέπει να επιλύονται μέσα στο ίδιο χρονικό διάστημα σε πραγματικό χρόνο.

Όταν κάποια στοιχεία του συστήματος προσομοίωσης αντικαθίστανται με τον αντίστοιχο πραγματικό εξοπλισμό, ο οποίος αλληλεπιδρά με το υπόλοιπο σύστημα που προσομοιώνεται, η προσομοίωση αναφέρεται ως "harware-in-the-loop" (HIL). Επίσης, όταν το στοιχείο που αντικαθίσταται είναι ο ελεγκτής, η προσομοίωση αναφέρεται ως "controller hardware-in-the-loop" (CHIL). Με αυτό τον τρόπο, μια καινούρια υλοποίηση ελέγχου μπορεί να δοκιμαστεί σε συνθήκες πραγματικού χρόνου, όπου η συμπεριφορά των πραγματικών στοιχείων του συστήματος αναπαριστάται με μεγαλύτερη ακρίβεια.

Με βάση τα πιο πάνω, πραγματοποιήθηκε μια CHIL προσομοίωση πραγματικού χρόνου, προκειμένου να επιβεβαιωθεί η αποτελεσματική λειτουργία των μεθόδων περιορισμού ρεύματος που υλοποιήθηκαν, σε συνθήκες πραγματικού χρόνου. Τα συστήματα ελέγχου υλοποιήθηκαν στον μικροεπεξεργαστή C2000 LAUNCHXL-F28379D της Texas Instruments, ενώ το υπόλοιπο σύστημα προσομοίωσης υλοποιήθηκε στον προσομοιωτή πραγματικού χρόνου RT Box 1 της Plexim. Πιο συγκεκριμένα, το RT Box προσομοιώνει το σύστημα ισχύος (π.χ δίκτυο, γραμμή μεταφοράς κλπ) και στέλνει τα αποτελέσματα για την τάση και το ρεύμα στον μικροεπεξεργαστή. Έπειτα, ο μικροεπεξεργαστής επεξεργάζεται τα σήματα που λαμβάνει με βάση τα υλοποιημένα συστήματα ελέγχου και παράγει τους παλμούς μεταγωγής των διακοπτικών στοιχείων του αντιστροφέα, τους οποίους στέλνει πίσω στο RT Box. Επιπλέον, χρησιμοποιήθηκε ένας παλμογράφος, προκειμένου να παρατηρηθούν οι κυματομορφές των σημάτων που παρέχει το RT Box ως έξοδο, όπως για παράδειγμα το τριφασικό ρεύμα εξόδου του αντιστροφέα.

Το σύστημα που προσομοιώνεται στο RT Box είναι πολύ παρόμοιο με το αντίστοιχο των offline προσομοιώσεων. Οι κύριες διαφορές είναι η προσθήκη ενός ωμικού φορτίου στο σημείο που συνδέεται ο αντιστροφέας στο δίκτυο και η χρήση του πλήρους μοντέλου του αντιστροφέα με τους διακόπτες ισχύος αντί του μοντέλου μέσης τιμής. Ανάλογα, τα συστήματα ελέγχου που υλοποιούνται στον μικροελεγκτή είναι παρόμοια με αυτά των offline προσομοιώσεων, με την διαφορά ότι έχει προστεθεί το σύστημα διαμόρφωσης SPWM και κάποια βαθυπερατά φίλτρα για την καταστολή του θορύβου.

Για την επιβεβαίωση των τεχνικών περιορισμού ρεύματος που υλοποιήθηκαν, πραγματοποιήθηκαν προσομοιώσεις πραγματικού χρόνου για βραχυκύκλωμα και για απότομη αλλαγή φάσης της τάσης του δικτύου. Στο παρακάτω Σχήμα παρουσιάζονται ενδεικτικά τα αποτελέσματα της προσομοίωσης του βραχυκυκλώματος για δύο μόνο από τις υλοποιημένες μεθόδους. Συγκεκριμένα η μια μέθοδος είναι αυτή της εικονικής εμπέδησης, ενώ η άλλη είναι ο περιοριστής μέτρου προκειμένου να φανούν οι διαφορές στην απόκριση των έμμεσων και άμεσων μεθόδων.

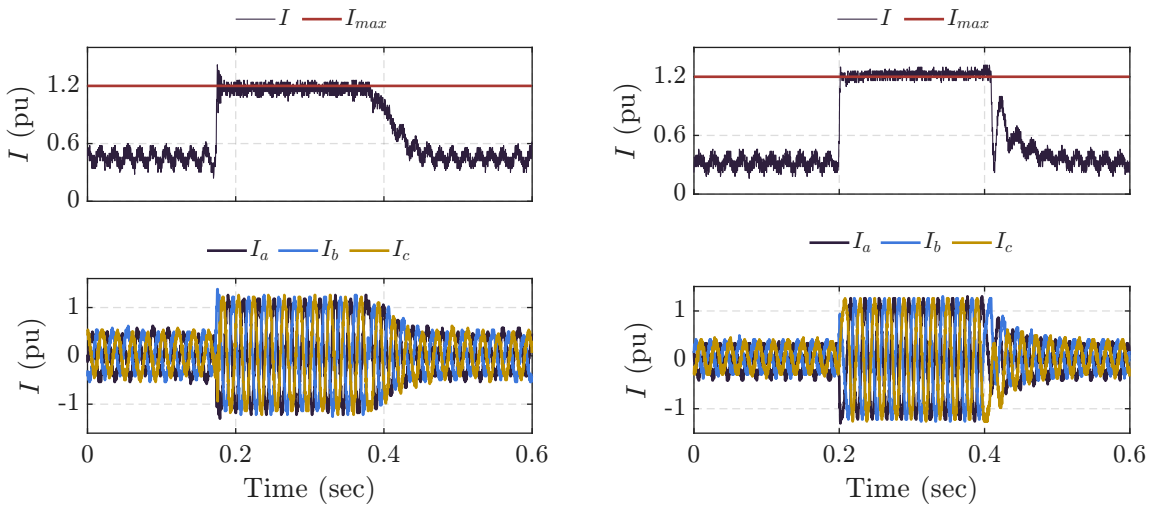
Φαίνεται ότι και οι δύο μέθοδοι περιορίζουν το μέτρο του ρεύματος. Σε αντίθεση με τον περιοριστή μέτρου, φαίνεται ότι στην περίπτωση της εικονικής εμπέδησης παρατηρείται μια προσωρινή υπερένταση στο αρχικό στάδιο του σφάλματος, γεγονός που συνάδει με τα αποτελέσματα της offline προσομοίωσης.

Συμπερασματικά, τα αποτελέσματα των προσομοιώσεων πραγματικού χρόνου δείχνουν ότι οι υλοποιημένες τεχνικές περιορισμού του ρεύματος του αντιστροφέα λειτουργούν αποτελεσματικά υπό συνθήκες πραγματικού χρόνου.

# Κεφάλαιο 5. Συμπεράσματα και προοπτικές

***Συμπεράσματα***

Οι GFMI συμπεριφέρονται ως πηγές τάσης με αποτέλεσμα το ρεύμα τους να είναι




Σχήμα: Αποτελέσματα προσομοίωσης πραγματικού χρόνου για βραχυκύκλωμα (Αριστερά) Εικονική εμπέδηση; (Δεξιά) Περιοριστής μέτρου

ευαίσθητο σε συνθήκες του δικτύου. Επομένως, σε περιπτώσεις μεγάλων διαταραχών, το ρεύμα τους μπορεί να υπερβεί την μέγιστη επιτρεπόμενη τιμή, καθιστώντας απαραίτητη την εφαρμογή μεθόδων περιορισμού του ρεύματος. Ωστόσο, με την ενεργοποίηση αυτών των μεθόδων παρακάμπτεται η κανονική λειτουργία, με αποτέλεσμα η δυναμική συμπεριφορά του αντιστροφέα κατά και μετά το σφάλμα να καθορίζεται κυρίως από την μέθοδο που εφαρμόζεται.

Οι περισσότερες μέθοδοι διαμόρφωσης δικτύου μπορούν να αναπαρασταθούν από ένα γενικό σύστημα ελέγχου πολλαπλών επιπέδων και υποσυστημάτων. Συχνά χρησιμοποιούμενες υλοποιήσεις για τον ελεγκτή ενεργού ισχύος περιλαμβάνουν τον ελεγκτή στατισμού με και χωρίς βαθυπερατό φίλτρο και την Εικονική Σύγχρονη Γεννήτρια. Η προσθήκη του βαθυπερατού φίλτρου στον ελεγκτή στατισμού εισάγει εικονική αδράνεια, γεγονός που επιβεβαιώνεται μέσω προσομοίωσης.

Οι μέθοδοι περιορισμού του ρεύματος διακρίνονται σε άμεσες, έμμεσες και υβριδικές. Μερικές συχνά χρησιμοποιούμενες μέθοδοι υλοποιήθηκαν στο λογισμικό προσομοίωσης PLECS και η αποτελεσματική λειτουργία τους επιβεβαιώθηκε μέσω προσομοιώσεων για βυθίσεις τάσης και απότομες αλλαγές φάσης. Η μέθοδος εικονικής εμπέδησης δεν μπορεί να αξιοποιήσει πλήρως το περιθώριο υπερέντασης του αντιστροφέα σε όλη τη διάρκεια του σφάλματος και μπορεί να εμφανίσει προσωρινή υπερένταση στο αρχικό στάδιο του σφάλματος. Αντίθετα, οι άμεσες μέθοδοι μπορούν να πετύχουν γρήγορο και ακριβή περιορισμό του ρεύματος, αξιοποιώντας πλήρως το περιθώριο υπερέντασης.

Η Εικονική Γωνία Ισχύος χρησιμοποιείται για την ανάλυση της μεταβατικής ευστάθειας των GFMI, μέσω των $P-\delta$ καμπύλων που προκύπτουν από μοντέλα μεγάλου σήματος, τα οποία διαφέρουν ανάλογα με τη μέθοδο περιορισμού ρεύματος που εφαρμόζεται. Εξηγείται ότι η πορεία της ενεργού ισχύος μετά από ένα βραχυκύκλωμα διαφέρει μεταξύ του ελέγχου με και χωρίς αδράνεια. Επιπλέον, οι $P-\delta$ καμπύλες που προκύπτουν για τον περιοριστή μέτρου και τον περιοριστή σε δεδομένη γωνία δείχνουν ότι ο περιορισμός ρεύματος μειώνει σημαντικά το περιθώριο μεταβατικής ευστάθειας. Ακόμη, η εφαρμογή της μεθόδου ίσων εμβαδών για τον υπολογισμό του κρίσιμου χρόνου εκκαθάρισης για βραχυκυκλώματα, οδηγεί σε συντηρητικά αποτελέσματα συγκριτικά με την αριθμητική ολοκλήρωση των δυναμικών εξισώσεων του συστήματος. Οι προσομοιώσεις που πραγματοποιήθηκαν επιβεβαιώνουν τα μοντέλα μεγάλου σήματος, καθώς και την θεωρητική ανάλυση.

Τέλος, μέσω προσομοίωσης πραγματικού χρόνου, επιβεβαιώθηκε ότι οι υλοποιημένες τεχνικές περιορισμού ρεύματος, μπορούν να περιορίζουν το ρεύμα σε σφάλματα όπως βραχυκύκλωμα και απότομη αλλαγή φάσης, υπό συνθήκες πραγματικού χρόνου.

***Προοπτικές***

Μια προοπτική μελλοντικής δουλειάς είναι η ανάπτυξη σχημάτων αντιμετώπισης της συσσώρευσης ολοκληρωτικού σφάλματος (anti-windup schemes) όταν χρησιμοποιείται ελεγκτής τάσης αντί βρόχος εικονικής αγωγιμότητας. Επίσης, η σχεδίαση μεθόδων περιορισμού ρεύματος για ασύμμετρα σφάλματα είναι απαραίτητη. Μπορούν επίσης να υλοποιηθούν και να συγκριθούν μεταξύ τους, διάφορες μέθοδοι ενίσχυσης της μεταβατικής ευστάθειας. Πολύ σημαντική είναι η εφαρμογή μεθόδων περιορισμού ρεύματος για πιο πολύπλοκες τοπολογίες μετατροπέων, όπως είναι οι αρθρωτοί πολυεπίπεδοι μετατροπείς (MMC). Τέλος, θεωρείται σημαντική η πειραματική επιβεβαίωση της λειτουργίας των μεθόδων περιορισμού ρεύματος.

# Chapter 1

# Introduction

## 1.1 Transformation of the power system

Traditional power systems are currently undergoing a major transformation, driven by the need to address global warming and reduce greenhouse gas emissions. There is a global shift towards cleaner forms of electric energy generation, resulting in a gradual replacement of large centralized thermal power plants with smaller scale Renewable Energy Sources (RES), such as solar and wind. This transition is being accelerated by ambitious national and international targets aimed at increasing the share of RES in the energy production mix, such as the EU commitment of achieving climate neutrality by 2050 [1], which sets a clear direction for the decarbonization of the power grid.

Conventional power grids were dominated by large Synchronous Generators (SGs), which were responsible for voltage and frequency regulation. Their low output impedance and the use of Automatic Voltage Regulators (AVR), allow them to operate as ideal voltage sources, which in combination with their high rotor inertia, are essential features for ensuring stable and reliable operation of the power system [2]. In contrast, most renewable energy sources are integrated into the grid via power electronic converters and are therefore referred to as Inverter-Based Resources (IBRs). Power electronic converters are significantly different than SGs, not only due to their hardware characteristics, but also in the way they respond to disturbances and grid events. Unlike SGs, their behavior is not governed by inherent physical properties such as rotor inertia, but it rather depends on their control algorithms [3]. Thus, the ongoing transformation from an SG-dominated grid to an IBR-dominated one, which is illustrated in Fig. 1.1, has introduced various engineering and operational challenges that need to be addressed, in order to ensure the stability and resilience of the future renewable-rich power grids.

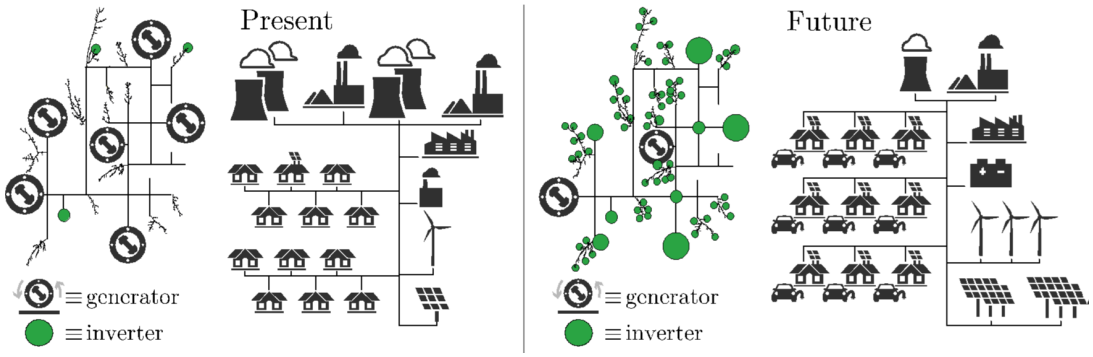



Figure 1.1: Transition of the power grid from SG-dominated to IBR-dominated [4]

## 1.2 Inverter Based Resources

The majority of renewable energy sources are connected to the grid through a series of power electronic converters, because the power they generate is not inherently compatible with the power system's frequency and voltage level requirements (e.g 50 Hz, 20 kV) [5]. Despite the fact that some IBRs utilize more than one converter, their behavior is primarily determined by the last dc/ac inverter as it is directly connected to the grid [6], hence the term "Inverter Based Resources". Other IBRs include battery energy storage systems (BESS), fuel cells, high voltage direct current (HVDC) converters etc.

In recent years, the dc/ac conversion is achieved utilizing Voltage Source Converters (VSCs). These inverters use fully controllable semiconductors, such as IGBTs and power MOSFETs, allowing fast and precise control of their output voltage and four quadrant operation. As shown in Fig. 1.2, a three phase VSC converts the dc-link voltage to a three phase ac voltage at a specified fundamental frequency along with various harmonic components, using Pulse Width Modulation (PWM) techniques. In lower voltage levels, such as the distribution network, RES are connected to the grid with two-level VSCs [7], whose configuration is shown in Fig. 1.3a. These are the simplest VSCs and they consist of a common dc link and three half-bridge legs, one for each phase. In order to meet the requirements for harmonic injection to the grid, two-level VSCs should either use high switching frequencies or excessive harmonic filters, which lead to an increase of switching losses and system complexity respectively [8]. For this reason, in high-voltage high-power applications, such as HVDC links, multilevel converters are typically used as an alternative to conventional two-level VSCs. The most popular multilevel converter is the Modular Multilevel Converter (MMC), shown in Fig. 1.3b, which consists of a number of submodules that can either be a half-bridge or full-bridge topology and capacitors that are distributed in each submodule [8], [9]. This structure allows MMCs to produce an output voltage with multiple levels, leading to high quality waveforms combined with high efficiency.

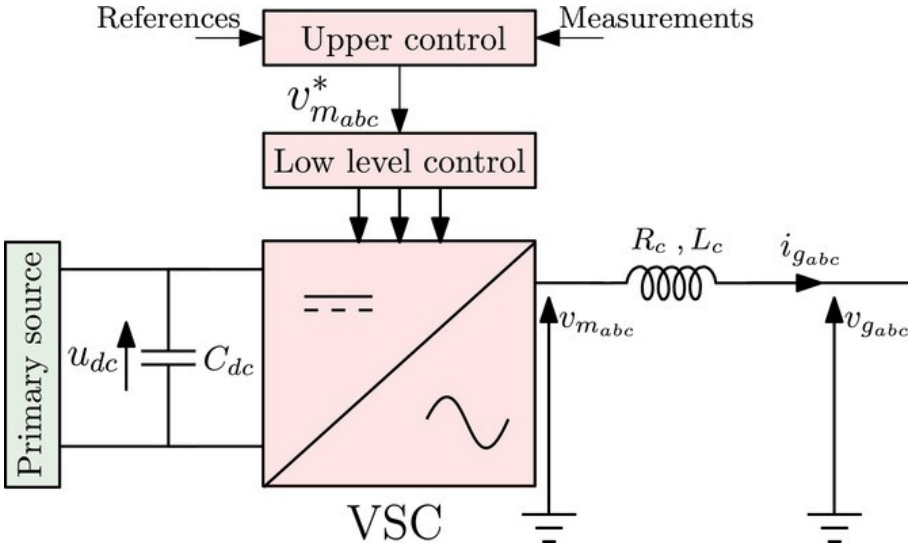
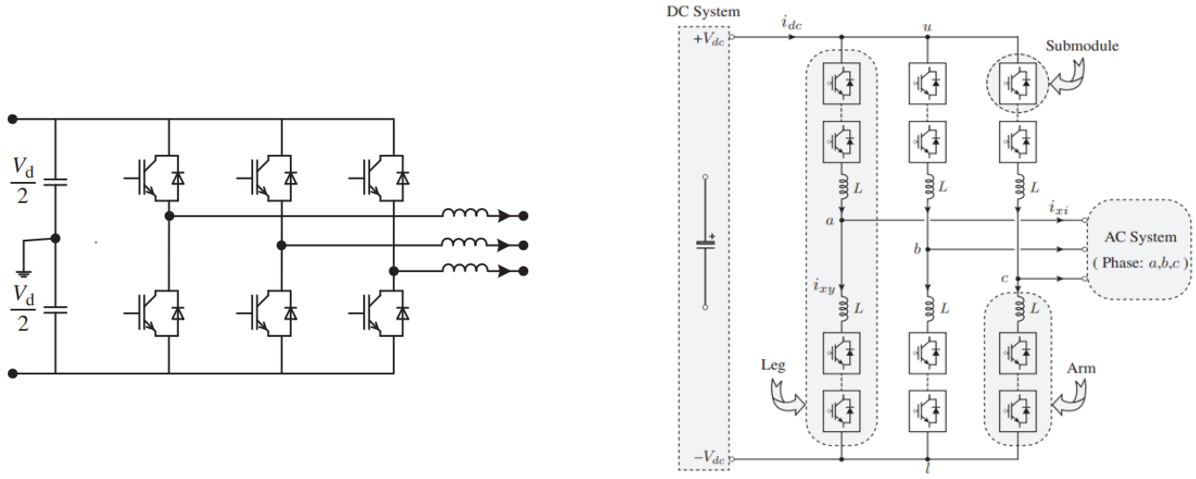



Figure 1.2: High level representation of a three phase Voltage Source Converter [10]

As illustrated in Fig. 1.2 the reference voltage fed to the PWM is generated by the inverter's control system. Due to the high modulation bandwidth, the fundamental component of the output voltage can be considered equal to the reference. Thus, assuming that the dc-link voltage is constant, the voltage at the VSC terminal is determined by the control system




(a) (b)

Figure 1.3: (a) Three phase two-level VSC [9]; (b) Three phase MMC with half-bridge or full-bridge submodules [11]

output. Depending on their control algorithm, grid-connected VSCs can be classified into two main categories, namely grid-following inverters (GFLIs) and grid-forming inverters (GFMIs) [5]. Despite having a very similar hardware configuration (dc link, output filters, switching valves etc) and sharing the common goal of injecting active and reactive power to the grid, GFMIs and GFLIs differ significantly in their control systems, modeling representation, response to grid events, and small signal stability under different grid strengths [12].

### Grid-Following Inverters

Currently, the vast majority of IBRs connected to the power system are controlled as grid following inverters. Traditionally, the main objective of GFLIs was to synchronize with the grid and supply active power, while maintaining their power factor close to unity [2]. GFLIs utilize a dedicated synchronization unit, such as a phase-locked loop (PLL), to track the angle of the voltage at the Point of Common Coupling (PCC). Then this angle is used to transform the measured voltage and current to the synchronous reference frame (i.e., the dq frame), where it is easier to design and implement the inverter controllers. The active and reactive power injection of a GFLI can be independently controlled, by adjusting the d-axis and q-axis component of the current respectively [2]. This control scheme is usually referred to as current control, because the output current of the inverter is directly controlled, and it is widely used in grid connected, as well as motor drive applications [4]. Because of the control principle that was explained above, it is evident that the behavior of GFLIs can be approximated as a current source with high parallel impedance [2], [4], [12].

Due to the growing number of IBRs that are connected to the grid and the replacement of synchronous generators, grid operators require that larger-scale IBRs have to actively support the power system, by exchanging active and reactive power depending on the type of disturbance. For instance, German grid operators require that IBRs should support the voltage by supplying (absorbing) reactive current, if the measured voltage decreases (increases) beyond a predefined dead-band [5], [13]. GFLIs can achieve this by accordingly adjusting active and reactive power set-points, while respecting the hardware limitations of the converter [12]. Due to the lack of inherent inertia in IBRs, another grid supporting function that can be added to the control system of GFLIs, is the so-called “synthetic inertia” or fast

frequency response (FFR), which regulates the active power output of the converter during frequency disturbances [14], [15]. The drawback of the FFR provided by GFLIs, is that frequency estimation and control delays can limit the efficiency of the inertial response. Furthermore, the use of the frequency derivative can introduce additional noise, compromising the stability of the system [15].

Despite being the dominant approach currently in use, grid-following inverters have two main shortcomings. Many research works have demonstrated that the use of a PLL and other synchronization units can deteriorate the small-signal stability of IBRs connected to low-strength parts of the grid [16], [17], [18]. Therefore, GFLIs are generally unsuitable for weak grid applications (i.e., low short circuit ratio) such as offshore wind parks connected to the grid through long transmission lines, as they cannot ensure stable operation [15]. Moreover, GFLIs operate under the assumption that they can synchronize and "follow" a stiff and already formed voltage, hence the term "grid following". Consequently, a future power electronics dominated grid can not operate using only grid-following converters, because they will have no voltage to synchronize to, due to the lack of voltage forming units such as synchronous generators [5], [16]. For the same reason, GFLIs can not help in the procedure of restarting the power system after a blackout, which is referred to as "black start" [16].

### Grid-Forming Inverters

Although a formal and unified definition of GFMIs is still under discussion in academia and industry [12], there exist various different definitions, mainly proposed by grid codes, which describe the functionalities that a GFMI should have [19], [20]. Among all these definitions, the most common and accepted characteristic of GFMIs is their voltage-source behavior, which enables them to respond to grid events similar to SGs [21]. For instance, the North American Electric Reliability Corporation (NERC) states that grid-forming controls are "controls with the primary objective of maintaining an internal voltage phasor that is constant or nearly constant in the sub-transient to transient time frame" [22]. Thus, a GFMI can be defined as a converter controlled to behave as an AC voltage source, which is able to "form" the voltage without the need of other voltage forming units [21]. For this reason, grid-forming control of IBRs is widely recognized as a promising solution to enhance the stability of the future bulk power system.

The main difference between GFMIs and GFLIs is that they are controlled as voltage and current sources respectively[1], as illustrated in Fig. 1.4. However, there are various other differences between these two control strategies. First, unlike GFLIs, most GFM control strategies described in the literature, are able to achieve synchronization with the grid without using a dedicated synchronization unit, but rather by implementing the power synchronization principle of SGs in their controller [12], [23]. This feature of self-synchronization, in combination with their voltage source behavior, makes GFMIs more suitable than GFLIs for IBRs connected in weak grids. However, studies have shown that the small-signal behavior of GFLIs under strong grid scenarios is superior to that of GFMIs [24], [25].

Another difference lies in their grid supporting response during a disturbance. It has already been mentioned that GFLIs can support the grid by regulating their power output with the use of additional control loops. However, this response is not inherent and may therefore be inefficient [15], due to control and measurement delays [21]. On the other hand, because a GFMI is designed to mimic the behavior of a SG, it can provide an intrinsic response to

[1] The operating behavior of the inverter should not be confused with the term "Voltage Source Converter". Both GFMIs and GFLIs belong in the category of Voltage Source Converters, but the former is controlled to behave as a voltage source, while the latter is controlled to behave as a current source.

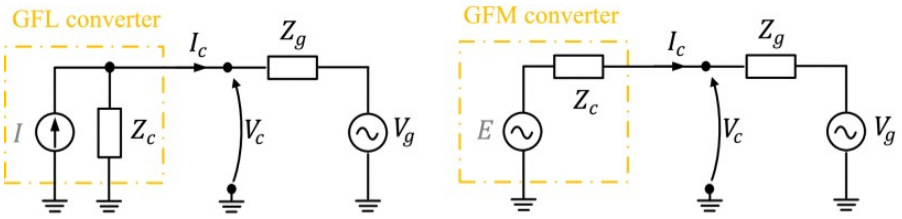



Figure 1.4: Modeling representation of grid-following and grid-forming inverters [12]

Table 1.1: Comparison of grid-following and grid-forming inverters

| **Grid-following inverters** | **Grid-forming inverters** |
|---|---|
| Assumes that the PCC voltage is already formed | Forms its terminal voltage |
| Operates as a current source | Operates as a voltage source |
| Uses a dedicated synchronization unit (e.g PLL) to synchronize to the grid | Doesn't need a PLL to synchronize to the grid (although some GFM control methods may use a PLL) |
| Cannot black start a system | Can potentially black start a system |
| Cannot operate at 100% IBR penetration | Can operate at 100% IBR penetration |
| Better performance in stiff grids | Stable operation at low system strengths |
| No inherent inertia support (needs additional controllers) | Some GFM control methods (e.g filtered droop and VSG) can provide inherent inertia |

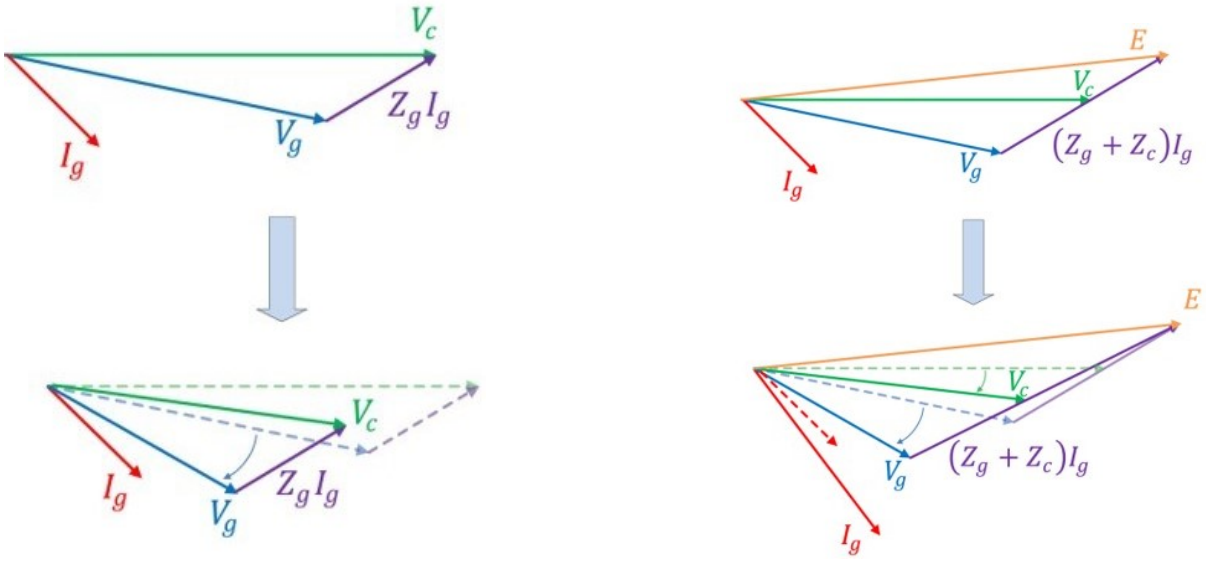
disturbances, i.e., independent of additional measurements and control algorithms, and help enhance the stability of the system. Finally, GFMIs can operate at 100% IBR penetration, as well as potentially black start a system [16], since they form the voltage at their terminal, instead of relying on other units to create a well-regulated voltage to synchronize to [5]. Table 1.1 summarizes the key differences between grid-forming and grid-following inverters.

## 1.3 Overcurrent limiting for grid-forming inverters

### 1.3.1 The need for current-limiting methods for grid-forming inverters

Since GFMIs and GFLIs operate as voltage and current sources respectively, their response to grid events can be significantly different, as illustrated in the phasor diagrams of Fig. 1.5. Referring to the simplified equivalent circuit of Fig. 1.4, where the upstream network is modeled as a Thevenin equivalent, when a disturbance causes the grid voltage phasor to change, the instantaneous response of a GFLI is to keep the current phasor unchanged. This occurs because the PLL must first re-synchronize with the grid voltage before feeding the new angle to the controller, which then determines the new current reference [12]. In contrast, due to its voltage source behavior, the instantaneous response of a GFMI is to maintain the internal voltage phasor constant, which leads to a change of the output current phasor [2], [12].

This inherent response to disturbances makes GFMIs very appealing for grid operators [26], as it is very similar to the behavior of SGs. However, it is evident that the output current




(a) (b)

Figure 1.5: Phasor diagrams for a grid disturbance (a) Grid-following inverter; (b) Grid-forming inverter [12]

of GFMIs is very sensitive to grid conditions, because it is not directly controlled. Therefore, in the case of severe disturbances, such as a three-phase short circuit, if no action is taken, the output current of the GFMI will exceed the nominal. Unlike synchronous machines, which can withstand currents around 6-8 times their nominal for a certain amount of time, power electronic converters have a limited overcurrent capability, typically 1.2-2 pu, due to their semiconductor devices [21]. However, grid operators require that GFMIs remain connected and actively support the grid during faults, despite their inability to withstand overcurrent. A possible solution to this problem, is to over-dimension the converter components in order to be able to handle larger currents and better emulate the behavior of SGs, but it comes with a major financial cost [21]. Thus, to prevent unwanted tripping of GFMIs, proper overcurrent protection methods are essential, in order to avoid damage to the converter hardware and contribute to grid resilience during contingencies. For the aforementioned reasons, in recent years, the implementation of current-limiting control methods for GFMIs as well as their effect on the stability of the system, is gaining a lot of interest from academia and industry [27], [28].

### 1.3.2 Challenges of current-limiting methods for grid-forming inverters

Over the last years, a lot of current-limiting control methods for GFMIs have been proposed in the literature. A simple solution is to switch to GFL control when a fault is detected, which requires a back-up PLL and mode switching between synchronization methods [21], [23]. Due to the drawbacks associated with the use of a PLL and the fact that the fault response of GFLIs has been extensively studied [29], this method will not be discussed in this work. Otherwise, the basic GFM control structure is maintained and additional current-limiting control methods can be implemented, which operate only when necessary. When a disturbance leads to the triggering of the current limiter, the inverter is not able to maintain the internal voltage phasor constant, because the normal operation is superseded by the current limiter [27]. Therefore, the dynamic behavior of a GFMI during and after a severe disturbance is mainly determined by the utilized current-limiting control method. This implies that while the primary purpose of these methods

is to protect the inverter semiconductor devices, they also influence power system aspects, such as protection coordination, transient stability, voltage support etc [28].

To that end, an effective current limiting method should be designed to meet certain requirements concerning both the power system and the device itself. First, the current limiter should be able to protect the semiconductor devices from thermal breakdown, by quickly and accurately limiting the current magnitude, so it does not exceed the maximum allowable level. This should be achieved without introducing undesired harmonic components in the current and also without compromising the small-signal stability of the GFMI [28]. Additionally, the GFMI should be able to provide the appropriate fault-current contribution, depending on the type of the disturbance, as specified in grid codes [19]. For instance, the inverter should inject reactive current to the grid during voltage sags, or provide active phase-jump power. Also, the GFMI has to be capable of riding-through faults and restoring its normal operating condition after the faults are cleared [27]. This includes ensuring the transient stability of the converter, i.e., the ability to remain synchronized with the grid during and after a severe fault.

Due to the various system- and device-level requirements, the design of a single current-limiting method that meets all of them is a challenging task. Each of the current-limiting methods that have been proposed in the literature has its upsides and drawbacks. Recently, the effect of current-limiting methods on system aspects such as the reactive current profile of the GFMI during faults, and transient stability analysis and enhancement methods under current-limiting conditions, is gaining a lot of interest from researchers [30], [31], [32]. Nevertheless, many open issues and research questions remain. For instance, the transient stability analysis for systems with multiple GFMIs through the development of simplified models is a challenging issue [27]. Another vital issue which will require more research efforts, is the development of power system protection solutions that account for the behavior of GFMIs under various current-limiting methods, as well as the compatibility of current limiters with traditional protection schemes [28]. Overall, further research and development is essential to gain a deep understanding of the behavior of GFMIs during contingencies that drive them into current limitation, especially in the case of IBR-rich power systems.

## 1.4 Objective and structure of this thesis

### 1.4.1 Objective and scope of this thesis

The primary objective of this thesis is to analyze and understand the techniques by which current limitation is achieved in grid-forming inverters and to assess the effect of these methods on the transient stability of the inverter. To achieve this, a comprehensive review of grid-forming and current-limiting control methods is first presented. Additionally, the most commonly used methods are implemented and validated through both offline and real-time simulations. The simulation aims to provide a better understanding of the operating principles of these methods. The scope of this thesis is limited to the study of current-limiting methods for symmetrical faults and for two-level VSCs. Therefore, more complicated VSC topologies, as well as asymmetrical disturbances and unbalanced operating conditions are outside the scope of this work and will not be considered.

### 1.4.2 Structure of this thesis

The structure of this thesis is as follows:

Chapter 1 describes the transformation of the power grid from being dominated by synchronous machines to being dominated by inverter-based resources. It provides a brief overview of inverter based resources, highlighting the differences between the behavior of grid-forming and grid-following inverters. Then, the necessity of current-limiting methods for grid-forming inverters is underlined and the main challenges associated with these methods are presented.

Chapter 2 introduces the general system of a grid-forming inverter, followed by a comprehensive review of grid-forming and current-limiting control methods. The most frequently used methods are then implemented in the PLECS simulation software and time-domain simulations are performed, in order to validate their performance under various operating scenarios.

Chapter 3 studies the effect of current-limiting methods on the transient stability of the grid-forming inverter. First, the theoretical basis is established by presenting the large-signal models corresponding to the employed current-limiting method, along with the theoretical behavior of the grid-forming inverter during and after the fault. Then, time-domain simulations under various types of disturbances are carried out, to validate the large-signal models and the presented theoretical transient stability analysis.

Chapter 4 validates the effectiveness of the implemented current-limitation techniques under real-time conditions. It begins with a brief overview of real-time simulations, followed by the description of the real-time simulation setup. The implementation of the real-time simulation models and controllers is then presented and the differences from their offline simulation counterparts are highlighted. Finally, the real-time simulation results are shown.

Chapter 5 concludes the thesis, by summarizing the key points of each Chapter and discussing future work directions.

# Chapter 2

# Grid-forming inverters and current-limiting methods

This Chapter provides an overview of various GFM control methods and current-limitation techniques that are commonly used in the literature. First, the general control structure of GFMIs is presented, followed by common GFM control methods. Then, the basic categories of current-limiting control methods are explained and the most frequently used methods from each category are described. The implementations of various GFM and current-limiting control methods in the PLECS simulation software are presented and time-domain simulations are performed to validate the controllers.

## 2.1 Grid-forming control methods

### 2.1.1 General control structure of grid-forming inverters

The most significant difference between the various GFM methods is their controller implementation. Despite the variety of GFM controls proposed in the literature, most of them can be represented by the general control structure of Fig. 2.1, where both the hardware and the software of a GFMI are shown. Regarding the hardware, the converter is connected to the grid (which is modeled as a Thevenin equivalent) though a filter, such as an LCL or a simple inductive filter. The purpose of this filter is to mitigate the harmonic distortion in currents and voltages caused by the switching behavior of the converter [21]. The inputs of the control system are the measured three-phase currents and voltages, as well as references for active/reactive power, frequency and voltage magnitude, and the output is the reference voltage that is fed to the PWM [12].

As shown in Fig. 2.1, a general control system of a typical GFMI consists of multiple subsystems and layers, which are responsible for different functionalities. For instance, the outmost layer, i.e., the outer loops, generate the characteristics of the voltage source reference, while the inner layer, i.e., the inner loops, are responsible for tracking this reference [21]. Due to the cascading structure of these layers, it is evident that in order to ensure the stability of the system, they have to operate at different time scales. More specifically, the outer loops are linked to the electromechanical transient dynamics, while the inner loops are associated with the electromagnetic transient behavior. [21].

The outer layer includes the power synchronization loop and the voltage profile management loop, which are responsible for synchronization with the grid and voltage regulation respectively. The power synchronization loop aims to regulate the active power

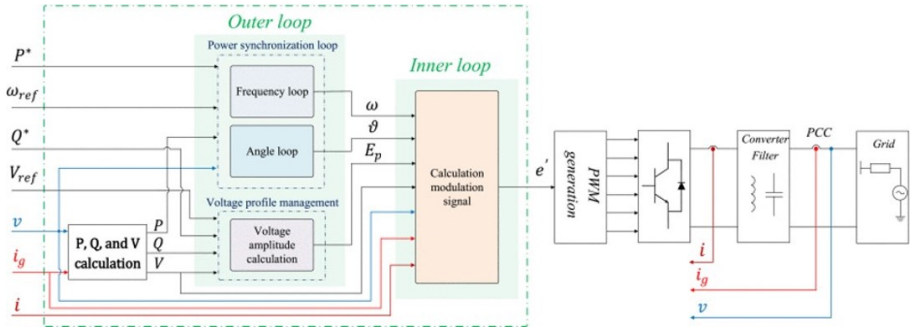



Figure 2.1: Generalized structure of a grid forming inverter [12]

output of the converter and it generates the angle/frequency of the internal voltage source (IVS) of the GFMI. This angle is also used for the transformation of measured three phase current and voltage to the dq reference frame. On the other hand, the voltage profile management loop is related to the reactive power output of the GFMI and it provides the magnitude of the IVS. This follows the traditional link of active power with angle/frequency and reactive power with voltage magnitude, which is valid in predominantly inductive grids, such as the high-voltage transmission system. In contrast, for a low X/R ratio there is coupling between reactive power and frequency. Thus, the voltage is regulated through the active power and the frequency is controlled through the reactive power [2]. Additionally, in the case of comparable inductive and resistive parts of the grid (i.e the X/R ratio is close to 1), the voltage and frequency are linked with both active and reactive power, which requires a different controller structure [2]. However, by applying virtual impedance methods, the line impedance seen from the inverter can be adjusted to have a high X/R ratio [2]. For this reason, and because the focus will mainly be on high-voltage applications, only the outer loop structure that is shown in Fig. 2.1 will be considered in this work.

The inner loops can include additional voltage and current controllers that regulate the capacitor voltage and the inverter current respectively. Note that the output of the outer layer is sufficient for implementing the voltage source behavior of GFMIs and can be fed directly to the PWM. Thus, the inner loops are optional and can be bypassed. However, the use of a current controller can include certain benefits, such as active damping of the voltage controller, as well as the capability of simpler implementations of current-limitation techniques [21]. Also, the absence of an AC voltage controller, can cause distortion in the voltage waveform, in case of unbalanced or non linear loads [21]. The control structure without inner loops, also referred to as open loop control, is seldom used in practice [21].

Finally, the control system of the GFMI includes additional control blocks responsible for coordinate transformations, calculation of output power and voltage/current magnitude based on the measurements provided etc. For example, the active and reactive power are calculated using the following equations:

$$P = 1.5(i_d V_{PCC,d} + i_q V_{PCC,q}) \,, \tag{2.1}$$

$$Q = 1.5(i_d V_{PCC,q} - i_q V_{PCC,d}) \,. \tag{2.2}$$

There exist various control methods for the implementation of each subsystem that is shown in Fig. 2.1. The combination of these methods leads to multiple GFM control methods, which differ in the implementation of power synchronization loop, voltage profile management loop and the inner loops. In the following sections, an overview of the most common methods used for each subsystem will be provided.

### 2.1.2 Outer control loops

**Power synchronization loop**

The power synchronization loop (or Active Power Controller) generates the frequency and angle of the internal voltage source of the GFMI. Therefore, it is responsible for the synchronization of the converter with the grid [5]. Some of the most frequently used implementations of this control loop are described below.

*Droop control*

The first grid-forming control method used was the droop control, which was initially proposed to be used in isolated ac systems and uninterruptible power supplies [33]. This technique is inspired by the governor behavior, which allows the parallel operation of multiple SGs [2]. The droop controller calculates the frequency of the IVS as a linear function of the output active power, which is described by

$$\omega = \omega_0 + k_p(P_{ref} - P), \tag{2.3}$$

where $k_p$ is the droop coefficient, $\omega_0$ is the nominal angular frequency, $P_{ref}$ is the active power set-point, and $P$ is the measured instantaneous active power. The angle of the IVS is then calculated by integrating the frequency, as shown in the block diagram of Fig. 2.2a.

Despite being the simplest implementation of the Active Power Controller (APC), the droop control is highly effective and is able to synchronize without the need of other synchronization units under normal operating conditions [12].

As indicated in (2.3), a deviation of the instantaneous active power from its set-point will cause a step change in the frequency of the IVS of the GFMI [34]. Therefore, the droop controller does not provide inertia support, which is one of the main shortcomings of this method [2].

To mitigate fluctuations from the active power measurement, the droop controller can be equipped with a low pass filter (LPF) as shown in Fig. 2.2b. In this case, the equation describing the active power controller becomes

$$\omega = \omega_0 + k_p \frac{\omega_p}{s + \omega_p} \left(P_{ref} - P\right), \tag{2.4}$$

with $\omega_p$ being the cut-off frequency of the LPF.

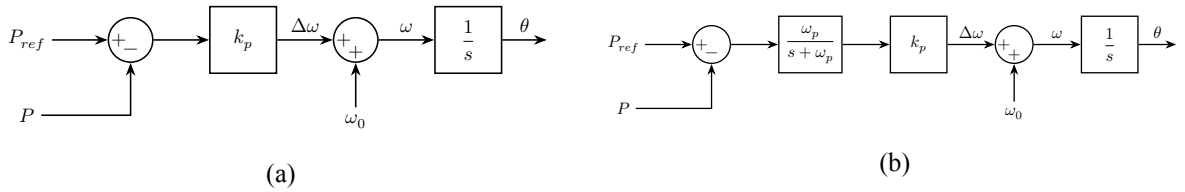



Figure 2.2: Block diagram of (a) Active power droop controller; (b) Active power droop controller with LPF

*Virtual synchronous generator*

To address the decrease of inertia in future power systems and to better emulate the behavior of synchronous generators, the virtual synchronous generator (VSG) method was proposed [35], [36]. A simple approach to provide virtual inertia, is to implement the swing

equation of synchronous machines in the control of GFMIs [21]. To that end, the control function that generates the frequency of the IVS for the VSG method is the following [37]

$$\omega = \frac{1}{Js}\left(P_{ref} - P + D_p(\omega_0 - \omega)\right), \tag{2.5}$$

where $D_p$ is the droop coefficient (or damping factor) and $J$ is the virtual moment of inertia. Fig. 2.3 shows the block diagram of the Active Power Controller of a VSG.

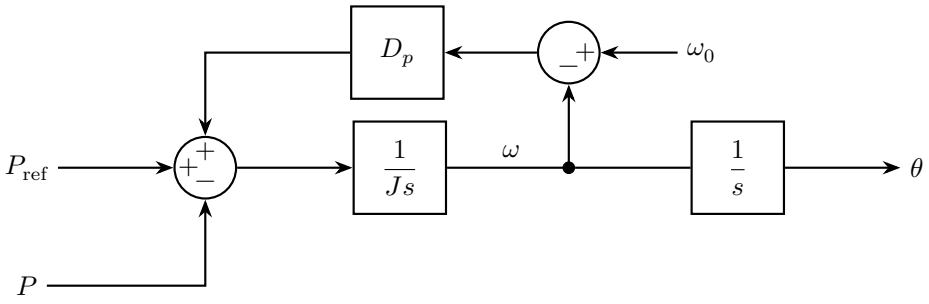



Figure 2.3: Block diagram of the Virtual Synchronous Generator

It has been shown in [38], that the droop controller with the low-pass filter is equivalent to the VSG, thus making it a specific case of a VSG. Therefore, although the initial purpose of the low-pass filter was to mitigate fluctuations in the measured active power, it also provides virtual inertia to the GFMI.

*Power synchronization control*

The concept of power synchronization control (PSC) was proposed in [23] for a VSC-HVDC system, to provide voltage support when connected to a weak grid. The synchronization principle used in this method is similar to the operation of synchronous machines. The equation that describes the synchronization loop of the PSC is

$$\theta = \omega_0 t + k_p \int (P_{ref} - P), \tag{2.6}$$

where $k_p$ is the controller gain. The block diagram of this control loop is given in Fig. 2.4. Taking the derivative of both sides in the above equation gives

$$\frac{d\theta}{dt} = \omega = \omega_0 + k_p(P_{ref} - P). \tag{2.7}$$

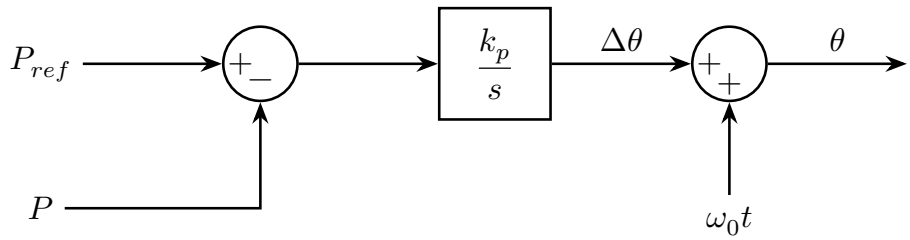



Figure 2.4: Block diagram of the power synchronization control

Comparing (2.7) and (2.3) as well as Fig. 2.2a and Fig. 2.4, it becomes evident that droop control and PSC are mathematically equivalent, despite being initially developed for different

applications. Therefore, PSC can be considered to be a specific version of the droop controller. Note that despite the fact that the PSC is able to synchronize with the grid without the use of a PLL, in case of faults the converter switches to GFL control using a backup PLL [23].

*Other control methods*

Another control method that was proposed to allow parallel operation of converters is the virtual oscillator control [39]. Unlike the other methods presented, the virtual oscillator control is not based on the operating principle of synchronous machines, but is rather inspired by the phenomenon of synchronization in networks of coupled oscillators. This method offers the benefits of faster synchronization and improved overall stability [21].

Additionally, a dc-link voltage controller that enables synchronization and dc-link voltage regulation is proposed in [40]. This method is referred to as ViSynC and it allows GFMIs to exhibit power-frequency characteristics similar to those of synchronous machines. Also with the use of certain control parameters, the damping and inertia can be tuned in a way that the dc link voltage remains in the acceptable range.

**Voltage profile management loop**

The voltage profile management loop (or Reactive Power Controller) is responsible for the calculation of the magnitude of the GFMI internal voltage source. Some of the methods proposed in the literature are presented below.

*Droop control*

Similar to the APC, the droop controller can be used in the Reactive Power Controller (RPC) as well. In this case, the magnitude of the IVS is calculated as a linear function of the reactive power output, which is described by [2]

$$E = V_0 + k_q(Q_{ref} - Q), \tag{2.8}$$

where $k_q$ is the droop coefficient, $V_0$ is the nominal voltage, $Q_{ref}$ is the reactive power set point and $Q$ is the measured reactive power output.

In analogy with the active power droop control, a low-pass filter can be used to mitigate fluctuations of the measured reactive power [37]. Then the control function becomes

$$E = V_0 + k_q \frac{\omega_q}{s + \omega_q} \left(Q_{ref} - Q\right), \tag{2.9}$$

with $\omega_q$ being the cut-off frequency of the LPF. The block diagrams of the reactive power droop controller with and without low-pass filter are shown in Fig. 2.5.

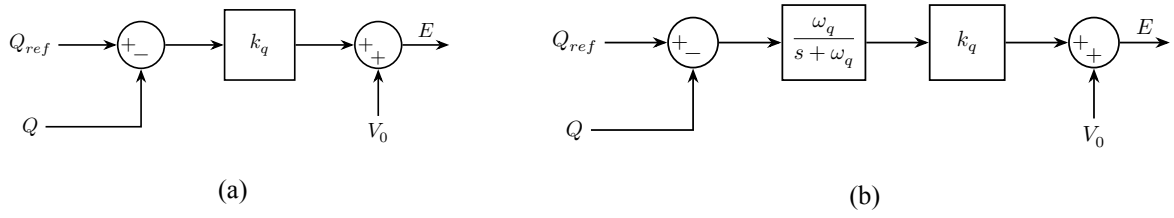



Figure 2.5: Block diagram for (a) Reactive power droop controller; (b) Reactive power droop controller with LPF

*PI-based voltage control*

Another control method proposed for the voltage profile management loop is using a PI controller, which controls the magnitude of the measured PCC voltage to track its reference value [41]. This method was proposed for a STATCOM operating as a Virtual Synchronous Machine. The control function is the following:

$$E = (V_{ref} - V)G(s) \tag{2.10}$$

where $V_{ref}$ is the reference voltage magnitude, $V$ is the measured PCC voltage magnitude and $G(s)$ is the transfer function of the PI controller. The transfer function of a basic PI controller is

$$G(s) = k_p + \frac{k_i}{s}, \tag{2.11}$$

with $k_p$ and $k_i$ being the proportional and integral gain of the PI controller, respectively.

*PI-based reactive power control*

Another PI-based control method, is the control of the reactive power output to follow its set-point, by utilizing a PI controller and an additional term for the feedforward of the voltage reference [12], [42]. The control function is

$$E = V_{ref} + (Q_{ref} - Q)G(s), \tag{2.12}$$

with $G(s)$ being the transfer function of the PI controller. The block diagram of the PI-based voltage and reactive power control is shown in Figures 2.6a and 2.6b respectively.

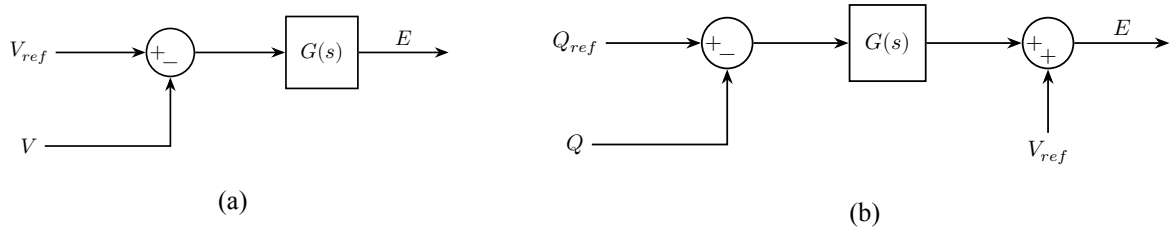



Figure 2.6: Block diagram of the (a) PI-based voltage controller; (b) PI-based reactive power controller [12]

*Other control methods*

In addition to the control methods presented above, cascaded control structures including both PI-based and droop controllers have been proposed. For instance, in [23] the first (outer) layer is a PI controller regulating the reactive power, similar to the above, and the second (inner) layer is an Alternating Voltage Controller with a droop characteristic. Another popular implementation consists of a droop controller for the voltage difference in the first layer and then a PI controller regulating the reactive power in the second layer [12], [43].

### 2.1.3 Inner control loops

As it was previously explained, the GFMI synchronizes with the grid via the power synchronization loop, which generates the angle reference and the voltage profile management loop provides the magnitude of the IVS. Additional inner loops can be used for current limitation, voltage control, power-quality enhancement etc [21]. As shown in Fig. 2.1 the output of the inner loops is the reference voltage, which is then normalized (multiplied by

$2/V_{dc}$) and fed to the modulation. Various inner-loop implementations have been proposed in the literature, some of which are presented below.

***Direct voltage synthesis***

The most straight-forward approach is to directly feed the output of the outer loops to the PWM [44]. Because the angle generated by the APC is used for coordinate transformations, the synchronous reference frame is aligned with the internal voltage source of the GFMI. Thus, the q-axis component of the IVS is zero, while the d-axis component is equal to the magnitude of the IVS, as provided by the voltage profile management loop. The direct voltage synthesis or open loop control is shown in Fig. 2.7. Despite having the benefit of simple implementation, this method lacks controllability over both the current and output voltage (i.e., after the filter impedance) of the GFMI. As a result, the output voltage cannot be maintained at its nominal value under different power generation scenarios and the GFMI may also suffer from overcurrent during faults [21].

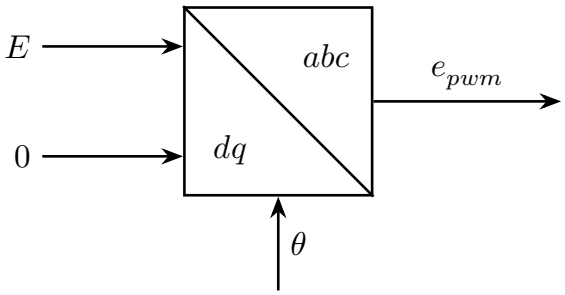



Figure 2.7: Illustration of the open loop control

***Single-loop voltage magnitude control***

The single-loop voltage magnitude (SLVM) control uses an integrator to regulate the output voltage amplitude to track the reference provided by the voltage profile management loop [21]. Fig. 2.8 shows the implementation of the SLVM control, where an LPF is used to suppress high-frequency noise in the measured output-voltage magnitude. Unlike the open-loop control, the output-voltage magnitude can be maintained at the nominal value during different power generation scenarios, due to the use of the integrator [21]. However, because of its typically low bandwidth, the SLVM exhibits similar dynamics with the open-loop control across a wide frequency range [21], [45]. Despite the output voltage amplitude control of the SLVM, it still lacks current controllability and thus it may also suffer from overcurrent during faults, if no additional current limiting techniques are used.

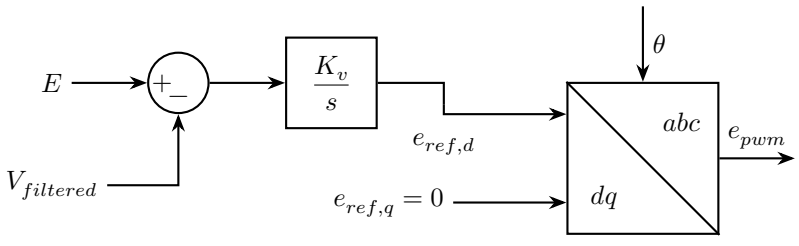



Figure 2.8: Illustration of the single loop voltage magnitude control

***Dual-loop vector voltage current control***

To address the lack of current controllability in the previous methods, a dual-loop voltage and current control is often used, which consists of a voltage controller in the first (outer) layer, followed by a current controller in the second (inner) layer [12]. The output of the current controller is the reference voltage fed to the PWM, as shown in the general block diagram of Fig. 2.9. The voltage and current controllers can either be implemented in the αβ or dq frame, using PR (Proportional+Resonant) or PI controllers respectively. The use of the current controller allows for easier implementation of current limiting methods.

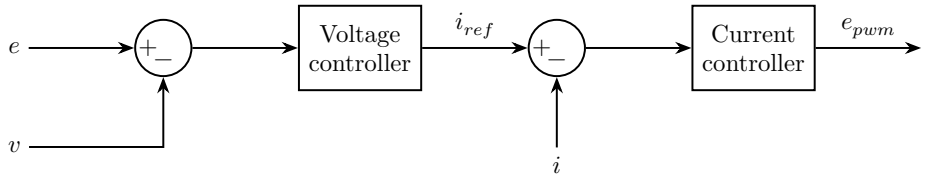



Figure 2.9: General block diagram of the dual-loop vector voltage current control

Fig. 2.10 shows the implementation of the dual-loop vector voltage current control in the dq reference frame, which consists of four PI controllers, two for each component of the voltage and current. Additionally, coupling terms and disturbances (such as $\omega_0 L_f i_{dq}$, $\omega_0 C_f V_{PCC,dq}$ and $i_{g,dq}$, $V_{PCC,dq}$) are compensated with the appropriate decoupling and feedforward terms [15].

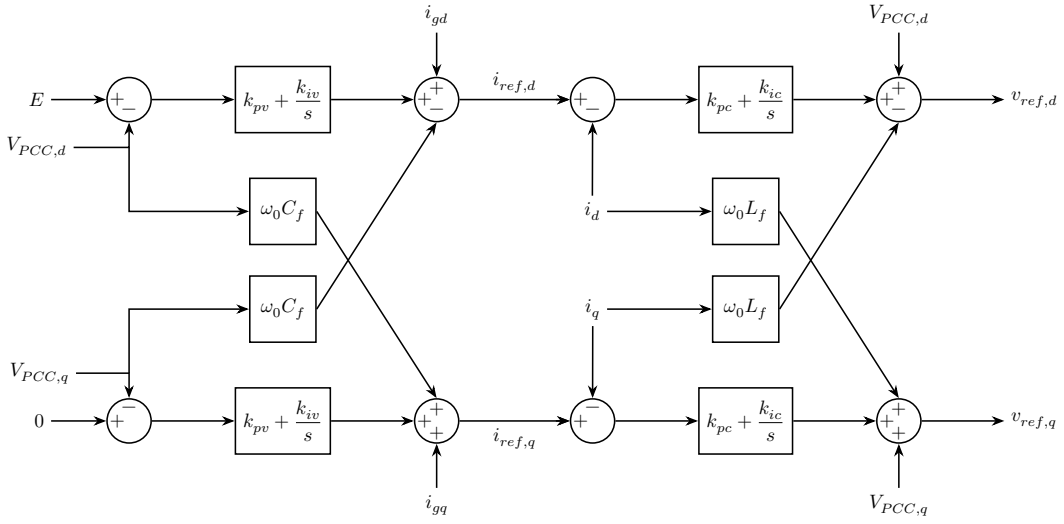



Figure 2.10: Implementation of the dual-loop vector voltage current control in the dq-frame

***Virtual admittance control***

Another multi-loop control architecture is the virtual admittance control, which is illustrated in Fig. 2.11. The control structure is very similar to the dual-loop vector voltage current control, but the voltage controller is replaced with a virtual-admittance emulation function [46]. Thus, when the virtual admittance control is used, the converter output impedance can be better regulated [47]. However, due to the emulated virtual admittance, the GFMI's output voltage quality is inferior to that achieved with the dual-loop vector voltage current control [21].

The virtual admittance block emulates a series virtual impedance between the GFMI's

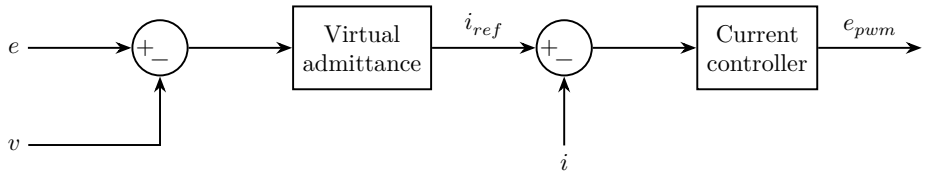



Figure 2.11: General block diagram of the virtual admittance control

internal voltage source and the PCC voltage. Therefore the current reference in the αβ frame is given by [46]

$$i^*_{\alpha\beta} = \frac{E_{\alpha\beta} - V_{PCC,\alpha\beta}}{R_v + sL_v}, \tag{2.13}$$

with $R_v$, $L_v$ being the emulated virtual resistance and inductance, and $E_{\alpha\beta}$, $V_{PCC,\alpha\beta}$ being the IVS and PCC voltage in the αβ reference frame respectively.
Transforming (2.13) to the dq reference frame results in [48]

$$i^*_d = \frac{E_d - V_{PCC,d} + \omega_0 L_v i^*_q}{R_v + sL_v}, \tag{2.14}$$

$$i^*_q = \frac{E_q - V_{PCC,q} - \omega_0 L_v i^*_d}{R_v + sL_v}. \tag{2.15}$$

The control block implementation of the above equations, which is called the dynamic implementation of the virtual admittance [49], is shown in Fig. 2.12a. This dynamic implementation has been shown to exhibit a poorly damped response for low virtual resistance values [49]. Therefore, in order to avoid the coupling of active and reactive power caused by a large virtual resistance value and to allow a wider range of virtual admittance values, a quasi-stationary implementation of the virtual-admittance loop can be used [48], [49]. The quasi-stationary implementation is proposed in [50] and the control equations are

$$\begin{bmatrix} i^*_d \\ i^*_q \end{bmatrix} = \frac{1}{R_v^2 + X_v^2} \begin{bmatrix} R_v & X_v \\ -X_v & R_v \end{bmatrix} \begin{bmatrix} E_d - V_{PCC,d} \\ E_q - V_{PCC,q} \end{bmatrix}, \tag{2.16}$$

where $X_v = \omega_0 L_v$ is the virtual reactance at nominal angular frequency.

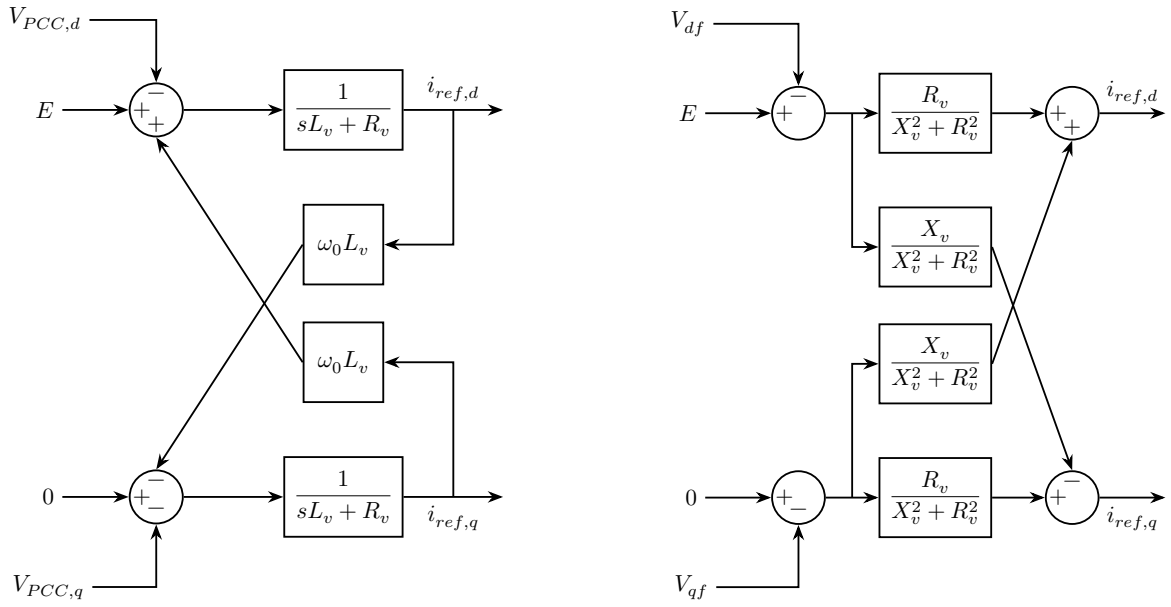
Additionally, in [49] it is identified that a low-pass filter should be used for the PCC voltage measurement, in order to prevent oscillatory or unstable response of the quasi-stationary implementation. In that case, the virtual admittance emulation function becomes

$$\begin{bmatrix} i^*_d \\ i^*_q \end{bmatrix} = \frac{1}{R_v^2 + X_v^2} \begin{bmatrix} R_v & X_v \\ -X_v & R_v \end{bmatrix} \begin{bmatrix} E_d - V_{df} \\ E_q - V_{qf} \end{bmatrix}, \tag{2.17}$$

where $V_{df}$ and $V_{qf}$ are the filtered dq components of the PCC voltage. The controller implementation of (2.17) is shown in Fig. 2.12b.

## 2.2 Current-limiting control methods for grid-forming inverters

The simplified equivalent circuit of a grid-forming inverter connected to the grid is depicted in Fig. 2.13, where the GFMI is represented by the IVS behind an equivalent output impedance and the grid is modeled as a Thevenin equivalent. The IVS is determined by the output of the outer loops, namely $E$ and $\theta$, while the output impedance of the GFMI ($Z_{eq}$) is shaped by the filter impedance and the specific inner-loop implementation [21].




(a) (b)

Figure 2.12: Implementation of the VA loop (a) Dynamic model; (b) Quasi-stationary model

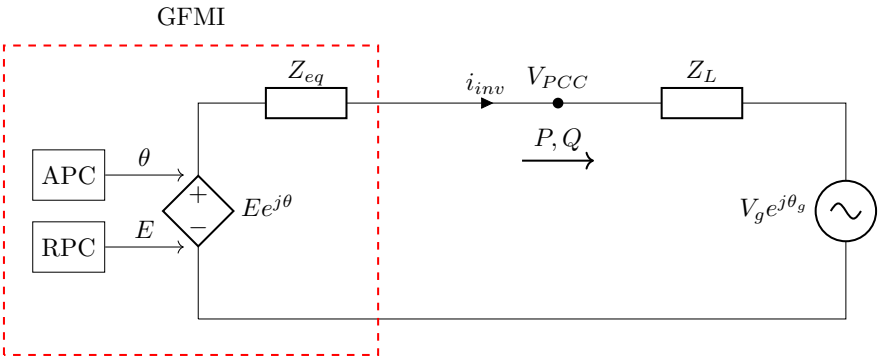



Figure 2.13: Simplified equivalent circuit of a GFMI connected to the grid [21]

The output-current magnitude of the GFMI in the per unit system is given by

$$I = \frac{||\mathbf{E} - \mathbf{V_{PCC}}||}{Z_{eq}}, \tag{2.18}$$

where $\mathbf{E}$ and $\mathbf{V_{PCC}}$ are the phasors of the IVS and the PCC voltage respectively, $Z_{eq}$ is the magnitude of the equivalent output impedance of the GFMI and $||\cdot||$ represents the magnitude of a complex number. During grid faults such as voltage sags and phase jumps, the magnitude of the voltage drop that appears in the numerator of (2.18) can become larger. As a result the output current magnitude may surpass the maximum permissible value of the converter [27].

To protect the converter from hardware damage and successfully ride-though disturbances, various current-limiting methods have been proposed in the literature, which can be classified into direct, indirect or hybrid methods, depending on the way they achieve current limitation [28], [51]. More specifically, direct current limiters attempt to maintain the converter's current within the maximum permissible value, by appropriately adjusting the reference values provided to the current controller [28]. On the other hand, indirect current-limiting methods aim to limit the current indirectly, by decreasing the voltage difference in the numerator of

(2.18), by adjusting the power set-points of the inverter, or by raising the value of the equivalent output impedance [28], [51]. Hybrid methods restrict the inverter's current by utilizing a combination of multiple direct and/or indirect current limiters [51]. In the following, some of the most commonly used current-limiting methods are presented.

### 2.2.1 Direct current-limiting methods

As illustrated in Fig. 2.14, direct current-limiting methods utilize saturation algorithms to adjust the current reference provided by the virtual-admittance loop or the voltage controller, such that its magnitude doesn't exceed the maximum allowed value [28]. Due to the high bandwidth of the inner current-control loop, the current is able to follow its reference, and therefore this type of methods can achieve quick and accurate current limitation [27]. In the following, several current saturation algorithms (CSA) proposed for direct current-limiting methods are described.

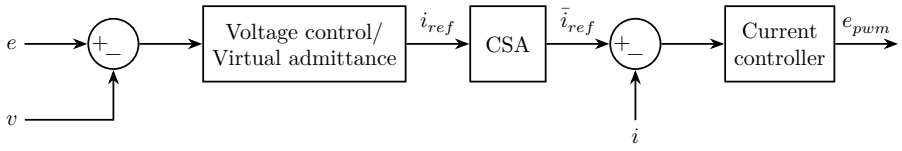



Figure 2.14: General block diagram for implementation of direct current limiters

***Instantaneous limiter***

The instantaneous limiter can be designed in multiple reference frames based on the following equation [27], [52]:

$$\bar{i}_{ref,i} = \begin{cases} i_{ref,i}, & |i_{ref,i}| \leq I_{max,i} \\ \text{sgn}(i_{ref,i}) I_{max,i}, & |i_{ref,i}| > I_{max,i} \end{cases} \tag{2.19}$$

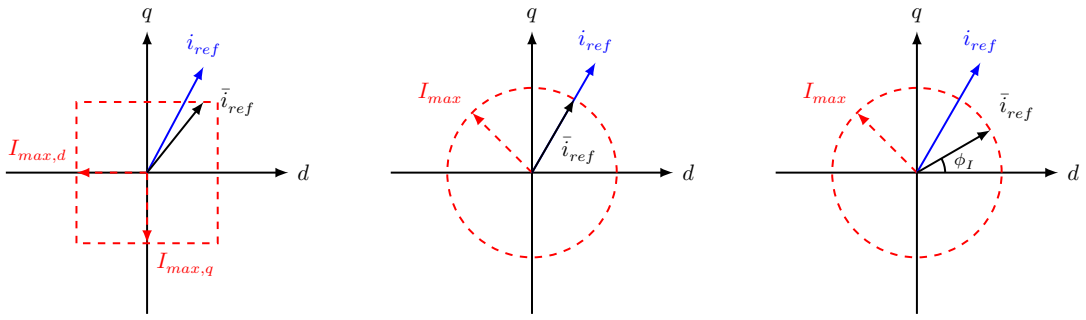
where $i$ is the reference frame axis (namely a,b,c/ α,β/ d,q), $i_{ref,i}$ are the unsaturated current references provided by the voltage controller or the virtual admittance loop, $\bar{i}_{ref,i}$ are the saturated current references and $I_{max,i}$ is the maximum allowed value of the current for each axis. Also the function $\text{sgn}(\cdot)$ represents the sign of a number. Fig. 2.15a illustrates the implementation of the instantaneous current limiter in the dq frame.

In case the instantaneous limiter is designed in the natural reference frame (abc-frame), $I_{max,i}$ is selected equal to $I_{max}$, whereas in the stationary or synchronous reference frames (αβ- and dq-frame), $I_{max,i}$ is typically chosen as $I_{max}/\sqrt{2}$, such that $\sqrt{(\bar{i}_{ref,\alpha/d})^2 + (\bar{i}_{ref,\beta/q})^2} \leq I_{max}$ always holds [27].

***Magnitude limiter***

The magnitude limiter (or circular limiter) restricts the magnitude of the current reference, while keeping its angle unchanged [27], as illustrated in Fig. 2.15b. The initial design of the magnitude limiter was in the stationary or synchronous reference frame and it is expressed as follows [51]:

$$\bar{i}_{ref} = \begin{cases} i_{ref}, & ||i_{ref}|| \leq I_{max} \\ \dfrac{I_{max}}{||i_{ref}||} i_{ref}, & ||i_{ref}|| > I_{max} \end{cases} \tag{2.20}$$




(a) (b) (c)

Figure 2.15: Graphical illustration of different direct current limiting methods (a) Instantaneous limiter; (b) Magnitude limiter; (c) Fixed angle limiter

where $i_{ref}$ and $\bar{i}_{ref}$ are the original and saturated current reference in the αβ or dq frame respectively and $||\cdot||$ is the modulus of the complex variable.

A generalized implementation of the magnitude limiter in the abc frame has been developed [53], which is described as follows:

$$\bar{i}_{ref,i} = \begin{cases} i_{ref,i}, & I_{ref,i} \leq I_{max} \\ \dfrac{I_{max}}{I_{ref,i}} i_{ref,i}, & I_{ref,i} > I_{max} \end{cases} \tag{2.21}$$

where $i = a, b, c$ and $I_{ref,i}$ is the magnitude of $i_{ref,i}$.

***Fixed angle limiter***

Fig. 2.15c illustrates the fixed angle limiter in the dq frame. When this current limiter is activated, it curtails the magnitude of the current reference to $I_{max}$ and also sets its angle to a certain value $\phi_I$. Therefore, this angle corresponds to the angle difference of the saturated current reference and the d-axis, which is aligned with $\theta$ provided by the outer loops [27]. The implementation of the fixed angle limiter in the synchronous reference frame is given by [32]

$$\bar{i}_{ref} = \begin{cases} i_{ref}, & ||i_{ref}|| \leq I_{max} \\ I_{max} e^{j\phi_I}, & ||i_{ref}|| > I_{max} \end{cases} \tag{2.22}$$

The angle of the saturated current reference is a control parameter and can therefore be selected arbitrarily. In some works [54] $\phi_I$ is chosen equal to zero, but other selections are possible as well. For instance, in [32] it is selected based on an optimization method, in order to enhance the transient stability of the GFMI.

***Priority based limiter***

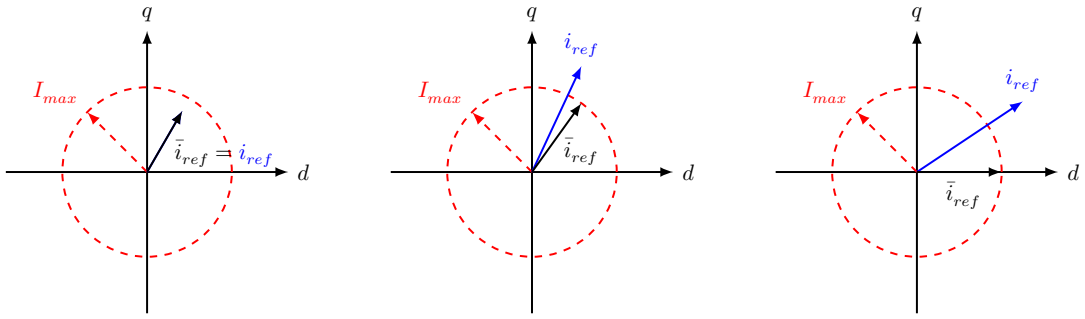
The priority based limiter gives priority to the d-axis or the q-axis component of the current reference when the current limiter engages. The d-axis priority limiter is described by the following equation [55]:

$$\begin{aligned} \bar{i}_{ref,d} &= \text{sgn}(i_{ref,d}) \min(I_{max}, |i_{ref,d}|) \\ \bar{i}_{ref,q} &= \text{sgn}(i_{ref,q}) \min\left(\sqrt{I_{max}^2 - (\bar{i}_{ref,d})^2}, |i_{ref,q}|\right) \end{aligned} \tag{2.23}$$

Similarly, the q-axis priority limiter is expressed as

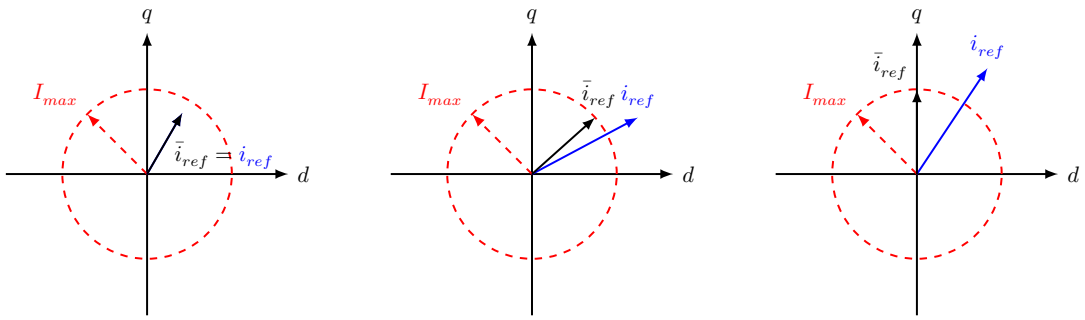
$$\begin{aligned} \bar{i}_{ref,q} &= \text{sgn}(i_{ref,q}) \min(I_{max}, |i_{ref,q}|) \\ \bar{i}_{ref,d} &= \text{sgn}(i_{ref,d}) \min\left(\sqrt{I_{max}^2 - (\bar{i}_{ref,q})^2}, |i_{ref,d}|\right) \end{aligned} \tag{2.24}$$

The d- and q-axis priority limiters are graphically illustrated in Fig. 2.16 and Fig. 2.17 respectively.




(a) (b) (c)

Figure 2.16: Graphical illustration of d-axis priority current limiter (a) Case 1: $||i_{ref}|| \leq I_{max}$; Case 2: $||i_{ref}|| > I_{max}$ with $i_{ref,d} \leq I_{max}$; Case 3: $i_{ref,d} > I_{max}$




(a) (b) (c)

Figure 2.17: Graphical illustration of q-axis priority current limiter (a) Case 1: $||i_{ref}|| \leq I_{max}$; Case 2: $||i_{ref}|| > I_{max}$ with $i_{ref,q} \leq I_{max}$; Case 3: $i_{ref,q} > I_{max}$

**Comparison of direct current-limiting methods**

Despite achieving effective current limiting, all direct current-limiting methods may exhibit transient overcurrent, due to the dynamics of the current controller [21]. Although the instantaneous limiter is the easiest to implement, when designed in the abc or αβ frame, it can distort the current waveform due to clipping of the sinusoidal current reference [27]. Also, when the implementation is in the αβ or dq frame, the current limits of each axis may be conservative (e.g $I_{max,i} = I_{max}/\sqrt{2}$), resulting in decreased utilization of the inverter capacity [21]. For example, if $I_{max} = 1.2$ pu the current limit for the d- and q- axis will be $I_{max,dq} = I_{max}/\sqrt{2} \approx 0.85$ pu. Consider as an example, an original current reference in the dq frame of $i_{ref} = 0.8 + j1.3$, with magnitude 1.53 pu. In this case, only the q-component of the current exceeds its limit, resulting in a saturated current equal to $i_{ref} = 0.8 + j0.85$, whose magnitude is 1.17 pu. It is evident that although the initial current reference magnitude was larger than the inverter current limit, the saturated current magnitude is restricted at a value below the maximum allowed current. Consequently, the full overcurrent capability of

the inverter is not utilized. In contrast, the rest of the presented current limiters can utilize the full overcurrent capability of the inverter, while maintaining a non distorted current, but require an additional calculation of the current reference magnitude [27].

Additionally, due to the fact that direct current limiters achieve current limitation by saturating the current reference feeding into the current control loop, when the current limiter is triggered, the integrators of vector voltage and voltage magnitude controllers may suffer from windup issues, which can compromise the fault recovery capability [56]. To that end, proper anti-windup schemes should be used for the outer voltage controllers [27], [28].

### 2.2.2 Indirect current-limiting methods

Indirect current-limiting methods aim to curtail the current of the GFMI by adjusting the power references of the outer loops, using voltage limiters to decrease the voltage difference between the IVS and the PCC voltage, or by appropriately shaping the equivalent output impedance of the GFMI through virtual impedance/admittance methods [28].

***Power reference adjustment current limiting***

This method adjusts the active and reactive power set-points of the GFMI outer loops during disturbances, in order to ensure that $\sqrt{P_{ref}^2 + Q_{ref}^2} \leq V_{PCC} I_{max}$. Thereafter, current limitation can be achieved if the adjusted power references are tracked by the outer loop controllers [51].

The modified power references are typically chosen in accordance to grid codes [19] as illustrated by the following example [51]:

$$Q_{ref} = \begin{cases} Q^*, & V_{PCC} \geq 0.9 \text{ pu} \\ V_{PCC} I_q, & 0.5 \text{ pu} < V_{PCC} < 0.9 \text{ pu} \\ V_{PCC} I_{max}, & V_{PCC} \leq 0.5 \text{ pu} \end{cases} \tag{2.25}$$

$$P_{ref} \leq \sqrt{V_{PCC}^2 I_{max}^2 - Q_{ref}^2} \tag{2.26}$$

where $V_{PCC}$ is the magnitude of the PCC voltage, $I_q$ is the reactive current requirement for a PCC voltage range of 0.5 pu to 0.9 pu and $Q^*$ is the initial reactive power set-point.

***Virtual impedance current limiting***

Virtual Impedance (VI) methods curtail the current by increasing the equivalent output impedance of the inverter. This is achieved by passing the measured current through a virtual impedance and subtracting the resulting voltage drop terms from the original voltage reference [55], [57]. Therefore, while direct current limiters act directly on the current reference, virtual impedance methods aim to adjust the voltage reference so that the resulting current does not exceed the maximum allowed value [28]. To prevent unnecessary voltage drop during normal operation, the virtual impedance should be activated only when the current magnitude exceeds a predefined threshold. Therefore, this threshold should not be selected lower than the nominal current, yet it must remain smaller than $I_{max}$ to prevent overcurrent [58].

The parameters of the VI can be chosen to be constant, state-depended or time-varying [51]. The constant VI limiter activates a fixed VI when the current magnitude exceeds a predefined threshold and therefore can excessively limit the output current even in less severe faults. This results in the inverter overcurrent capability not being fully utilized, and thus the

constant VI limiter is not frequently used [59]. A widely used state-depended calculation of the VI parameters is the following [3], [57]:

$$X_{vi} = \sigma R_{vi} \quad R_{vi} = \begin{cases} 0, & I \leq I_{thres} \\ K_{VI}(I - I_{thres}), & I > I_{thres} \end{cases} \tag{2.27}$$

where $R_{vi}$ and $X_{vi}$ are the resistive and inductive part of the VI respectively, $I$ and $I_{thres}$ are the current magnitude and its threshold, $\sigma$ is the predefined X/R ratio of the VI and $K_{VI}$ is a constant control parameter.

Generally, VI parameters are tuned such that the current doesn't exceed the maximum allowed value, even under the worst-case scenario, which is typically considered to be a three-phase bolted fault at the terminals of the GFMI [57]. The X/R ratio of the VI must be sufficiently high to ensure a predominantly inductive VI, thereby avoiding the coupling of active and reactive power [57]. At the same time, the X/R ratio should not be selected excessively high, as the resistive part is necessary for damping, with $\sigma = 5$ providing a good tradeoff [3]. Once the X/R ratio is determined, the $K_{VI}$ is calculated such that $||i|| \leq I_{max}$ is satisfied under the worst-case scenario. Two cases are considered, namely the VI with inner loops and the VI without inner loops.

The implementation of the *virtual impedance method with inner loops* is shown in Fig. 2.18. Assuming that the new voltage reference, i.e., with the fictitious voltage drop on the VI, can be quickly tracked by the voltage controller, the resulting equivalent circuit for this method is that of Fig. 2.19 [27]. Therefore, the equivalent output impedance of the GFMI consists only of the VI.

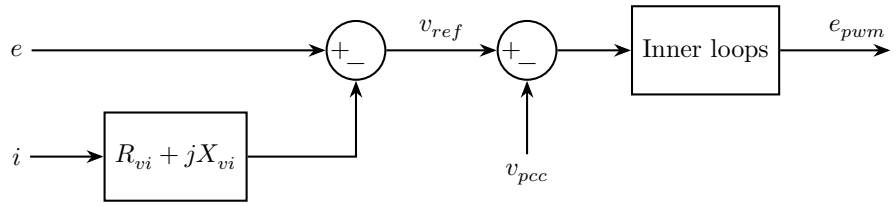



Figure 2.18: Implementation of the virtual impedance current limiter with inner loops

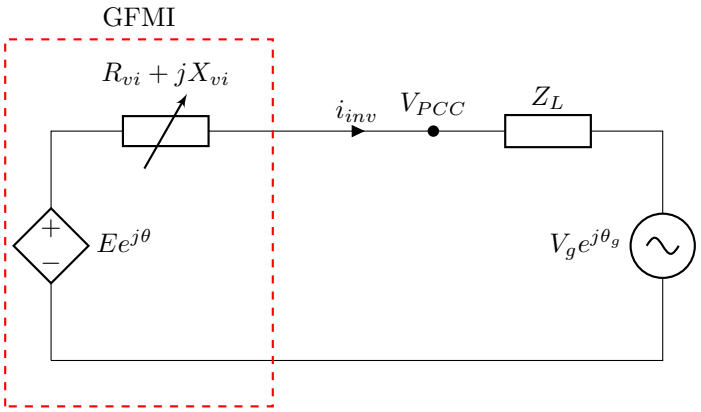



Figure 2.19: Equivalent circuit of the GFMI when the virtual impedance method with inner loops is used [27]

According to (2.18), in order to effectively limit the current under the worst-case scenario,

the following condition should be satisfied:

$$I = \frac{V_{max}}{Z_{VI}} \leq I_{max} \implies Z_{VI} \geq \frac{V_{max}}{I_{max}}$$

where $Z_{VI} = ||R_{vi} + jX_{vi}||$ is the modulus of the virtual impedance and $V_{max}$ is the maximum expected voltage difference magnitude between the IVS and the PCC voltage (i.e., $||\mathbf{E} - \mathbf{V_{PCC}}||_{max}$). To calculate the lower boundary of $K_{VI}$, the case where the current is limited exactly to $I_{max}$ under the worst-case scenario is considered. Using $I = I_{max}$ in (2.27) and substituting in the above equation, the minimum value of $K_{VI}$ is obtained as [27]:

$$Z_{VI} = \sqrt{R_{vi}^2 + X_{vi}^2} = K_{VI}(I_{max} - I_{thres})\sqrt{1+\sigma^2} \geq \frac{V_{max}}{I_{max}} \tag{2.28}$$

The implementation of the *virtual impedance method without inner loops* is shown in Fig. 2.20. In this case the modulation reference is directly modified by subtracting the fictitious voltage drop on the VI, resulting in the equivalent circuit of Fig. 2.21 [27].

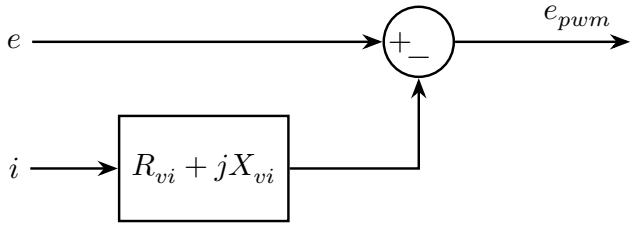



Figure 2.20: Implementation of the virtual impedance current limiter without inner loops

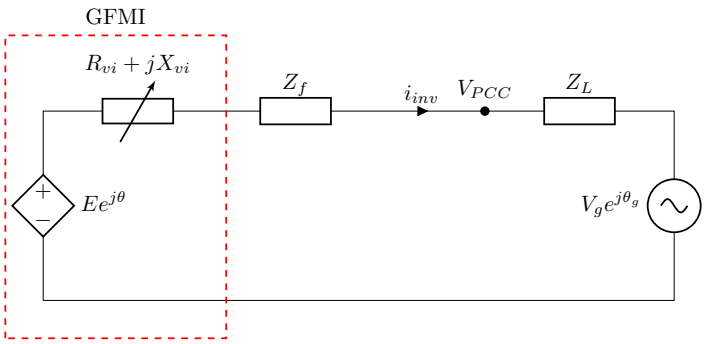



Figure 2.21: Equivalent circuit of the GFMI when the virtual impedance method without inner loops is used [27]

When this method is used, the filter impedance is included in the equivalent output impedance, in series with the VI [45]. Similar to before, $K_{VI}$ can be calculated by substituting (2.27), with $I = I_{max}$, into the following [27]:

$$||R_{vi} + jX_{vi} + Z_f|| \geq \frac{V_{max}}{I_{max}} \tag{2.29}$$

***Virtual admittance current limiting***

The virtual admittance (VA) current-limiting method intends to limit the inverter current by increasing the equivalent output impedance. In contrast to VI methods that use a derivative

controller to emulate a virtual inductance $L_{vi}$ or a virtual reactance $X_{vi}$ at $\omega_0$, the VA method emulates a virtual inductor within the bandwidth of the current controller [27], as depicted in Fig. 2.22. On the other hand, with the VA method it is essential to have non zero $R_v$ and $X_v$ during normal operation, due to the use of a virtual admittance loop to generate the current control reference [27]. Thus, the selection of the virtual admittance parameters may not be identical with the VI method, but they are rather given by [27], [60]

$$\begin{aligned} R_v &= \max\{R_{vn}, Z_v/\sqrt{1+\sigma^2}\} \\ L_v &= \max\{L_{vn}, \sigma R_v/\omega_0\} \end{aligned} \tag{2.30}$$

where $L_{vn}$ and $R_{vn}$ are the virtual inductance and resistance in normal operation respectively, and $Z_v = ||\mathbf{E} - \mathbf{V_{PCC}}||/I_{max}$. The equivalent circuit of the virtual admittance method is depicted in Fig. 2.23.

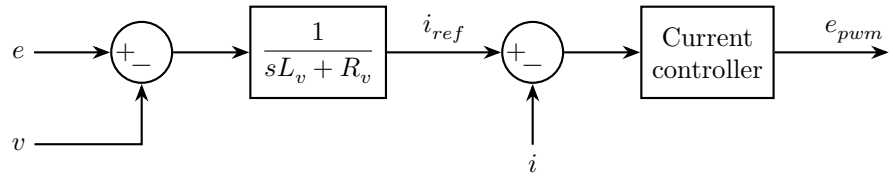



Figure 2.22: Implementation of the virtual admittance current limiting method

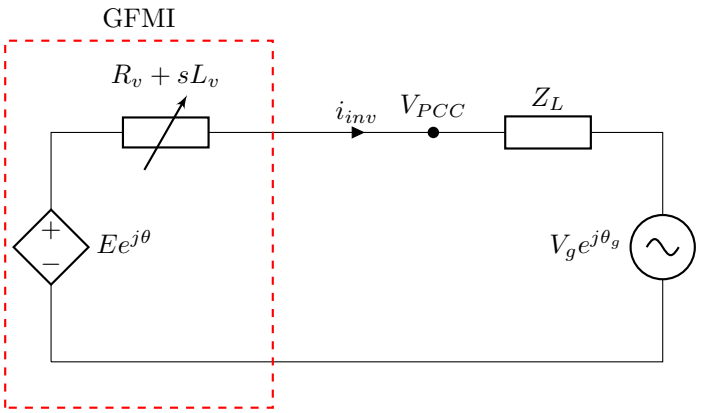



Figure 2.23: Equivalent circuit of the GFMI when the virtual admittance current limiting method is used [27]

### *Voltage limiters*

Voltage limiters intend to decrease the voltage difference $||\mathbf{e_{pwm}} - \mathbf{V_{PCC}}||$ to remain below $Z_f I_{max}$, by adjusting the references provided by the outer loops [61]. In these methods, the modulation voltage reference $\mathbf{e_{pwm}}$ is equal to the saturated IVS reference, because the inner loops are typically transparent [51]. Therefore the equivalent circuit of this method is that of Fig. 2.24.

The adjustment of the outer loop references by the voltage limiter can be expressed as

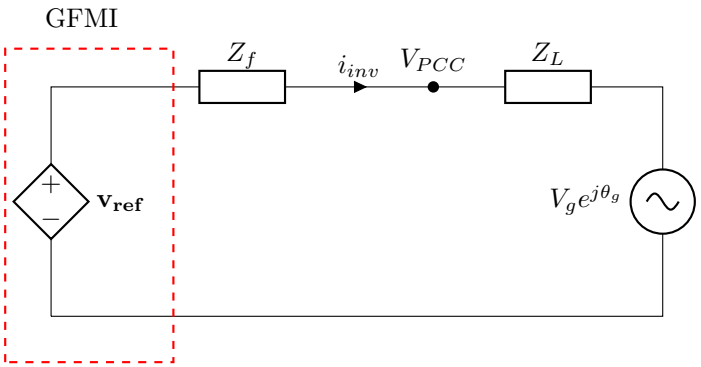



Figure 2.24: Equivalent circuit of the GFMI when the voltage limiter is used [27]

follows [61]:

$$V_{ref} = \begin{cases} V_{PCC} + E_{lim}, & E > V_{PCC} + E_{lim} \\ E, & V_{PCC} - E_{lim} \leq E \leq V_{PCC} + E_{lim} \\ V_{PCC} - E_{lim}, & E < V_{PCC} - E_{lim} \end{cases} \tag{2.31}$$

where $V_{ref}$ is the magnitude of the saturated reference voltage ($\mathbf{v_{ref}}$), and

$$\theta_{ref} = \begin{cases} \theta_{PCC} + \delta_{lim}, & \theta > \theta_{PCC} + \delta_{lim} \\ \theta, & \theta_{PCC} - \delta_{lim} \leq \theta \leq \theta_{PCC} + \delta_{lim} \\ \theta_{PCC} - \delta_{lim}, & \theta < \theta_{PCC} - \delta_{lim} \end{cases} \tag{2.32}$$

where $\theta_{ref}$ is the angle of the saturated reference voltage and $\theta_{PCC}$ is the angle of the PCC voltage. $E_{lim}$ and $\delta_{lim}$ are the maximum permissible magnitude and angle difference respectively and they are chosen such that $||\mathbf{v_{ref}} - \mathbf{V_{PCC}}||$ does not exceed $Z_f I_{max}$ [27].

**Comparison of indirect current-limiting methods**

The virtual impedance method with inner loops effectively limits the current, by assuming that the voltage controller can quickly follow its reference. However, because of the relatively low bandwidth of the voltage controller, the inverter may suffer from temporary overcurrent during the initial stage of the disturbance [55]. The VI method without inner loops is faster, because there are no additional delays from the inner loops, but since the current is not directly controlled, temporary overcurrent may still be observed. Similarly, power limiters rely on outer loops to quickly track their references to achieve current limitation. However, since the bandwidth of the outer loops is typically designed to be relatively low (up to ten fundamental cycles [62]), significant overcurrent may be observed at the initial stage of a disturbance. For this reason, power limiters are not a suitable choice for a stand-alone current limiter [28].

Additionally, it is evident from (2.28) that the virtual impedance/admittance parameters are selected such that the inverter current is limited to $I_{max}$ during the worst-case scenario. Consequently, in case of less severe faults, the overcurrent capability of the GFMI will be underused [28].

Unlike direct current limiters, virtual impedance/admittance methods do not require anti-windup schemes for the inner loop controllers, as they do not directly saturate the current reference [21]. However anti-windup control schemes remain essential for the outer voltage magnitude control loop [21].

In regard to the voltage limiter, it can be implemented without the need of the current magnitude and angle measurement, but it requires additional information of the terminal voltage magnitude and angle [27]. Also, since the references for voltage magnitude $E$ and the angle $\theta$ provided by the outer loops are saturated, proper anti-windup schemes are required to avoid compromising the inverter's fault recovery capability [27].

### 2.2.3 Hybrid current-limiting methods

Each direct and indirect current-limiting method has strengths and weaknesses. Hybrid current limiters combine a number of different current limiters, in order to exploit the advantages of each method and achieve satisfactory performance across multiple requirements, such as efficient current limitation, fault current injection and transient stability.

For instance, it was identified in [55] that current reference saturation methods achieve fast and effective current limitation during the fault duration, whereas the VI method offers larger transient stability margins. To leverage the advantages of both methods, a hybrid method is proposed, which combines the priority-based limiter with a VI. To prevent simultaneous operation of both methods, the maximum allowed current value for the priority-based limiter is selected slightly higher than the one of the VI. This way, at the beginning stage of the fault, the priority-based limiter dominates the dynamic behavior, to avoid the temporary overcurrent, which would happen if the VI was solely used. After the initial transient of the fault, the VI takes over and the priority-based limiter is deactivated. Therefore, this method preserves the superior transient stability margins of the VI method, while avoiding the temporary overcurrent that is typically observed when the VI is used as a stand-alone current limiter.

Reference [59] proposed another hybrid current limiter combining a VI with a direct current limiter. This method uses a virtual impedance in the anti-windup path of the current reference saturation limiter. In this way, the use of the VI enables shaping of the output impedance angle, and at the same time, the GFMI overcurrent capability is fully used, which is not possible with the VI method.

Additionally, power limiters can be used to meet the steady-state fault current injection required by grid codes, but they exhibit poor current limiting performance during the initial stage of the fault [51]. Therefore hybrid methods combining power limiters with the magnitude limiter have been proposed to achieve the fault current injection requirements, while avoiding the temporary overcurrent caused by the power limiters [62].

## 2.3 Implementation of grid-forming and current-limiting control methods

### 2.3.1 Description of the studied system

The system used to simulate the implemented GFM and current-limiting control methods is shown in Fig. 2.25. It consists of a two-level GFMI connected to the grid through an RL filter and a transmission line. The grid is modeled as an ideal three-phase voltage source. In Fig. 2.25, $V_{ref,\alpha}$ and $V_{ref,\beta}$ correspond to the components of the voltage reference of the GFMI in the αβ frame, i.e the output of the inverter control system. Moreover, $V_{grid}$ and $I_{grid}$ are the voltage and current of the grid, $V_{inv}$ and $I_{inv}$ are the GFMI's voltage and current and $V_{pcc}$ is the voltage at the PCC, all in the abc-frame. Also, "GFMIen" is a digital value used to control the state of the three phase breaker, which connects the GFMI to the grid. In the following, the different components of the studied system are presented in more detail.

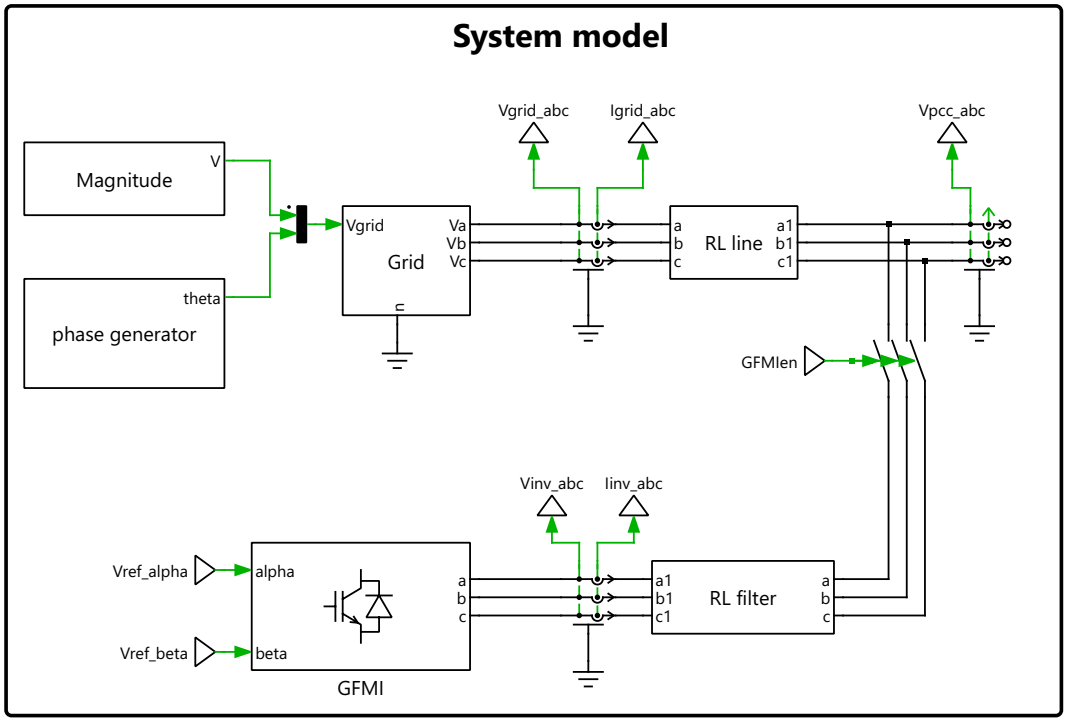



Figure 2.25: Simulation model of the studied system

***Grid-forming inverter***

Fig. 2.26a shows the general control system of the GFMI. The inputs of the system are the reference values for active and reactive power, the angular frequency and voltage magnitude. Additional inputs are the measurements of the three-phase PCC voltage and the output current of the inverter. Also, the control input "GFM_ctrl" is used to determine the control loop structure of the GFMI. More specifically, when GFM_ctrl $= 0$, the open loop control is used, whereas when GFM_ctrl $= 1$, the inner control loops are activated. The outputs of the control system are the αβ components of the voltage reference of the inverter.

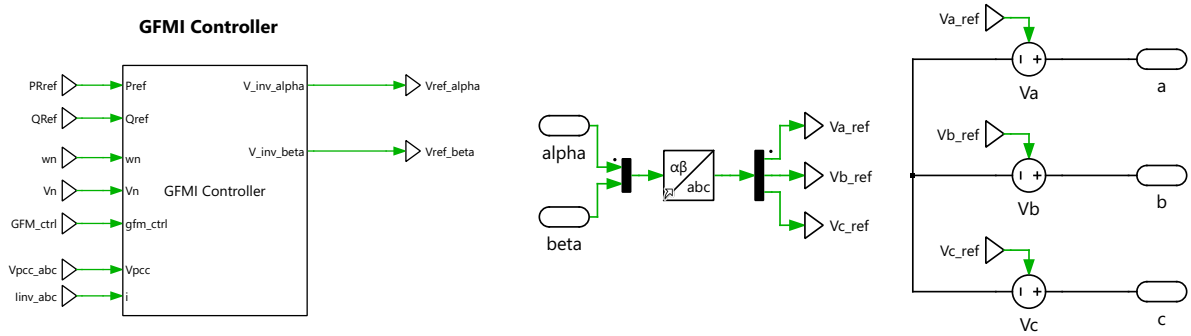
Generally, the inverter voltage reference should be appropriately scaled and fed to the modulation scheme. Thereafter, the modulation determines the switching instants of the semiconductor switches, in order to ensure that the average value of the phase voltages during the transistor switching period is equal to the associated reference, i.e., $\langle V_{inv,abc} \rangle_{T_s} = V^*_{inv,abc}$ [14]. Therefore, the VSC can be approximated by an ideal three phase voltage source, where each phase voltage is equal to the corresponding voltage reference, as illustrated in Fig. 2.26b [14]. This inverter representation is referred to as the "Average Value Modeling" (AVM) and it decreases the simulation time compared to full switching models, while still accurately capturing the inverter control dynamics [5], [63]. In the remainder of this thesis the GFMI will be modeled using the AVM approach unless mentioned otherwise.

***Inverter output filter and transmission line***

The output filter of the inverter as well as the transmission line are represented by a three phase series RL impedance, as shown in Fig. 2.27. It is worth noting that by tuning the parameters of the transmission line, the behavior of the GFMI under various SCR scenarios can be simulated.

***AC grid***

The AC grid to which the GFMI is connected, is represented by an ideal three phase voltage




(a) (b)

Figure 2.26: Grid forming inverter simulation models (a) General control structure; (b) Average model of the inverter

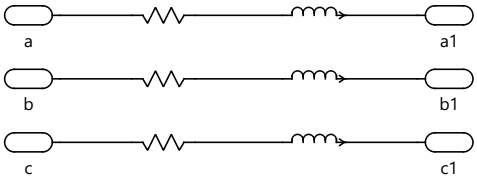



Figure 2.27: RL series impedance

source. The magnitude and angle of the voltage source can be controlled, in order to simulate various disturbances such as voltage sags and phase jumps. Once the magnitude and angle of the grid voltage are calculated, the grid phase voltages are obtained by

$$
\begin{aligned}
u_{g,a} &= V cos(\theta), \\
u_{g,b} &= V cos(\theta - 2\pi/3), \\
u_{g,c} &= V cos(\theta + 2\pi/3),
\end{aligned}
$$

where $V$ is the voltage magnitude and $\theta$ is the angle of the voltage of phase a. The implementation of the AC grid voltage is illustrated in Fig. 2.28.

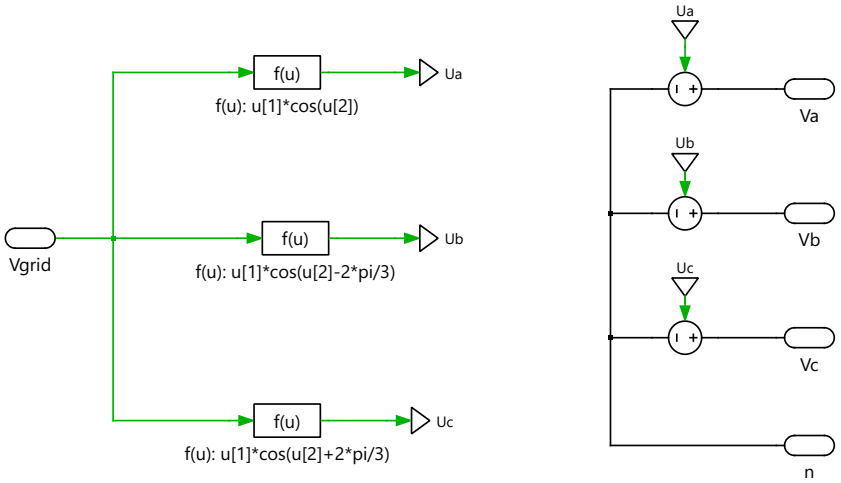



Figure 2.28: Implementation of the AC grid voltage

### 2.3.2 Implementation of outer loops

Regarding the outer loops of the GFMI, it was mentioned above that the PSC is equivalent to the droop controller and the VSG can be equivalent to the droop control with a low-pass filter. Therefore, in order to represent both the non-inertial and inertial controls in the active power control loop, the droop control with and without LPF were implemented. More complicated controllers, such as the ViSynC or the Virtual Oscillator Control were not implemented, because the main focus of this thesis is on current limitation control methods. For the same reason, only the droop controller was employed for the reactive power control loop, due to its simplicity.

Fig. 2.29 shows the implementation of the active-power droop controller with and without low-pass filter, as well as the reactive-power droop controller, which align with (2.3), (2.4) and (2.8), respectively. The control method used in the Active Power Controller can be selected by manually changing the state of the "APC switch". Additionally, $\theta = \text{mod}(\theta', 2\pi)$ is used, to maintain the value of $\theta$ in the range of $[0, 2\pi]$. It is worth noting that the pre-synchronization control system is only used before the connection of the GFMI, in order to synchronize with the grid voltage and achieve a smoother transient behavior during the connection. The outputs of the outer loops are the angle ($\theta_{APC}$) and the voltage magnitude ($E_{d,ref}$), which are provided either to the output of the control system (i.e., open loop control) or to the inner loops.

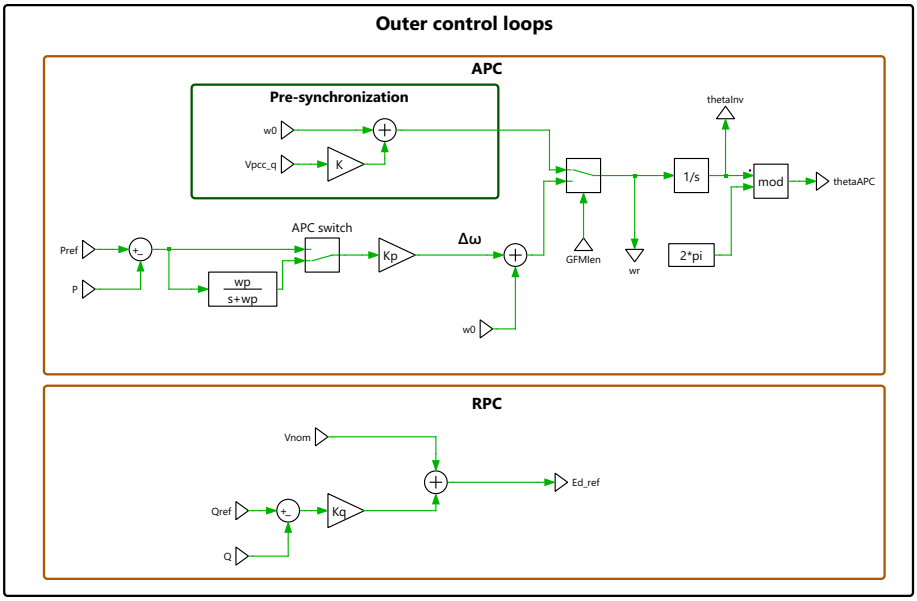


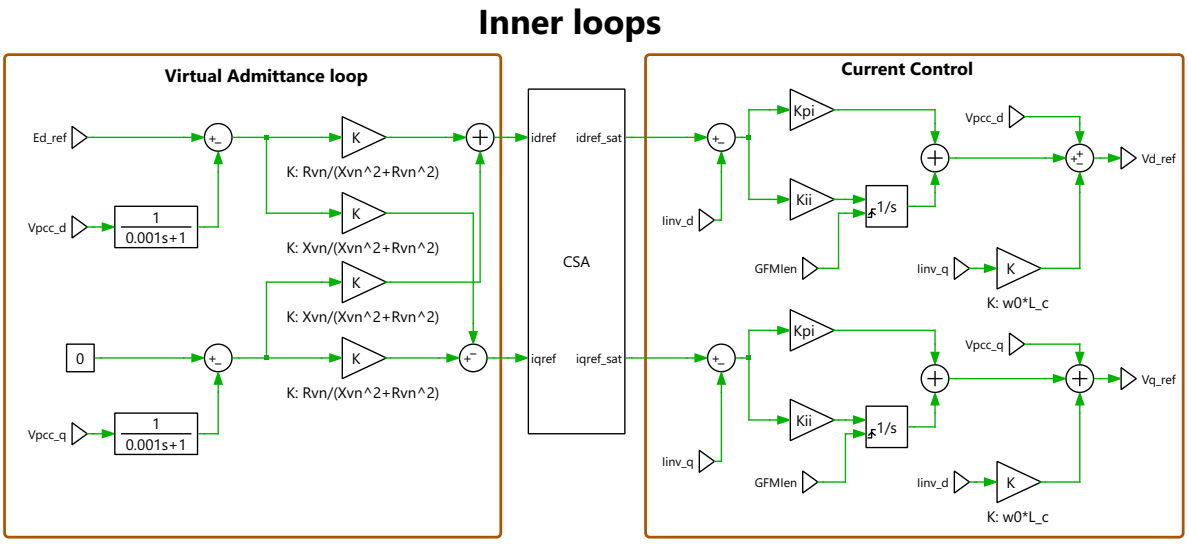

Figure 2.29: Implementation of the outer loops of the GFMI

### 2.3.3 Implementation of inner loops

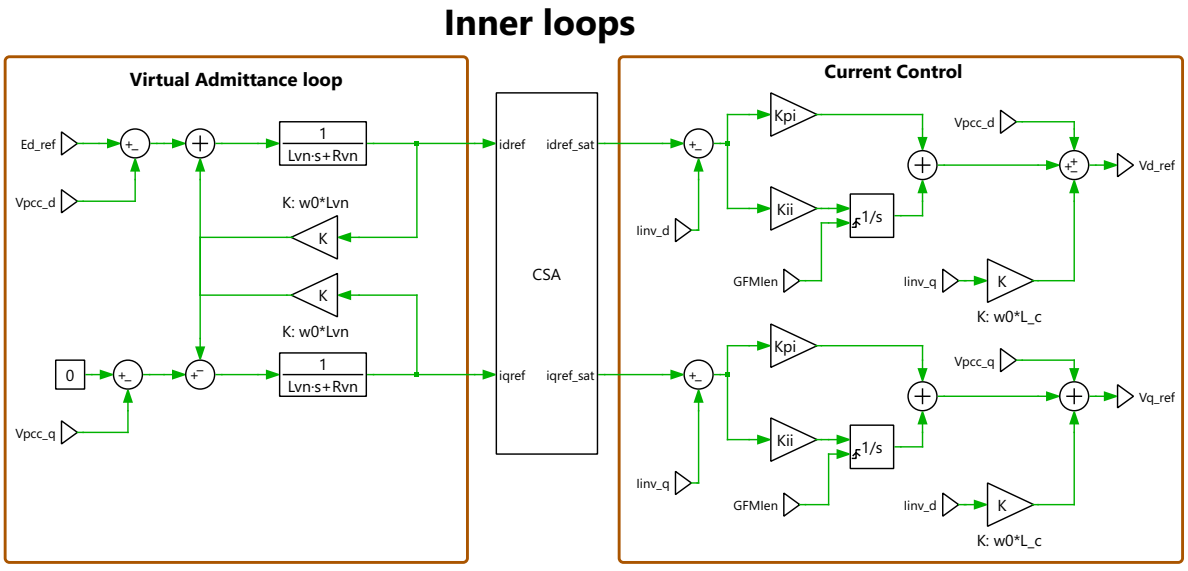
Due to the simplicity of the implementation and the fact that only symmetrical conditions have been considered, all the controllers are implemented in the dq frame.The open loop control consists of passing the references provided from the outer loops to the output of the system. As explained before, the d-axis component of the reference voltage is equal to the voltage magnitude provided by the reactive power controller and the q-axis component is zero, because the dq-frame is aligned with the internal voltage source. In the other control structure, the outputs of the outer loops are fed to the inner loops, which in turn generate the references $V_{d,ref}$ and $V_{q,ref}$.

To implement current saturation algorithms, the inner loops require a multi-loop

configuration to generate current references. To that end, the virtual admittance control architecture was implemented. Fig. 2.30 illustrates the implementation of the current controller and both the dynamic and quasi-stationary model of the virtual admittance loop. The current controller includes feed-forward and decoupling terms, as well as an external reset for the integrator to clear the error that is accumulated when the inverter is not connected.




(a)




(b)

Figure 2.30: Implementation of the virtual admittance control using a (a) quasi-stationary model; (b) dynamic model

### 2.3.4 Implementation of current-limiting control methods

The most frequently used current-limiting control methods in the literature are virtual impedance methods and current saturation algorithms [55], [64]. Therefore, from the indirect current limiters only the VI method was implemented and for the direct current limiters, the magnitude, fixed angle, d-axis and q-axis priority based limiters were implemented. Due to

the lack of current controllability of the open-loop control, current saturation algorithms cannot be implemented. Therefore the VI current-limiting method was employed in combination with the open-loop control. In contrast, the current-saturation algorithms were used in conjunction with the inner loops control structure.

***Virtual impedance method***

Based on (2.27), the implementation of the VI current limiting method is illustrated in Fig. 2.31. It consists of calculating the current magnitude, the VI parameter values and the fictitious voltage drop on the VI. The dq components of the voltage drop are calculated as follows:

$$\begin{aligned} &\Delta \mathrm{V}_{dq} = i_{dq} Z_{vi} = (i_d + j i_q) \cdot (R_{vi} + j X_{vi}) \\ \Longrightarrow\ &\Delta \mathrm{V}_{dq} = i_d R_{vi} + j i_d X_{vi} + j i_q R_{vi} - i_q X_{vi} \\ \Longrightarrow\ &\Delta \mathrm{V}_d = i_d R_{vi} - i_q X_{vi}, \quad \Delta \mathrm{V}_q = i_d X_{vi} + i_q R_{vi}. \end{aligned} \tag{2.33}$$

Once the voltage drop is obtained, the new voltage references are given by

$$\begin{aligned} E'_d &= E - \Delta \mathrm{V}_d, \\ E'_q &= -\Delta \mathrm{V}_q \end{aligned} \tag{2.34}$$

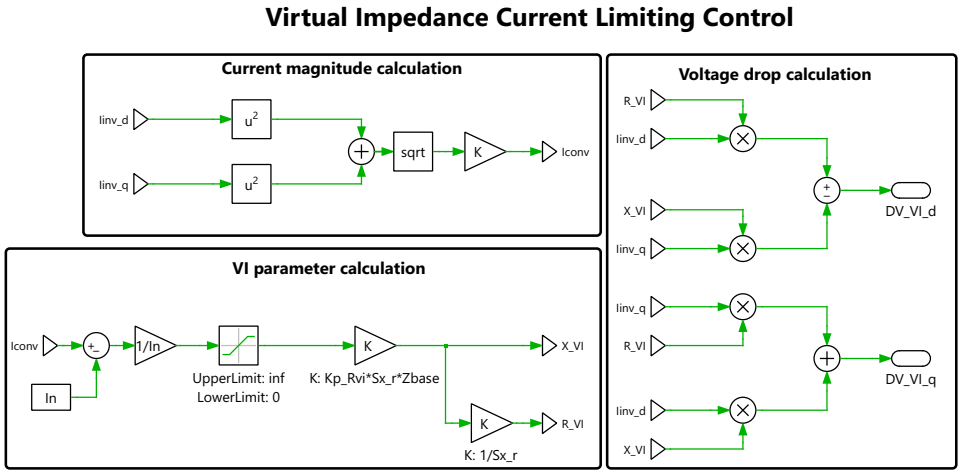



Figure 2.31: Implementation of the virtual impedance current limiter

***Magnitude limiter***

An alternative expression of (2.20), which describes the magnitude limiter is the following

$$\bar{i}_{ref,dq} = \frac{I_{max}}{\max\left(I_{max}, ||i_{ref,dq}||\right)} i_{ref,dq}, \tag{2.35}$$

where $||i_{ref,dq}|| = \sqrt{i^2_{ref,d} + i^2_{ref,q}}$, is the modulus of the unsaturated current reference. The implementation of (2.35) is depicted in Fig. 2.32.

***Fixed angle limiter***

The fixed angle limiter is described by (2.22), which can be easily implemented using a C-Script block, as illustrated in Fig. 2.33. The input signals of this block are the maximum

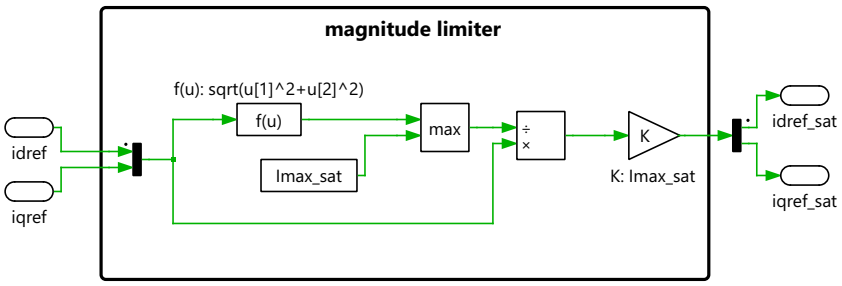



Figure 2.32: Implementation of the magnitude limiter

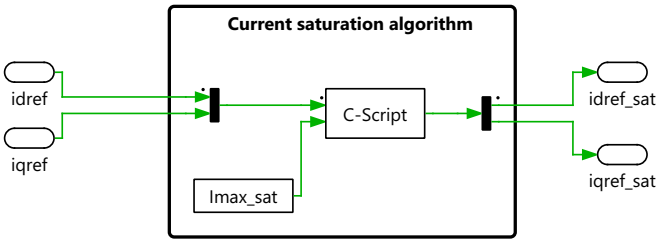



Figure 2.33: Implementation of a current saturation algorithm using a C-Script block

allowed current magnitude value and the unsaturated current reference in the synchronous reference frame. The angle $\phi_I$ is introduced as an additional parameter. The output signal is the dq components of the saturated current reference. The pseudo-code that represents the implementation of the fixed angle limiter is given in Fig. 2.34.

**Fixed angle limiter**

$i_{ref,d} = \text{InputSignal}(0,0)$
$i_{ref,q} = \text{InputSignal}(0,1)$
$I_{max} = \text{InputSignal}(1,0)$
$I = \sqrt{i_{ref,d}^2 + i_{ref,q}^2}$

**if** $I > I_{max}$ **then**
  $\bar{i}_{dref} = I_{max} \cdot \cos(\phi_I)$
  $\bar{i}_{qref} = I_{max} \cdot \sin(\phi_I)$
**else**
  $\bar{i}_{dref} = i_{ref,d}$
  $\bar{i}_{qref} = i_{ref,q}$
**end if**

$\text{OutputSignal}(0,0) = \bar{i}_{dref}$
$\text{OutputSignal}(0,1) = \bar{i}_{qref}$

Figure 2.34: Illustrative pseudo-code for the implementation of the fixed angle limiter

***Priority-based limiter***

The d-axis and q-axis priority-based limiter can be implemented using a C-Script block with the same configuration as Fig. 2.33. The pseudo-code that corresponds to (2.23) and (2.24), which describe the d- and q-axis priority-based limiter respectively, is shown in Fig. 2.35.

The new voltage references after the implementation of current-limiting methods are shown

**d-axis priority limiter**

$i_{ref,d} = \text{InputSignal}(0,0)$
$i_{ref,q} = \text{InputSignal}(0,1)$
$I_{max} = \text{InputSignal}(1,0)$

**if** $i_{ref,d} \geq 0$ **then**
  $sign\_id = 1$
**else**
  $sign\_id = -1$
**end if**

**if** $i_{ref,q} \geq 0$ **then**
  $sign\_iq = 1$
**else**
  $sign\_iq = -1$
**end if**

**if** $|i_{ref,d}| \geq I_{max}$ **then**
  $\bar{i}_{ref,d} = sign\_id \cdot I_{max}$
**else**
  $\bar{i}_{ref,d} = i_{ref,d}$
**end if**

**if** $|i_{ref,q}| < \sqrt{I_{max}^2 - \bar{i}_{ref,d}^2}$ **then**
  $\bar{i}_{ref,q} = i_{ref,q}$
**else**
  $\bar{i}_{ref,q} = sign\_iq \cdot \sqrt{I_{max}^2 - \bar{i}_{ref,d}^2}$
**end if**

$\text{OutputSignal}(0,0) = \bar{i}_{ref,d}$
$\text{OutputSignal}(0,1) = \bar{i}_{ref,q}$

**q-axis priority limiter**

$i_{ref,d} = \text{InputSignal}(0,0)$
$i_{ref,q} = \text{InputSignal}(0,1)$
$I_{max} = \text{InputSignal}(1,0)$

**if** $i_{ref,d} \geq 0$ **then**
  $sign\_id = 1$
**else**
  $sign\_id = -1$
**end if**

**if** $i_{ref,q} \geq 0$ **then**
  $sign\_iq = 1$
**else**
  $sign\_iq = -1$
**end if**

**if** $|i_{ref,q}| \geq I_{max}$ **then**
  $\bar{i}_{ref,q} = sign\_iq \cdot I_{max}$
**else**
  $\bar{i}_{ref,q} = i_{ref,q}$
**end if**

**if** $|i_{ref,d}| < \sqrt{I_{max}^2 - \bar{i}_{ref,q}^2}$ **then**
  $\bar{i}_{ref,d} = i_{ref,d}$
**else**
  $\bar{i}_{ref,d} = sign\_id \cdot \sqrt{I_{max}^2 - \bar{i}_{ref,q}^2}$
**end if**

$\text{OutputSignal}(0,0) = \bar{i}_{ref,d}$
$\text{OutputSignal}(0,1) = \bar{i}_{ref,q}$

Figure 2.35: Illustrative pseudo-code for the implementation of the d-axis and q-axis priority based limiter

in Fig. 2.36. The VI method is applied for the open-loop control by subtracting the voltage drop terms from the initial references, as described by (2.34). In the case of the multi-loop control structure, the voltage references are still provided by the current controller, since the CSAs act solely on the current reference.

## 2.4 Simulation results

To validate the implemented GFM control methods and the current-limitation techniques, time-domain simulations have been performed using the system shown in Fig. 2.25. The system and control parameters are given in Table 2.1, where $R_f$, $X_f$ are the resistance and reactance of the filter, $R_L$, $X_L$ are the resistance and reactance of the line, and $T_f$ is the time constant of the LPF used in the quasi-stationary implementation of the VA loop. The nominal power of the inverter is selected as the base power value.

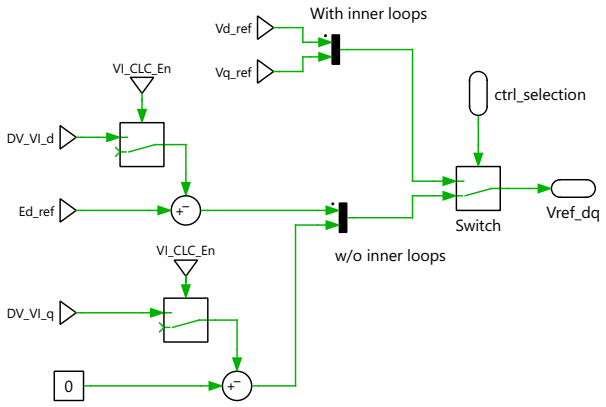



Figure 2.36: Illustration of inner loop selection including current-limiting methods

Table 2.1: System and control parameters

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $V_n$ | 130 kV | $k_q$ | $0.05\hat{V}_n/Q_{max}$ |
| $\omega_0$ | $100\pi$ rad/sec | $\omega_p$ | $2\pi \cdot 0.8$ rad/sec |
| $S_N$ | 60 MVA | $k_{pi}$ | 325.6 Ω |
| $R_L$ | 4.2 Ω (0.015 pu) | $k_{ii}$ | 10229 Ω/s |
| $X_L$ | 21.44 Ω (0.076 pu) | $X_v$ | 0.3 pu |
| $R_f$ | 4.65 Ω (0.0165 pu) | $R_v$ | 0.1 pu |
| $X_f$ | 46.5 Ω (0.165 pu) | $T_f$ | 1 msec |
| $k_p$ | $0.02\omega_0/P_{max}$ | $I_{max}$ | 1.2 pu |

### 2.4.1 Grid-forming control methods

In the following, the different outer and inner loop configurations are simulated under two different scenarios, namely step changes of the active-power reference and minor grid-voltage disturbances. More specifically, the performance of the active-power droop controller, with and without low-pass filter, is assessed for both the open-loop and virtual admittance control cases. In all simulations, the droop controller is used for the voltage profile management loop.

***Step changes in active-power reference***

Figures 2.37a and 2.37b show the simulation results for step changes of the active power setpoint, for the open-loop and virtual admittance control respectively. It is observed that, the active power follows its reference in the steady state for all combinations of the outer- and inner-loop control system. The main difference in the presented results is that, due to its first-order nature, the droop controller exhibits an overdamped response, whereas the addition of the LPF increases the order of the system to two, leading to overshoot and oscillations [37].

Another major difference between the droop controller with and without the LPF, is their inertia provision capability. Particularly, Figures 2.37a and 2.37b illustrate that in the case of the droop controller, a step change in $P_{ref}$ causes a corresponding step change of the GFMI's internal frequency, in accordance with (2.3). Consequently, the droop controller lacks virtual inertia and therefore belongs in the category of *non-inertial grid-forming controls* [37]. On the other hand, the addition of the LPF introduces a virtual inertia term, which makes the active power controller equivalent to the VSG. This term prevents the internal frequency from changing in a stepwise manner, thereby providing virtual inertia. For this reason, the droop control with low-pass filter is included in the category of *inertial grid-forming controls* [37].

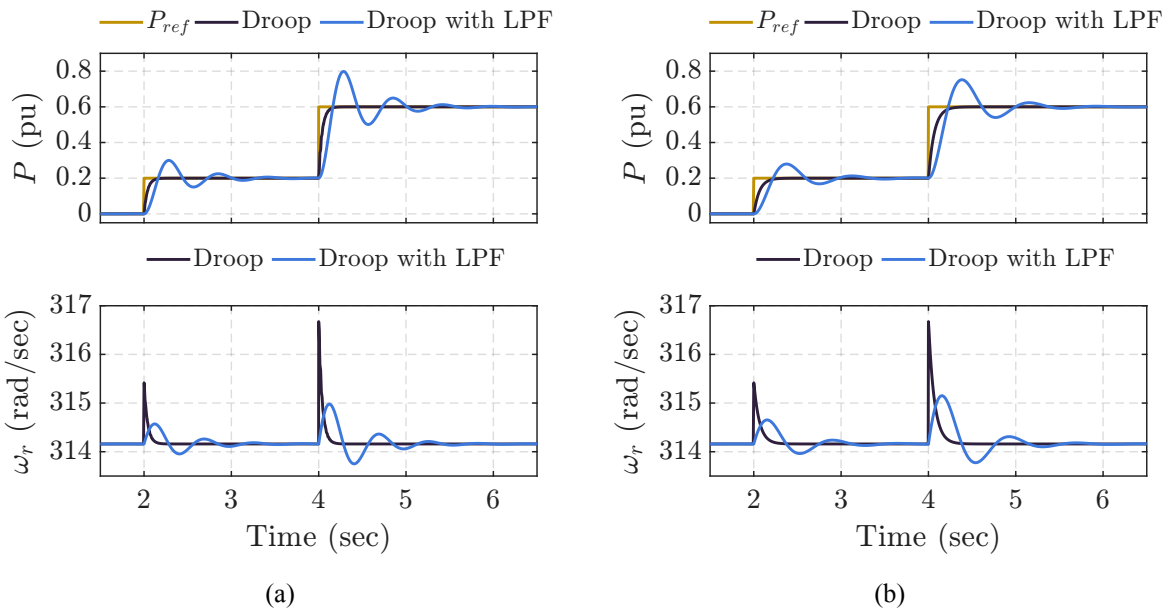



Figure 2.37: Simulation results for step changes in $P_{ref}$ (a) Open loop control; (b) VA control

***Grid voltage drop to 0.85 pu***

Figures 2.38 and 2.39 show the results for a minor disturbance of a 15% dip at the grid voltage, with $P_{ref} = 0.2$ pu and $Q_{ref} = 0$. It is observed that due to the voltage source behavior of the GFMI, its output current increases immediately after the disturbance and reactive power is injected during the voltage dip to support the grid. Although the current does not exceed the maximum allowed value, its sensitivity to grid conditions becomes evident. Thus, for more severe disturbances, this behavior will trigger the current limiters, to prevent overcurrent.

Also, during the fault, the voltage magnitude reference provided by the reactive droop controller decreases, in accordance with (2.8) (since $Q_{ref} - Q < 0$). In the case of the VA control, the large virtual impedance used ($X_v = 0.3$ pu, $R_v = 0.1$ pu) leads to degraded voltage control. For these reasons, the inverter voltage slightly changes during the fault.

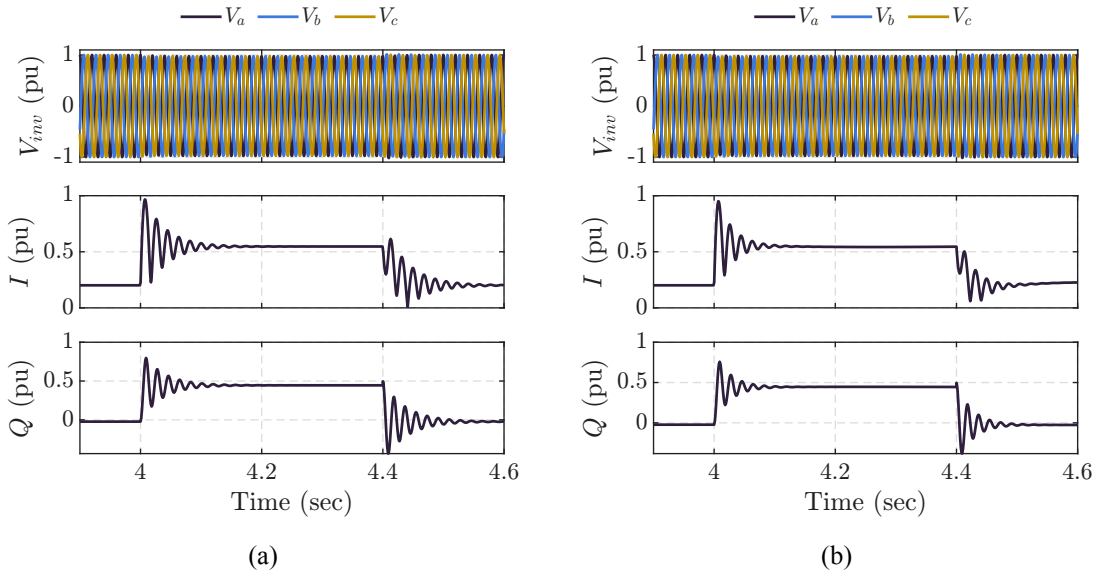



Figure 2.38: Simulation results for a grid voltage dip to 0.85 pu (a) Droop and open loop control; (b) Droop with LPF and open loop control

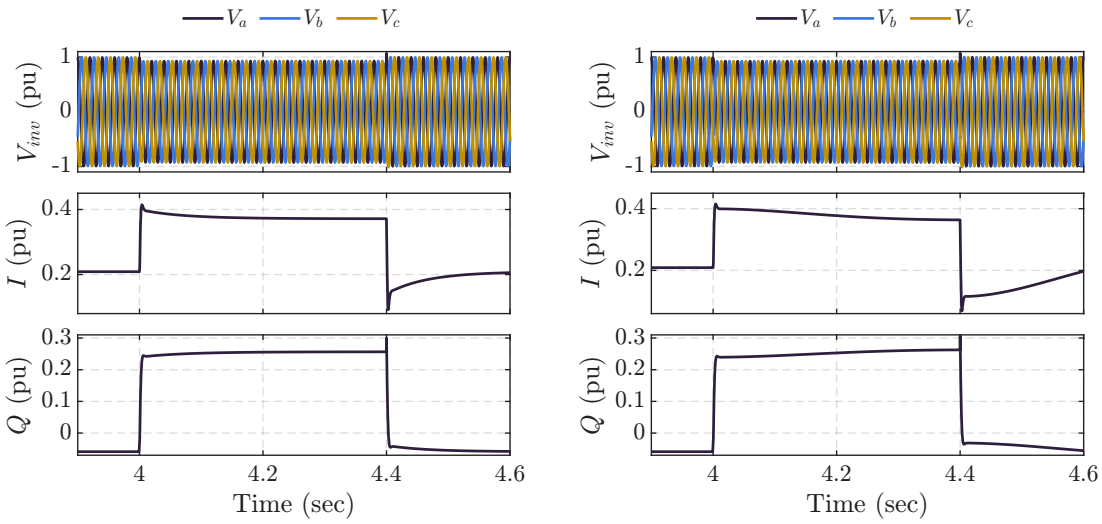



Figure 2.39: Simulation results for a grid voltage dip to 0.85 pu (a) Droop and VA control; (b) Droop with LPF and VA control

### 2.4.2 Current-limiting control methods

Since the sensitivity of the inverter current to grid conditions has been confirmed, more severe disturbances are simulated, in order to activate the implemented current-limitation methods and assess their effectiveness. To simplify the illustration of the results, only the droop controller was used for the active power controller. In what follows, the implemented current-limitation techniques are validated under two different fault scenarios, namely a grid voltage dip to 0.3 pu for 100 msec and a -45° phase jump of the grid voltage, which are illustrated in Fig. 2.40. The active and reactive power set-points are set to $P_{ref} = 0.2$ pu and $Q_{ref} = 0$ for all simulations.

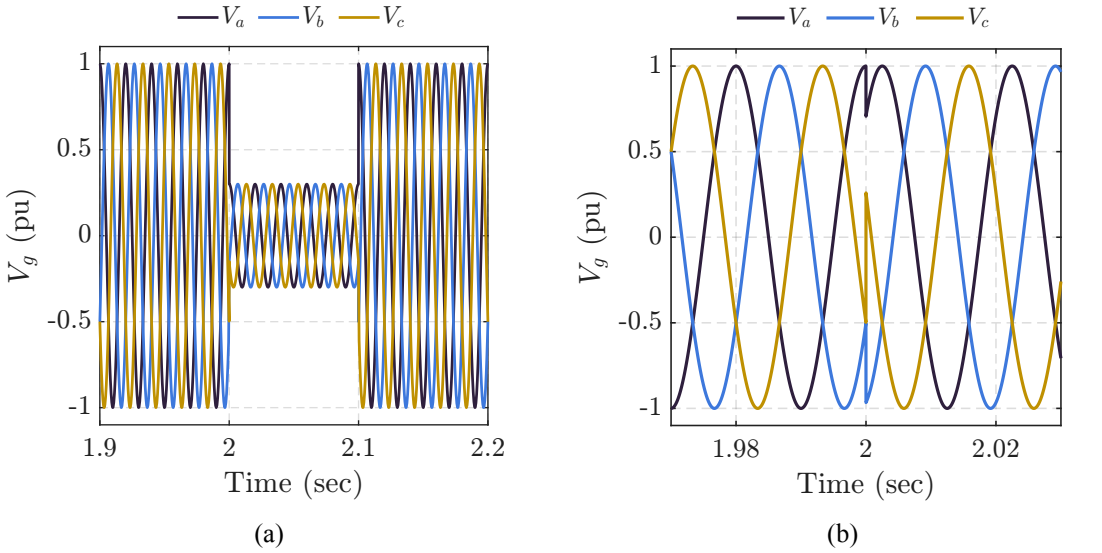



Figure 2.40: Grid voltage during fault scenarios (a) Voltage dip; (b) Phase jump

***Without current-limiting methods***

Fig. 2.41 shows the inverter output-current magnitude for both disturbances, when no current-limitation technique is employed. It is observed that, in every case, the current exceeds the maximum permissible value, for both the open loop and the VA control. Because the selected VA parameters are relatively large compared with the filter of the inverter, the impedance between the grid voltage and the IVS is higher in the case of the VA control compared with the open-loop control. Consequently, the resulting current for the open loop control is larger than that of VA control.

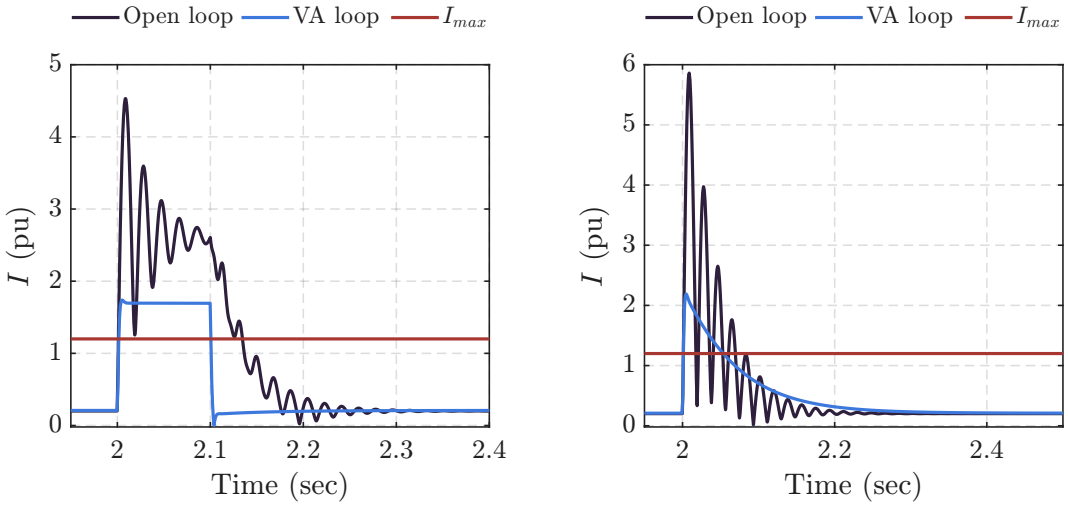



Figure 2.41: Output current magnitude without current-limiting methods (a) Voltage dip; (b) Phase jump

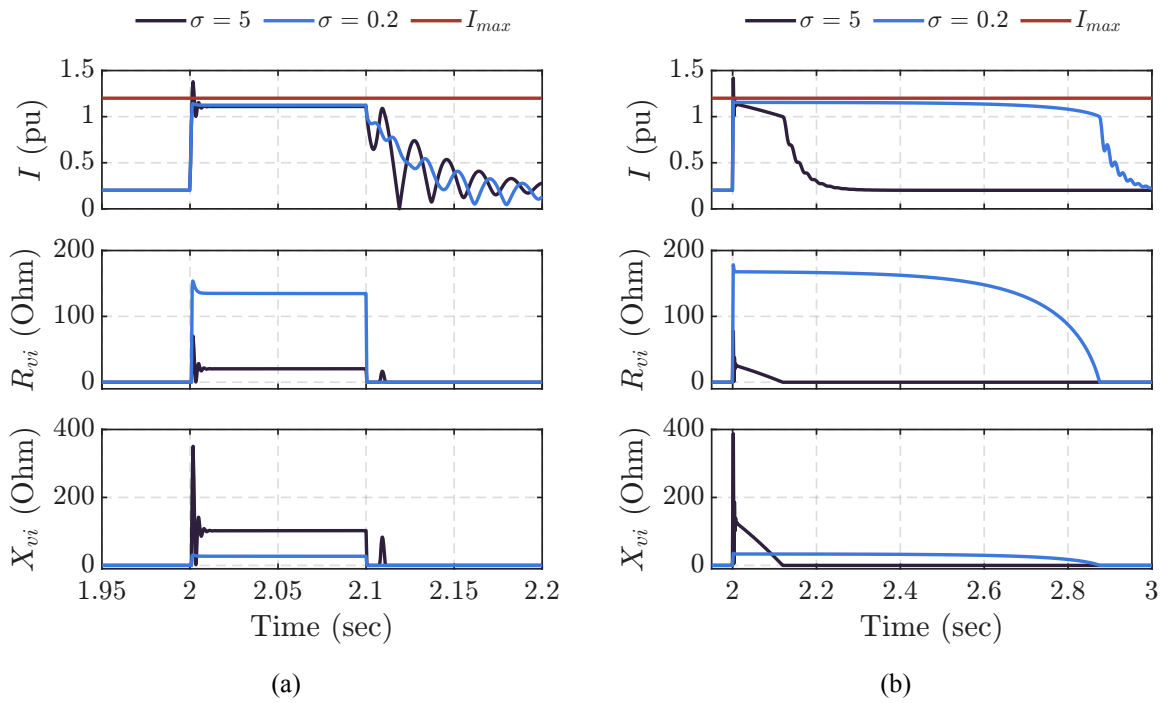
***Virtual impedance limiter***

Fig. 2.42 illustrates the performance of the VI limiter under the two fault scenarios, considering both the inductive ($\sigma = 5$) and the resistive ($\sigma = 0.2$) VI. According to (2.29), $K_{VI}$ is calculated equal to 0.658 and 3.85 respectively. During the disturbances, the VI parameters increase in order to limit the current, whereas in normal operation they remain equal to zero.

In the case of the inductive VI, a temporary overcurrent is observed, which is mainly caused by the transient DC component in the phase currents [65]. This overcurrent is decreased when the resistive VI is used, due to the increased virtual-resistance parameter ($R_{vi}$), which damps the DC component in the phase currents [27]. Lastly, since the simulated disturbances are less severe than the worst-case scenario (i.e., the three-phase bolted fault), the overcurrent capacity of the GFMI is not fully utilized.

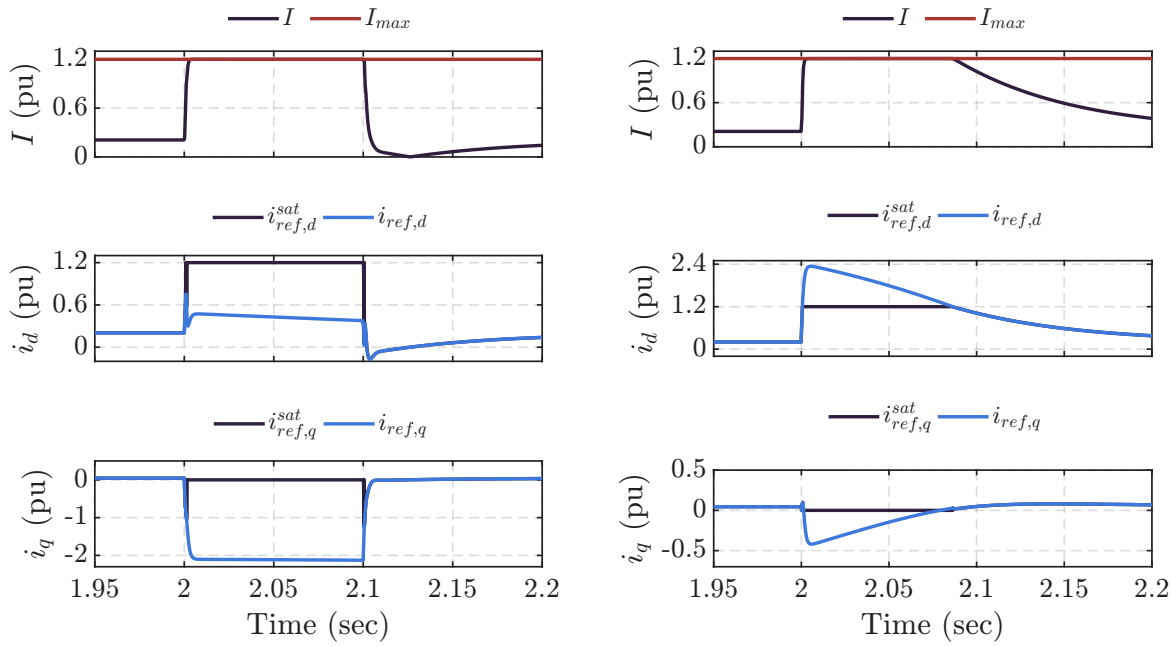
***Fixed angle limiter***

Fig. 2.43 shows the simulation results for the fixed angle limiter with $\phi_I = 0$. It is seen that during the fault (where $||i_{ref}|| > I_{max}$), the magnitude of the current reference is saturated to $I_{max}$, and it also becomes aligned with the d-axis (i.e., $\bar{i}_{ref} = I_{max} + j0$), due to the selection of $\phi_I = 0$. Similarly, $\phi_I$ can be selected to achieve different angles relative the d-axis during fault conditions. Then, due to the high bandwidth of the current controller, the current tracks its saturated reference and is therefore effectively limited.




(a) (b)

Figure 2.42: Output current magnitude and VI parameters with the VI limiter (a) Voltage dip; (b) Phase jump

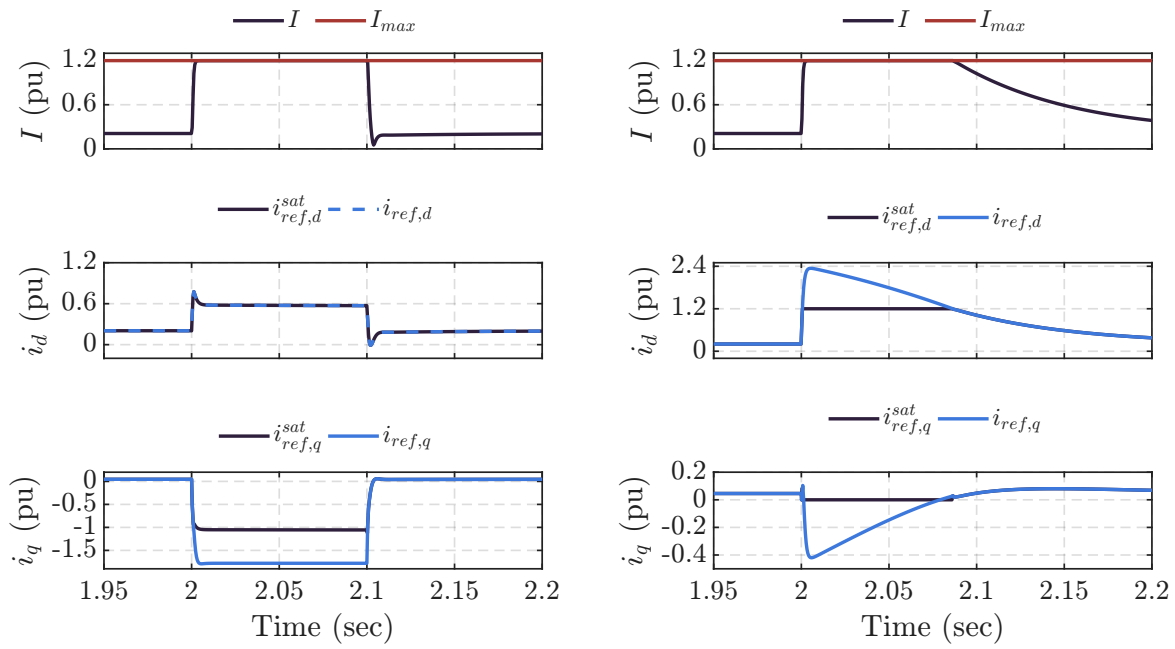



(a) (b)

Figure 2.43: Output current magnitude and current references with the Fixed angle limiter (a) Voltage dip; (b) Phase jump

***d-axis priority limiter***

Fig. 2.44 shows that the d-axis priority limiter can effectively limit the current for both voltage dips and phase jumps, while prioritizing the d-axis component of the current, in




(a) (b)

Figure 2.44: Output current magnitude and current references with the d-axis priority limiter (a) Voltage dip; (b) Phase jump

accordance with (2.23). Particularly, Fig. 2.44a shows that during the voltage dip, the d-axis component of the current reference remains unchanged, since it does not exceed $I_{max}$. In contrast, the q-axis component of the current reference is restricted, in order to ensure that $\sqrt{i_d^2 + i_q^2} \leq I_{max}$ holds.

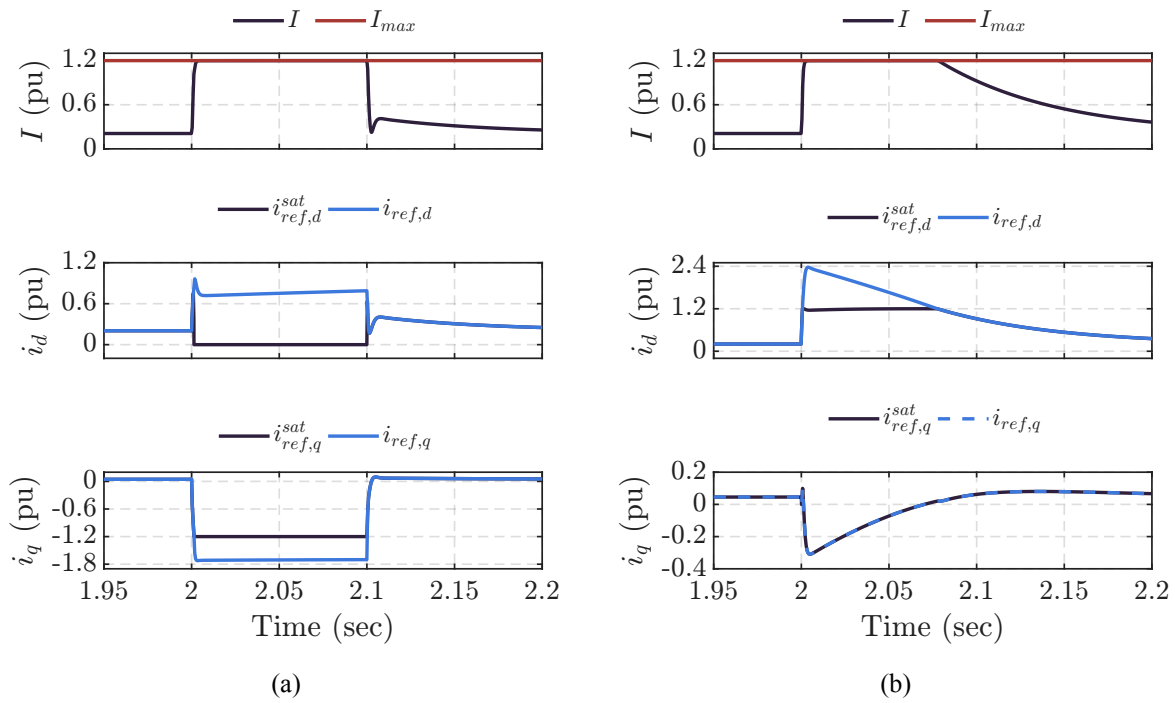
On the other hand, during the phase jump, the d-axis component of the original current reference surpasses $I_{max}$. Thus, according to (2.23), the d-axis component of the saturated current reference is equal to $I_{max}$, leaving no margin for the q-axis component, which is necessarily equal to zero, as shown in Fig. 2.44b. Therefore, in this case, the behavior of the d-axis priority limiter is equivalent with the fixed angle limiter with $\phi_I = 0$, since the saturated current is aligned with the d-axis.

### *q-axis priority limiter*

In analogy with the d-axis priority limiter, Fig. 2.45 illustrates that the q-axis priority limiter, restricts the magnitude of the current while prioritizing the q-axis component. More specifically, during the voltage drop, $|i_{ref,q}|$ is larger than $I_{max}$, which yields $\bar{i}_{ref,q} = -I_{max}$, because the original current reference is negative. Thus, there is no margin for the d-axis component, which is reduced to zero. On the other hand, in the case of the phase jump, the q-component of the current reference remains unchanged, since $|i_{ref,q}|$ does not exceed $I_{max}$, while the d-axis component of the current reference is restricted, in order to achieve $\sqrt{i_d^2 + i_q^2} \leq I_{max}$.

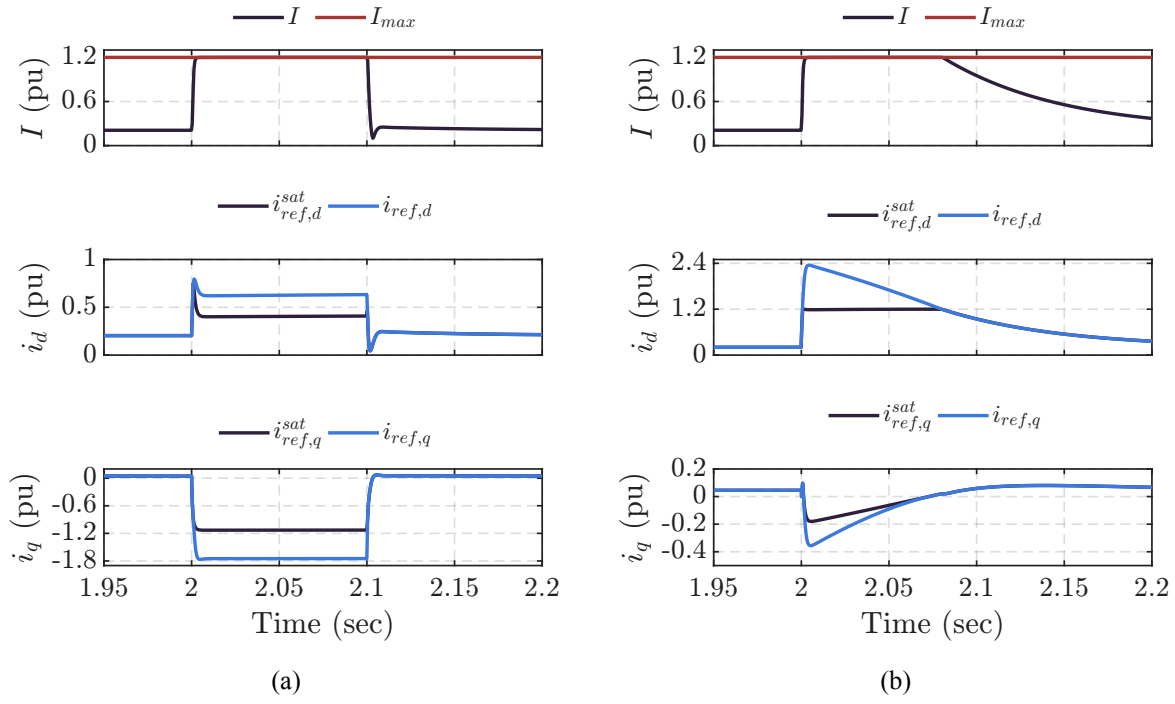
### *Magnitude limiter*

In contrast to the previous direct current limiters, Fig. 2.46 shows that the magnitude limiter effectively limits the current magnitude by scaling the original current reference components with the same coefficient ($I_{max}/||i_{ref}||$), as described by (2.35). This way, the magnitude of the current reference is limited, while its angle remains unchanged, which is illustrated in Fig. 2.47




(a) (b)

Figure 2.45: Output current magnitude and current references with the q-axis priority limiter (a) Voltage dip; (b) Phase jump




(a) (b)

Figure 2.46: Output current magnitude and current references with the magnitude limiter (a) Voltage dip; (b) Phase jump

for the phase-jump fault.

### *Comparison between different current limiters*

From the simulation results presented above, it is observed that all of the implemented

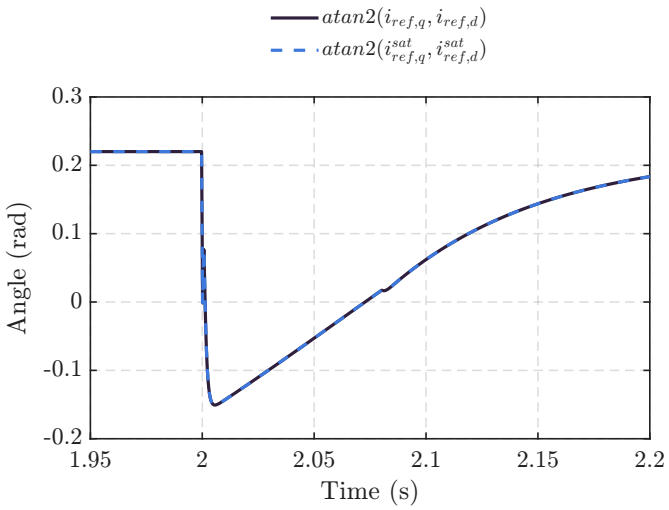



Figure 2.47: Angle of the saturated and unsaturated current reference relative with the d-axis for the phase jump disturbance

current-limitation methods are able to limit the current, during both voltage dips and phase jumps. The use of the VI limiter can introduce temporary overcurrent during the initial stage of the disturbance, whereas during the fault, the overcurrent capability of the GFMI cannot be fully utilized. Although the temporary overcurrent can be reduced with the use of a resistive VI, it can not be guaranteed that it will remain below $I_{max}$ for all disturbances. In contrast, direct current limiters can achieve fast and accurate current limiting, due to the saturation of the current reference, combined with fast reference tracking by the current controller. Thus, the direct limiters enable full use of the GFMI's overcurrent capability during disturbances.

Despite the fact that every direct current-limiting method restricts the current magnitude to $I_{max}$ during faults, their main difference lies in the resulting angle of the saturated current with respect to the d-axis, i.e., the d- and q-axis components of the current. Since the current magnitude is clamped to $I_{max}$, this angle dictates their performance regarding system wide aspects such as transient stability, voltage support etc.

# Chapter 3

# Effect of current-limiting methods on transient stability

The ability to remain synchronized with the grid during and after large disturbances is referred to as transient stability [32]. Traditionally, transient stability was linked to the rotor angle of synchronous generators. Despite the fact that grid-forming inverters do not have a physical rotor, they have an internal angle reference that is generated from the outer control loops, i.e., $\theta$ [28]. Thus, the angle difference between $\theta$ and the grid-voltage angle, which is defined as the *Virtual Power Angle* (VPA), is used for the transient stability analysis of GFMIs [54]. Based on its definition, the VPA is given by $\delta = \theta - \theta_g$ [54]. Therefore, by determining the power-angle characteristic of grid-forming inverters, i.e., the $P - \delta$ curve, the methods used for SGs in conventional power systems can be utilized for the transient stability assessment of GFMIs too [28]. During large disturbances the current limiters of the GFMI will likely be activated, and thus the employed current limitation method determines the power-angle characteristic of the inverter [21].

This Chapter presents the transient stability analysis of the GFMI through $P - \delta$ curves, with the focus mainly being on the operation under current limitation. To illustrate the synchronization process of the GFMI during and after faults, the specific case of a short circuit is used. Nevertheless, the transient stability of the GFMI under different types of disturbances, such as phase jumps or RoCoF (Rate of Change of Frequency) events, can be studied using the same $P - \delta$ curves [28]. First, the synchronization process of the GFMI without current limitation is presented, for both inertial and non-inertial control methods. Then, the effect of current-limiting methods on the transient stability of the GFMI is illustrated, using the fixed angle and the magnitude limiter as specific examples. To analyze the transient stability of the GFMI embedding these current-limiting methods, large signal models are presented, which are then validated through time-domain simulations, for various fault types.

## 3.1 Studied system and assumptions

Similarly to the traditional transient stability analysis for synchronous generators, the system consisting of a GFMI connected to an infinite bus is used, which is depicted in Fig. 2.25. To simplify the analysis in this Chapter, the transmission line is assumed to be purely inductive and the Q-V droop control is neglected, i.e., the magnitude of the internal voltage source $E$ is maintained at 1 pu. Additionally, in order to assess the transient stability of the GFMI, a quasi-steady state (QSS) model is utilized, where the electrical variables can be represented by their phasors [48]. To obtain this model, the inductor, VA-loop and current loop dynamics

Table 3.1: System and control parameters

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $V_n$ | 130 kV | $k_q$ | 0 |
| $\omega_0$ | $100\pi$ rad/sec | $\omega_p$ | $2\pi \cdot 0.4$ rad/sec |
| $S_N$ | 60 MVA | $k_{pi}$ | 325.6 Ω |
| $R_L$ | 0 | $k_{ii}$ | 10229 Ω/s |
| $X_L$ | 21.44 Ω (0.076 pu) | $X_v$ | 0.3 pu |
| $R_f$ | 4.65 Ω (0.0165 pu) | $R_v$ | 0.1 pu |
| $X_f$ | 46.5 Ω (0.165 pu) | $T_f$ | 1 msec |
| $k_p$ | $0.05\omega_0/P_{max}$ | $I_{max}$ | 1.2 pu |

are neglected [31]. Ignoring the current-controller dynamics means that the inverter current is assumed to be equal to its reference value. Based on the equivalent circuit of this phasor model, the power-angle characteristics of the GFMI can be determined, which are then used for the transient stability assessment. The system and control parameters used are given in Table 3.1.

## 3.2 Theoretical analysis

### 3.2.1 Non-inertial control

First, the synchronization process of the GFMI employing the active power droop controller with and without current limitation is illustrated, considering a short circuit on the grid side. In this case, the equivalent circuit consists of the IVS in series with the VA parameters ($R_v$ and $X_v$), the transmission line reactance and the infinite grid voltage. It is known from Chapter 2, that the angle of the IVS is equal to the reference provided from the outer loops, i.e., $\theta$. Therefore, based on the definition of the VPA, if the phase of the IVS phasor is selected as the phase reference (i.e., the phasor of the IVS has zero phase), then the phase of the grid voltage is equal to $-\delta$, where $\delta$ is the virtual power angle.

Based on the equivalent circuit of Fig. 3.1, the power-angle characteristic of the GFMI under normal operation in the per unit system, is the following

$$P = \frac{-V_g^2 R_v + R_v E V_g \cos\delta + X_{tot} E V_g \sin\delta}{R_v^2 + X_{tot}^2}, \tag{3.1}$$

where $P$ is the output active power at the PCC, and $X_{tot} = X_v + X_L$ is the total reactance between the IVS and infinite bus. It is important to note that the active power at the PCC is equal to the active power at the infinite bus, due to the assumption of a purely inductive line ($Z_L = jX_L$).

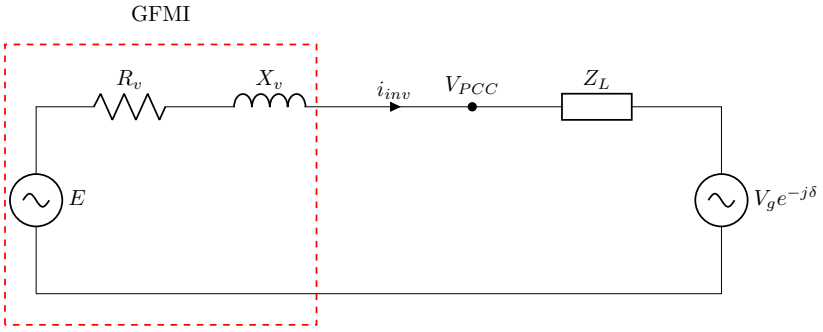



Figure 3.1: Equivalent circuit of the GFMI with the VA control when no current limiter is used

The active power droop controller dynamics are repeated here for convenience,

$$\theta = \int \left[k_p(P_{ref} - P) + \omega_0\right]. \tag{3.2}$$

Taking the derivative of both sides of the above equation gives [21]

$$\dot{\delta} = k_p(P_{ref} - P). \tag{3.3}$$

If the per unit values for $k_p$, $P_{ref}$ and $P$ are used, (3.3) becomes

$$\dot{\delta} = k_{p,pu}\frac{\omega_0}{P_{max}}(P_{ref} - P) \overset{P_{max}=P_N=S_N}{\Longrightarrow} \dot{\delta} = k_{p,pu}\omega_0(P_{ref,pu} - P_{pu}). \tag{3.4}$$

Hereafter, the subscript "pu" is omitted for convenience.

The synchronization process of the GFMI during and after a short circuit is explained through different phases, as illustrated in Fig. 3.2. The active power set-point $P_{ref}$ is assumed to be constant during and after the fault. Additionally, Fig. 3.2 shows that for a given $P_{ref}$, the equation $P(\delta) = P_{ref}$ has two solutions, one of which corresponds to the stable equilibrium point, whereas the other one corresponds to the unstable equilibrium point.

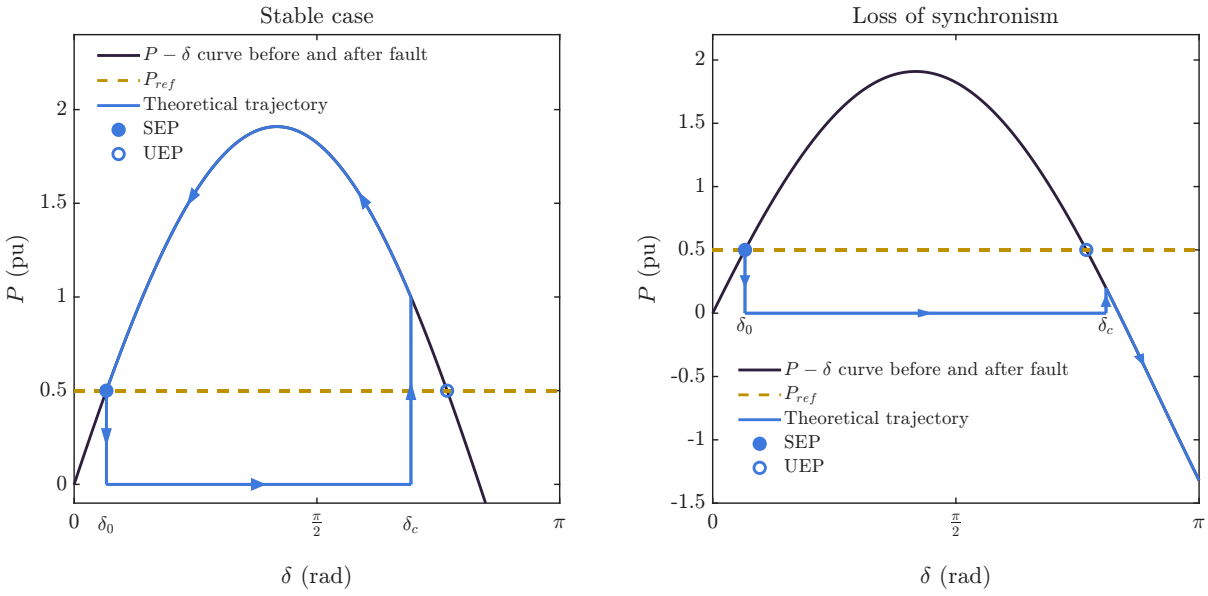



Figure 3.2: Illustration of the $P-\delta$ trajectory of a droop based GFMI without current limiting, for a short circuit

*Phase 1:* When a short circuit occurs, no active power can flow into the infinite bus, because $V_g = 0$. Thus, the VPA dynamics become

$$\dot{\delta} = k_p\omega_0 P_{ref}. \tag{3.5}$$

Because $P_{ref}$ is typically positive, the VPA increases due to its positive derivative. Generally, when $P_{ref}$ is larger than $P$, the VPA increases in accordance to (3.3).

*Phase 2:* When the short circuit is cleared, i.e., $V_g = 1$ pu[1], the result is a vertical line from zero power to the post-fault $P-\delta$ curve, with the VPA being equal to the clearing angle.

[1] After the fault, the grid voltage is assumed to instantaneously recover to 1 pu

*Phase 3:* This phase can be different, depending on the value of the clearing angle. More specifically, if the clearing angle $\delta_c$ is less than the angle corresponding to the unstable equilibrium point of the post-fault $P - \delta$ curve, then the active power output at the clearing angle, i.e., $P(\delta_c)$ is larger than the active power reference. According to (3.3), this results in a decrease of the VPA, due to the negative derivative. Then, the VPA continues to decrease until it reaches the stable equilibrium point, where $P = P_{ref}$ and $\dot{\delta} = 0$.

In contrast, if the clearing angle is larger than the one corresponding to the unstable equilibrium point, then $P_{ref}$ is larger than $P(\delta_c)$, resulting in further increase of the VPA. In this case, the VPA reaches the new stable equilibrium point after around one cycle of oscillation [66]. Therefore, the GFMI loses synchronism with the grid for one cycle. In general, due to the first-order nature of the droop controller, the GFMI can re-synchronize with the grid as long as a stable equilibrium point exists [66]. However, this large fluctuation of the power is not a desired behavior.

### 3.2.2 Inertial control

If the inertial control is used (e.g the droop controller with LPF), the large signal equivalent circuit and the power-angle characteristic remain unchanged. The only modification is the dynamics of the active power controller, which in the case of the droop with low-pass filter are expressed by

$$\Delta\omega = \frac{k_p\omega_p}{s+\omega_p}(P_{ref} - P). \tag{3.6}$$

Similar to the droop control, if the per-unit values for $k_p$, $P_{ref}$, and $P$ are used, the equation becomes

$$\Delta\omega = \frac{k_{p,pu}\omega_0}{P_{max}}\frac{\omega_p}{s+\omega_p}(P_{ref} - P) \implies \Delta\omega = \omega_0\frac{k_{p,pu}\omega_p}{s+\omega_p}(P_{ref,pu} - P_{pu}). \tag{3.7}$$

Again, the subscript "pu" will be omitted for convenience.

Since this implementation is equivalent to the VSG, this equation can be rewritten using the inertia constant H and the damping (droop) coefficient D, to align the transient stability analysis with that of a synchronous generator. The new equation is as follows

$$\Delta\omega = \omega_0\frac{1}{2Hs+D}(P_{ref} - P), \tag{3.8}$$

where $H = 1/(2k_p\omega_p)$ and $D = 1/k_p$. In this case, the dynamics of the VPA are governed by the following system of equations

$$\dot{\delta} = \Delta\omega, \tag{3.9}$$

$$\frac{2H}{\omega_0}\dot{\Delta\omega} = P_{ref} - P - \frac{D}{\omega_0}\Delta\omega. \tag{3.10}$$

For the same active power reference, the initial operating point is the same as the non-inertial system, i.e., $(\delta, \Delta\omega) = (\delta_0, 0)$. If the short circuit is considered again, the active-power trajectory during and after the fault is as follows:

*Phase 1:* During the short circuit the active power is zero. If the damping (droop) coefficient $D$ is ignored, which is a conservative assumption, (3.10) becomes

$$\frac{2H}{\omega_0}\dot{\Delta\omega} = P_{ref}, \tag{3.11}$$

resulting in the increase of $\Delta\omega$, since $P_{ref}$ is positive. Due to the fact that $\Delta\omega$ was equal to zero in normal operation, the increase makes it positive. This, in turn, results in the increase of $\delta$, since its derivative is positive, based on (3.9).

*Phase 2:* When the short circuit is cleared, i.e., $V_g = 1$ pu, the result is a vertical line from zero power to the post-fault $P - \delta$ curve, with the VPA being equal to the clearing angle.

*Phase 3:* Similar to the non-inertial case, if the clearing angle is larger than the one corresponding to the unstable equilibrium point, then $P_{ref}$ is larger than $P(\delta_c)$, resulting in further increase of $\Delta\omega$ and of the VPA. In this case the synchronization with the grid is lost.

On the other hand, if the clearing angle is less than the angle corresponding to the unstable equilibrium point of the post-fault $P - \delta$ curve, then the active power output at the clearing angle, i.e., $P(\delta_c)$, is larger than the active power reference. Thus, $\Delta\omega$ decreases due to

$$\frac{2H}{\omega_0}\dot{\Delta\omega} = (P_{ref} - P) < 0.$$

However, in contrast with the non-inertial case, the VPA does not decrease, because $\Delta\omega$ is still positive. Therefore, according to (3.9), the VPA continues to increase, but with a slower rate.

*Phase 4:* If $\Delta\omega$ becomes zero before the VPA reaches the unstable equilibrium point, it continues to decrease because $(P_{ref} - P) < 0$ still holds. Thus, $\Delta\omega$ becomes negative and the VPA starts to decrease, due to its negative derivative, and moves towards the stable equilibrium point. If the damping coefficient is not considered, the VPA will oscillate around the stable equilibrium point. However, because the damping coefficient is implemented in the active power controller, the VPA will eventually settle to the equilibrium. Therefore, in this case, the synchronization with the grid is restored.

On the other hand, if the VPA reaches the unstable equilibrium point before $\Delta\omega$ becomes zero, then $P_{ref}$ becomes larger than $P$, so $\Delta\omega$ starts to increase again and the synchronization with the grid is lost. The $P - \delta$ trajectory of the GFMI with inertial control is illustrated in Fig. 3.3.

### 3.2.3 Fixed angle limiter

When the fixed angle current limiter is triggered, the GFMI is operating as a constant current source, as described by

$$i_d = I_{max} cos\phi_I, \quad i_q = I_{max} sin\phi_I. \tag{3.12}$$

For the following analysis, the case of $\phi_I = 0$ is considered. Thus, the constrained current becomes, $i_{dq} = I_{max} + j0$. The analysis of the power trajectory during and after the fault is the same as without current limiting. The only difference is the expression for the active power of the GFMI when it is operating under current limitation. Specifically, the per-unit active power under current limitation is given by

$$P = \mathrm{Re}\{\mathbf{V_g}\mathbf{I_{sat}^*}\} = \mathrm{Re}\{\left[V_g \cos(-\delta) + jV_g \sin(-\delta)\right] \cdot I_{max}\} = V_g I_{max} \cos\delta. \tag{3.13}$$

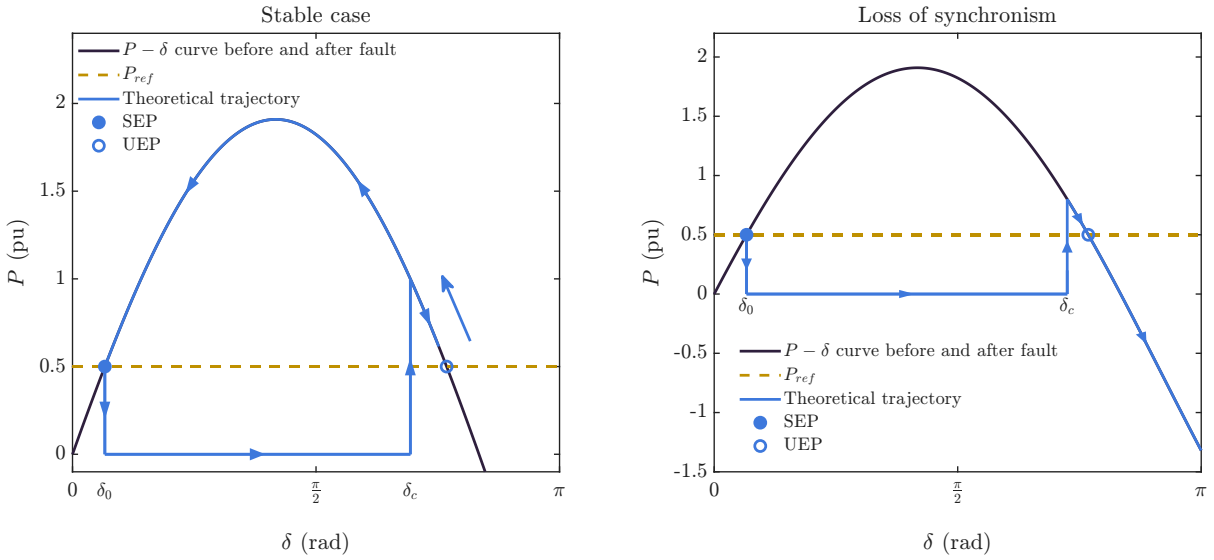



Figure 3.3: Illustration of the $P-\delta$ trajectory of a VSG based GFMI without current limiting, for a short circuit

Based on this equation and the synchronization process presented above, the active power trajectory for the non-inertial GFMI with the fixed angle limiter during and after a short circuit is given in Fig. 3.4. It is worth noting that in the stable case, the GFMI is assumed to exit current limiting mode at the intersection of the saturated and unsaturated $P-\delta$ curve [32].

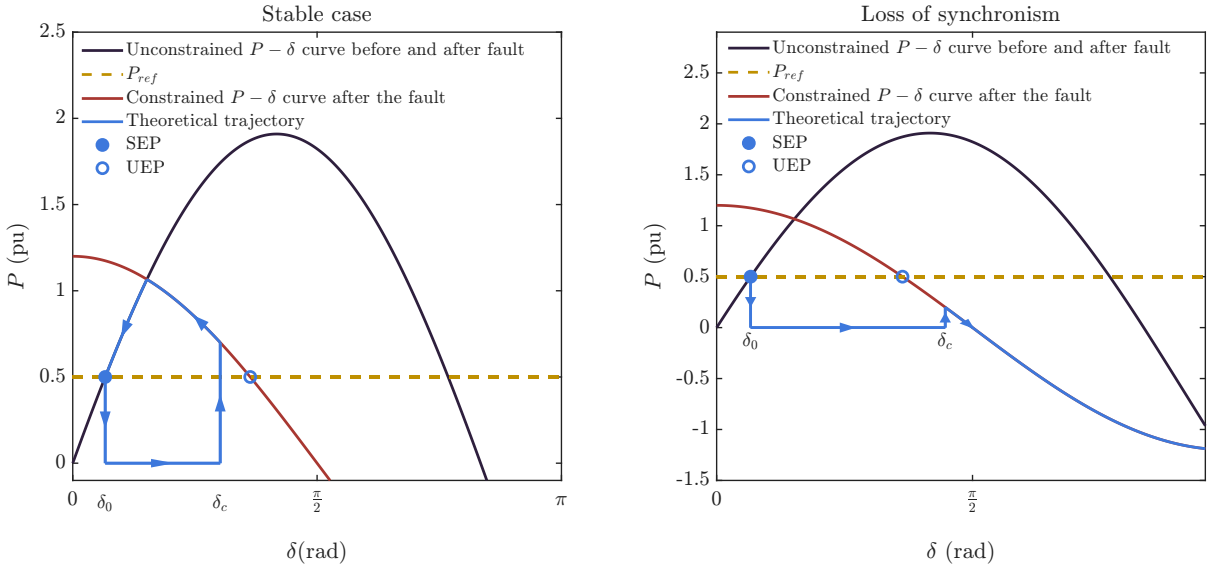



Figure 3.4: Illustration of the $P-\delta$ trajectory of a droop based GFMI with the fixed angle limiter, for a short circuit

It can be easily observed that, the unstable equilibrium point of the new post-fault $P-\delta$ curve has moved closer to the initial operating point. Therefore, the due to the current limitation, the transient stability margin of the GFMI has deteriorated. Additionally, the active-power trajectory for the GFMI with the inertial control is the same as without current limitation, with the only difference being the post-fault power-angle curve.

### 3.2.4 Magnitude limiter

The magnitude limiter is described by (2.20), which can be expressed as

$$\bar{i}_{ref} = \frac{i_{ref}}{k}, \quad k = \max\left(1, \frac{||i_{ref}||}{I_{max}}\right). \tag{3.14}$$

When the VA loop is used, the unsaturated current references are given by

$$i_{ref,\alpha\beta} = \frac{E_{\alpha\beta} - V_{PCC,\alpha\beta}}{Z_v}, \tag{3.15}$$

where $Z_v = R_v + sL_v$. Combining the two previous equations and assuming that $i_{inv} = \bar{i}_{ref}$, the following expression is obtained:

$$i_{inv,\alpha\beta} = \bar{i}_{ref} = \frac{i_{ref}}{k} = \frac{E_{\alpha\beta} - V_{PCC,\alpha\beta}}{kZ_v} \tag{3.16}$$

$$\implies E_{\alpha\beta} - V_{PCC,\alpha\beta} = i_{inv,\alpha\beta}(kZ_v) = i_{inv,\alpha\beta}Z'_v, \tag{3.17}$$

where $Z'_v = kZ_v$. Therefore, the VA loop combined with the magnitude current limiter can be modeled as a voltage source in series with a variable virtual impedance [48], i.e., $kZ_v$, as illustrated in Fig. 3.5. Based on (3.14), when the current limiter is not activated, the virtual admittance parameters are equal to the normal values ($R'_v = R_v$ and $X'_v = X_v$), due to $k = 1$. Otherwise, when the current limiter is activated, $Z_v$ will be scaled up by a factor of $k$ (due to $k > 1$ under current limitation), in order to restrict the current to $I_{max}$ [48].

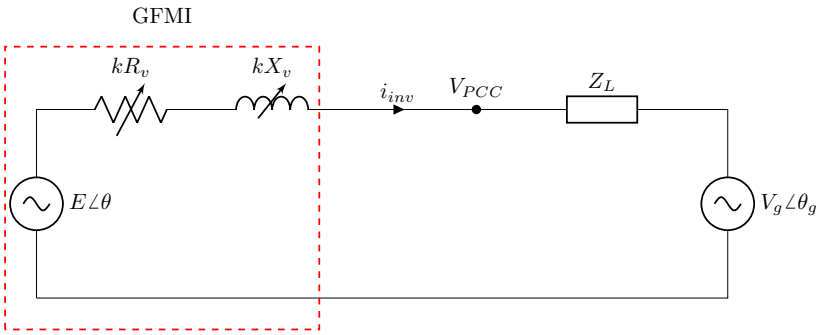



Figure 3.5: Equivalent circuit of the GFMI with the VA control and the magnitude limiter

To obtain the power-angle characteristic of the GFMI with the magnitude current limiter, the equivalent circuit of Fig. 3.5 is used. The following analysis is based on [48]. For this analysis, the grid voltage is considered to have zero phase, therefore the internal voltage source of the GFMI has phase $\delta$.

Using Kirchhoff's voltage law for the equivalent circuit yields

$$\mathbf{E} - \mathbf{V_g} = \mathbf{I_{inv}}\mathbf{Z_{tot}},$$

where $\mathbf{Z_{tot}} = \mathbf{Z_L} + k\mathbf{Z_v}$. Under current limiting operation, where $k > 1$, the modulus of $\mathbf{Z_{tot}}$ is given by

$$Z_{tot}(\delta) = \frac{||E\cos\delta + jE\sin\delta - V_g||}{||\mathbf{I_{inv}}||} = \frac{\sqrt{(E\cos\delta - V_g)^2 + (E\sin\delta)^2}}{I_{max}}, \tag{3.18}$$

which is only a function of $\delta$. Additionally, according to the definition of $\mathbf{Z_{tot}}$, the square of the modulus is given by

$$\begin{aligned} Z_{tot}^2(\delta) &= \mathbf{Z_{tot}} \cdot \mathbf{Z_{tot}^*} = (\mathbf{Z_L} + k\mathbf{Z_v})\,(\mathbf{Z_L^*} + k\mathbf{Z_v^*}) \\ Z_{tot}^2(\delta) &= Z_L^2 + k^2 Z_v^2 + 2k\mathrm{Re}\{\mathbf{Z_v}\mathbf{Z_L^*}\} \\ &\implies k^2 Z_v^2 + 2k\mathrm{Re}\{\mathbf{Z_v}\mathbf{Z_L^*}\} + (Z_L^2 - Z_{tot}^2(\delta)) = 0. \end{aligned} \tag{3.19}$$

The above is a second order equation for $k$, which has one positive and one negative root, since $\mathrm{Re}\{\mathbf{Z_v}\mathbf{Z_L^*}\} = R_v R_L + X_v X_L > 0$ and $Z_L^2 - Z_{tot}^2(\delta) < 0$ always hold. The negative root of this equation does not have any physical meaning. Thus, only the positive solution of $k$ is kept, which is given by

$$k_{sol}(\delta) = \frac{-\mathrm{Re}\{\mathbf{Z_v}\mathbf{Z_L^*}\} + \sqrt{\left[\mathrm{Re}\{\mathbf{Z_v}\mathbf{Z_L^*}\}\right]^2 - Z_v^2\left(Z_L^2 - Z_{tot}^2(\delta)\right)}}{Z_v^2}. \tag{3.20}$$

Since $k > 1$ under current-limiting operation, the above solution is only valid when it is larger than 1. Thus, the scaling factor of the emulated series virtual impedance as a function of the VPA, is given by

$$k(\delta) = \max\left(1, k_{sol}(\delta)\right). \tag{3.21}$$

After the scaling factor has been determined, the current and PCC voltage phasors can be calculated using the equivalent circuit equations as follows:

$$\mathbf{I_{inv}}(\delta) = \frac{\mathbf{E} - \mathbf{V_g}}{k(\delta)\mathbf{Z_v} + \mathbf{Z_L}}, \tag{3.22}$$

$$\mathbf{V_{PCC}}(\delta) = \mathbf{V_g} + \mathbf{Z_L}\mathbf{I_{inv}}(\delta). \tag{3.23}$$

Then, the per-unit power-angle characteristic is obtained by $P = \mathrm{Re}\{\mathbf{V_{PCC}}(\delta)\mathbf{I_{inv}^*}(\delta)\}$. Fig. 3.6 shows the resulting $P - \delta$ curves for different virtual admittance angles, with the magnitude fixed to the value of Table 3.1. It is observed that increasing the resistive part (i.e., a smaller angle) shrinks the $P-\delta$ curve and shifts the unstable equilibrium points to the left. This leads to reduced transient stability margin, as will be explained later. Hereafter, the virtual admittance parameters of Table 3.1 are used, which correspond to $\angle Z_v = 71.6°$, providing relatively good transient stability margins as illustrated in Fig. 3.6.

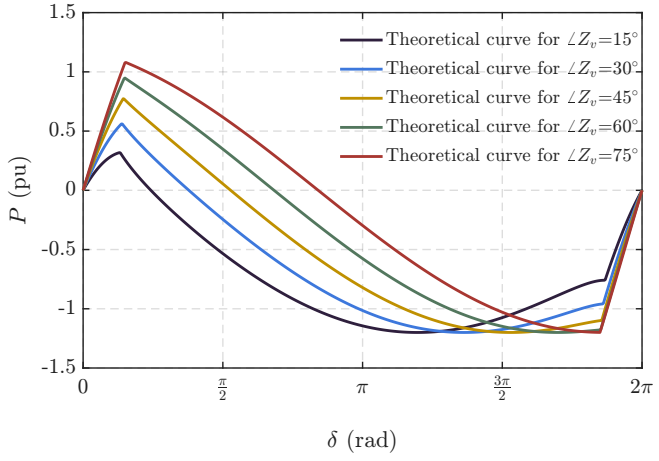



Figure 3.6: Power-angle characteristics for the magnitude limiter for various virtual admittance angles

Based on the derived power-angle characteristics, the active power trajectory for the GFMI employing the magnitude limiter, during and after a short circuit, is depicted in Fig. 3.7. As explained before, the active power trajectory for the GFMI with the inertial control is the same as without current limitation, with the only difference being the post-fault power-angle curve.

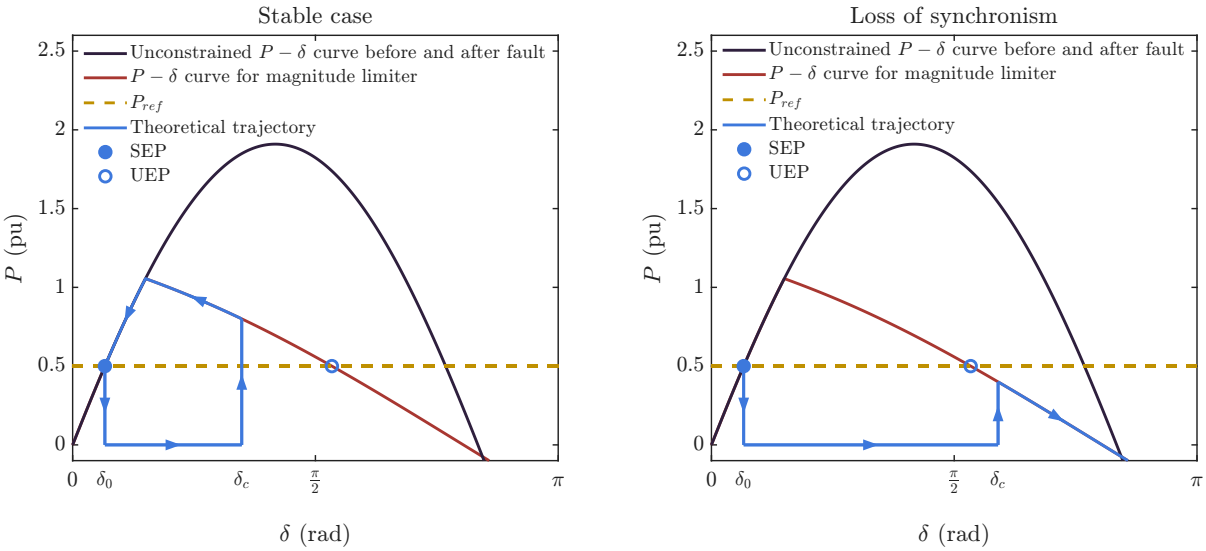



Figure 3.7: Illustration of the $P-\delta$ trajectory of a droop based GFMI with VA control and the magnitude limiter, for a short circuit

### 3.2.5 Calculation of the critical clearing time

Based on the illustration of the active power trajectories during the short circuit, it is evident that there is a maximum clearing angle that ensures the transient stability of the system. This angle is referred to as the critical clearing angle (CCA) and it corresponds to a critical clearing time (CCT), which is the maximum fault duration that ensures the transient stability [31]. It is apparent that the CCA depends on the unstable equilibrium point of the post-fault $P-\delta$ curve. Thus, once the power-angle characteristic is derived, the CCA can then be calculated.

In what follows, the CCT of the inertial and non-inertial APC is calculated, considering again the case of the short circuit, since the active power during the fault is reduced to zero, allowing for simpler and closed-form solutions. The resulting CCT is different for the inertial and non-inertial case, since the dynamics of the VPA are dependent on the utilized active power controller.

***Non-inertial control***

In case of the non-inertial control (e.g droop controller), the VPA during the short circuit can be obtained by integrating (3.5)

$$\delta(t) = k_p \omega_0 P_{ref} t + \delta_0. \tag{3.24}$$

According to the presented active-power trajectory, the critical clearing angle is equal to the unstable equilibrium point angle [31]. Thus, the critical clearing time can be calculated by setting $\delta(t_{cr}) = \delta_{uep}$ in the above equation, yielding

$$t_{cr} = \frac{\delta_{uep} - \delta_0}{k_p \omega_0 P_{ref}}, \tag{3.25}$$

where $k_p$ and $P_{ref}$ are in per unit. This equation indicates that the CCT is decreased for higher values of $P_{ref}$ and $k_p$. The unstable equilibrium point angle can be obtained from the $P-\delta$ curves derived above, depending on the employed current-limitation method.

For example, for the fixed angle limiter, due the simple expression of the active power after the fault, the unstable equilibrium point angle can be calculated by the following closed-form equation:

$$\delta_{uep} = \arccos\left(\frac{P_{ref}}{P_{max,sat}}\right) = \arccos\left(\frac{P_{ref}}{V_g I_{max}}\right).$$

Similarly, the unstable equilibrium point can be found for other methods, by solving the equation $P(\delta_{uep}) = P_{ref}$ and choosing the solution that corresponds to the unstable part of the $P-\delta$ curve.

The resulting CCT from (3.25) and the CCT obtained from time-domain simulations[2], for the system with the parameters of Table 3.1, and for various active power set-points, are shown in Fig. 3.8. It is observed that the simulation CCTs are close to the theoretical ones. Also, as expected, when the GFMI employs a current-limitation method, the transient stability margin is significantly reduced. Additionally, for this specific VA parameter selection, the magnitude limiter offers better transient stability margin, compared with the fixed angle limiter with $\phi_I = 0$.

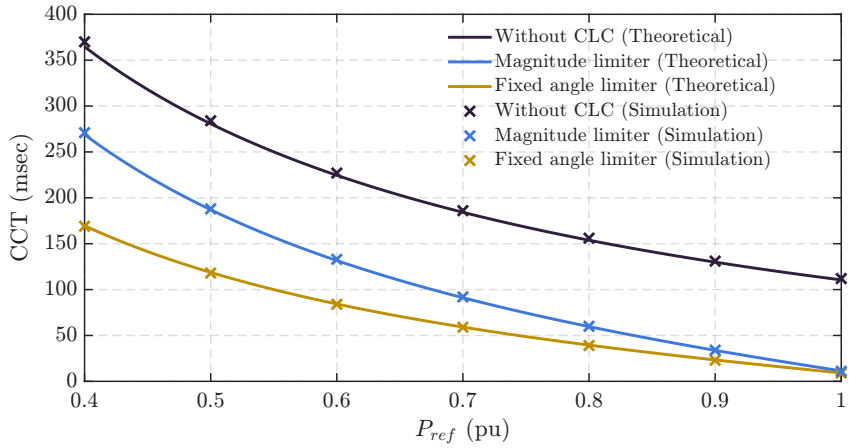



Figure 3.8: Comparison between the theoretical and simulation values for critical clearing time, for the droop control based GFMI, with and without current limiter

These results can be explained by Fig. 3.9, which compares the $P-\delta$ curves of the two current-limitation methods with the case without current limitation. More specifically, it is observed that when current limiters are used, the curves shift to the left, causing the unstable equilibrium points to move closer to the stable ones, and thereby decreasing the transient stability margin. Similarly, comparing the $P-\delta$ curves of the two current limiting methods, it is seen that in this case, the magnitude limiter exhibits better transient stability performance.

***Inertial control***

For the inertial control, the CCA can be calculated using the traditional method of the Equal Area Criterion (EAC) [32]. More specifically, this method considers that the acceleration area (corresponding to Phase 1) is equal to the deceleration area (corresponding to Phase 3) [32]. To calculate the CCA, the case where the deceleration stops exactly at the unstable equilibrium

[2]To obtain the CCT from time-domain simulations, the clearing time is increased with a step of 1 msec until the GFMI loses synchronism

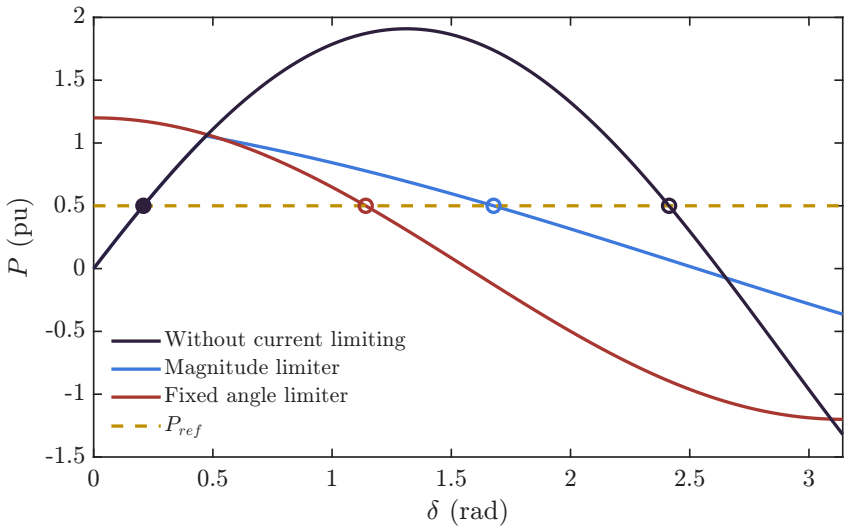



Figure 3.9: Comparison of $P-\delta$ curves for the GFMI with and without current limiter

point is considered:

$$\int_{\delta_0}^{\delta_{cr}} P_{ref} d\delta = \int_{\delta_{cr}}^{\delta_{uep}} (P_{post}(\delta) - P_{ref}) d\delta, \tag{3.26}$$

where $P_{post}(\delta)$ is the post-fault $P-\delta$ curve. For example, $P_{post}(\delta)$ is given by $V_g I_{max} \cos\delta$ for the fixed angle limiter with $\phi_I = 0$. Once the CCA, i.e., $\delta_{cr}$, is calculated for the employed current-limitation method, the CCT can be obtained by determining the expression of the VPA during the fault. Integrating (3.11) yields

$$\frac{2H}{\omega_0}\int_0^t \ddot{\delta} d\tau = \int_0^t P_{ref} d\tau \overset{\dot{\delta}(0)=\Delta\omega(0)=0}{\Longrightarrow} \frac{2H}{\omega_0}\dot{\delta} = P_{ref} t \implies \delta(t) = \frac{P_{ref}\omega_0}{4H} t^2 + \delta_0, \tag{3.27}$$

as in [32], and substituting $\delta(t_{cr}) = \delta_{cr}$:

$$t_{cr} = \sqrt{\frac{4H(\delta_{cr} - \delta_0)}{P_{ref}\omega_0}}. \tag{3.28}$$

Note that in the above analysis, the effect of the damping coefficient is neglected, therefore giving conservative results for the CCT [67]. To illustrate this, the CCT obtained from (3.28) is compared with the one calculated with numerical integration of the VPA dynamics. For this illustration, the fixed angle limiter is used, because it simplifies the calculation of the integral in (3.26), allowing for an analytical expression for the CCA, due to the sinusoidal form of its post-fault $P-\delta$ curve. Therefore, substituting the $P-\delta$ curve in (3.26) yields

$$\begin{aligned} &P_{ref}\delta_{cr} - P_{ref}\delta_0 = P_{ref}\delta_{cr} - P_{ref}\delta_{uep} + P_{max,fa}\int_{\delta_{cr}}^{\delta_{uep}} \cos\delta \, d\delta \\ &\implies P_{ref}(\delta_{uep} - \delta_0) = P_{max,fa}\sin\delta_{uep} - P_{max,fa}\sin\delta_{cr} \\ &\implies \delta_{cr} = \arcsin\left(\sin\delta_{uep} - \frac{P_{ref}(\delta_{uep} - \delta_0)}{P_{max,fa}}\right). \end{aligned} \tag{3.29}$$

Then by further substituting $\delta_{cr}$ in (3.28), the CCT based on the EAC is obtained. Fig. 3.10 shows the comparison of the critical clearing time for the fixed angle limiter, calculated using

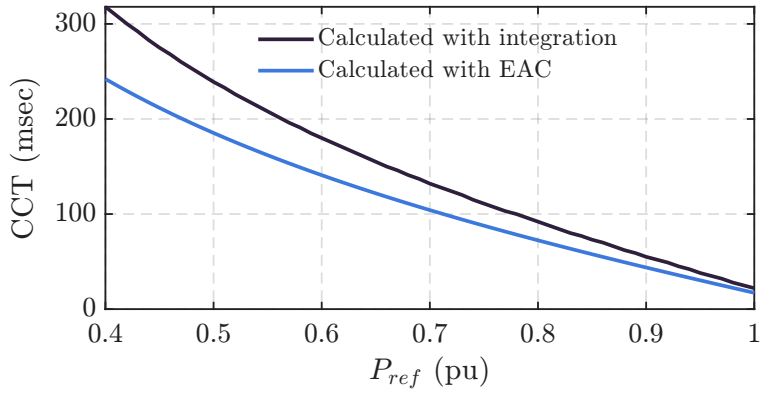



Figure 3.10: Comparison between the CCTs calculated from the EAC method with those obtained by numerical integration

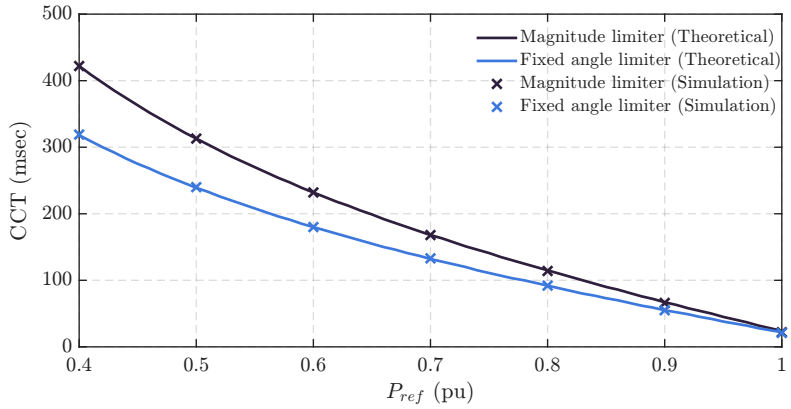



Figure 3.11: Comparison between the theoretical (through numerical integration) and simulation values for critical clearing time, for the inertial control based GFMI, with the fixed angle and magnitude limiter

the EAC method and numerical integration. It is evident that neglecting the damping coefficient gives conservative results for the transient stability margin of GFMIs [67].

Fig. 3.11 shows the comparison between the theoretical critical clearing times, calculated through numerical integration of the VPA dynamics, and those obtained from time-domain simulations, for both the magnitude and fixed angle limiter. It is observed that the time-domain CCTs are close to the theoretical CCTs, thereby validating the large-signal model and the conservativeness of the EAC method for the transient stability assessment of GFMIs.

## 3.3 Validation of the large-signal models through simulations

To further validate the large-signal models and the presented transient stability analysis, time-domain simulations are performed for voltage dips, short circuits and phase jumps, using both the inertial and non-inertial control methods. The dynamic curves obtained from simulations are compared with those derived from the theoretical analysis. The active power set-point is selected as $P_{ref} = 0.5$ pu for every simulation.

### 3.3.1 Non-inertial control

***Short circuit***

The $P - \delta$ trajectories obtained from the simulation of a short circuit at the grid voltage, for the droop-based GFMI, employing the fixed angle and the magnitude limiter are depicted in

Fig. 3.12 and Fig. 3.13, respectively. It is seen that the dynamical $P-\delta$ curves closely match with the theoretical trajectories explained before, for every case, thereby verifying the analysis.

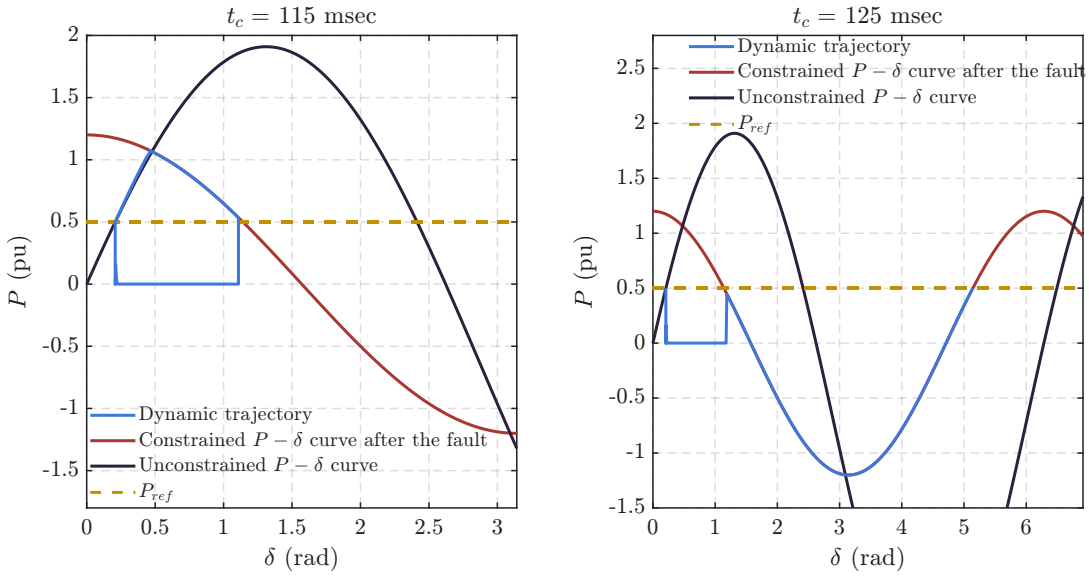



Figure 3.12: Simulation $P-\delta$ trajectories for the fixed angle limiter in case of a short circuit at the grid voltage, for the droop active power controller

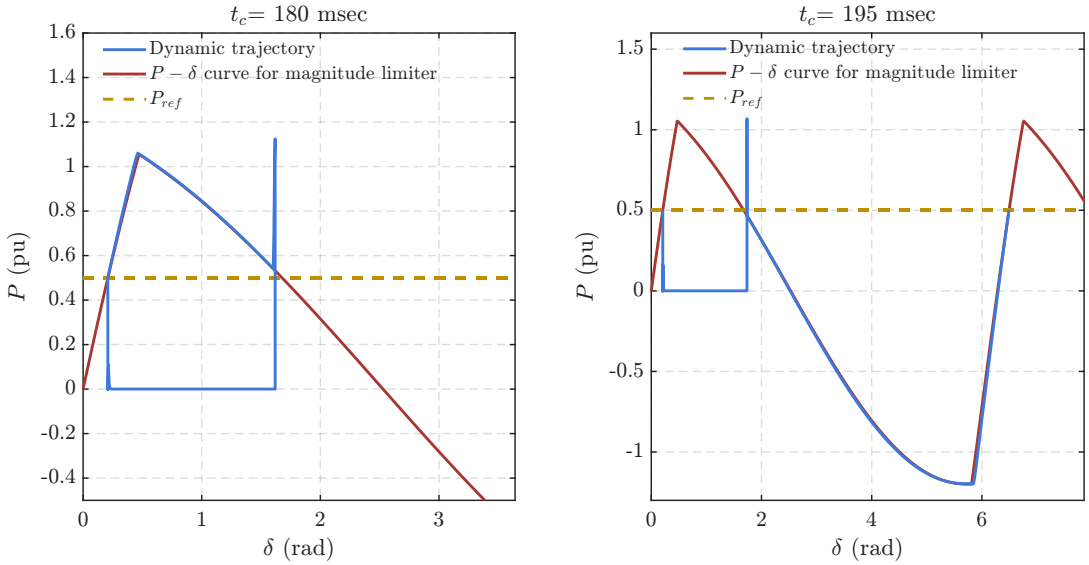
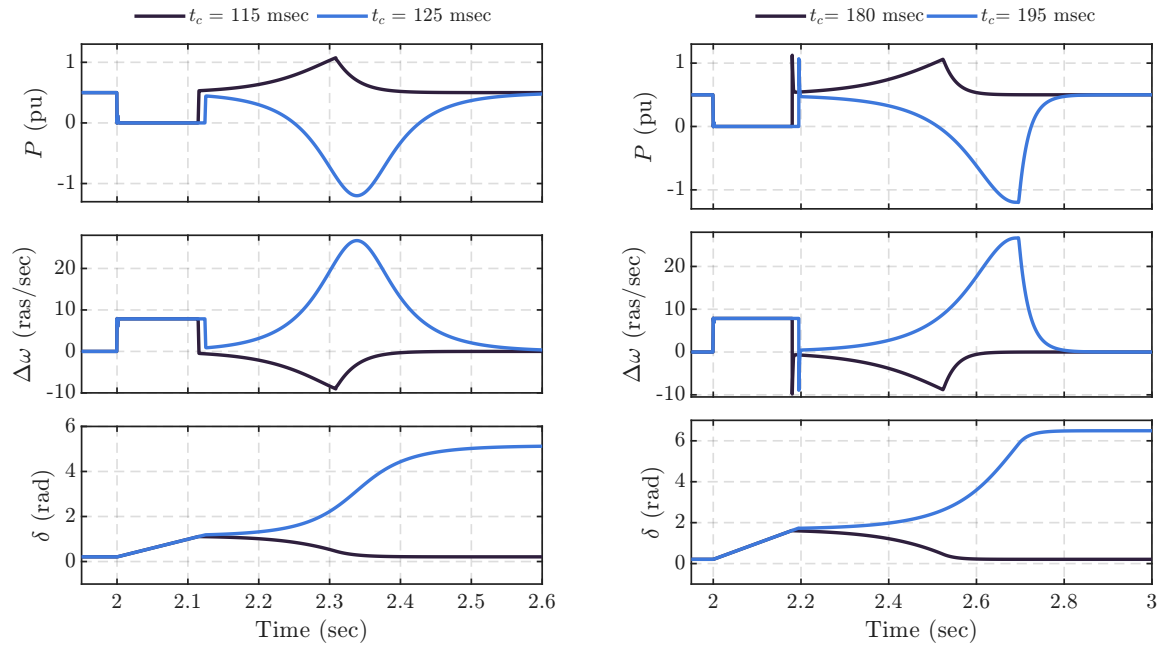



Figure 3.13: Simulation $P-\delta$ trajectories for the magnitude limiter in case of a short circuit at the grid voltage, for the droop active power controller

The alignment of the theoretical analysis with the simulation results can be better explained by Fig. 3.14, which shows the time-domain simulation waveforms of the active power, deviation of the inverter frequency ($\Delta\omega$), and the Virtual Power Angle. More specifically, the active power drops to zero when the short circuit occurs and remains equal to zero for the duration of the fault, leading to a positive $\Delta\omega$, which causes the increase of the VPA according to (3.5). When the fault is cleared, the active power jumps to the post-fault $P-\delta$ curve, which is different depending on the current-limiting method used. If the fault is cleared before the VPA reaches the unstable equilibrium point of the post-fault $P-\delta$ curve,




(a) (b)

Figure 3.14: Simulation results for active power ($P$), deviation of inverter frequency ($\Delta\omega$) and VPA ($\delta$) for the droop active power controller (a) Fixed angle limiter; (b) Magnitude limiter

$\Delta\omega$ instantaneously becomes negative, due to $P > P_{ref}$, causing the VPA to decrease and finally settle to the initial operating point. In contrast, if the clearing angle is larger than the unstable equilibrium point angle, $\Delta\omega$ remains positive (due to $P < P_{ref}$), which leads to further increase of the VPA and loss of synchronization with the grid.

It is important to notice that due to the first-order nature of the droop controller, even in cases where synchronization is lost, the GFMI is able settle to a new stable equilibrium point after around one oscillation cycle, thus regaining synchronization with the grid. This can be observed in Fig. 3.14, where in the cases with $t_c = 125$ msec for the fixed angle limiter and $t_c = 195$ msec for the magnitude limiter, after the fault, the active power becomes equal to its set-point, $\Delta\omega$ goes to zero and the Virtual Power Angle settles at an angle that is larger than its initial operating point. When the fixed angle limiter is used, the new stable equilibrium point can be in the current limiting mode [56], as seen in Fig. 3.12. In this case, the GFMI is continuously operating under current limitation. In contrast, when the magnitude limiter is employed, the GFMI exits the current limitation mode and the normal operation is restored.

***Voltage dip***

Figures 3.15 and 3.16 show the simulation $P-\delta$ trajectories, in case of a voltage dip of the grid voltage to 0.2 pu, for both the fixed angle and magnitude limiter. Similarly to the short-circuit case, the active power during the fault drops below its set-point, leading to the increase of the VPA. Since the grid voltage recovers to $V_g = 1$ pu after the fault, the post-fault $P-\delta$ curve is the same as with the short-circuit case. Therefore, in order to maintain the synchronization with the grid, the fault should be cleared before the VPA reaches the unstable equilibrium point of the post-fault power-angle curve. The only difference with the short circuit case, is that during the voltage dip the active power output is not zero. More specifically, the active power of the GFMI, when the fixed angle limiter is activated during a voltage dip, is given by $P(\delta) = V_{g,dip} I_{max} \cos\delta$. Additionally, to obtain the active power of the GFMI when the magnitude

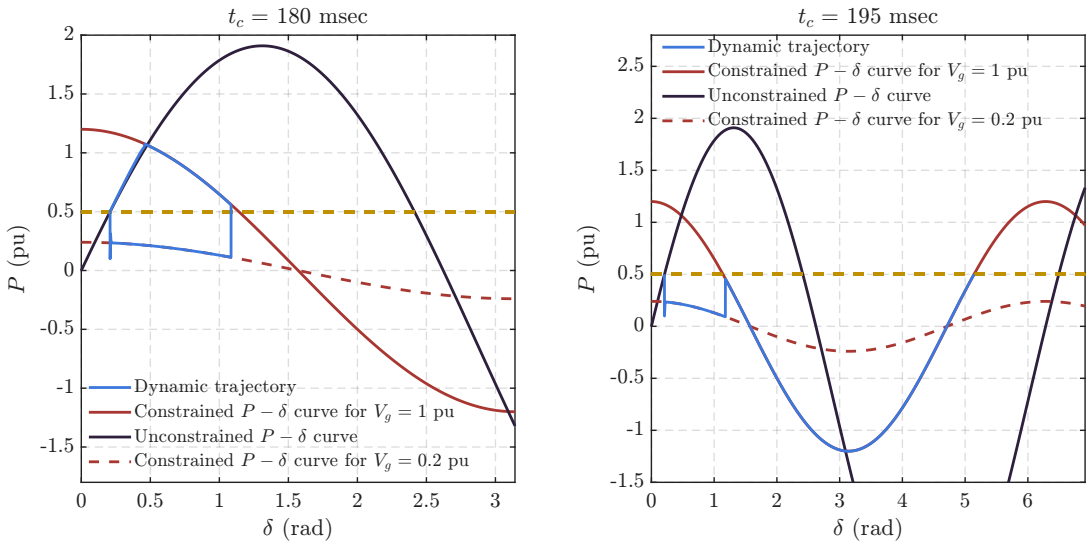



Figure 3.15: Simulation $P-\delta$ trajectories for the fixed angle limiter in case of an 80% voltage dip at the grid voltage, for the droop active power controller

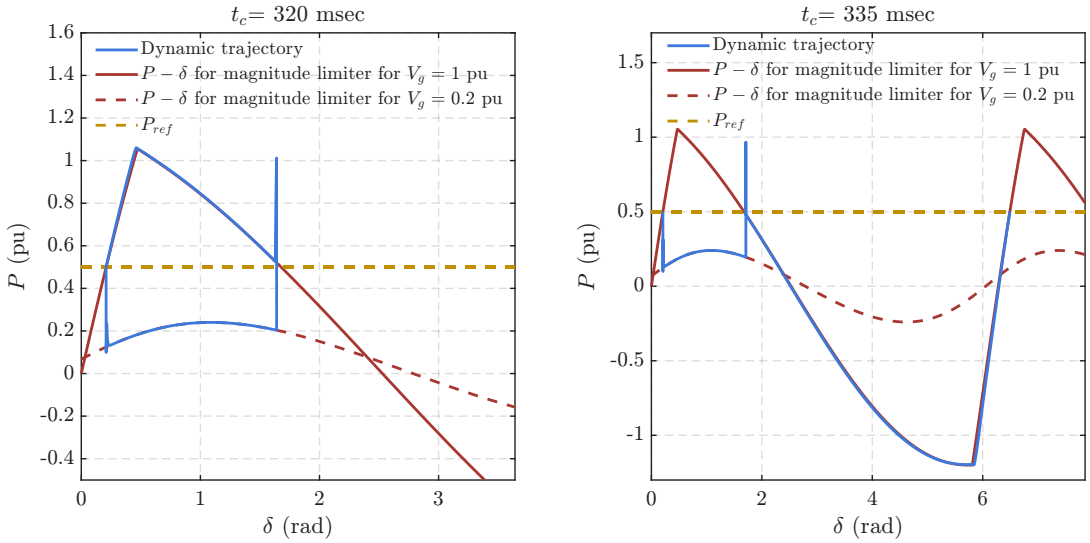



Figure 3.16: Simulation $P-\delta$ trajectories for the magnitude limiter in case of an 80% voltage dip at the grid voltage, for the droop active power controller

limiter is employed, $V_g = V_{g,dip}$ is substituted into (3.18), (3.22) and (3.23). The resulting theoretical power-angle characteristics during the voltage dip are shown in Figures 3.15 and 3.16 for the fixed angle and magnitude limiter respectively. It is observed that in every case, the dynamic trajectories closely match the theoretical curves, which validates the analysis for the $P-\delta$ curves during the voltage dip. It is also seen that, again for the fixed angle limiter, the new stable equilibrium point is in the current limiting mode.

***Phase jump***

The comparison of the dynamic and theoretical power-angle curves in case of phase jumps at the grid voltage is shown in Figures 3.17 and 3.18, for the fixed angle and magnitude limiter respectively. Although phase jumps are different from voltage dips, the same $P-\delta$ curves can be used to assess the transient stability of the GFMI. More specifically, because only the phase angle of the grid voltage is changed during phase jumps, i.e., the voltage magnitude remains constant, the post-fault power-angle curve is the same as the voltage dip and short circuit. Since

the angle of the IVS in the sub-transient frame remains constant, if the phase angle of the grid voltage increases (decreases) by $\Delta\theta_g$, the Virtual Power Angle decreases (increases) by the same amount when the phase jump occurs. This is explained by the following equations [68]

$$\delta = \theta - \theta_g = \theta - (\theta_{g,bef} + \Delta\theta_g) = (\theta - \theta_{g,bef}) - \Delta\theta_g = \delta_{bef} - \Delta\theta_g. \tag{3.30}$$

Therefore, a negative phase jump of the grid voltage angle, i.e., $\Delta\theta_g < 0$, leads to an increase of the VPA according to the above equation. In this case, to avoid the loss of synchronization with the grid, $|\Delta\theta_g|$ should not exceed the angle difference between the initial operating point and the unstable equilibrium point of the post-fault $P-\delta$ curve, i.e., $|\Delta\theta_g| < (\delta_{uep} - \delta_0)$. Figures 3.17 and 3.18 show that the GFMI with the magnitude limiter is able to withstand a $-60°$ phase jump without losing synchronism, unlike the GFMI employing the fixed angle limiter, due to the fact that $\delta_{uep}$ is larger for the magnitude limiter as illustrated by Fig. 3.9. Similarly to the previous two fault scenarios, it is observed that, for the fixed angle limiter, the new stable equilibrium point is in the current limiting mode.

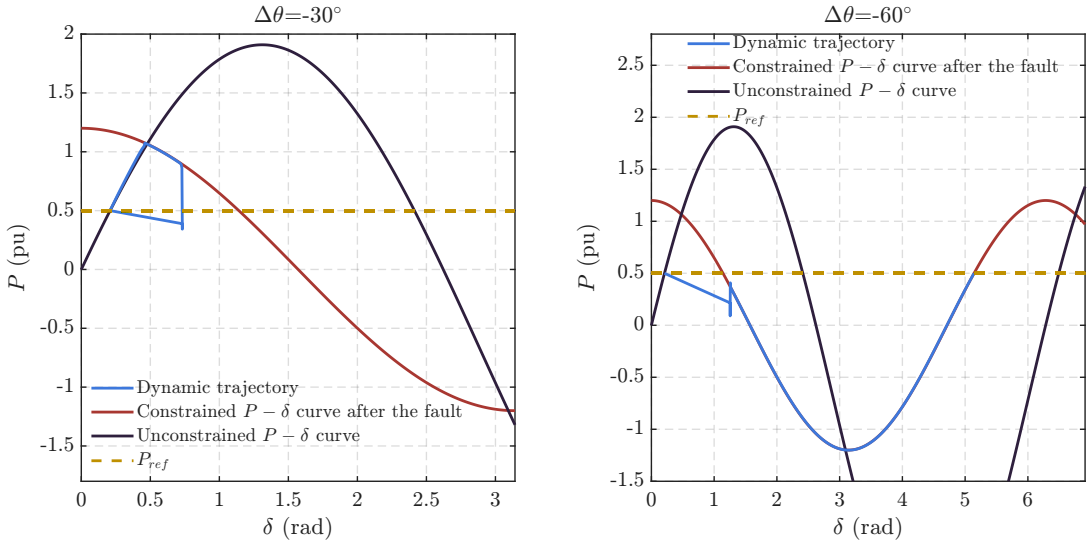



Figure 3.17: Simulation $P-\delta$ trajectories for the fixed angle limiter in case of phase jumps at the grid voltage, for the droop active power controller

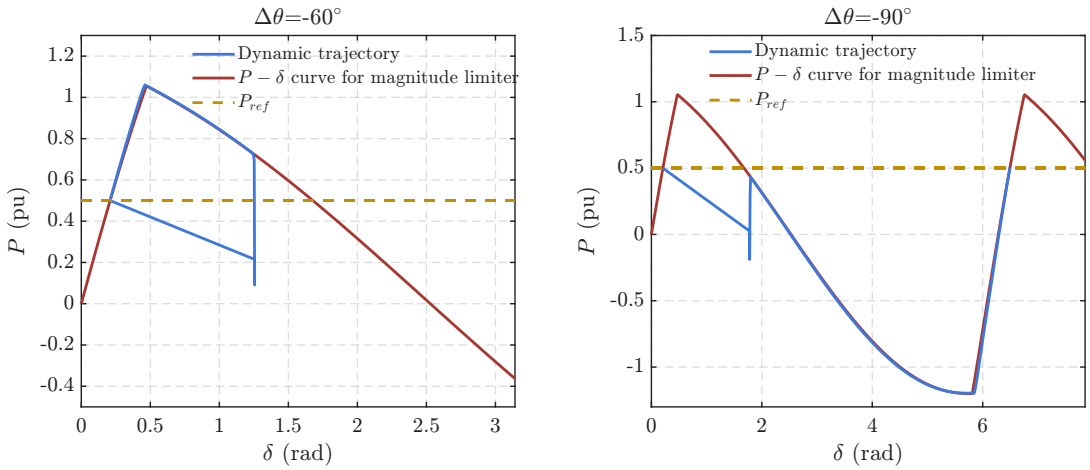



Figure 3.18: Simulation $P-\delta$ trajectories for the magnitude limiter in case of phase jumps at the grid voltage, for the droop active power controller

### 3.3.2 Inertial control

For the inertial control (e.g droop control with LPF), a short circuit at the grid voltage was simulated for the GFMI with the magnitude and the fixed angle limiter. In Figures 3.19 and 3.20 the dynamic $P - \delta$ curves obtained from the simulations and the theoretical trajectory that was previously presented are compared, for the magnitude and fixed angle limiter respectively. Similarly, Figures 3.21 and 3.22 show the time-domain waveforms of the active power, deviation of inverter frequency ($\Delta\omega$) and the Virtual Power Angle, during and after the disturbance.

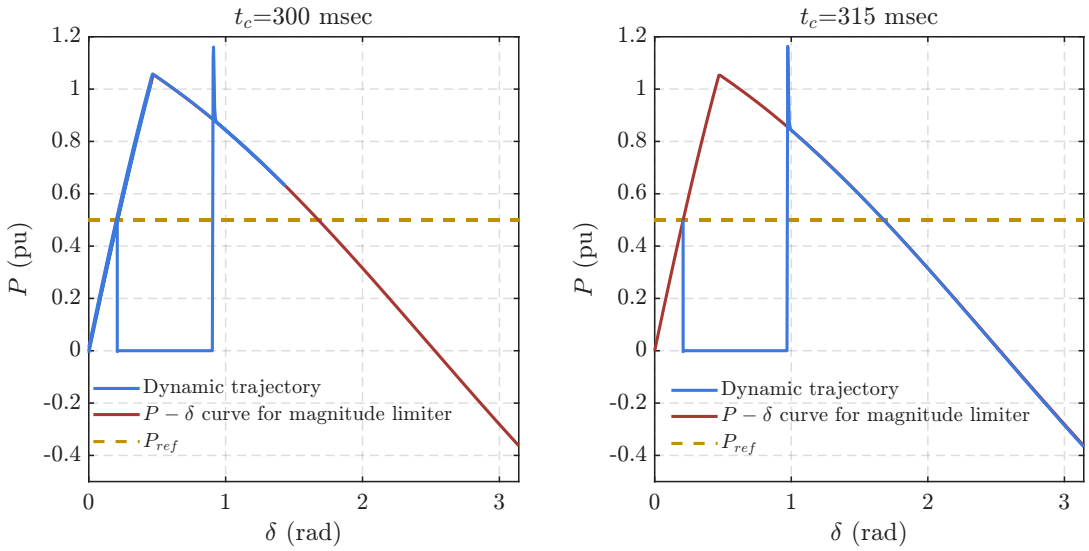



Figure 3.19: Simulation $P - \delta$ curves for the magnitude limiter in case of a short circuit at the grid voltage, for the inertial active power controller

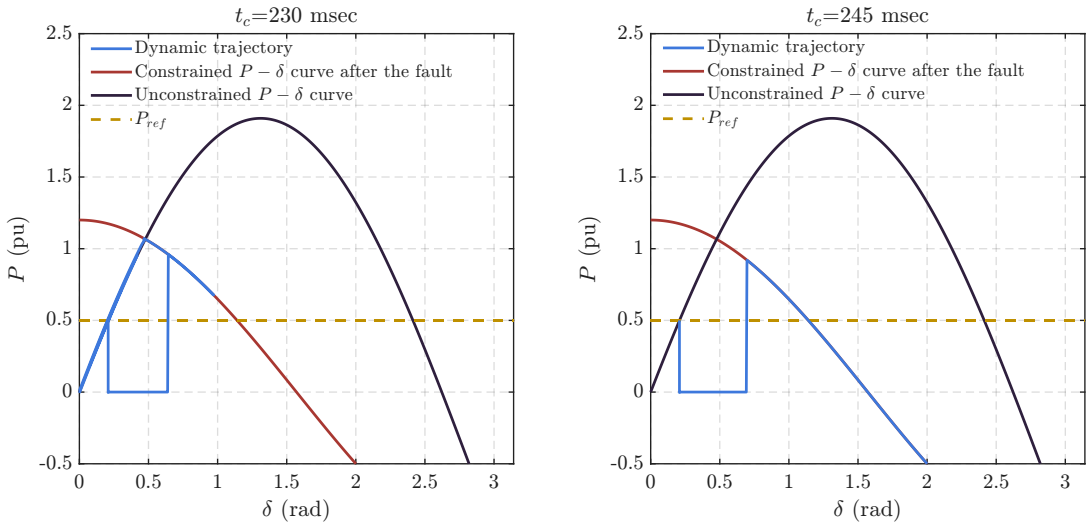



Figure 3.20: Simulation $P - \delta$ curves for the fixed angle limiter in case of a short circuit at the grid voltage, for the inertial active power controller

It is observed that, for every case, the simulation $P - \delta$ trajectory is very close to the theoretical one, which validates the analysis presented before. It is also seen that when the fault duration is longer than the critical clearing time (which is theoretically equal to 313 and 240 msec for the respective current-limitation method), synchronization with the grid is lost.

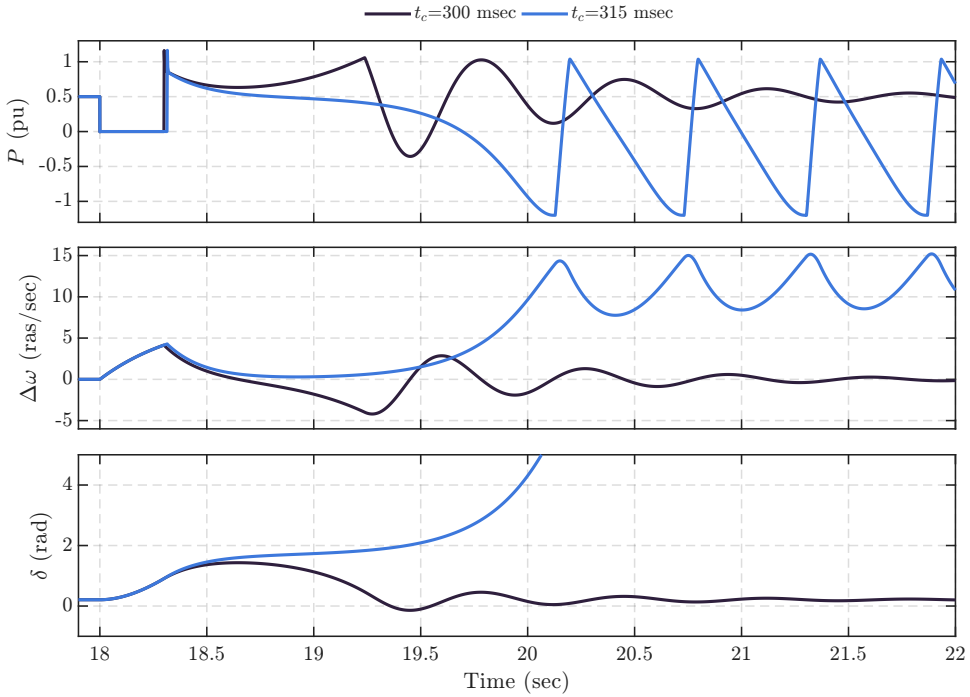



Figure 3.21: Simulation results for active power ($P$), variation of inverter frequency ($\Delta\omega$) and VPA ($\delta$) for the magnitude limiter in case of a short circuit at the grid voltage, for the inertial active power controller

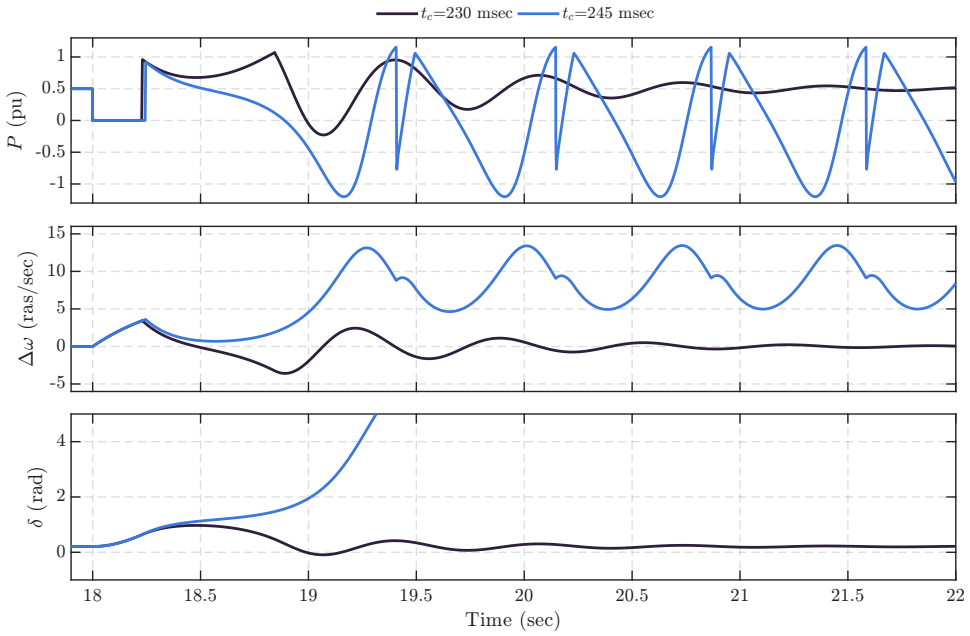



Figure 3.22: Simulation results for active power ($P$), variation of inverter frequency ($\Delta\omega$) and VPA ($\delta$) for the magnitude limiter in case of a short circuit at the grid voltage, for the inertial active power controller

On the other hand, if the fault duration does not exceed the critical clearing time, the GFMI returns to the stable equilibrium point after several oscillations around it.

Additionally, the results of Figures 3.21 and 3.22 are in accordance with the presented theoretical active power trajectory for the inertial control. More specifically, prior to the fault the GFMI operates at the stable equilibrium point $(\delta, \Delta\omega) = (\delta_0, 0)$. During the fault, the active power output is reduced to zero, due to the short circuit, leading to the increase of the

internal frequency. Then, when the fault is cleared, the internal frequency decreases (because $P_{ref} - P < 0$), but $\Delta\omega$ remains positive, causing the VPA to increase. When the fault is cleared in 300 msec (for the magnitude limiter) and 230 msec (for the fixed angle limiter), $\Delta\omega$ becomes negative, while the active power is still larger than $P_{ref}$. In this case, the VPA decreases and synchronization is restored. In contrast, when the fault clearing time is 315 msec (for the magnitude limiter) and 245 msec (for the fixed angle limiter), the active power drops below $P_{ref}$, while $\Delta\omega > 0$ still holds. In this case, the VPA continues to increase and the GFMI loses synchronization with the grid.

Furthermore, unlike the non-inertial control case, when the GFMI loses synchronism with the grid, it cannot settle to a new stable equilibrium point after one cycle. In contrast, for the inertial control, the synchronization with the grid is lost, as indicated by the oscillations observed in the time-domain waveforms.

# Chapter 4

# Hardware-in-the-loop real-time simulation

In this Chapter the current-limitation methods that were previously implemented in offline simulations, are implemented and simulated using controller hardware-in-the-loop Real-Time Simulation. First, a brief introduction on Real-Time Simulations is presented, describing their applications and how they differ from offline simulations. Then, the configuration of the Real-Time Simulation used for the verification of grid-forming controls and current-limitation methods is presented, along with the models of the physical plant and the controllers, highlighting the differences from the corresponding offline simulation models. Finally, the results for the Real-Time Simulation of the current limiting methods under short circuits and phase jumps are shown.

## 4.1 Brief introduction on Real-Time Simulations

Digital Real-Time Simulators (DRTS) are able to solve the differential equations that govern the simulated system at real-world clock time, by utilizing digital hardware and parallel computing methods [69]. The difference between RTS and offline simulations (or non-RT simulations) lies in the time needed to solve the differential equations and provide the output results, which is referred to as the execution time of the simulation [69]. More specifically, during the fixed simulation time step, the amount of real-world time needed to solve all the equations may be larger or smaller than the chosen time step [70]. In offline simulations, the instant at which the results are available is insignificant, as seen in Fig. 4.1. In this case, the speed in which the equations are solved is dependent on the computational power and the complexity of the simulated system [70]. In contrast, an RT-simulator should solve the differential equations for a single simulation time-step, within the same time duration in a real-world clock [71]. Therefore, the time duration in which the RT simulator calculates the solution, should be smaller than the real-clock duration of the chosen time step [70], as illustrated in Fig. 4.1. To that end, if the simulation operations are not completed during the chosen fixed time step, the RT-simulation is considered to be incorrect [70].

The applications of RT simulations range from power systems, electrical machines and power electronics, to thermal, fluid, mechanical dynamics etc [69]. Real-time simulations can be used for various purposes. For example, in the design stage of a new product/system, a fully digital RTS model can be used, where every system component (such as physical plant, controllers, protection etc) is represented in the simulator, without any external input or output signals [71]. A fully digital RTS provides faster and more accurate results in comparison with its offline simulation counterparts [69]. Generally, having accurate model representations of the system in the design stage is crucial, in order to enable more precise experiments later on

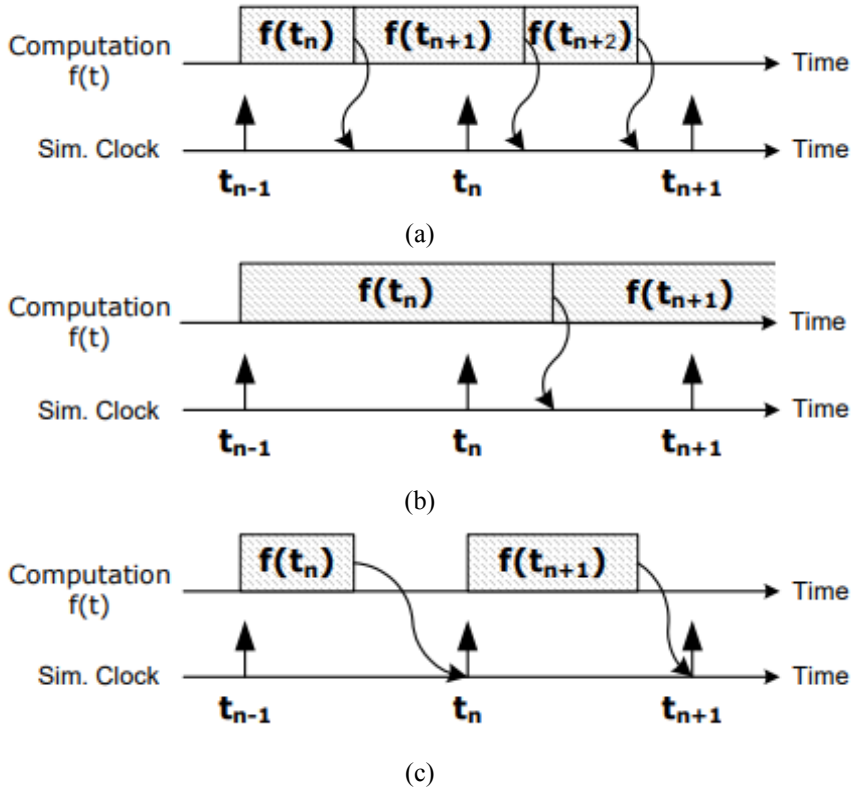



Figure 4.1: Illustration of the difference between real time and offline simulation (a) Offline simulation (faster than real-time); (b) Offline simulation (slower than real-time); (c) Real-time simulation (synchronized) [70]

[69].

Except of the fully digital real time simulation, the other main category of DRTS is hardware-in-the-loop (HIL) real-time simulation, where some components (e.g the controller) of the fully Digital RTS (DRTS) are replaced with physical equipment [71]. In fact, the DRTS is most frequently used in HIL mode for testing devices in real-time conditions, where it enables the modeling of the real surrounding physical plant on the RT simulator [69]. This way, the DRTS provides accurate representation of the behavior of the system equipment in the real field [69].

When the HIL setup consists of the physical controller hardware interacting with the rest of the simulated system, it is referred to as "controller hardware-in-the-loop" [71]. This way, a new controller implementation can be tested, by getting feedback signals from the real-time simulator and generating the appropriate output signals, which are then provided to the real-time simulator [71]. Controller HIL enables the testing of new controller designs when the physical experiment benches are unavailable, as well as the testing of extreme events without causing damage to real hardware equipment [70].

## 4.2 Configuration of the real-time simulation

Based on the aforementioned advantages of DRTS, a controller hardware-in-the-loop RT simulation is performed, in order to evaluate the performance of the implemented current-limiting methods in real-time conditions, which are closer to the behavior of real field equipment, in comparison with the offline simulations.

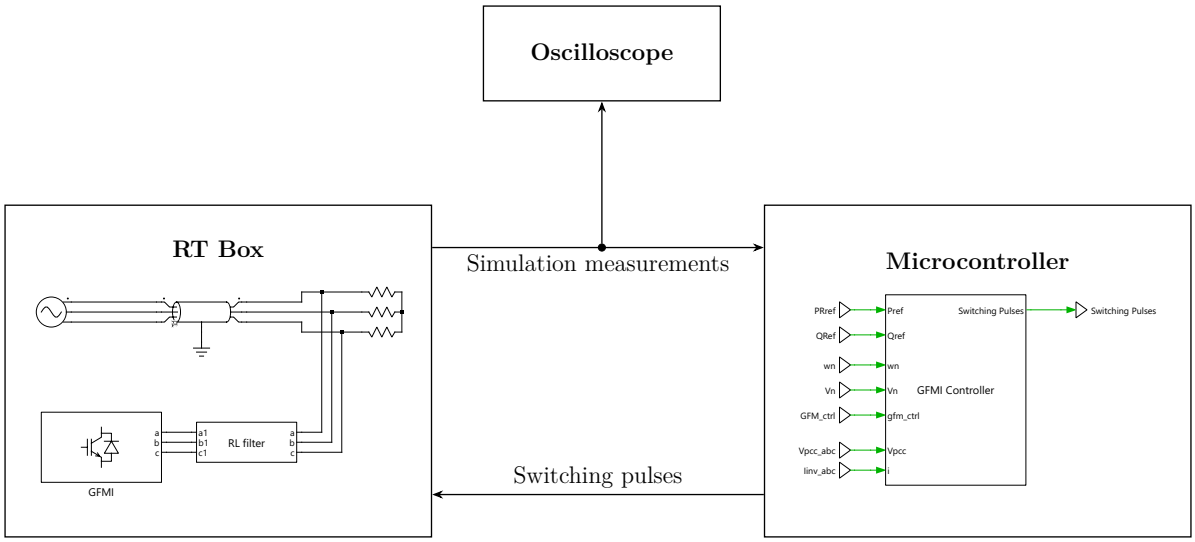



Figure 4.2: Illustration of the Real-Time Simulation setup

As mentioned previously, in controller HIL simulations, the real controller hardware is interacting with the virtual plant which is modeled inside the real-time simulator. The setup used for the real-time simulation is depicted in Fig. 4.2. It consists of a microcontroller, a real time simulator and an oscilloscope. The utilized RT simulator is the Plexim RT Box 1 [72] and the control systems are implemented using the C2000 LAUNCHXL-F28379D microcontroller of Texas Instruments [73].

The RT Box simulates the virtual plant, including components such as the infinite voltage source of the grid, transmission lines, inverter connection filters, loads, the three-phase inverter etc. The measurements from the simulated virtual plant, such as three-phase voltage and current, are provided from the analog outputs of the RT Box to the analog input pins of the microcontroller. Then, the microcontroller processes these signals based on the implemented control systems and generates the switching pulses for the corresponding inverter switches. The switching pulses, which are the output of the control system, are fed to the corresponding digital inputs of the RT-box, in order to drive the inverter switches. Furthermore, the measurement signals from the RT box outputs are connected to an oscilloscope, in order to observe the resulting waveforms during both steady state operation and transients conditions.

### 4.2.1 RT Box

The Plexim RT Box 1, which was used in the RT simulation, is shown in Fig. 4.3. It has 16 Analog Input and 16 Analog Output channels, as well as 32 Digital Input and 32 Digital Output channels [72]. The analog input channels voltage range, can be selected as $\pm 10$ V or $\pm 5$ V, and each channel can be configured for either single-ended or differential measurement [72]. The analog output channels produce voltage signals from the measurements of the simulated virtual plant, whose full-scale range can be selected as $\pm 10$ V, $\pm 5$ V, $0 - 10$ V, $0 - 5$ V [72]. However, the analog output signals that are fed to the microcontroller should be limited through the simulation, in the range of $0 - 3.3$ V, in order to match with the microcontroller inputs and avoid potential damage. Therefore, despite the fact that the virtual plant is simulated with the actual voltage and current values, the signals that are provided to the microcontroller and the ones observed on the oscilloscope, are scaled to be in the acceptable voltage range. As it was previously mentioned, the switching pulses are provided to the RT Box through the Digital Input channels.

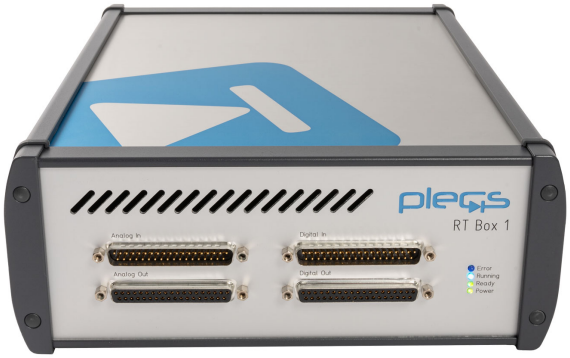



Figure 4.3: Picture of RT Box 1 [72]

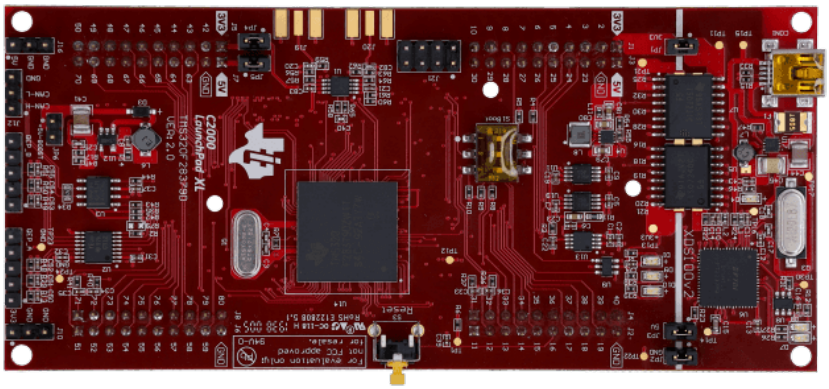


Figure 4.4: Picture of the TI C2000 LAUNCHXL-F28379D microcontroller [73]

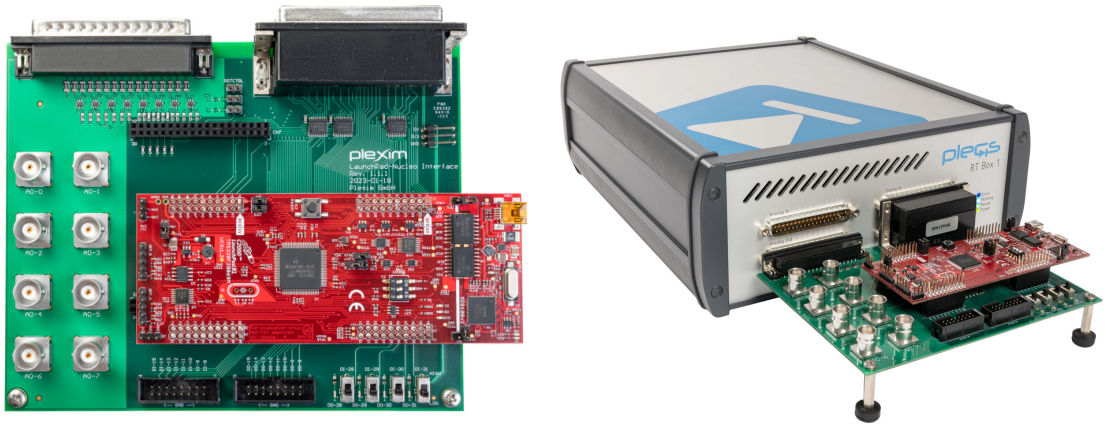
### 4.2.2 TI C2000 LAUNCHXL-F28379D microcontroller

The grid-forming control and the current-limitation methods are implemented on the C2000 LAUNCHXL-F28379D of Texas Instruments [73], which is shown in Fig. 4.4. This microcontroller can be directly programmed through PLECS, using already developed library blocks, such as ADCs, PWM etc. This allows for very simple implementation of the controllers used in the offline simulations, with only a few modifications to adapt to the needs of real-time simulations. Additionally, the "external mode" operation enables the modification of parameter values during the real-time simulation, without the need of rebuilding the code on the microcontroller.

The microcontroller peripherals consist of Analog to Digital Converters (ADCs), Digital to Analog Converters (DACs), GPIO pins (General Purpose Input/Output pins) etc [74]. The ADCs are used to get measurements, for example from the analog output channels of the RT Box, whereas the DACs are used to output voltage signals. GPIO pins are used to read digital input signals, or provide digital output signals such as the switching pulses that are provided to the RT Box.

### 4.2.3 RT Box launchpad interface

In order to simplify the connection of external hardware and the accessibility of inputs and outputs of the RT Box, the "RT Box LaunchPad Interface" can be used [75]. With this



(a) (b)

Figure 4.5: Illustration of the LaunchPad interface (a) Microcontroller connected to the LaunchPad interface [75]; (b) Microcontroller connected to the RT Box through the LaunchPad interface [72]

interface, certain microcontrollers can be easily connected to the RT Box, without the need for the development of new interface hardware from the user [75]. A microcontroller connected to the LaunchPad Interface is shown in Fig. 4.5a and their connection to the RT Box is depicted in Fig. 4.5b.

It can be seen that the interface connects the pins of the microcontroller with specific inputs and outputs of the RT Box. It also provides access to a number of RT Box analog outputs through BNC connectors, which can be connected to an oscilloscope to observe measurements from the real time simulation. Additionally, the interface board enables the access to unused digital input/output signals through header pins and also includes sliding switches and LEDs for easier communication of the state of the digital outputs [75].

## 4.3 Virtual plant model in RT Box

As explained in previous sections, in control hardware-in-the-loop RT simulations, the power stage of the system is simulated inside the real-time simulator, i.e., the RT Box, and it is referred to as virtual plant or virtual power circuit. The simulated system is similar to the one used in the offline simulations and it is shown in Fig. 4.6. It consists of the infinite voltage source representing the grid, a transmission line, a resistive load connected to the PCC and a two-level three-phase inverter, which is connected to the PCC through an inductive filter. The main differences from the offline simulation system are the addition of the resistive load and the use of a full switching model for the converter instead of the average model.

***RT Box digital inputs and outputs***

The pulses which determine the state of the switches of the inverter are given by the logical AND operation of a digital variable “PWMen” with the switching pulses that are provided to the digital inputs of the RT Box from the microcontroller. The variable “PWMen” is used to enable the PWM of the inverter and it is controlled using one of the sliding switches (digital inputs) of the LaunchPad interface, as illustrated in Fig. 4.7. It is seen that except of the AND operation, this digital variable is also given as an output in two RT Box digital outputs, one of which is an LED of the interface to show if the pulses are enabled and the other one is fed to the microcontroller as an input, which will be explained later.

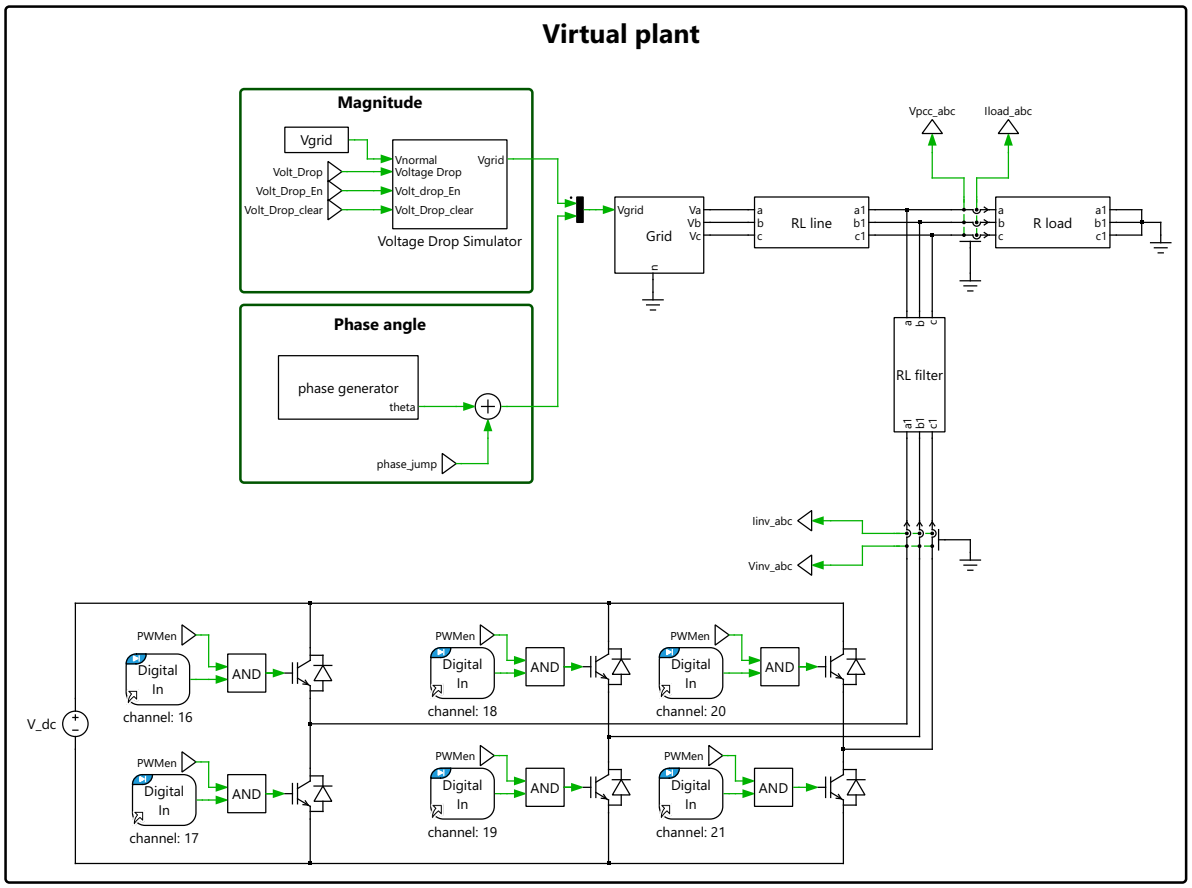



Figure 4.6: Virtual plant model simulated inside the RT Box

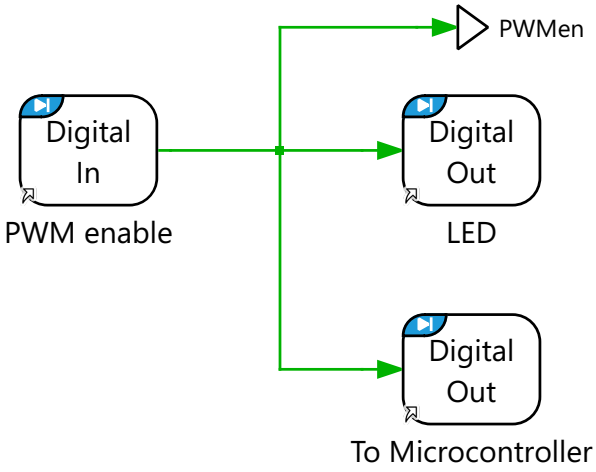



Figure 4.7: Illustration of the control of the PWM enable digital variable

***Grid voltage calculation***

Similarly to the offline simulation, the voltage magnitude and angle are fed to the grid voltage, which produces a three-phase positive sequence sinusoidal signal. To allow for the simulation of disturbances such as phase jumps and voltage dips, the variable "phase_jump" and the subsystem "Voltage Drop Simulator" are used respectively, which are controlled with the variables shown in Fig. 4.8. It is worth noting that these variables can be modified in real time, i.e., while the simulation is running.

The "phase_jump" variable is the angle change of the grid voltage in radians and it is

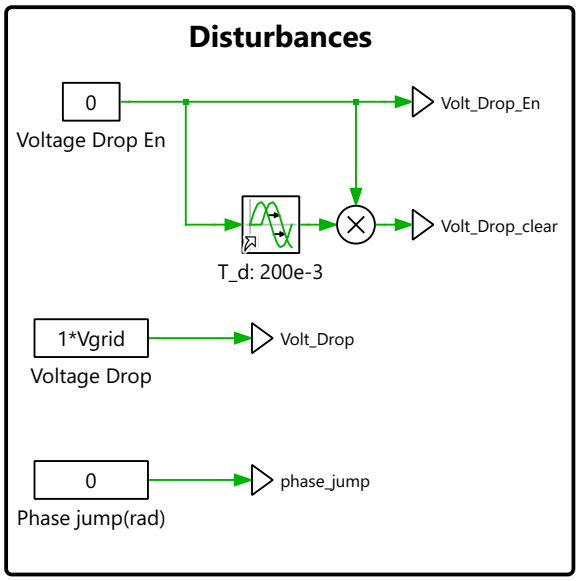



Figure 4.8: Control variables for the simulation of phase jumps and voltage dips

simply added to the angle of the grid voltage to simulate a phase jump, as seen in Fig. 4.6. Additionally, to simulate voltage dips, the "Volt_Drop_En", "Volt_Drop_clear" and "Volt_Drop" variables are fed to the Voltage Drop Simulator subsystem, whose output is the grid-voltage magnitude, and its implementation is shown in Fig. 4.9. Specifically, when the "Volt_Drop_En" is zero, so is the "Volt_Drop_clear" due to the multiplication block, as seen in Fig. 4.8. In this case, the switches states in Fig. 4.9 do not change, which results in nominal voltage magnitude, i.e., normal operation. On the other hand, when "Volt_Drop_En" is set to 1, the state of the first switch changes, thus reducing the grid voltage magnitude by an amount equal to the "Volt_Drop" variable. After a specified time duration, which is implemented through the transport-delay block, "Volt_Drop_clear" becomes equal to 1, causing the state of the second switch to change. Therefore, the grid-voltage magnitude is restored to its nominal value, which means that the fault has been cleared. Then, "Volt_Drop_En" and consequently "Volt_Drop_clear" can be set to 0, which restores the switches to their initial state. In that case, the grid-voltage magnitude is still nominal and the voltage drop can be simulated again

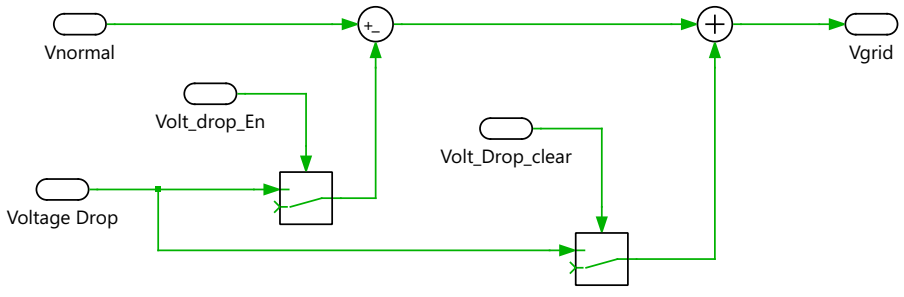



Figure 4.9: Voltage Drop Simulator subsystem

***RT Box analog outputs***

As was previously mentioned, the analog output channels of the RT Box are used to provide simulation measurements to the microcontroller and to the oscilloscope to observe the time-domain waveforms. The measurements needed for the grid-forming controller are the three-phase voltages at the PCC, and the three-phase output currents of the inverter, as illustrated in

Fig. 2.26a. Additionally, the magnitude of the output current is an important measurement, in order to validate the implemented current-limitation methods. To that end, the analog output signals of the RT Box are the instantaneous measurements of the PCC voltage and the inverter output current, which are fed to the microcontroller, and the output-current magnitude, which is connected to the oscilloscope, in order to observe its value. Furthermore, the simulation measurements should be scaled, such that the analog outputs are in the scale of $0 - 3.3$ V. Therefore, the three-phase voltage and current measurements are first divided by two times their nominal value (i.e., $2\hat{V}_n$ and $2\hat{i}_n$) and shifted with an offset of 1.65, while the current-magnitude value is only normalized by its nominal value (i.e., $\hat{i}_n$). Also, a maximum and minimum output voltage value of 3.3 V and 0 V, respectively, are set in the Analog Out block, in order to avoid potential damage of the microcontroller.

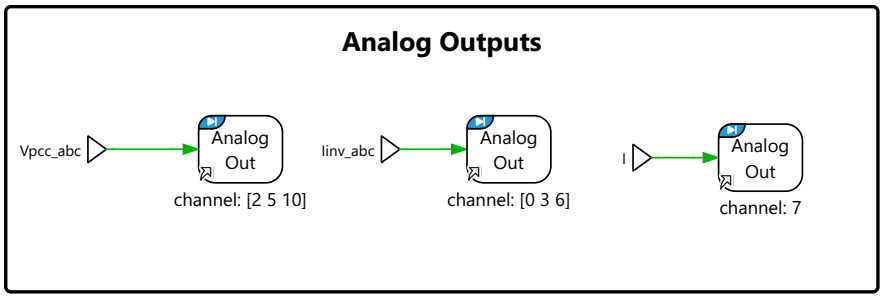



Figure 4.10: Analog outputs of the RT Box

## 4.4 Controller implementation

The general structure of the grid-forming controller is the same as the one depicted in Fig. 2.26a, which was used in the offline simulations. The Virtual Impedance limiter, is again used for the open-loop control, whereas the direct current limiters are used in combination with the Virtual Admittance inner-loop control.

Despite the general structure being the same, the control systems of the offline and real-time simulation have some differences. First, a low-pass filter with time constant $T_{fp}$ is used in the active and reactive power calculation, to filter out the high frequency noise caused by the harmonics. Additionally, unlike the offline simulation, the dynamic-model implementation of the virtual admittance loop shown in Fig. 2.12a, is used in the real-time simulation.

The implementation of the active power controller was slightly modified, as shown in Fig. 4.11. Specifically, a low-pass filter is used for the measured q-axis component of the PCC voltage, which was used for pre-synchronization purposes. Also, instead of the modulo operation used in offline simulations, the output of the integrator, which produces the reference angle of the GFMI, was wrapped within the range $0 - 2\pi$. This modification prevents the integrator output from continuously increasing, which could potentially create overflow issues during long real-time simulations.

***Microcontroller inputs***

As explained earlier, the measurements from the real-time simulation are supplied to the microcontroller, in order to be used by the implemented control systems. Figures 4.7 and 4.10 show that the RT Box provides the measurements for the three-phase voltages and currents, as well as the state of the PWM-enable switch. To obtain the PWM-enable state, the Digital Input block is used, as illustrated in Fig. 4.12. The selected microcontroller pin in the Digital In block

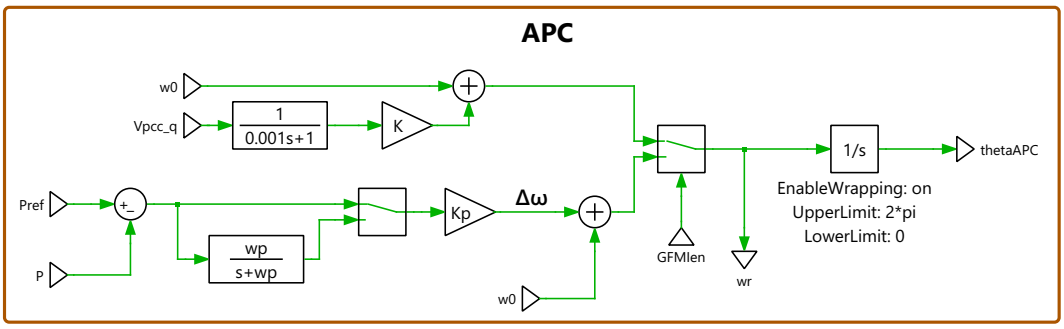



Figure 4.11: Implementation of the Active Power Controller for the real-time simulation

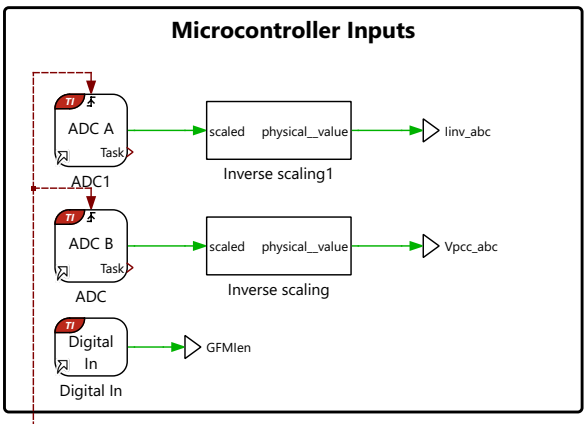



Figure 4.12: Inputs of the microcontroller

is the one that is connected to the PWM-enable state digital output of the RT Box, as described in [75]. This digital variable is then used to change the position of the pre-synchronization switch in the active power controller and to reset the current-controller integrators, in order to avoid windup when the PWM is disabled.

Additionally, it is seen from Fig. 4.12 that the three-phase PCC voltage and output current measurements are obtained using the ADC blocks. For these blocks, the appropriate input channels should be used, to match with the corresponding analog outputs of the RT Box. The connections between the RT Box analog outputs and the microcontroller ADC inputs, are listed in the LaunchPad Interface manual [75]. It is worth noting that the output of the ADC block contains the scaled measurement values from the RT Box analog outputs. Therefore, in order to use these measurements in the control systems, the offset is first removed and the result is then multiplied by the inverse of the scaling factor used.

***Microcontroller outputs***

Another major difference from the offline simulations, which was not previously mentioned, is that due to the use of the full switching model of the inverter, the voltage references provided by the grid-forming control system, are not fed to the ideal voltage source of the average model, but rather to the inverter modulation scheme.

The modulation of the inverter is performed using the PWM block. This block takes the modulation reference signals as input, compares them with the carrier signal and outputs the resulting switching pulses at the specified microcontroller pins, which should match with the corresponding digital inputs of the RT Box, according to [75]. It is known that, in order to obtain the modulation reference signals of the SPWM, the original voltage reference should be multiplied with a factor of $2/V_{dc}$. Additionally, because the carrier signals of the PWM block

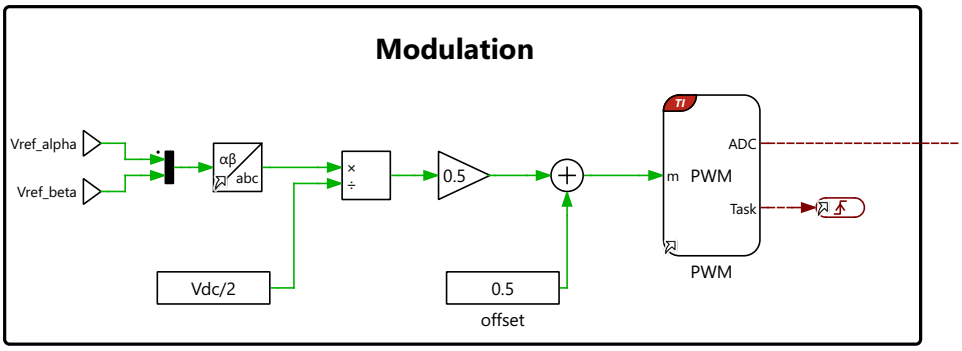



Figure 4.13: Sinusoidal pulse width modulation of the inverter

are in the range of $[0, 1]$ instead of $[-1, 1]$, the modulation references are multiplied with 0.5 and then shifted upward with an offset of 0.5, in order to align with the range of the carrier. Therefore, the implementation of the inverter modulation is depicted in Fig. 4.13.

## 4.5 Real-time simulation results

Finally, the implemented current-limiting methods are tested in real-time conditions, under a short circuit at the grid voltage for 200 msec and a 60° phase jump of the grid-voltage angle. The parameters of the system and the controller are listed in Table 4.1, where $T_s$ is the time-step for the RT Box, $T_{ctrl}$ is the microcontroller time-step, and $f_c$ is the frequency of the PWM carrier signal. For the real-time simulations, a small-scale system is used, in order to represent an experimental setup that can be built in the lab. Additionally, the droop-based active power controller was used in all the real-time simulations.

Table 4.1: System and control parameters

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $V_n$ | $10\sqrt{3}$ V | $k_p$ | $0.04\omega_0/P_{max}$ |
| $\omega_0$ | $100\pi$ rad/sec | $k_q$ | $0.1\hat{V}_n/Q_{max}$ |
| $S_N$ | 15 VA | $\omega_p$ | $2\pi \cdot 0.6$ rad/sec |
| $R_L$ | 1 Ω (0.05 pu) | $L_v$ | 0.3 pu |
| $X_L$ | 5 Ω (0.25 pu) | $R_v$ | 0.1 pu |
| $R_f$ | 0.3 Ω (0.015 pu) | $T_{fp}$ | 0.01 sec |
| $X_f$ | 3 Ω (0.15 pu) | $k_{pi}$ | 21.01 Ω |
| $R_{load}$ | 10 Ω (0.5 pu) | $k_{ii}$ | 660 Ω/s |
| $V_{dc}$ | 34 V | $I_{max}$ | 1.2 pu |
| $T_s$ | 10 μs | $I_{thres}$ | 1 pu |
| $f_c$ | 4 kHz | $K_{VI}$ | 1.09 |
| $T_{ctrl}$ | 0.25 msec | $\sigma$ | 3 |

The results of the real-time simulations for all implemented current-limiting methods are presented in Figures 4.14 and 4.15 for the short-circuit and phase-jump faults, respectively. More specifically, for each current limiter, the instantaneous values of the three-phase inverter output current, as well as its magnitude, are shown.

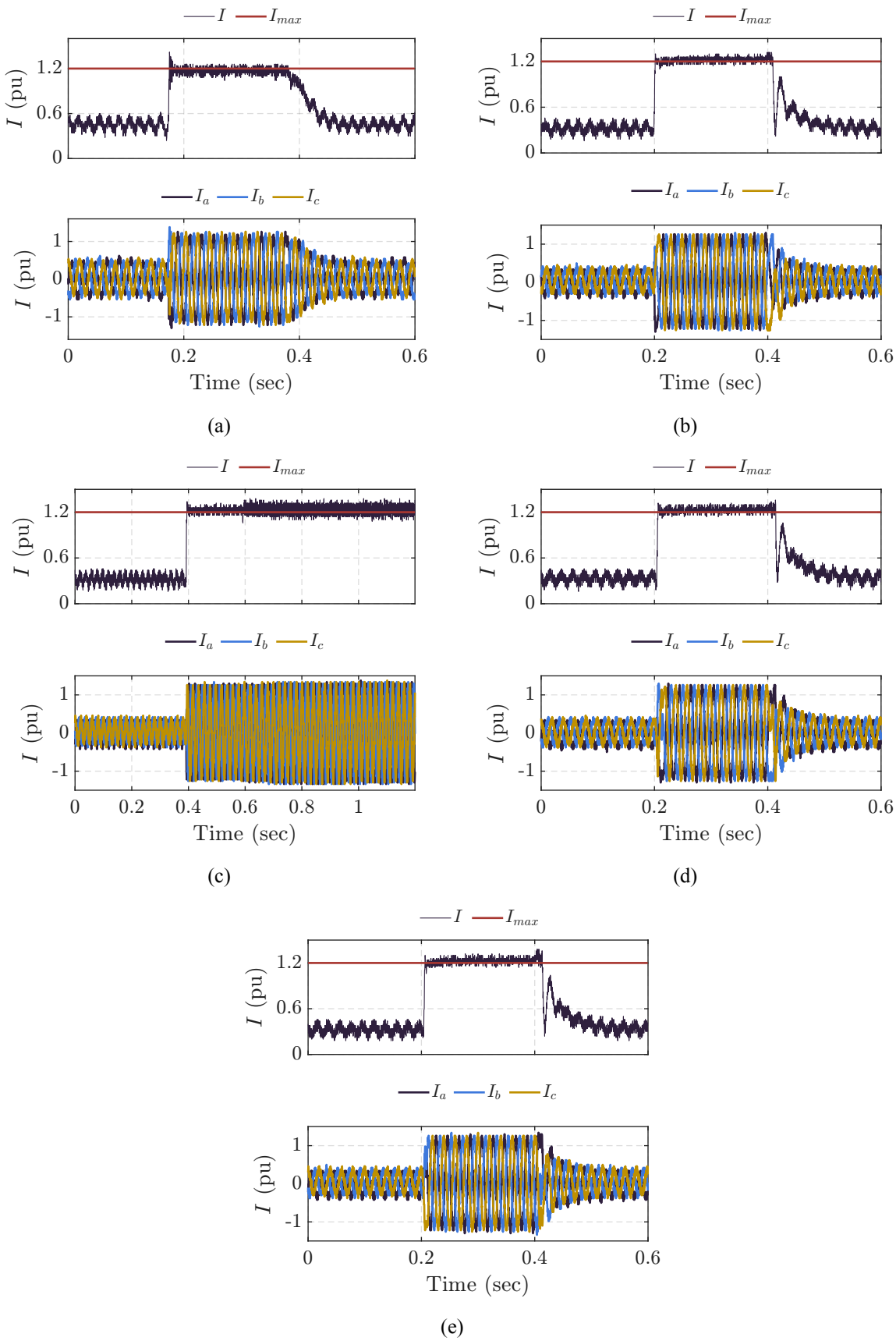



Figure 4.14: Real-time simulation results for a 200 msec short circuit at the grid voltage (a) Virtual impedance; (b) Magnitude limiter; (c) Fixed angle limiter; (d) d-axis priority limiter; (e) q-axis priority limiter

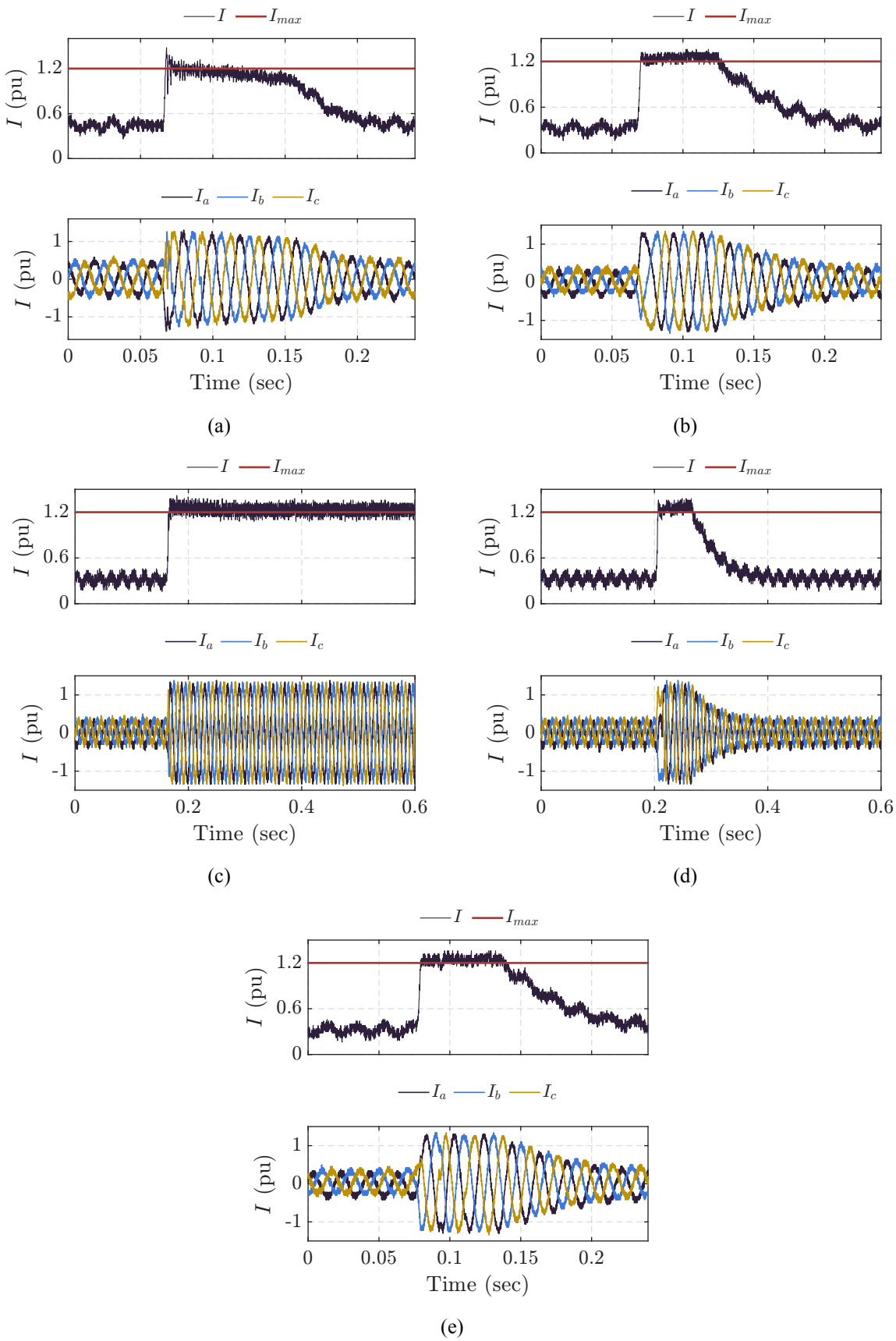



Figure 4.15: Real-time simulation results for a 60° phase jump of the grid voltage angle (a) Virtual impedance; (b) Magnitude limiter; (c) Fixed angle limiter; (d) d-axis priority limiter; (e) q-axis priority limiter

It can be observed that, for both types of disturbance, each current-limitation method effectively restricts the magnitude of the inverter output current. The noise which is observed in the resulting waveforms is caused by the high-frequency harmonic components. In the case of the fixed angle limiter, after the disturbances are cleared, the inverter remains in the current limiting operation mode, similar to the simulation results of Figures 3.12, 3.15 and 3.17. Nevertheless, even in this case, the magnitude of the inverter output current continues to be restricted. Furthermore, Figures 4.14a and 4.15a show that for both disturbances, a temporary overcurrent is observed when the virtual impedance limiter is used, which aligns with the results of the offline simulations.

The results of the real-time simulations indicate that in the event of a grid disturbance, the implemented current-limiting methods can effectively limit the output current of the grid-forming inverter, under real-time conditions.

# Chapter 5

# Conclusions and Future Work

## 5.1 Conclusions

Grid-forming inverters are controlled to behave as voltage sources. Therefore their output current is very sensitive to grid conditions, and in the case of severe disturbances, it may exceed the maximum permissible value, if no protective action is taken. To that end, overcurrent protection methods are essential to avoid damage to the converter hardware. When activated, current limiters override the normal operation, and thus, the dynamic behavior of a GFMI during and after disturbances is mainly determined by the employed method.

Despite the fact that multiple grid-forming control methods are proposed in the literature, the majority can be represented by a general control system, which consists of multiple layers and subsystems. Common implementations for the active power controller subsystem include the droop controller without and with low-pass filter and the Virtual Synchronous Generator. The droop controller without the low-pass filter exhibits first-order dynamics. Adding an LPF to the droop controller makes it equivalent to the VSG, both exhibiting second-order dynamics. Furthermore, although the droop controller does not provide virtual inertia, the addition of the low-pass filter introduces a virtual-inertia term, which is confirmed through simulations.

Current-limiting methods are classified into direct, indirect and hybrid methods. Direct methods adjust the references supplied to the current controller, while indirect methods reduce the voltage difference between the inverter and the PCC, adjust power set-points, or increase the equivalent output impedance. Hybrid methods use a combination of multiple direct and/or indirect methods. Several commonly used methods were implemented in the PLECS simulation software and their effectiveness was validated through time-domain simulations of voltage dips and phase jumps. However, when the virtual impedance method is used, which is an indirect method, the inverter cannot utilize its full overcurrent capability in the whole duration of the fault, and additionally temporary overcurrent can occur in the initial stage of the fault. In contrast, direct limiters can quickly and accurately limit the current, while making full use of the overcurrent capability.

The Virtual Power Angle (VPA) is used to assess the transient stability of GFMIs, through $P - \delta$ curves derived from large-signal models, which are different depending on the utilized current-limiting method. It is explained that the post-fault active power trajectory for a short circuit differs between inertial and non-inertial control, regardless of the applied current limiter. Additionally, the derived $P - \delta$ curves for the magnitude and fixed angle limiter show that current limitation significantly reduces the transient stability margin. Also, for the specific virtual-admittance parameters used, the magnitude limiter provides a higher transient stability

margin than the fixed angle limiter with $\phi_I = 0$. Furthermore, applying the EAC method to calculate the CCT of GFMIs during short circuits, yields conservative results compared with the numerical integration of the system dynamics. Time-domain simulations validate the derived large-signals models and the theoretical analysis.

Finally, a controller hardware-in-the-loop RT simulation is carried out, in order to assess the performance of the implemented current-limiting methods under real-time conditions. The control systems were implemented on a microcontroller, while the rest of the system was simulated on a real-time simulator. Real-time simulations were then performed for a short circuit and a phase jump of the grid voltage. The simulation results indicate that the implemented current limiters can effectively curtail the current under real-time conditions.

## 5.2 Future work

Some important topics that were not addressed in this work and can be considered as future work are presented below:

***Anti-windup schemes***: When the dual-loop vector voltage current control is used instead of the virtual-admittance loop, proper anti-windup schemes should be designed and implemented, in order to facilitate the successful fault recovery of the grid-forming inverter.

***Current-limiting techniques for unbalanced faults***: This work focused on current limitation for symmetrical disturbances. However the majority of power system faults are unbalanced and thus implementing current-limiting methods for unbalanced faults is of major importance.

***Current-limiting techniques for grid-forming MMCs***: This thesis only considers current limitation techniques for two-level grid-forming inverters. However, modular multilevel converters (MMCs) are the preferred choice for high-voltage, high-power applications. Therefore, the implementation of current-limiting methods for grid-forming MMCs, as well as the study of their effect on the internal dynamics of the MMC, is an important and interesting topic.

***Transient stability enhancement methods***: It has been identified that the use of current-limiting methods reduces the transient stability margin of grid-forming inverters. To that end, several methods that enhance the transient stability of the GFMI can be implemented and compared across various types of disturbances.

***Experimental validation of the implemented current-limiting methods***: It is important to validate the effectiveness of the implemented current-limitation techniques on a small-scale experimental system, since it further verifies the theoretical analysis and simulation results.

# Bibliography


[1] European Commission, "European climate law," Tech. Rep. Jun. 2021. [Online]. Available: https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32021R1119.

[2] D. B. Rathnayake et al., "Grid forming inverter modeling, control, and applications," *IEEE Access*, vol. 9, pp. 114 781–114 807, 2021. DOI: 10.1109/ACCESS.2021.3104617.

[3] G. Denis, T. Prevost, M.-S. Debry, F. Xavier, X. Guillaud, and A. Menze, "The migrate project: The challenges of operating a transmission grid with only inverter-based generation. a grid-forming control improvement with transient current-limiting control," *IET Renewable Power Generation*, vol. 12, no. 5, pp. 523–529, 2018.

[4] Y. Lin et al., "Research roadmap on grid-forming inverters," National Renewable Energy Laboratory, Golden, CO, Technical Report NREL/TP-5D00-73476, 2020, Accessed: 2025-08-06. [Online]. Available: https://www.nrel.gov/docs/fy21osti/73476.pdf.

[5] N. Baeckeland, "Design and modeling of inverter control for fault behavior and power system protection analysis," Ph.D. dissertation, KU Leuven, 2022.

[6] B. Kroposki et al., "Achieving a 100% renewable grid: Operating electric power systems with extremely high levels of variable renewable energy," *IEEE Power and energy magazine*, vol. 15, no. 2, pp. 61–73, 2017.

[7] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid converters for photovoltaic and wind power systems*. John Wiley & Sons, 2011.

[8] A. Antonopoulos, "On the internal dynamics and ac-motor drive application of modular multilevel converters," Ph.D. dissertation, KTH Royal Institute of Technology, 2014.

[9] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, control, and application of modular multilevel converters for HVDC transmission systems*. John Wiley & Sons, 2016.

[10] Y. Lamrani, F. Colas, T. Van Cutsem, C. Cardozo, T. Prevost, and X. Guillaud, "On the stabilizing contribution of different grid-forming controls to power systems," *IET Generation, Transmission & Distribution*, vol. 18, no. 23, pp. 3863–3877, 2024. DOI: https://doi.org/10.1049/gtd2.13269. eprint: https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/gtd2.13269. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/gtd2.13269.

[11] S. Du, A. Dekka, B. Wu, and N. Zargari, *Modular multilevel converters: analysis, control, and applications*. John Wiley & Sons, 2017.

[12] R. Rosso, X. Wang, M. Liserre, X. Lu, and S. Engelken, "Grid-forming converters: Control approaches, grid-synchronization, and future trends—a review," *IEEE Open Journal of Industry Applications*, vol. 2, pp. 93–109, 2021. DOI: 10.1109/OJIA.2021.3074028.

[13] VDN, "TransmissionCode-2007. Network and System Rules of the German Transmission System Operators," Tech. Rep., Aug. 2007.

[14] C. Cardozo et al., "Promises and challenges of grid forming: Transmission system operator, manufacturer and academic view points," *Electric Power Systems Research*, vol. 235, p. 110 855, 2024, ISSN: 0378-7796. DOI: https://doi.org/10.1016/j.epsr.2024.110855. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0378779624007417.

[15] T. Qoria, "Grid-forming control to achieve a 100% power electronics interfaced power transmission systems," Ph.D. dissertation, HESAM Université, 2020.

[16] B. Bahrani et al., "Grid-forming inverter-based resource research landscape: Understanding the key assets for renewable-rich power systems," *IEEE Power and Energy Magazine*, vol. 22, no. 2, pp. 18–29, 2024. DOI: 10.1109/MPE.2023.3343338.

[17] L. Harnefors, M. Bongiorno, and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3323–3334, 2007. DOI: 10.1109/TIE.2007.904022.

[18] B. Wen, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Shen, "Analysis of d-q small-signal impedance of grid-tied inverters," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 675–687, 2016. DOI: 10.1109/TPEL.2015.2398192.

[19] A. Johnson, "Minimum specification required for provision of gb grid forming (gbgf) capability (formerly virtual synchronous machine/vsm capability)," *Nat. Grid ESO, Warwick, UK, Final Modification Rep. GC*, vol. 137, 2021.

[20] AEMO, "Voluntary specification for grid-forming inverters," *Australian Energy Market Operator (AEMO), Melbourne*, 2023.

[21] J. Fang, J. Liu, H. Wu, J. Chen, and F. Blaabjerg, *Grid-Forming Converters: Principles, Control, and Applications in Modern Power Systems*. Elsevier, 2024.

[22] NERC, *White paper: Grid forming functional specifications for bps-connected battery energy storage systems*, 2023.

[23] L. Zhang, L. Harnefors, and H.-P. Nee, "Power-synchronization control of grid-connected voltage-source converters," *IEEE Transactions on Power Systems*, vol. 25, no. 2, pp. 809–820, 2010. DOI: 10.1109/TPWRS.2009.2032231.

[24] Y. Liao, X. Wang, F. Liu, K. Xin, and Y. Liu, "Sub-synchronous control interaction in grid-forming vscs with droop control," in *2019 4th IEEE Workshop on the Electronic Grid (eGRID)*, 2019, pp. 1–6. DOI: 10.1109/eGRID48402.2019.9092640.

[25] X. Wang, M. G. Taul, H. Wu, Y. Liao, F. Blaabjerg, and L. Harnefors, "Grid-synchronization stability of converter-based resources—an overview," *IEEE Open Journal of Industry Applications*, vol. 1, pp. 115–134, 2020. DOI: 10.1109/OJIA.2020.3020392.

[26] A. Johnson, *GC0100-Fast Fault Current Injection, Fault Ride Through and Banding*, 2017.

[27] B. Fan, T. Liu, F. Zhao, H. Wu, and X. Wang, "A review of current-limiting control of grid-forming inverters under symmetrical disturbances," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 955–969, 2022. DOI: 10.1109/OJPEL.2022.3227507.

[28] N. Baeckeland, D. Chatterjee, M. Lu, B. Johnson, and G.-S. Seo, "Overcurrent limiting in grid-forming inverters: A comprehensive review and discussion," *IEEE Transactions on Power Electronics*, vol. 39, no. 11, pp. 14 493–14 517, 2024. DOI: 10.1109/TPEL.2024.3430316.

[29] "Fault-Ride Through Performance Analysis of Grid Forming Inverter-Based Resources," Electric Power Research Institute (EPRI), Palo Alto, CA, Tech. Rep. 3002029578, 2024.

[30] F. Zhao, X. Wang, H. Wu, Y. Wu, T. Zhu, and Y. Sun, "Reactive current profile of grid-forming wind power plant under symmetrical faults," in *22nd Wind and Solar Integration Workshop (WIW 2023)*, vol. 2023, 2023, pp. 498–504. DOI: 10.1049/icp.2023.2779.

[31] T. Qoria, F. Gruson, F. Colas, G. Denis, T. Prevost, and X. Guillaud, "Critical clearing time determination and enhancement of grid-forming converters embedding virtual impedance as current limitation algorithm," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1050–1061, 2020. DOI: 10.1109/JESTPE.2019.2959085.

[32] E. Rokrok, T. Qoria, A. Bruyere, B. Francois, and X. Guillaud, "Transient stability assessment and enhancement of grid-forming converters embedding current reference saturation as current limiting strategy," *IEEE Transactions on Power Systems*, vol. 37, no. 2, pp. 1519–1531, 2022. DOI: 10.1109/TPWRS.2021.3107959.

[33] M. Chandorkar, D. Divan, and R. Adapa, "Control of parallel connected inverters in standalone ac supply systems," *IEEE Transactions on Industry Applications*, vol. 29, no. 1, pp. 136–143, 1993. DOI: 10.1109/28.195899.

[34] C. Schöll and H. Lens, "Design- and simulation-based comparison of grid-forming converter control concepts," in *20th International Workshop on Large-Scale Integration of Wind Power into Power Systems as well as on Transmission Networks for Offshore Wind Power Plants (WIW 2021)*, 2021, pp. 310–316. DOI: 10.1049/icp.2021.2630.

[35] J. Driesen and K. Visscher, "Virtual synchronous generators," in *2008 IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century*, 2008, pp. 1–3. DOI: 10.1109/PES.2008.4596800.

[36] S. D'Arco and J. A. Suul, "Virtual synchronous machines — classification of implementations and analysis of equivalence to droop controllers for microgrids," in *2013 IEEE Grenoble Conference*, 2013, pp. 1–7. DOI: 10.1109/PTC.2013.6652456.

[37] D. Pan, X. Wang, F. Liu, and R. Shi, "Transient stability of voltage-source converters with grid-forming control: A design-oriented study," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1019–1033, 2020. DOI: 10.1109/JESTPE.2019.2946310.

[38] S. D'Arco and J. A. Suul, "Equivalence of virtual synchronous machines and frequency-droops for converter-based microgrids," *IEEE Transactions on Smart Grid*, vol. 5, no. 1, pp. 394–395, 2014. DOI: 10.1109/TSG.2013.2288000.

[39] B. B. Johnson, S. V. Dhople, A. O. Hamadeh, and P. T. Krein, "Synchronization of parallel single-phase inverters with virtual oscillator control," *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 6124–6138, 2014. DOI: 10.1109/TPEL.2013.2296292.

[40] L. Huang et al., “A virtual synchronous control for voltage-source converters utilizing dynamics of dc-link capacitor to realize self-synchronization,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1565–1577, 2017. DOI: 10.1109/JESTPE.2017.2740424.

[41] C. Li, R. Burgos, I. Cvetkovic, D. Boroyevich, L. Mili, and P. Rodriguez, “Analysis and design of virtual synchronous machine based statcom controller,” in *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2014, pp. 1–6. DOI: 10.1109/COMPEL.2014.6877134.

[42] D. Remon, A. M. Cantarellas, E. Rakhshani, I. Candela, and P. Rodriguez, “An active power synchronization control loop for grid-connected converters,” in *2014 IEEE PES General Meeting | Conference & Exposition*, 2014, pp. 1–5. DOI: 10.1109/PESGM.2014.6939250.

[43] M. Ndreko, S. Rüberg, and W. Winter, “Grid forming control for stable power systems with up to 100% inverter based generation: A paradigm scenario using the ieee 118-bus system,” in *Proceedings of the 17th International Wind Integration Workshop, Stockholm, Sweden*, 2018, pp. 16–18.

[44] R. Rosso, X. Wang, M. Liserre, X. Lu, and S. Engelken, “Grid-forming converters: An overview of control approaches and future trends,” in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 4292–4299. DOI: 10.1109/ECCE44975.2020.9236211.

[45] W. Du et al., “A comparative study of two widely used grid-forming droop controls on microgrid small-signal stability,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 963–975, 2020. DOI: 10.1109/JESTPE.2019.2942491.

[46] P. Rodriguez, I. Candela, C. Citro, J. Rocabert, and A. Luna, “Control of grid-connected power converters based on a virtual admittance control loop,” in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10. DOI: 10.1109/EPE.2013.6634621.

[47] P. Rodriguez, I. Candela, and A. Luna, “Control of pv generation systems using the synchronous power controller,” in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 993–998. DOI: 10.1109/ECCE.2013.6646811.

[48] Y. Zhang, C. Zhang, R. Yang, M. Molinas, and X. Cai, “Current-constrained power-angle characterization method for transient stability analysis of grid-forming voltage source converters,” *IEEE Transactions on Energy Conversion*, vol. 38, no. 2, pp. 1338–1349, 2023. DOI: 10.1109/TEC.2023.3236620.

[49] O. Mo, S. D’Arco, and J. A. Suul, “Evaluation of virtual synchronous machines with dynamic or quasi-stationary machine models,” *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5952–5962, 2017. DOI: 10.1109/TIE.2016.2638810.

[50] Y. Hirase, K. Abe, K. Sugimoto, and Y. Shindo, “A grid-connected inverter with virtual synchronous generator model of algebraic type,” *Electrical Engineering in Japan*, vol. 184, no. 4, pp. 10–21, 2013.

[51] B. Fan and X. Wang, “Current-limiting control of grid-forming inverters: State-of-the-art and open issues,” *Authorea Preprints*, 2022.

[52] N. Bottrell and T. C. Green, "Comparison of current-limiting strategies during fault ride-through of inverters to prevent latch-up and wind-up," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3786–3797, 2014. DOI: 10.1109/TPEL.2013.2279162.

[53] I. Sadeghkhani, M. E. Hamedani Golshan, J. M. Guerrero, and A. Mehrizi-Sani, "A current limiting strategy to improve fault ride-through of inverter interfaced autonomous microgrids," *IEEE Transactions on Smart Grid*, vol. 8, no. 5, pp. 2138–2148, 2017. DOI: 10.1109/TSG.2016.2517201.

[54] L. Huang, H. Xin, Z. Wang, L. Zhang, K. Wu, and J. Hu, "Transient stability analysis and control design of droop-controlled voltage source converters considering current limitation," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 578–591, 2019. DOI: 10.1109/TSG.2017.2749259.

[55] T. Qoria, F. Gruson, F. Colas, X. Kestelyn, and X. Guillaud, "Current limiting algorithms and transient stability analysis of grid-forming VSCs," *Electric Power Systems Research*, vol. 189, p. 106 726, 2020, ISSN: 0378-7796. DOI: https://doi.org/10.1016/j.epsr.2020.106726. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0378779620305290.

[56] B. Fan and X. Wang, "Fault recovery analysis of grid-forming inverters with priority-based current limiters," *IEEE Transactions on Power Systems*, vol. 38, no. 6, pp. 5102–5112, 2023. DOI: 10.1109/TPWRS.2022.3221209.

[57] A. D. Paquette and D. M. Divan, "Virtual impedance current limiting for inverters in microgrids with synchronous generators," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1630–1638, 2015. DOI: 10.1109/TIA.2014.2345877.

[58] A. Gkountaras, S. Dieckerhoff, and T. Sezi, "Evaluation of current limiting methods for grid forming inverters in medium voltage microgrids," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 1223–1230. DOI: 10.1109/ECCE.2015.7309831.

[59] N. Baeckeland and G.-S. Seo, "Novel hybrid current limiter for grid-forming inverter control during unbalanced faults," in *2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia)*, 2023, pp. 1517–1522. DOI: 10.23919/ICPE2023-ECCEAsia54778.2023.10213960.

[60] R. Rosso, S. Engelken, and M. Liserre, "On The Implementation of an FRT Strategy for Grid-Forming Converters Under Symmetrical and Asymmetrical Grid Faults," *IEEE Transactions on Industry Applications*, vol. 57, no. 5, pp. 4385–4397, 2021. DOI: 10.1109/TIA.2021.3095025.

[61] J. M. Bloemink and M. R. Iravani, "Control of a multiple source microgrid with built-in islanding detection and current limiting," *IEEE Transactions on Power Delivery*, vol. 27, no. 4, pp. 2122–2132, 2012. DOI: 10.1109/TPWRD.2012.2198497.

[62] M. G. Taul, X. Wang, P. Davari, and F. Blaabjerg, "Current limiting control with enhanced dynamics of grid-forming converters during fault conditions," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1062–1073, 2020. DOI: 10.1109/JESTPE.2019.2931477.

[63] T. Wijnhoven, J. Tant, and G. Deconinck, "Inverter modelling techniques for protection studies," in *2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2012, pp. 187–194. DOI: 10.1109/PEDG.2012.6253999.

[64] Y. Laba, A. Bruyère, F. Colas, and X. Guillaud, "Virtual power-based technique for enhancing the large voltage disturbance stability of hv grid-forming converters," in *2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe)*, 2023, pp. 1–8. DOI: 10.23919/EPE23ECCEEurope58414.2023.10264486.

[65] T. Liu, X. Wang, F. Liu, K. Xin, and Y. Liu, "A current limiting method for single-loop voltage-magnitude controlled grid-forming converters during symmetrical faults," *IEEE Transactions on Power Electronics*, vol. 37, no. 4, pp. 4751–4763, 2022. DOI: 10.1109/TPEL.2021.3122744.

[66] H. Wu and X. Wang, "Design-oriented transient stability analysis of grid-connected converters with power synchronization control," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 8, pp. 6473–6482, 2019. DOI: 10.1109/TIE.2018.2875669.

[67] D. Chatterjee, B. Johnson, and G.-S. Seo, "Is equal area criterion applicable for transient stability assessment of grid-forming inverters?" *Authorea Preprints*, 2025.

[68] S. Jiang, Y. Zhu, and G. Konstantinou, "Transient behavior of grid-forming converters during phase jumps," in *2025 IEEE 16th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2025, pp. 162–167. DOI: 10.1109/PEDG62294.2025.11060291.

[69] X. Guillaud et al., "Applications of real-time simulation technologies in power and energy systems," *IEEE Power and Energy Technology Systems Journal*, vol. 2, no. 3, pp. 103–115, 2015. DOI: 10.1109/JPETS.2015.2445296.

[70] J. Bélanger, P. Venne, J.-N. Paquin, et al., "The what, where and why of real-time simulation," *Planet Rt*, vol. 1, no. 1, pp. 25–29, 2010.

[71] M. D. Omar Faruque et al., "Real-time simulation technologies for power systems design, testing, and analysis," *IEEE Power and Energy Technology Systems Journal*, vol. 2, no. 2, pp. 63–73, 2015. DOI: 10.1109/JPETS.2015.2427370.

[72] Plexim, *RT Box 1*, https://www.plexim.com/products/rt_box/rt_box_1, [Online].

[73] Texas Instruments, *LAUNCHXL-F28379D*, https://www.ti.com/tool/LAUNCHXL-F28379D, [Online].

[74] Plexim, *TI C2000 Target Support User Manual, Version 1.10*. [Online]. Available: https://www.plexim.com/sites/default/files/c2000manual.pdf.

[75] Plexim, *RT Box LaunchPad Interface*. [Online]. Available: https://www.plexim.com/sites/default/files/launchpadinterfacemanual.pdf.