National Technical University of Athens
School of Electrical and Computer Engineering
Division of Information Transmission Systems
and Material Technology

Design and Manufacturing of an RF Power Amplifier for linear accelerators

Diploma Thesis

Panagiotis Vlachos

Supervisor: Athanasios Panagopoulos,
Professor, National Technical University of Athens

Athens, October, 2025

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Approved by the three-member scientific committee on the 20 October 2025

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Περίληψη

Η Ευρωπαϊκή Πηγή Σκέδασης Νετρονίων (ESS) είναι μια διεπιστημονική ερευνητική εγκατάσταση που κατασκευάζεται στο Λουντ της Σουηδίας και θα είναι ο πιο ισχυρός γραμμικός επιταχυντής πρωτονίων που έχει κατασκευαστεί ποτέ όταν ολοκληρωθεί η κατασκευή. Παρόλο που το ESS θα συμβάλει σημαντικά στη μελλοντική έρευνα, η εγκατάσταση θα είναι ένας μεγάλος καταναλωτής ενέργειας με σημαντικό περιβαλλοντικό αντίκτυπο. Επομένως, πραγματοποιούνται περιβαλλοντικά βιώσιμες εξελίξεις με στόχο την υιοθέτηση βελτιωμένων ενεργειακά αποδοτικών προσεγγίσεων. Ένα παράδειγμα αυτής της προσέγγισης θα είναι το νέο σύστημα που θα εφαρμοστεί για την τροφοδοσία 26 κοιλοτήτων spoke. Οι κοιλότητες Spoke είναι το πρώτο στάδιο της υπεραγώγιμης επιτάχυνσης στον γραμμικό επιταχυντή (LINAC) του ESS, αποτελούμενοι από 26 διπλές κοιλότητες spoke, με απαίτηση ισχύος 400kW ανά θάλαμο για να λειτουργήσουν. Το νέο σύστημα είναι ένας Ενισχυτής Ισχύος Στερεάς Κατάστασης (SSPA) που θα αντικαταστήσει τους ενισχυτές τετρόδου λόγω της υψηλής κατανάλωσης ισχύος τους.

Αυτή η διπλωματική εργασία επικεντρώνεται στον σχεδιασμό, προσομοίωση και κατασκευή ενός Ενισχυτή Στερεάς Κατάστασης (SSPA) ειδικά προσαρμοσμένου ώστε να λειτουργεί ως το πρώτο στάδιο του οδηγού μέσα στο σύστημα των 400kW SSPA που θα εγκατασταθεί για να τροφοδοτεί τις υπεραγώγιμες διπλές κοιλότητες spoke στην Ευρωπαϊκή Πηγή Σκέδασης Νετρονίων. Αυτή η μελέτη ξεκινά με μια εις βάθος ανάλυση των απαιτήσεων του συστήματος και των λειτουργικών παραμέτρων ολόκληρου του συστήματος, εντοπίζοντας βασικές μετρικές απόδοσης όπως η ισχύς εξόδου, η γραμμικότητα και η αποδοτικότητα. Μέσα από εντατική προσομοίωση και βελτιστοποίηση με τη χρήση λογισμικών εργαλείων (Advanced Design System (ADS) και Altium Designer), αναπτύσσεται μια αρχιτεκτονική SSPA, ικανή να ικανοποιήσει τις αυστηρές προδιαγραφές που απαιτεί η εφαρμογή ενώ μετριάζει ζητήματα όπως η αρμονική παραμόρφωση και η απαγωγή ισχύος. Ιδιαίτερη προσοχή δίνεται στην επιλογή και ολοκλήρωση τρανζίστορ, δικτύων προσαρμογής εμπέδησης και συστημάτων ψύξης ώστε να διασφαλιστεί η βέλτιστη λειτουργικότητα και μακροζωία υπό μεταβαλλόμενες συνθήκες λειτουργίας. Επιπλέον, πραγματοποιείται πειραματική επικύρωση του σχεδιασμένου πρωτοτύπου SSPA, η οποία περιλαμβάνει ολοκληρωμένες δοκιμές και χαρακτηρισμό σε όλο το εύρος λειτουργίας. Οι μετρικές απόδοσης, συμπεριλαμβανομένων της ισχύος εξόδου, της αποδοτικότητας, της απόκρισης συχνότητας και της γραμμικότητας, αξιολογούνται διεξοδικά, αποδεικνύοντας την αποτελεσματικότητα και αξιοπιστία του προτεινόμενου σχεδιασμού.

Λέξεις Κλειδιά: Γραμμικός Επιταχυντής, ESS, Στερεά Κατάσταση, Ενισχυτής Ισχύος , ραδιοσυχνότητα , spoke κοιλότητα, διάταξη τυπωμένου κυκλώματος, κατασκευή, μετρήσεις, LDMOS, μικροταινία, πυρηνική φυσική

Abstract

The European Spallation Source (ESS) is a multidisciplinary research facility that is being built in Lund, Sweden and is the most powerful linear proton accelerator ever built. Even though ESS will contribute greatly to the future research, the facility will be a large power consumer with significant environmental impact. Therefore, environmentally- sustainable developments are undertaken towards the adoption of energy savings and improved energy-efficient approaches. One example of that approach will be the new system that will be implemented to power 26 spoke cavities. The Spoke cavities are the first stage of superconducting acceleration at the ESS linear accelerator (LINAC), consisted of 26 double spoke cavities, with 400kW power per cavity requirement to operate. The new system is a Solid-State Power Amplifier (SSPA) that will replace the tetrode amplifiers due to their high-power consumption.

This thesis focuses on designing, simulating and manufacturing a Solid-State Power Amplifier (SSPA) tailored specifically to serve as the first stage of the driver within the 400kW SSPA system that will be installed to power the superconducting double spoke cavities at European Spallation Source. This study begins with an in-depth analysis of the system requirements and operational parameters of the entire system, identifying key performance metrics such as output power, linearity and efficiency. Through rigorous simulation and optimization using software tools (Advanced Design System (ADS) and Altium Designer), a robust SSPA architecture is developed, capable of meeting the stringent specifications demanded by the application while mitigating issues such as harmonic distortion and power dissipation. Special attention is given to the selection and integration of high-power transistors, impedance matching networks, and cooling systems to ensure optimal functionality and longevity under varying operating conditions. Furthermore, experimental validation of the designed SSPA prototype is conducted, involving comprehensive testing and characterization across the entire operational range. Performance metrics including output power, efficiency, frequency response, and linearity are thoroughly evaluated, demonstrating the efficacy and reliability of the proposed design.

Key Words: Linear Accelerator, ESS, Solid-State, Power Amplifier, Radio Frequency, spoke cavities, layout, manufacturing, measurements, LDMOS, microstrip, nuclear physics

"Every great and deep difficulty bears in itself its own solution.
It forces us to change our thinking in order to find it."

Niels Bohr

"Life can only be understood backwards;
but it must be lived forwards."

Søren Kierkegaard

Acknowledgements

With this thesis, I complete my five-year studies at the School of Electrical and Computer Engineering of the National Technical University of Athens. These years form the foundation of my life from this point onward. The person I have become during this time, not only academically, but also personally, is shaped by scientific thinking and perseverance. These studies will remain the solid ground upon which I will continue to build, nurture, and cultivate future opportunities and a life of fulfillment and happiness.

I would first like to express my sincere gratitude to Professor Athanasios Panagopoulos, my thesis advisor, for his continuous guidance, trust, and the numerous discussions we had throughout his courses. His teaching reflects his genuine dedication to cultivating engineers with critical thinking skills and a strong foundation of knowledge. Through his instruction, together with that of Emeritus Professor Panagiotis Cottis, I became truly fascinated by the field of telecommunications engineering and was able to find my academic identity. Attending their lectures was always something I looked forward to and deeply enjoyed. I will always be grateful for having been their student.

I would also like to thank the other members of my thesis committee, Professor Hercules Avramopoulos and Assistant Professor Dimitrios Apostolopoulos, for their support during the preparation of this thesis and for the valuable knowledge I gained through their courses.

Special thanks are due to the RF Sources Group at the European Spallation Source (ESS) for offering me the opportunity to work in such an inspiring and challenging environment. I would particularly like to thank Morten Jensen, RF Group Leader, for his supportive and guiding role, Bruno Lagoguez, RF Engineer, for our collaboration and valuable discussions; and Slavisa Micic, Electronics Engineer, for the technical insights and the many laughs we shared while soldering. My sincere appreciation also goes to all the other members of the RF group who made my stay at ESS both educational and memorable.

My time in Lund, Sweden, played a decisive role in my development as both an engineer and a person. I am deeply thankful to Emmanouil Trachanas, Accelerator Electrical Engineer, for his support during my stay in Sweden and for stepping up as a true role model, a source of professionalism, integrity, and kindness that continues to inspire me.

To my family, thank you for your support, patience, and belief in me throughout these years. To my grandmother, whose dream of studying nuclear physics continues to live through me, this work is as much yours as it is mine.

Finally, I wish to warmly thank my friends and all those I met during my academic years for their friendship, laughter, and shared experiences, as well as everyone I encountered in Lund and at ESS, the place where my life, both personal and scientific, truly began.

Panagiotis Vlachos
Athens, October 2025

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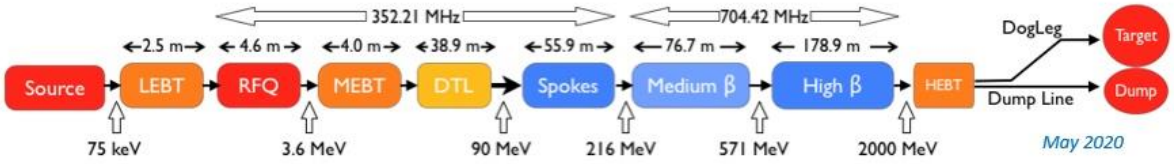
Εκτενή Περίληψη στα Ελληνικά/ Extensive Summary in Greek

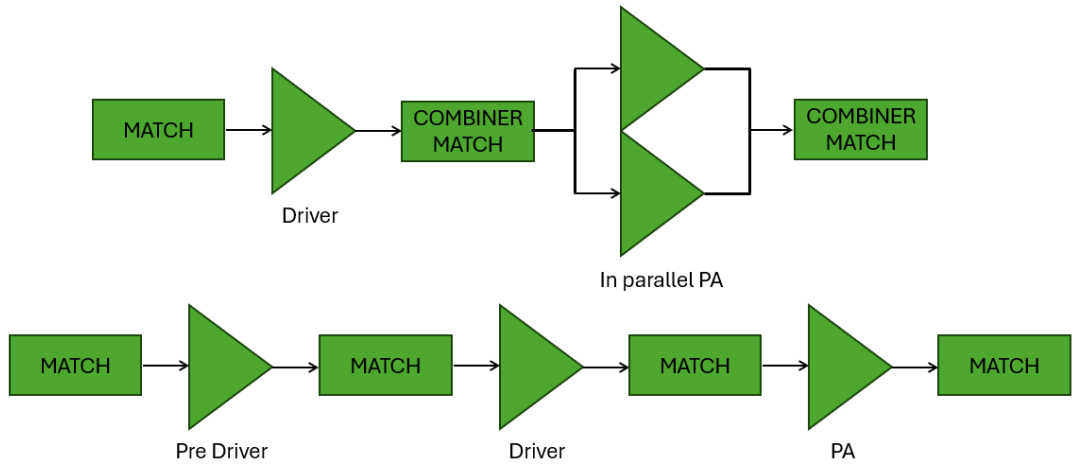
Οι επιταχυντές σωματιδίων αποτελούν θεμελιώδη εργαλεία της σύγχρονης επιστήμης και τεχνολογίας. Πρόκειται για συστήματα ικανά να επιταχύνουν φορτισμένα σωματίδια σε υψηλές ταχύτητες, χρησιμοποιώντας ηλεκτρικά και μαγνητικά πεδία. Σήμερα υπάρχουν χιλιάδες επιταχυντές σε λειτουργία παγκοσμίως, οι οποίοι βρίσκουν εφαρμογή σε ένα ευρύ φάσμα πεδίων: από τη βασική έρευνα στη φυσική υψηλών ενεργειών και την πυρηνική φυσική, έως την ιατρική απεικόνιση και θεραπεία, τη βιομηχανία και τις τεχνολογίες υλικών. Η παρούσα διπλωματική εργασία που υποβλήθηκε στην Σχολή Ηλεκτρολόγων Μηχανικών και Μηχανικών Υπολογιστών του Εθνικού Μετσόβιου Πολυτεχνείου εκπονήθηκε με βάση την εργασία του συγγραφέα στο European Spallation Source (ESS) το διάστημα Μάρτιος 2024-Αύγουστος 2024. Το European Spallation Source ή Ευρωπαϊκή Πηγή Θρυμματισμού θα αποτελέσει τον ισχυρότερο του είδους επιταχυντή όταν ολοκληρωθεί η κατασκευή του. Πρόκειται για να έναν γραμμικό επιταχυντή όπου πρωτόνια μέσω ηλεκτρομαγνητικών πεδίων επιταχύνονται και συγκρούονται με έναν στόχο μόλυβδου, με τα σκεδαζόμενα νετρόνια έπειτα να συλλέγονται και να χρησιμοποιούνται για τα ποικίλα πειράματα που στεγάζει το ερευνητικό κέντρο.



Το σχηματικό διάγραμμα του γραμμικού επιταχυντή του ESS, Μάιος 2020

Σε αυτό το διάστημα η ομάδα των πηγών ραδιοσυχνοτήτων διενεργούσε συνεργασία με το πανεπιστήμιο Uppsala University (UU) για την διερεύνηση εναλλακτικών πηγών τροφοδότησης των spoke κοιλοτήτων του γραμμικού επιταχυντή. Το ESS θα αποτελέσει κόμβο ανάπτυξης και έρευνας για την Ευρώπη, έχοντας όμως μεγάλες ενεργειακές ανάγκες. Αποφασίστηκε να διερευνηθούν εναλλακτικοί τρόποι τροφοδότησής που μπορούν να αντικαταστήσουν τις υπάρχουσες λύσεις με άλλες αποδοτικότερες. Επιλέχθηκε να χρησιμοποιηθεί η τεχνολογία ενισχυτών ισχύος στερεάς κατάστασης καθώς συνδυάζουν υψηλή αποδοτικότητα που κυμαίνεται στο διάστημα 50 με 80 % σε χαμηλές ανάγκες τροφοδοσίας. Συγκεκριμένα, για να καλυφθούν οι ενεργειακές ανάγκες των spoke κοιλοτήτων, για κάθε μια από αυτές θα κατασκευαστεί είναι σύστημα ενισχυτών ισχύος στερεάς κατάστασης (SSPA) με ισχύ εξόδου 400kW. Η υπάρχουσα λύση ήταν οι ενισχυτές τετρόδων, με αποδοτικότητα περίπου στο 50%. Ένας ακόμα λόγος για την στροφή στην τεχνολογία στερεάς κατάστασης είναι πως γενικότερα η τεχνολογία στις μικροκυματικές συχνότητες στρέφεται προς εκείνη την κατεύθυνση. Καθώς το πλάνο του ESS είναι λειτουργία για τουλάχιστον 40 χρόνια είναι αναγκαίο να έχουν βρεθεί λύσεις που θα επιτρέπουν την ομαλή λειτουργία του επιταχυντή με τεχνολογίες που εξελίσσονται παράλληλα στην αγορά.

Το πρώτο κεφάλαιο της διπλωματικής έχοντας εισάγει τον αναγνώστη στο εγχείρημα για βελτίωση της ενεργειακής απόδοσης του ESS, παραθέτει και αναλύει την λύση που επιλέχθηκε. Συγκεκριμένα, η τοπολογία θα αποτελείται από πολλά παράλληλα και σε σειρά στάδια ενίσχυσης με συνεχή επίβλεψη της διαδικασίας από εξωτερικά συστήματα για να διασφαλιστεί η ομαλή λειτουργία.

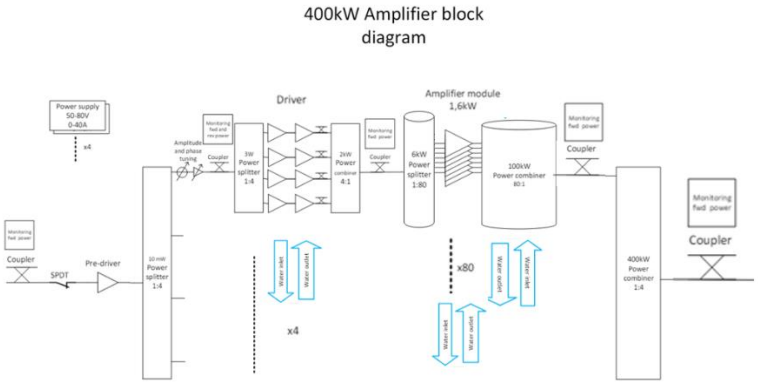


Τοπολογίες ενισχυτών ισχύος

Σκοπός της διπλωματικής αυτής είναι ο σχεδιασμός και η κατασκευή ενός ενισχυτή ισχύος όπου θα λειτουργεί ως πρώτο στάδιο του οδηγού σε αυτή την αλυσίδα με τις εξής προδιαγραφές: 352,21 MHz συχνότητα λειτουργίας, αποδοτικότητα μεγαλύτερη από 50% και ισχύς εξόδου 50W. Μέσω αυτής της εργασίας δίνεται η δυνατότητα να παρεισφρήσει ο συγγραφέας στον κόσμο της σχεδίασης ραδιοσυχνοτήτων όπου αναζητείται ο ιδανικός συμβιβασμός ανάμεσα στα βασικά χαρακτηριστικά ενός ενισχυτή: θόρυβος, ισχύς, συχνότητα, κέρδος, τάση τροφοδοσίας και γραμμικότητα.

Στο δεύτερο κεφάλαιο παρατίθεται το απαραίτητο θεωρητικό υπόβαθρο ώστε να γίνουν αντιληπτά τα βήματα που ακολουθήθηκαν για την σχεδίαση.

Στο τρίτο κεφάλαιο αναλύεται το σύστημα SSPA των 400 kW, το οποίο προορίζεται για την τροφοδότηση των 26 spoke κοιλοτήτων του γραμμικού επιταχυντή (LINAC) του ESS, καθεμία εκ των οποίων απαιτεί ισχύ 400 kW στα 352.21 MHz. Παρουσιάζεται η αρχιτεκτονική του συστήματος, οι λόγοι επιλογής της συγκεκριμένης τοπολογίας, καθώς και η λειτουργία και επιλογή των επιμέρους υποσυστημάτων και εξαρτημάτων. Επιπλέον, παρουσιάζεται η συμβολή του συγγραφέα στη διαμόρφωση του καταλόγου υλικών Bill of Materials και στην ανάλυση κόστους του συστήματος, με τις τιμές να αντιστοιχούν στον Απρίλιο του 2024.



Το μπλοκ διάγραμμα της τοπολογίας 400kW SSPA

Η τοπολογία του συστήματος αποτελείται από πέντε διαδοχικά στάδια ενίσχυσης: προενισχυτή, ρυθμιστή πλάτους και φάσης, 1ο στάδιο οδηγού, 2ο στάδιο οδηγού και κύριο ενισχυτή ισχύος, τα οποία λειτουργούν σε παράλληλη διάταξη με πολλούς ενισχυτές για λόγους αξιοπιστίας και βελτιστοποίησης της εξόδου. Καθ' όλη τη διαδρομή του σήματος, κατευθυντικοί συζεύκτες παρέχουν πληροφορίες για την κατάσταση λειτουργίας, επιτρέποντας την παρακολούθηση και προστασία του συστήματος. Το στάδιο εισόδου περιλαμβάνει έναν συζεύκτη για την παρακολούθηση της ισχύος εισόδου, έναν διακόπτη τύπου SPDT για προστασία από υπερφόρτωση, έναν προενισχυτή και έναν διαχωριστή ισχύος 1:4. Σκοπός του είναι η αρχική ενίσχυση του σήματος από 1 mW σε 10 mW και η διανομή του σε τέσσερα παράλληλα κανάλια.

Το στάδιο οδηγού αποτελεί το κύριο αντικείμενο της διπλωματικής εργασίας. Αποτελείται από ρυθμιστή πλάτους, ρυθμιστή φάσης, διαιρέτη 1:4, το πρώτο και δεύτερο στάδιο ενίσχυσης του οδηγού, καθώς και έναν συνδυαστή ισχύος 4:1. Τρεις κατευθυντικοί συζεύκτες τοποθετούνται σε καίρια σημεία για έλεγχο της ενίσχυσης και ανίχνευση πιθανών απωλειών. Η χρήση ρυθμιστών πλάτους και φάσης εξασφαλίζει την ορθή προσαρμογή του ηλεκτρομαγνητικού κύματος και την αποφυγή σπινθηρισμών ή αστοχιών κατά τη λειτουργία. Το κύριο στάδιο ενίσχυσης είναι το τελευταίο και ισχυρότερο τμήμα της αλυσίδας, υπεύθυνο για τη μεγιστοποίηση της συνολικής παραγόμενης ισχύος. Οι διαιρέτες και συνδυαστές ισχύος του σταδίου αυτού έχουν σχεδιαστεί από το Πανεπιστήμιο της Ουψάλας, καθώς δεν διατίθενται αντίστοιχα εμπορικά εξαρτήματα που να καλύπτουν αυτά τα επίπεδα ισχύος. Το στάδιο εξόδου περιλαμβάνει τέσσερις συζεύκτες για την παρακολούθηση της ισχύος κάθε κύριου ενισχυτή και έναν τελικό συνδυαστή 4×100 kW. Ένας ισχυρός τελικός συζεύκτης τοποθετείται πριν από την κοιλότητα για την παρακολούθηση και προστασία έναντι τόξων.

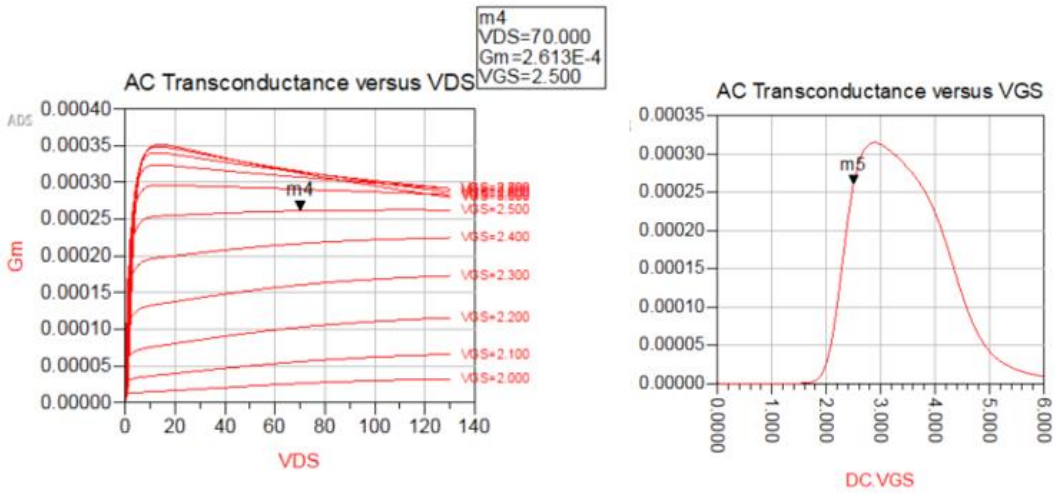
Παράλληλα, εξετάζονται τα συστήματα παρακολούθησης, τα συστήματα ψύξης, καθώς και το υποστηρικτικό υλικό του συστήματος. Οι πληροφορίες από τους συζεύκτες επεξεργάζονται από τα συστήματα παρακολούθησης που αναπτύσσει η ομάδα RF Sources, ενώ η απαγωγή θερμότητας επιτυγχάνεται μέσω του υδρόψυκτου συστήματος του εργαστηρίου RF. Το υποστηρικτικό υλικό περιλαμβάνει συνδετήρες τύπου N, πυκνωτές προστασίας, ικριώματα και καλωδιώσεις. Τέλος, παρουσιάζεται αναλυτικά ο Πίνακας Υλικών (BoM), ο οποίος καταρτίστηκε ώστε να εκτιμηθεί το συνολικό κόστος του έργου (534.024,79 €), να οργανωθούν τα δεδομένα της αρχιτεκτονικής και να αποκτηθεί βαθύτερη κατανόηση των RF εξαρτημάτων και των τεχνικών προδιαγραφών τους.

Στο τέταρτο κεφάλαιο αναλύεται διεξοδικά η διαδικασία σχεδίασης του πρώτου σταδίου του οδηγού του ενισχυτή στερεάς κατάστασης (SSPA) των 400 kW. Στόχος του σταδίου είναι η ενίσχυση του σήματος εισόδου στα απαραίτητα επίπεδα ισχύος ώστε να οδηγήσει με ασφάλεια τα επόμενα στάδια της αλυσίδας ενίσχυσης. Η διαδικασία περιλαμβάνει την επιλογή κατάλληλου τρανζίστορ, τη βελτιστοποίηση των τάσεων πόλωσης, τη διαμόρφωση των κυκλωμάτων πόλωσης, καθώς και τη διερεύνηση της ιδανικής εμπέδησης εισόδου και εξόδου που θα παρουσιαστεί στον ενισχυτή, αλλά και της σταθερότητας του ενισχυτή μέσω προσομοιώσεων μικρού και μεγάλου σήματος στο λογισμικό Advanced Design System (ADS) της Keysight.

Η πρώτη φάση του σχεδιασμού αφορά την επιλογή της κατάλληλης τεχνολογίας τρανζίστορ. Μελετήθηκαν οι διαθέσιμες ημιαγώγιμες τεχνολογίες, βάσει της σχέσης συχνό-

τητας λειτουργίας και παραγόμενης ισχύος. Μετά από σύγκριση, επιλέχθηκε η τεχνολογία LDMOS (Laterally Diffused Metal Oxide Semiconductor/ Πλευρικά Διάχυτος Ημιαγωγός Οξειδίου Μετάλλου), η οποία προσφέρει εξαιρετική γραμμικότητα, υψηλή απόδοση και ανθεκτικότητα σε θερμικές και ηλεκτρικές καταπονήσεις. Επιπλέον, είναι η πλέον ώριμη τεχνολογία για εφαρμογές υψηλής ισχύος στην περιοχή των VHF και UHF, καλύπτοντας πλήρως τη συχνότητα λειτουργίας των 352.21 MHz του επιταχυντή ESS. Ως ενεργό στοιχείο επιλέχθηκε το τρανζίστορ ART35FE της εταιρείας Ampleon. Η επιλογή αυτή έγινε λόγω της υψηλής απόδοσης, του μεγάλου περιθωρίου λειτουργίας σε υψηλές θερμοκρασίες και τάσεις, και της εγγυημένης μακροχρόνιας διαθεσιμότητας, στοιχείο κρίσιμο για βιομηχανικά και ερευνητικά έργα μεγάλης διάρκειας όπως το ESS. Το τρανζίστορ διαθέτει ονομαστική ισχύ εξόδου 35 W, τυπικό κέρδος 30 dB και αποδοτικότητα 70% στα 108 MHz, γεγονός που το καθιστά ιδανικό για χρήση ως πρώτο στάδιο οδηγού, πριν το κύριο στάδιο ισχύος που χρησιμοποιεί το μεγαλύτερο τρανζίστορ ART2K0FEG της ίδιας εταιρείας. Η συνδυασμένη χρήση αυτών των δύο τρανζίστορ εξασφαλίζει βέλτιστη μεταφορά ισχύος μεταξύ των σταδίων και υψηλή συνολική αποδοτικότητα.

Αφού επιλέχθηκε το ενεργό στοιχείο, η επόμενη φάση του σχεδιασμού ήταν η βελτιστοποίηση των τάσεων πόλωσης. Για τον σκοπό αυτό πραγματοποιήθηκαν DC προσομοιώσεις στο περιβάλλον του ADS, προκειμένου να καθοριστεί το σημείο λειτουργίας που προσφέρει τον καλύτερο συμβιβασμό μεταξύ ισχύος εξόδου, αποδοτικότητας και θερμικής σταθερότητας.



Αποτελέσματα προσομοιώσεων για εξάρτηση της διαγωγιμότητας με την τάση του drain και του gate

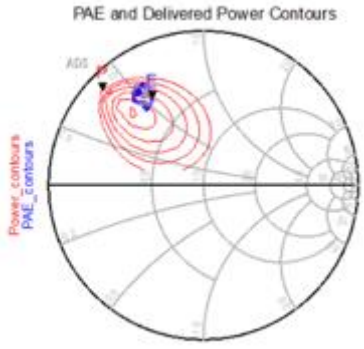
Από τις προσομοιώσεις του ρεύματος ως συνάρτηση της τάσης πύλης (ID–VGS) προέκυψε ότι η αγωγιμότητα του τρανζίστορ ξεκινά γύρω στα 2 Volt, ενώ η μέγιστη διαγωγιμότητας επιτυγχάνεται κοντά στα 2.9 Volt. Με βάση αυτά τα αποτελέσματα επιλέχθηκε τάση πόλωσης πύλης VGS = 2.5 V, τιμή που εξασφαλίζει λειτουργία στη γραμμική περιοχή με επαρκή περιθώριο για διακυμάνσεις. Στη συνέχεια πραγματοποιήθηκε ανάλυση της χαρακτηριστικής καμπύλης ID–VDS, προκειμένου να καθοριστεί η τάση drain. Μελετώντας τις καμπύλες φόρτου και τα αντίστοιχα σημεία λειτουργίας για διαφορετικές τιμές τάσης, επιλέχθηκε VDS = 70 V. Η τιμή αυτή υπερβαίνει ελαφρώς την ονομαστική τάση του τρανζίστορ

(65 V), αλλά γίνεται εκμετάλλευση της αυξημένη ανθεκτικότητα της σειράς ART και επιτρέποντας τη μέγιστη δυνατή ισχύ εξόδου. Οι προσομοιώσεις έδειξαν ότι με αυτές τις συνθήκες το τρανζίστορ λειτουργεί στην τάξη AB, επιτυγχάνοντας αποδοτικότητα περίπου 54% και ισχύ εξόδου γύρω στα 53 W. Η συγκεκριμένη τάξη λειτουργίας προσφέρει έναν βέλτιστο συνδυασμό αποδοτικότητας και γραμμικότητας, καθώς το τρανζίστορ άγει για περισσότερο από τη μισή περίοδο του σήματος.

Αφού καθορίστηκαν τα σημεία πόλωσης, το επόμενο βήμα ήταν η σχεδίαση των κυκλωμάτων πόλωσης. Σκοπός τους είναι η σταθερή τροφοδοσία του τρανζίστορ με συνεχές ρεύμα χωρίς να επηρεάζεται η ραδιοσυχνότητα του σήματος. Τα κυκλώματα αυτά αποτελούνται από πυκνωτές αποσύζευξης, πυκνωτές σύζευξης και πηνία RF choke. Οι πυκνωτές αποσύζευξης συνδέονται παράλληλα με τις γραμμές τροφοδοσίας ώστε να "γείωνουν" κάθε ανεπιθύμητο AC σήμα, εξασφαλίζοντας σταθερή πόλωση και αποφυγή ταλαντώσεων. Η συμπεριφορά τους εξαρτάται έντονα από τη συχνότητα συντονισμού και την εσωτερική τους αντίσταση, γι' αυτό χρησιμοποιείται συνδυασμός πυκνωτών διαφορετικών τιμών για τη βελτίωση της απόκρισης γύρω από τα 352 MHz. Οι πυκνωτές σύζευξης, αντίστοιχα, επιτρέπουν τη διέλευση της RF ισχύος ενώ απομονώνουν τα DC κυκλώματα των σταδίων μεταξύ τους. Ιδιαίτερη σημασία δόθηκε και στην επιλογή των RF chokes, που εμποδίζουν τη διέλευση της RF ισχύος προς την πηγή τροφοδοσίας επιτρέποντας παράλληλα την απρόσκοπτη διέλευση του DC ρεύματος. Στην είσοδο του κυκλώματος χρησιμοποιήθηκε αντίσταση υψηλής τιμής αντί για πηνίο, δεδομένου ότι το ρεύμα πύλης είναι πρακτικά μηδενικό. Αντίθετα, στην έξοδο απαιτείται επαγωγικό στοιχείο υψηλής ποιότητας και αντοχής, καθώς το ρεύμα που διαρρέει το τρανζίστορ φθάνει σε επίπεδα αρκετών αμπέρ. Η επιλογή του κατάλληλου πηνίου βασίστηκε στην ανάλυση του συντελεστή ποιότητας, της μέγιστης τιμής RMS ρεύματος και της συχνότητας συντονισμού, ώστε να εξασφαλιστεί σταθερή συμπεριφορά στην περιοχή λειτουργίας.

Για να επιβεβαιωθεί η θερμική και ηλεκτρική ανθεκτικότητα του σχεδιασμού, πραγματοποιήθηκαν επιπλέον υπολογισμοί βασισμένοι στο εργαλείο αξιολόγησης της Ampleon. Οι υπολογισμοί απέδειξαν ότι για τις επιλεγμένες συνθήκες λειτουργίας (VDS = 70 V, ID ≈ 1 A) ο μέσος χρόνος αστοχίας του τρανζίστορ υπερβαίνει τα 18 έτη, ενώ η μέγιστη θερμοκρασία σύνδεσης φθάνει στους 99°C, τιμές που επιβεβαιώνουν τη βιωσιμότητα του σχεδιασμού με την προϋπόθεση ύπαρξης επαρκούς συστήματος ψύξης.

Στη συνέχεια πραγματοποιήθηκαν load-pull προσομοιώσεις, μία από τις σημαντικότερες διαδικασίες στο σχεδιασμό ενισχυτών ισχύος.



Το διάγραμμα Smith με τις γραφικές της PAE και της ισχύος εξόδου του ενισχυτή

Οι προσομοιώσεις αυτές επιτρέπουν την εύρεση των βέλτιστων τιμών εισόδου και εξόδου σύνθετης αντίστασης που μεγιστοποιούν την αποδοτικότητα και την ισχύ εξόδου. Με τη χρήση του εργαλείου load-pull του ADS, σαρώθηκαν οι αντιστάσεις εισόδου και εξόδου και παρατηρήθηκαν τα αντίστοιχα περιγράμματα ισχύος και απόδοσης πάνω στο διάγραμμα Smith. Με αυτόν τον τρόπο προσδιορίστηκαν οι τιμές αντιστάσεων που παρουσιάζουν στο τρανζίστορ τη βέλτιστη φόρτιση για τις επιθυμητές επιδόσεις.

Η τελική φάση του σχεδιασμού περιλαμβάνει τη μελέτη σταθερότητας του ενισχυτή. Εξετάστηκε τόσο η σταθερότητα μικρού σήματος όσο και η σταθερότητα μεγάλου σήματος. Στην πρώτη περίπτωση, πραγματοποιήθηκε προσομοίωση S-παραμέτρων για χαμηλή ισχύ εισόδου, προκειμένου να διασφαλιστεί ότι ο ενισχυτής δεν θα ταλαντώνει. Η ανάλυση έδειξε ότι οι καμπύλες σταθερότητας καλύπτουν ολόκληρη την περιοχή του διαγράμματος Smith, ενώ ο παράγοντας Rollet (K-factor) υπερβαίνει τη μονάδα, υποδεικνύοντας άνευ όρων σταθερότητα. Για τη δεύτερη περίπτωση, πραγματοποιήθηκε προσομοίωση μεγάλης ισχύος με ανάλυση αρμονικής ισορροπίας, ώστε να επιβεβαιωθεί η σταθερότητα ακόμη και σε συνθήκες κορεσμού. Οι υπολογισμοί των παραμέτρων Κ και Δ, καθώς και των παραγόντων σταθερότητας πηγής και φορτίου μ, επιβεβαίωσαν ότι ο ενισχυτής παραμένει σταθερός σε όλο το εύρος λειτουργίας.

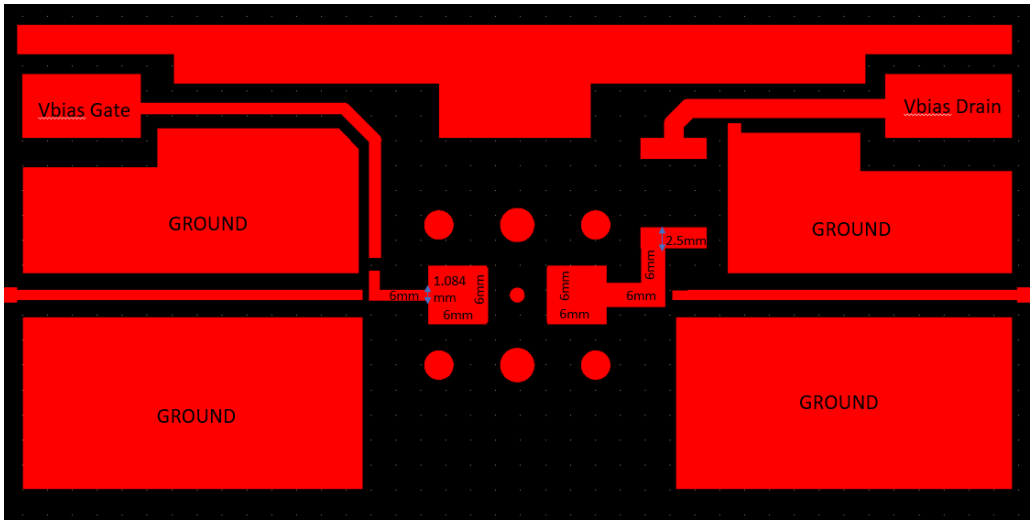
Στο πέμπτο κεφάλαιο αναλύεται διεξοδικά η διαδικασία σχεδίασης της διάταξης του ενισχυτή. Η ανάπτυξη της διάταξης, που ολοκληρώθηκε στο Altium Designer, αποτελεί κρίσιμο στάδιο της συνολικής σχεδίασης, καθώς καθορίζει την ηλεκτρική συμπεριφορά, τη θερμική σταθερότητα και την αξιοπιστία του κυκλώματος. Τα βασικά βήματα που ακολουθήθηκαν είναι η επιλογή του υλικού του υποστρώματος, η επιλογή της τεχνολογίας γραμμών μεταφοράς, ο σχεδιασμός των δικτύων προσαρμογής, η ανάπτυξη του συστήματος ψύξης και, τέλος, η προσομοίωση της τελικής διάταξης στο λογισμικό ADS.

Η διαδικασία ξεκινά με την επιλογή του κατάλληλου υλικού για το υπόστρωμα του κυκλώματος. Η επιλογή αυτή επηρεάζει καθοριστικά την απόδοση, τη θερμική συμπεριφορά και τη σταθερότητα της συχνότητας. Το υλικό που επιλέχθηκε είναι το RO3210 της Rogers Corporation, ένα κεραμικά ενισχυμένο υλικό ειδικά σχεδιασμένο για εφαρμογές υψηλών συχνοτήτων. Η υψηλή διηλεκτρική του σταθερά (10.8) επιτρέπει τη σχεδίαση πολύ συμπαγών κυκλωμάτων, κάτι που είναι κρίσιμο, καθώς στο σύστημα του ESS θα κατασκευαστούν δεκαέξι ενισχυτές του πρώτου σταδίου οδηγού και ο διαθέσιμος χώρος στον θάλαμο είναι περιορισμένος. Παράλληλα, ο χαμηλός συντελεστής απωλειών του (0.0027) εξασφαλίζει ελάχιστες απώλειες ισχύος, συμβάλλοντας στη συνολική ενεργειακή αποδοτικότητα του SSPA. Εξίσου σημαντικό ρόλο παίζει η θερμική συμπεριφορά του υλικού. Ο θερμικός συντελεστής της διηλεκτρικής σταθεράς (-459 ppm/°C) σημαίνει ότι το υλικό παρουσιάζει μικρή μεταβολή των ηλεκτρικών χαρακτηριστικών με τη θερμοκρασία, γεγονός ιδιαίτερα σημαντικό σε εφαρμογές υψηλής ισχύος όπου το θερμικό φορτίο είναι σημαντικό. Η θερμική αγωγιμότητα 0.81 W/m/K επιτρέπει την αποτελεσματική διάχυση της παραγόμενης θερμότητας, ενώ σε συνδυασμό με το σύστημα ψύξης που θα αναλυθεί παρακάτω, εξασφαλίζει τη σταθερή λειτουργία του ενισχυτή.

Αφού καθορίστηκε το υλικό του PCB, ακολούθησε η επιλογή της τεχνολογίας γραμμών μεταφοράς. Εξετάστηκαν οι τρεις κύριες τεχνολογίες, μικροταινιακή γραμμή, η ενδο-

στρωματική ταινιογραμμή και ο συνεπίπεδος κυματοδηγός. Η τεχνολογία μικροταινίας προσφέρει απλότητα κατασκευής και ευκολία πρόσβασης στα επιφανειακά εξαρτήματα, ενώ ο συνεπίπεδος κυματοδηγός προσφέρει καλύτερο έλεγχο της εμπέδησης και βελτιωμένη θερμική διαχείριση, καθώς οι γειτονικές γειώσεις συμβάλλουν στη διάχυση θερμότητας. Η ενδοστρωματική ταινιογραμμή, αν και εξαιρετικά αποδοτική ως προς την απομόνωση, απαιτεί πολυστρωματικά PCB και είναι πιο δύσκολη στην κατασκευή. Έτσι, επιλέχθηκε συνδυασμός μικροταινιακής γραμμής και ενδοστρωματικής ταινιογραμμής, επιτυγχάνοντας τον βέλτιστο συμβιβασμό μεταξύ ευκολίας κατασκευής, ακρίβειας εμπέδησης και απόδοσης.

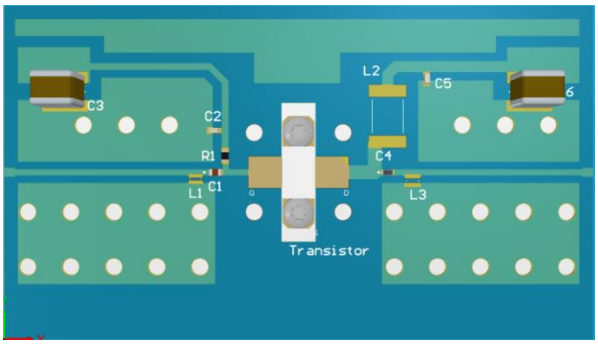
Για τη γραμμή μεταφοράς σχεδιάστηκαν οι διαστάσεις ώστε να διατηρείται χαρακτηριστική εμπέδηση 50 Ω, κάτι απαραίτητο για την ελαχιστοποίηση ανακλάσεων και απωλειών. Το πλάτος των ιχνών καθορίστηκε με βάση τη διηλεκτρική σταθερά και το πάχος του υποστρώματος, ενώ πραγματοποιήθηκαν προσομοιώσεις στο ADS για να επιβεβαιωθεί η σωστή εμπέδηση. Ιδιαίτερη μέριμνα δόθηκε στην ικανότητα των αγωγών να χειρίζονται τα αναμενόμενα ρεύματα λειτουργίας. Για το σημείο σύνδεσης του τρανζίστορ με το πηνίο RF choke, όπου το ρεύμα αγγίζει τα 4 A, η γραμμή μεταφοράς σχεδιάστηκε με πλάτος 2.2 mm ώστε να αποτρέπονται απώλειες λόγω φαινομένου επιδερμικού βάθους και υπερθέρμανσης. Η τοποθέτηση του τρανζίστορ στην πλακέτα αποτέλεσε κρίσιμο στάδιο, καθώς επηρεάζει τόσο τη μηχανική σταθερότητα όσο και τη θερμική αγωγιμότητα. Το τρανζίστορ τοποθετείται επιφανειακά και απαιτείται εξαιρετικά ακριβής προσαρμογή των επιφανειών σύνδεσης (pad) της πύλης και της αποχέτευσης. Οι διαστάσεις των pad καθορίστηκαν ώστε να εξασφαλίζουν βέλτιστη μεταφορά ισχύος και θερμική επαφή. Επιπλέον, λόγω των μηχανικών τάσεων που δημιουργούνται κατά τη λειτουργία, προτάθηκαν δύο λύσεις στήριξης: άμεση κόλληση του τρανζίστορ πάνω στο PCB ή χρήση 3D εκτυπωμένων υποστηρικτικών μπλοκ από PLA που ασκούν ομοιόμορφη πίεση στα pad, εξασφαλίζοντας σταθερή επαφή. Η δεύτερη λύση επιτρέπει την ευκολότερη επαναχρησιμοποίηση του τρανζίστορ σε επόμενες δοκιμές, μειώνοντας το κόστος. Στη συνέχεια, ενσωματώθηκαν οι RF συνδέσεις τύπου N, απαραίτητες για τη σύνδεση του ενισχυτή με το υπόλοιπο σύστημα μέσω ομοαξονικών καλωδίων. Η μηχανική τους τοποθέτηση υπολογίστηκε με ακρίβεια, ώστε να διασφαλιστεί ηλεκτρική συνέχεια, σωστή εμπέδηση 50 Ω και μηχανική σταθερότητα.



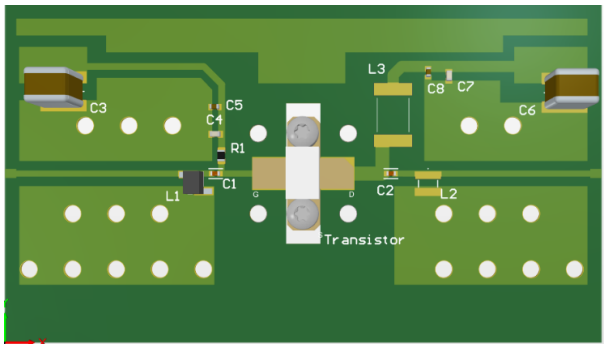
Η διάταξη των στρωμάτων χαλκού όπως σχεδιάστηκε στο Altium

Το επόμενο στάδιο ήταν ο σχεδιασμός των δικτύων προσαρμογής (matching networks). Στόχος τους είναι η βελτιστοποίηση της μεταφοράς ισχύος μεταξύ του τρανζίστορ και των υπολοίπων σταδίων του κυκλώματος, παρουσιάζοντας στα άκρα του τρανζίστορ τη συζυγή εμπέδηση των θυρών του. Οι τιμές των βέλτιστων εμπεδήσεων προήλθαν από τις load-pull προσομοιώσεις του προηγούμενου κεφαλαίου. Ο σχεδιασμός ξεκίνησε με απλές διατάξεις συνδυασμού μικροταινιακών γραμμών και διακριτών εξαρτημάτων (πηνίων και πυκνωτών) και εξελίχθηκε μέσω επαναλαμβανόμενων βελτιώσεων.

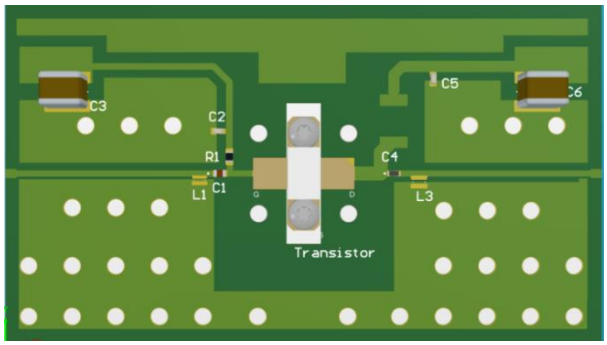
Στην πρώτη έκδοση, ο ενισχυτής παρήγαγε την επιθυμητή ισχύ μόνο στο θεωρητικό μοντέλο, καθώς ο προσομοιωτής του τρανζίστορ ξεκινούσε 0.7 mm εντός του σώματος του εξαρτήματος, με αποτέλεσμα να μην επιτυγχάνεται σωστή προσαρμογή. Μετά από επικοινωνία με τον κατασκευαστή και διόρθωση του μοντέλου, η δεύτερη έκδοση παρουσίασε ικανοποιητική προσαρμογή και σταθερή συμπεριφορά. Ακολούθησαν τρεις ακόμη βελτιώσεις. Στην τρίτη έκδοση, οι αιχμηρές γωνίες των ιχνών στρογγυλοποιήθηκαν για να μειωθεί η πυκνότητα ρεύματος και οι απώλειες, ενώ οι επίπεδες γειώσεις συνδέθηκαν για την αποφυγή βρόχων γείωσης. Στην τέταρτη έκδοση, η υπερθέρμανση του πυκνωτή σύζευξης αντιμετωπίστηκε με χρήση μεγαλύτερου εξαρτήματος και τροποποίηση των αποστάσεων των στοιχείων. Τέλος, στην πέμπτη έκδοση, το δίκτυο εξόδου απλοποιήθηκε με μια ευρύτερη επιφάνεια σύνδεσης και μικρότερη απόσταση εξαρτημάτων, μειώνοντας τις απώλειες και τη θερμική φόρτιση.



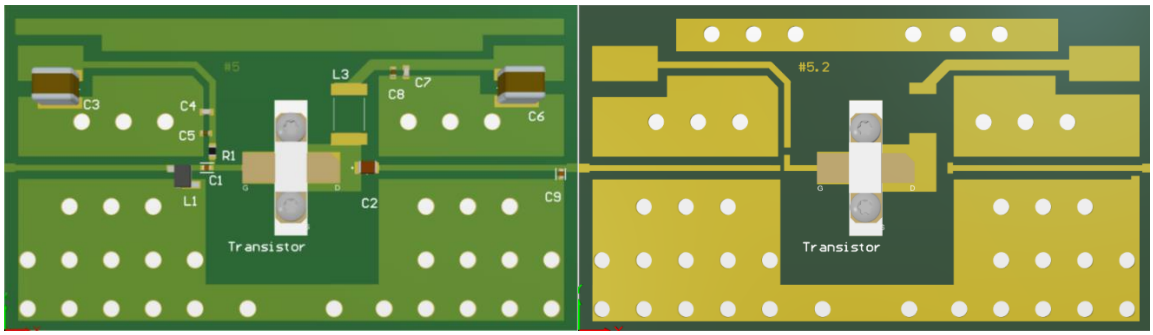
1η έκδοση



2η έκδοση

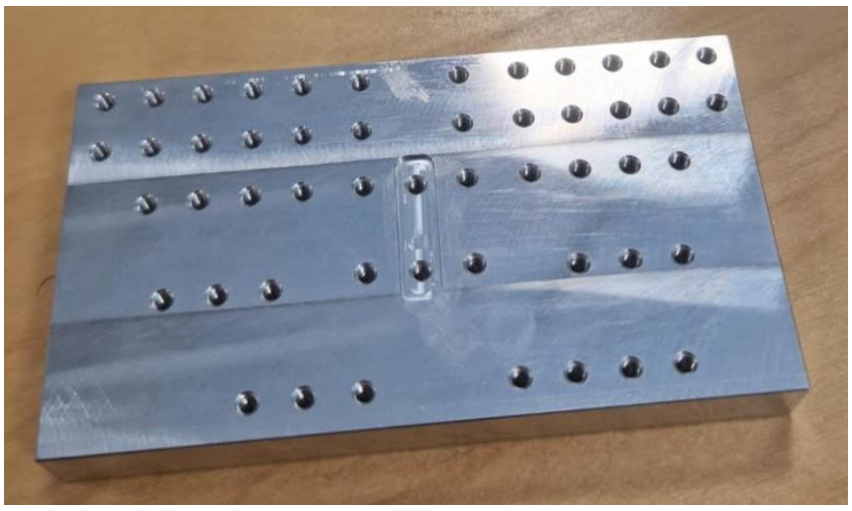


3η και 4η έκδοση



5η και 5.2 έκδοση

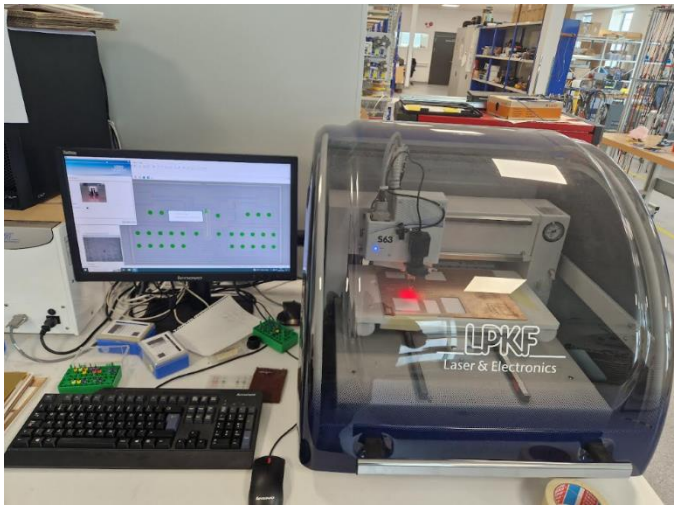
Αφού ολοκληρώθηκε η ηλεκτρική σχεδίαση, ακολούθησε ο μηχανικός σχεδιασμός του συστήματος ψύξης. Ο ενισχυτής λειτουργεί σε συνθήκες υψηλής ισχύος, συνεπώς η θερμική διαχείριση είναι καθοριστική. Το heatsink σχεδιάστηκε από αλουμίνιο διαστάσεων 60×106 mm, με πλήθος οπών για βίδες M3, ώστε να επιτρέπει την ασφαλή στήριξη του PCB, του τρανζίστορ και των υποστηρικτικών μπλοκ. Στο σημείο τοποθέτησης του τρανζίστορ έχει διαμορφωθεί εσοχή, ώστε το εξάρτημα να έρχεται σε πλήρη επαφή με το αλουμίνιο, το οποίο λειτουργεί τόσο ως μηχανική βάση όσο και ως επίπεδο γείωσης. Η συγκεκριμένη διάταξη βελτιώνει σημαντικά τη μεταφορά θερμότητας, επιτρέποντας τη σταθερή λειτουργία ακόμη και σε παρατεταμένη χρήση.



Το heatsink

Το τελικό στάδιο της διαδικασίας περιλαμβάνει την προσομοίωση της διάταξης στο ADS, με χρήση ρεαλιστικών μοντέλων για όλα τα εξαρτήματα. Οι προσομοιώσεις πραγματοποιήθηκαν τόσο σε επίπεδο συχνότητας όσο και σε επίπεδο ισχύος. Τα αποτελέσματα έδειξαν ότι για ισχύ εισόδου 20 dBm ο ενισχυτής αποδίδει ισχύ εξόδου 50 W, επιτυγχάνοντας απόδοση 64%. Οι αρμονικές παραμορφώσεις παραμένουν σε αποδεκτά επίπεδα, ενώ οι παράμετροι S έδειξαν σταθερότητα και καλή προσαρμογή στο εύρος λειτουργίας. Ο υπολογισμός του παράγοντα σταθερότητας K έδωσε τιμή 1.136, αποδεικνύοντας ότι ο ενισχυτής είναι άνευ όρων σταθερός σε όλες τις συνθήκες λειτουργίας.

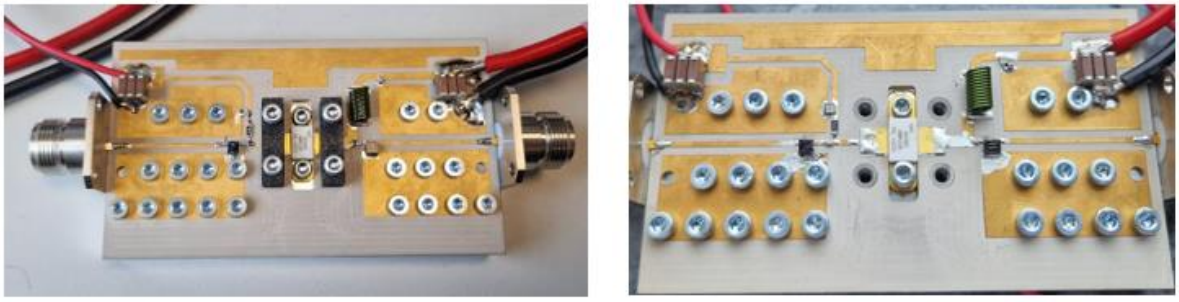
Στη συνέχεια περιγράφονται οι διαδικασίες κατασκευής και οι μετρήσεις που πραγματοποιήθηκαν, ως φυσική συνέχεια του προηγούμενου κεφαλαίου. Η παραγωγή ξεκίνησε με την εξαγωγή των Gerber από το Altium, επιλέγοντας μόνο ό,τι απαιτείται για υψηλή συχνότητα: περίγραμμα πλακέτας για τον ακριβή καθορισμό διαστάσεων, επάνω στρώση χαλκού με ίχνη και επίπεδα γείωσης (η κάτω παραμένει πλήρης γείωση), καθώς και τα αρχεία διάτρησης για όλες τις οπές στερέωσης, τους συνδέσμους τύπου N και την εγκοπή τοποθέτησης του τρανζίστορ ώστε να έρχεται σε άμεση επαφή με το heatsink. Τα αρχεία φορτώθηκαν στο LPKFS63 και κατεργαστήκαμε φύλλα RO3210, με μηχανική συγκράτηση για σταθερότητα. Σε αρκετές επαναλήψεις εμφανίστηκαν ζητήματα φθοράς κοπτικών και περιορισμών του μηχανήματος· σε στροφές 270° και σε ασυνέχειες πλάτους μικροταινίας παρατηρήθηκε υπερκοπή, ενώ σε άλλες περιπτώσεις η διάτρηση υπολείπονταν του ονομαστικού βάθους. Αυτά οδήγησαν σε μικροαποκλίσεις γεωμετρίας που μετατοπίζουν ελαφρά τη χαρακτηριστική εμπέδηση και, τελικά, τους συντονισμούς.



Το μηχάνημα LPKFS63

Η συναρμολόγηση εστίασε στην ποιότητα των κολλήσεων και την μηχανική σταθερότητα. Εφαρμόστηκε flux, προθέρμανση επιφανειών και στη συνέχεια συγκόλληση ώστε να αποφεύγονται κενά, γέφυρες κασσίτερου ή υπερβολική ποσότητα που αυξάνει απώλειες. Οι συνδετήρες N βιδώθηκαν πρώτα στο heatsink για μηχανική ακαμψία και κατόπιν κολλήθηκαν στην ταινιογραμμή, ώστε να διασφαλιστεί ομοιόμορφη γείωση και ελαχιστοποίηση παρασιτικών από την πλευρά του μεταλλικού σώματος. Το heatsink ελέγχθηκε ως προς την τραχύτητα, καθώς η ποιότητα επαφής επηρεάζει εξίσου την θερμική αγωγιμότητα και το επί-

πεδο γείωσης. Για τη σύνδεση των pads του τρανσίστορ με τη μικροταινία δοκιμάστηκαν δύο μέθοδοι: άμεση κόλληση και μηχανική πίεση με εκτυπωμένα μπλοκ PLA. Η δεύτερη διευκόλυνε συγκρίσεις πλακετών και επαναχρησιμοποίηση του τρανζίστορ, αλλά εισήγαγε μια επιπλέον διηλεκτρική οδό ($\varepsilon_r \approx 3.2$) και μικρή παρασιτική σύζευξη προς γη. Η τελική εικόνα ήταν σαφής: η απευθείας κόλληση δίνει μεγαλύτερη ισχύ εξόδου και σταθερότερη θερμική συμπεριφορά. Μετά τη συναρμολόγηση, κόπηκαν και κολλήθηκαν τα bias καλώδια με σύντομες RF διαδρομές.



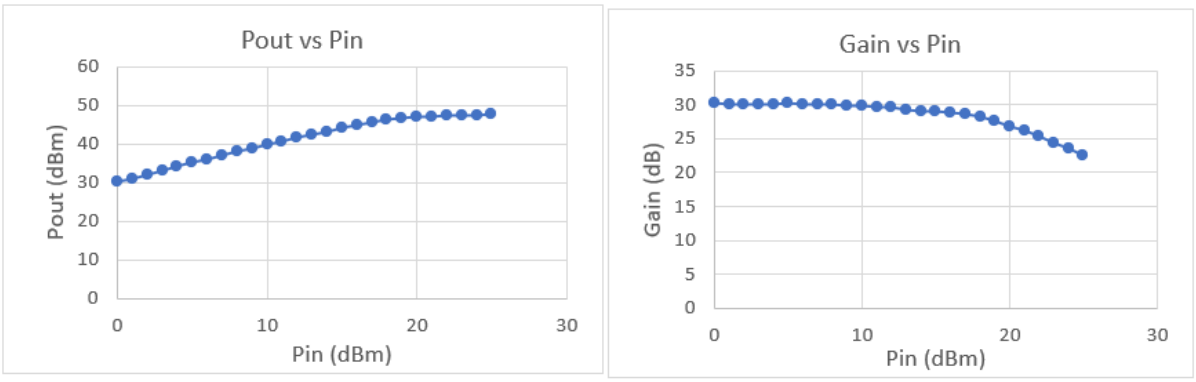
Η κατασκευασμένη πλακέτα με το τρανζίστορ αριστερά συγκρατημένο με PLA και δεξιά με συγκόλληση

Στην πράξη, οι μη ιδανικότητες της κατασκευής αποτυπώθηκαν στις μετρήσεις. Ανομοιόμορφη κοπή χαλκού/διηλεκτρικού γύρω από οπές ή στις ακμές ιχνών μεταβάλλει την τοπική εμπέδηση και την κατανομή ρεύματος. Αχρησιμοποίητες οπές στο heatsink λειτούργησαν σαν μικρές κοιλότητες που εγκλωβίζουν πεδία. Μικρές γωνιακές αποκλίσεις ή υπερβολική κόλληση στους N-συνδετήρες πρόσθεσαν χωρητικά παρασιτικά. Επίσης, οποιαδήποτε μικροκενά επαφής ανάμεσα σε PCB– heatsink ή heatsink–dissipator επιδείνωσαν ταυτόχρονα θερμική αγωγιμότητα και συνέχεια γείωσης. Η εφαρμογή θερμικής πάστας και ελεγχόμενης πίεσης με μπλοκ από PLA συνέβαλε στον περιορισμό των ανακριβειών.

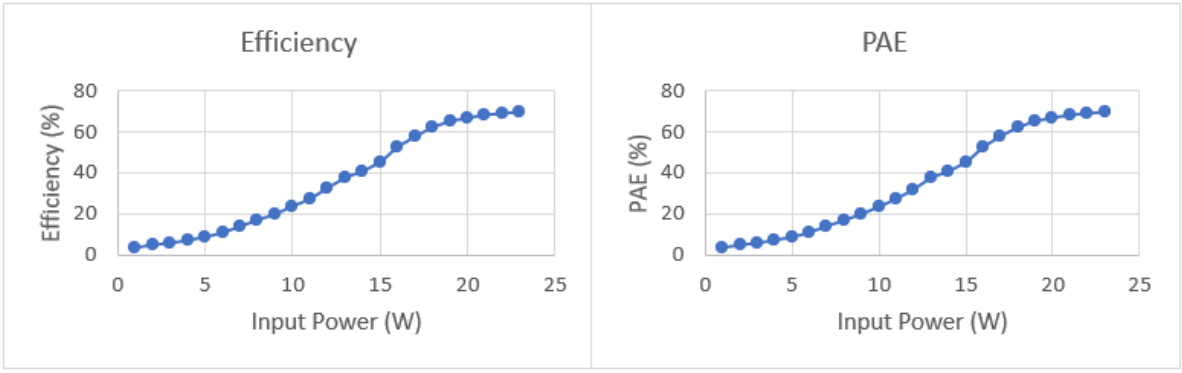
Οι δοκιμές συνοδεύτηκαν από αναλυτική παρουσίαση και τεχνική αξιολόγηση των οργάνων και εξαρτημάτων που χρησιμοποιήθηκαν στο σύστημα μετρήσεων. Περιγράφονται οι γεννήτριες σήματος που παρείχαν την απαιτούμενη ισχύ και δυνατότητα παραγωγής παλμών, τα τροφοδοτικά για τη ρύθμιση και τον έλεγχο των τάσεων πόλωσης, καθώς και τα όργανα μέτρησης που χρησιμοποιήθηκαν για την παρακολούθηση της ισχύος, του φάσματος και των S-παραμέτρων. Παρουσιάζονται επίσης τα παθητικά στοιχεία που συνέθεσαν το κύκλωμα μετρήσεων μαζί με την αιτιολόγηση επιλογής τους, τη συνδεσμολογία τους και τη συμβολή τους στη διασφάλιση της ακρίβειας και της προστασίας του εξοπλισμού κατά τη διαδικασία των μετρήσεων.

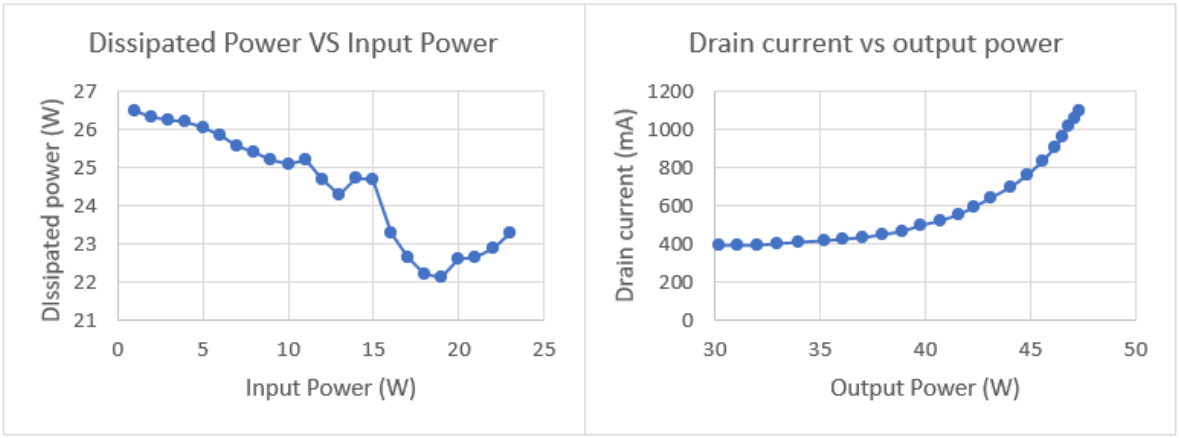
Στα αποτελέσματα της δεύτερης επανάληψης PCB, με ισχύ εισόδου 20 dBm μετρήθηκαν: ισχύς εξόδου 48.4 W και κέρδος 26.85 dB, στα 21 dBm η έξοδος ανέβηκε σε 51.3 W, επιβεβαιώνοντας ότι το στάδιο λειτουργεί βαθιά σε κορεσμό. Σε χαμηλές εισόδους το κέρδος υπερέβη τα 30 dB, και στη ζώνη λειτουργίας (10 dB δυναμικό) καταγράφηκε συμπίεση ~3 dB, όπως αναμενόταν. Η απόδοση και η απόδοση με πρόσθεση ισχύως αυξήθηκαν σημαντικά με την έξοδο, αγγίζοντας ~68% κοντά στα 48–54 W, ενώ η απωλούμενη ισχύς μειώθηκε αντίστοιχα. Η κατανάλωση ρεύματος ακολούθησε εκθετική σχέση με την ισχύ εξόδου, ένδειξη ότι πέρα από τα ονομαστικά όρια απαιτείται προσοχή. Η σύγκριση «κολλημένο τρανζί-

στορ» έναντι «PLA blocks» έδειξε συστηματικά χαμηλότερη ισχύ εξόδου για τη δεύτερη περίπτωση και υψηλότερες θερμοκρασίες. Με απευθείας κόλληση, η θερμοκρασία σταθεροποιήθηκε περί τους 50–55 °C σε CW και ~45 °C σε παλμική λειτουργία.

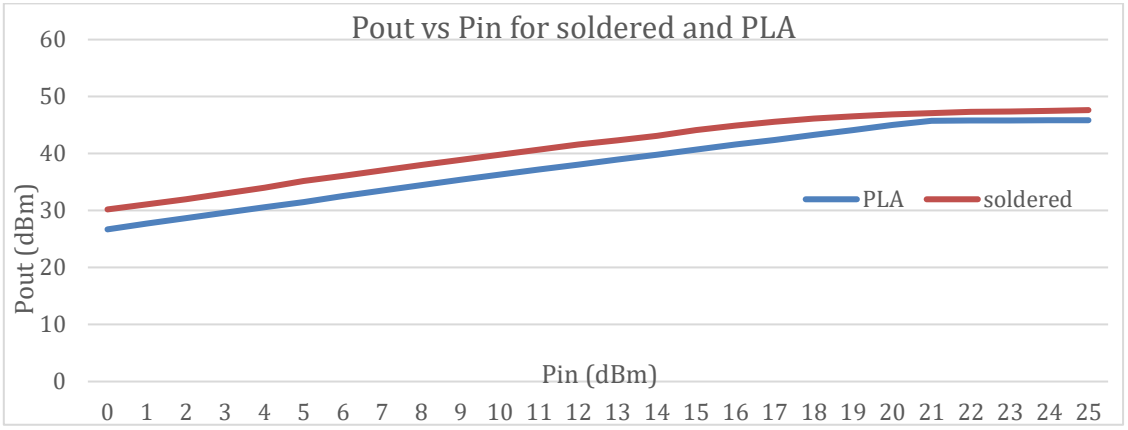


Μετρήσεις ισχύος εξόδου και κέρδους ως προς ισχύ εισόδου για την 2η εκδοχή





Μετρήσεις Απόδοσης, Απόδοσης Προστιθέμενης Ισχύος, Απώλειας Ισχύος και Ρεύματος Drain ως συνάρτηση της Ισχύος Εισόδου



Μετρήσεις ισχύος εξόδου ως συνάρτηση της ισχύος εισόδου για σύνδεση συγκολλημένου τρανζίστορ και με μπλοκ PLA

Ως προς το εύρος ζώνης, με sweep συχνότητας προέκυψε −1 dB εύρος ζώνης περίπου 50 MHz, με μια ελαφρά μετατόπιση συντονισμού που αποδίδεται σε μικροατέλειες κόλλησης και τοποθέτησης. Η φασματική ανάλυση σε CW κοντά στη λειτουργία έδωσε επίπεδα 2ης και 3ης αρμονικής περί −24 dBc και −22 dBc αντίστοιχα, τιμές συμβατές με την έντονα μη γραμμική περιοχή. Δεν παρατηρήθηκαν πλάγιοι λοβοί. Σε παλμική λειτουργία, η πτώση ισχύος εντός παλμού ήταν ~0.05 dB και η μεταβολή φάσης ~0.2°, χωρίς αξιοσημείωτο ripple και με εξαιρετική επαναληψιμότητα από παλμό σε παλμό. Επιπλέον ελέγχθηκαν μικρές μεταβολές της Vd (68–70 V) και καταγράφηκαν μεταβολές ισχύος/φάσης τάξης λίγων dB/μοιρών, επαληθεύοντας ανθεκτικότητα σε ρεαλιστικές τροφοδοτικές διακυμάνσεις.

Οι μετρήσεις για την σταθερότητα έδειξαν K > 1 και μS, μL > 1 σε χαμηλές ισχύς, άρα άνευ όρων σταθερότητα στη γραμμική περιοχή, ενώ η ομαδική καθυστέρηση μετρήθηκε ~6.5 ns, εντός στόχων. Το S11 κυμάνθηκε κοντά στα −13 dB (εξαρτώμενο από ισχύ), ενώ το S22 βελτιώθηκε με την ισχύ, από περίπου −2 dB σε χαμηλές στάθμες μέχρι -8.5 dB σε κορεσμό, όταν η έξοδος του υπό δοκιμή ενισχυτή «φορτίστηκε» με κατάλληλη συνθήκη αντιστοίχισης μέσω των ζευκτών. Σε δοκιμή διαδοχικής λειτουργίας με το 2ο στάδιο, επιβεβαιώθηκε ότι η απαιτούμενη ισχύς ανά κλάδο για το σύστημα μπορεί να επιτευχθεί με ισχύ εισόδου 16 dBm, παρέχοντας λειτουργικό περιθώριο. Παρατηρήθηκαν ωστόσο φαινόμενα πτώσης παλμού λόγω αύξησης του κέρδους του δεύτερου σταδίου εντός παλμού, καθώς και έντονα ίχνη ενδοδιαμόρφωσης γύρω στα 13–14 dBm εισόδου που χρήζουν στοχευμένης βελτιστοποίησης στην προσαρμογή και στο φιλτράρισμα των αρμονικών.

Παρακάτω ο συνολικός πίνακας με τις τεχνικές προδιαγραφές του ενισχυτή και αντίστοιχη τιμή της μέτρησης για την $2^{η}$ εκδοχή του ενισχυτή:

Parameter	Specification per 2024-02-12	Specification per 2024-08-12	Measurement For PCB#2
Operating frequency	352.21 MHz	352.21 MHz	352.21 MHz
-1 dB bandwidth	≥ ±1 MHz	≥ ±1 MHz	50MHz
Peak output power	30 W (or higher)	50 W	58W
RF pulse width	Up to 3.5 ms	Up to 3.5 ms	3.5 ms
Repetition rate	Up to 14 Hz	Up to 14 Hz	14 Hz
Gain	23 dB min	27 dB at 20dBm input	26.85 dB
Efficiency	> 50 %	> 50 %	68%
Maximum no-damage RF drive input	26 dBm	26 dBm	26 dBm
Harmonic con-tent at output power	< -30 dBc	< -30 dBc	-20 dBc, -27dBc
Spurious and sideband levels in ± 20 MHz	< -60 dBc	< -60 dBc	No spurious
RF Input Connector	N type, 50 Ω, Female	N type, 50 Ω, Female	N type, 50 Ω, Female
RF Output Connector	N type, 50 Ω, Female	N type, 50 Ω, Female	N type, 50 Ω, Female
Input/output impedance	50 Ω	50 Ω	50 Ω
Input VSWR	≤ 1.2:1 (if possible)	≤ 1.12:1 or -25dB (if possible)	1.5:1
output VSWR	≤ 1.2:1 (if possible)	≤ 1.12:1 or -25dB (if possible)	2.3:1
Load VSWR	Infinity	Infinity	
Gain flatness	ΔG ≤ ±0.5 dB (over 10dB dy-namic)	ΔG ≤ ±0.5 dB (over 10dB dynamic)	2.95 dB
Phase flatness	≤ 2°(over 10dB dynamic)	≤ 2° (over 10dB dynamic)	0.2°
RF Power Drop across the pulse	≤ 5% p-p (or Max 0,21dB) (power) (Within 3.5ms RF pulse excluding first 100µs of the	≤ 10% p-p (or Max 0,21dB) (power) (Within 3.5ms RF pulse excluding first 100µs of the pulse)	0.05 dB drop

	pulse)		
Power ripple across pulse	≤ 0.25% rms (Within 3.5ms RF pulse excluding first 100μs of the pulse)	≤ 0.25% rms (Within 3.5ms RF pulse excluding first 100μs of the pulse)	No
Phase shift across the pulse	≤ 5° (Within 3.5ms RF pulse excluding first 100μs of the pulse)	≤ 10° (Within 3.5ms RF pulse excluding first 100μs of the pulse)	0.2°
Phase ripple across pulse	≤ 0.25° rms (Within 3.5ms RF pulse excluding first 100μs of the pulse)	≤ 0.25° rms (Within 3.5ms RF pulse excluding first 100μs of the pulse)	No
Pulse-to-pulse power stability	≤ 2%	≤ 2%	0%
Pulse-to-pulse phase stability (repeatability)	≤ 2°	≤ 2°	0°
RF Pulse Rise/ Fall Time	≤ 1 μs	≤ 1 μs	
compression point @ 0,1dB	54 W	54 W	2 W
Total Group Delay (not sure we need this parameter)	≤ 50 ns	≤ 50 ns	6ns
Size	Max size of the PCB 20x10 cm	Max size of the PCB 20x10 cm	10.6x6 cm

Για πληρότητα, η πρώτη επανάληψη του PCB έδειξε συντονισμό περί τα 295 MHz. Ο έλεγχος της ταινιογραμμής με προσωρινό τερματισμό 50 Ω επιβεβαίωσε σωστή χαρακτηριστική εμπέδηση, άρα το θέμα εντοπίστηκε στο σημείο αναφοράς του μοντέλου συσκευασίας στο εργαλείο προσομοίωσης και διορθώθηκε στη δεύτερη επανάληψη. Η πέμπτη επανάληψη προσέφερε έως ~68–70 W με βελτιωμένη θερμική συμπεριφορά και χαμηλότερη κατανάλωση, χάρη σε πιο βελτιωμένη γεωμετρία εξόδου με ευρεία επιφάνεια σύνδεσης, μικρότερες αποστάσεις και περιορισμός επιρροής του κυκλώματος τροφοδοσίας.

Συνοψίζοντας, η εργασία ανέδειξε έναν ολοκληρωμένο κύκλο σχεδίασης–υλοποίησης–μέτρησης για έναν ενισχυτή ισχύος στερεάς κατάστασης που ανταποκρίνεται

στις λειτουργικές απαιτήσεις του ESS, επιτυγχάνοντας υψηλή αποδοτικότητα, επαναληψιμότητα σε παλμική λειτουργία και συμβατότητα με τα συστήματα του ESS. Η μεθοδική επιλογή υλικών και τοπολογιών, ο στοχευμένος σχεδιασμός και οι μετρήσεις στον πάγκο οδήγησαν σε τεκμηριωμένες βελτιστοποιήσεις, από διάταξη και προσαρμογή έως διαδικασίες συναρμολόγησης/γείωσης, ενώ ανέδειξαν σαφή περιθώρια περαιτέρω ωρίμανσης σε παραμέτρους όπως των S-παραμέτρων εξόδου, την θωράκιση και την έξυπνη πόλωση. Πέρα από το συγκεκριμένο πρωτότυπο, η παρούσα εργασία θέτει μια σταθερή βάση πάνω στην οποία μπορούν να αναπτυχθούν μελλοντικές βελτιώσεις και επεκτάσεις, οδηγώντας στην κατασκευή ακόμη πιο αποδοτικών ενισχυτών και συμβάλλοντας περαιτέρω στην εδραίωση της βιωσιμότητας ως βασικού χαρακτηριστικού του ESS.

Chapter 1: Introduction

1 Introduction

This chapter introduces the scope, background, motivation, and objectives of the thesis. It summarizes the design and validation work carried out during a six-month internship at the European Spallation Source (ESS) Radio Frequency (RF) group, provides an overview of the ESS and its applications, explains the motivation for adopting Solid-State Power Amplifier (SSPA) technology, and outlines the objectives focused on the design, simulation, manufacturing, and testing of a driver amplifier.

1.1 Scope

The purpose of this thesis is to document the design and validation work carried out during a six-month internship at ESS RF group. The focus of the internship was the design, development, and validation of an RF amplifier to serve as the 1st stage driver for a new Solid-State Power Amplifier system. The internship aimed to contribute to ESS's project of using SSPA technology to power spoke cavities, with each cavity requiring up to 400kW. This thesis highlights key deliverables, technical challenges, design optimizations and lessons learned.

1.2 The European Spallation Source

The European Spallation Source is a European Research Infrastructure Consortium (ERIC), a multi-disciplinary research facility based on the world's most powerful neutron source. It is currently under construction, in Lund, Sweden, while its Data Management and Software Centre is situated in Copenhagen, Denmark. There are 13 European member countries that are partners in the construction and operation of ESS: Czech Republic, Denmark, Estonia, France, Germany, Hungary, Italy, Norway, Poland, Spain, Sweden, Switzerland, and the United Kingdom.

Figure 1.1: The ESS campus

At the heart of the facility will be a linear accelerator (LINAC), designed to provide the world's most powerful proton beam—up to 2 GeV. This accelerator will drive the spallation process that produces neutrons, enabling scientists to observe and understand atomic structures and fundamental forces at time and length scales not achievable with other neutron sources. Upon completion, the ESS LINAC will be the most powerful proton accelerator ever built.

Parameter	Units	Value
Average beam power	MW	5
Proton kinetic energy	GeV	2.0
Pulse repetition rate	Hz	14
Energy per pulse	kJ	357
Average pulse current	mA	62.5
Maxro-pulse length	ms	2.86
Power during pulse	MW	125
Number of target stations		1
Number of moderators		2
Number of instruments in construction budget		16 (22)
Number of neutron beam ports		42
Average separation between ports	Degrees	6

Table 1: ESS high level parameters ([1] page 2)

The key high-level parameters of the European Spallation Source are summarized in Table 1. The accelerator is designed to deliver an average beam power of 5 MW, achieved through a 2.0 GeV proton beam operating at a pulse repetition rate of 14 Hz. Each pulse carries an energy of 357 kJ, with an average pulse current of 62.5 mA and a macro-pulse duration of 2.86 ms. The facility includes one target station equipped with two moderators, and will initially host 16 scientific instruments, with plans to expand to 22 in the future. Neutrons will be extracted through 42 beam ports, each separated by an average angular spacing of 6°.

The neutrons produced at ESS will enable groundbreaking research across a wide range of disciplines. In materials science, they will provide unique insights into structure, dynamics, and mechanical properties. In life sciences and medicine, neutron scattering will allow high-resolution studies of proteins, membranes, and other biological systems, aiding drug discovery and diagnostics. Neutrons are also being explored in cancer therapy, for example through Boron Neutron Capture Therapy, which can selectively target and destroy tumor cells. In the energy sector, neutrons are especially powerful because of their sensitivity to light elements such as hydrogen and lithium, making it possible to track ion movements inside batteries, study hydrogen storage materials, and optimize fuel cells—key steps toward next-generation sustainable energy technologies. In industry and engineering, non-destructive neutron testing will improve the design and validation of technologies ranging from aero-

space components to microelectronics. Finally, in archaeology, neutron imaging enables the safe study of artifacts, revealing hidden structures and compositions without causing damage.

Beyond its direct applications, ESS will serve as a hub for innovation, education, and international collaboration. By advancing accelerator technology, detector systems, data analysis, and high-performance computing, it will strengthen Europe's leadership in large-scale research infrastructures and remain a cornerstone of scientific discovery for decades to come.

1.3 Motivation

The European Spallation Source has set a strategic goal to operate as a green facility. To achieve that, environmentally sustainable developments are examined towards the adoption of energy saving and improved energy-efficient approaches. The RF group is responsible for providing power to the spoke cavities and therefore is responsible for optimizing the energy efficiency of those systems. Based on the ESS design[1], the spoke cavities are powered by tetrode amplifiers. Although they can provide the power needed, it was decided to develop an alternative solution. The new system will primarily focus on improving the efficiency of the system to help achieve the sustainability goals of ESS. Another important issue is that there is only one provider for the tetrode in use, putting the system at risk in case the product is discontinued. Tetrodes have a shorter lifespan compared to solid-state systems, due to their vacuum tube geometry, resulting in longer downtime whenever they need to be replaced.

For all these reasons the RF group in-kind collaboration with FREIA laboratory from Uppsala university has decided to design a new SSPA system to power the spoke cavities. Solid state RF amplifiers are being considered for an increasing number of accelerator applications, both circular and linear. Their capabilities extend from a few kW to several hundred kW, and from less than 100 MHz to above 1 GHz[2], [3], [4]. The reasons behind this shift towards SSPA technology are efficiency, reliability, modularity and compactness.

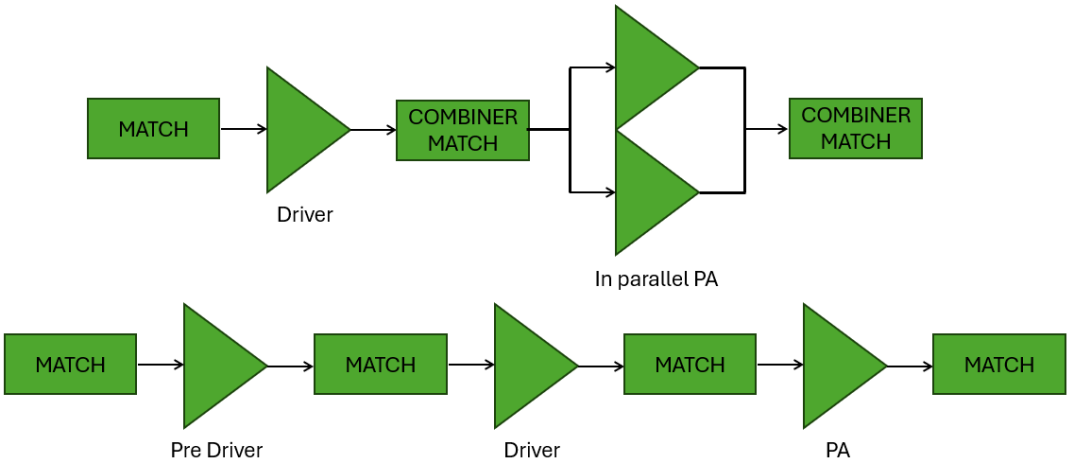


Figure 1.2: Amplification topologies

This technology can achieve high power efficiencies at lower supplied voltages, which reduces the operational cost and can operate at higher efficiencies across a wider range of output powers. If reliability is taken into consideration, SSPAs have a longer lifespan than the other choices and even in case of failure of one module because of the parallel operation of the amplifiers the system can continue operating with slightly reduced power, thus increasing reliability. In parallel architectures offer modularity in the designs simply by adding more modules and designing combiners with higher power handling capacity. Moreover, they are comprised from fewer parts that can fail and fewer parts in general, leading to lower maintenance requirements, higher reliability and more compact design.

1.4 Objectives

This project involves the design, simulation, manufacturing, and testing of a driver amplifier for the SSPA system, intended to power the spoke cavities at ESS. The design of an amplifier provides an opportunity to explore the trade-offs and interdependencies among amplifier specifications in a real application. The key parameters are noise, power, frequency, gain, supply voltage and linearity. Figure 1.3 below demonstrates their connection which will be analyzed in the following chapters:

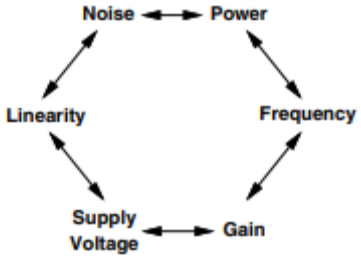


Figure 1.3: RF design trade-offs ([5] page 4)

The key specifications for the amplifier include:

- Operational Frequency: 352.21 MHz
- Efficiency: Greater than 50%
- Output Power: 50W

The project provided hands-on experience with circuit and electromagnetic modeling using Advanced Design System (ADS) by Keysight, PCB design using Altium Designer, and the manufacturing and testing processes essential for the development of a Solid-State Power Amplifier.

Chapter 2: Theoretical background

2 Introduction

This chapter provides the theoretical background required to understand the operation of microwave circuits and power amplifiers. It begins with an overview of the ESS linear accelerator, highlighting the role of high-power RF systems in the acceleration of proton beams. The discussion then focuses on the fundamental concepts of microwave theory that govern the behavior of high-frequency circuits. Finally, the operating principles of power amplifiers are presented, along with the main device technologies and classes of operation relevant to RF and microwave applications.

2.1 The ESS linear accelerator

Particle accelerators are devices that use electromagnetic fields to accelerate charged particles to high speeds and energies. The underlying principle is the Lorentz force, which describes the interaction of charged particles with electric and magnetic fields, as shown in the equation:

$$F = q\,(E + v\,x\,B) \tag{2.1}$$

where q is the particle charge, E the electric field, B the magnetic field, and v the particle velocity. Electric fields provide acceleration by increasing the kinetic energy of the particles, while magnetic fields are used to steer and focus the beam. Based on their geometry, accelerators are broadly divided into circular accelerators, where particles follow closed orbits and gain energy in repeated passes, and linear accelerators, where particles move in a straight path and gain energy in successive structures. Linacs are particularly well suited for applications that require very high proton energies without the synchrotron radiation losses associated with circular machines. For this reason, ESS employs a superconducting linear accelerator as the core of its facility.

At ESS a LINAC accelerates protons with pulsed RF signals that are 2.6ms long and with a repetition rate of 14 Hz. The protons then collide with a rotating, helium-cooled tungsten target to generate intense pulses of neutrons. Surrounding the tungsten target are baths of cryogenic hydrogen, which feed neutron supermirror guides. The operation is similar way to optical fibers, directing the intense beams of neutrons to experimental stations, where research is performed on a range of materials.

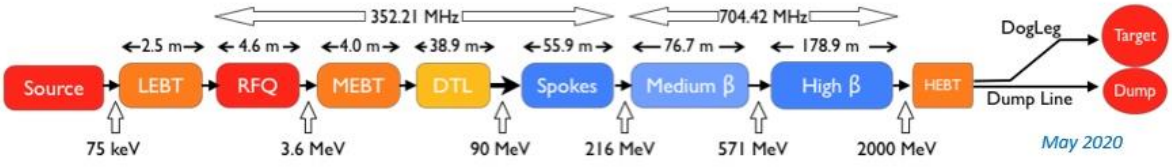


Figure 2.1: The ESS linac schematic as of May 2020[6]

Protons are generated in a dedicated ion source, where hydrogen gas is exposed to rapidly varying electromagnetic fields in the RF/microwave range. These fields ionize the hydrogen molecules by stripping away their electrons, creating plasma composed primarily of protons. From this plasma, protons are extracted and subsequently injected into the radio-frequency quadrupole (RFQ), which forms the first accelerating stage of the linear accelerator. Once the plasma is created, the ionized hydrogen atoms can bombard a cathode target, causing atoms or molecules from the target material to be ejected, creating pure proton plasma.

The first part of the accelerator, the normal conducting accelerator, is called the warm LINAC because it operates in room temperatures. It is composed of matching sections as well as accelerating components. As the velocity of the beam increases, the accelerating structures are adapted to make the acceleration more efficient. The proton beam is transported through a Low Energy Beam Transport (LEBT) section, which consists of two magnetic solenoids used for beam matching to achieve nominal functionalities in the structures, to the Radio Frequency Quadrupole (RFQ), where it is bunched and accelerated up to 3.6 MeV.

The Radio-Frequency Quadrupole (RFQ) is a linear accelerator that focuses and bunches the continuous beam and accelerates the proton beam from 75 keV to 3.6 MeV with high efficiency. It is the first RF accelerating structure. The radiofrequency is set to 352.21 MHz, which is a part of Ultra High Frequency (UHF) band.

The Medium Energy Beam Transport (MEBT) line matches the beam coming from the RFQ into the subsequent accelerating structure, the Drift Tube Linac (DTL). It uses RF bunching cavities and magnetic quadrupoles to match the beam in the longitudinal and the transverse planes.

The Drift Tube Linac is another type of linear accelerator. Inside a drift tube linac, the particles are subjected to a regularly oscillating electrical field. Electric fields accelerate them as they move from one tube to the next. Each time the field changes direction, they particles are directed into the next tube. This stage raises the beam energy from 3.62 MeV to 90 MeV. While the warm part of the accelerator provides 80% of the longitudinal phase, it supplies less than 5% of the particle energy. The rest of the energy is given by three families of superconducting cavities.

The second part of the accelerator, the cold LINAC, which is the first part of the superconducting RF section, is consisted of 26 double-spoke cavities (SPK) with a beta value of 0.5. Superconducting cavities operate at cryogenic temperatures, exhibiting zero electrical resistance, which allows for efficient energy transfer to the particle beam. The electromagnetic fields can traverse the cavities keeping their energy content intact due to great values of quality factor Q. To achieve the substantial acceleration needed, the cavities are supplied with up to 400 kW of power.

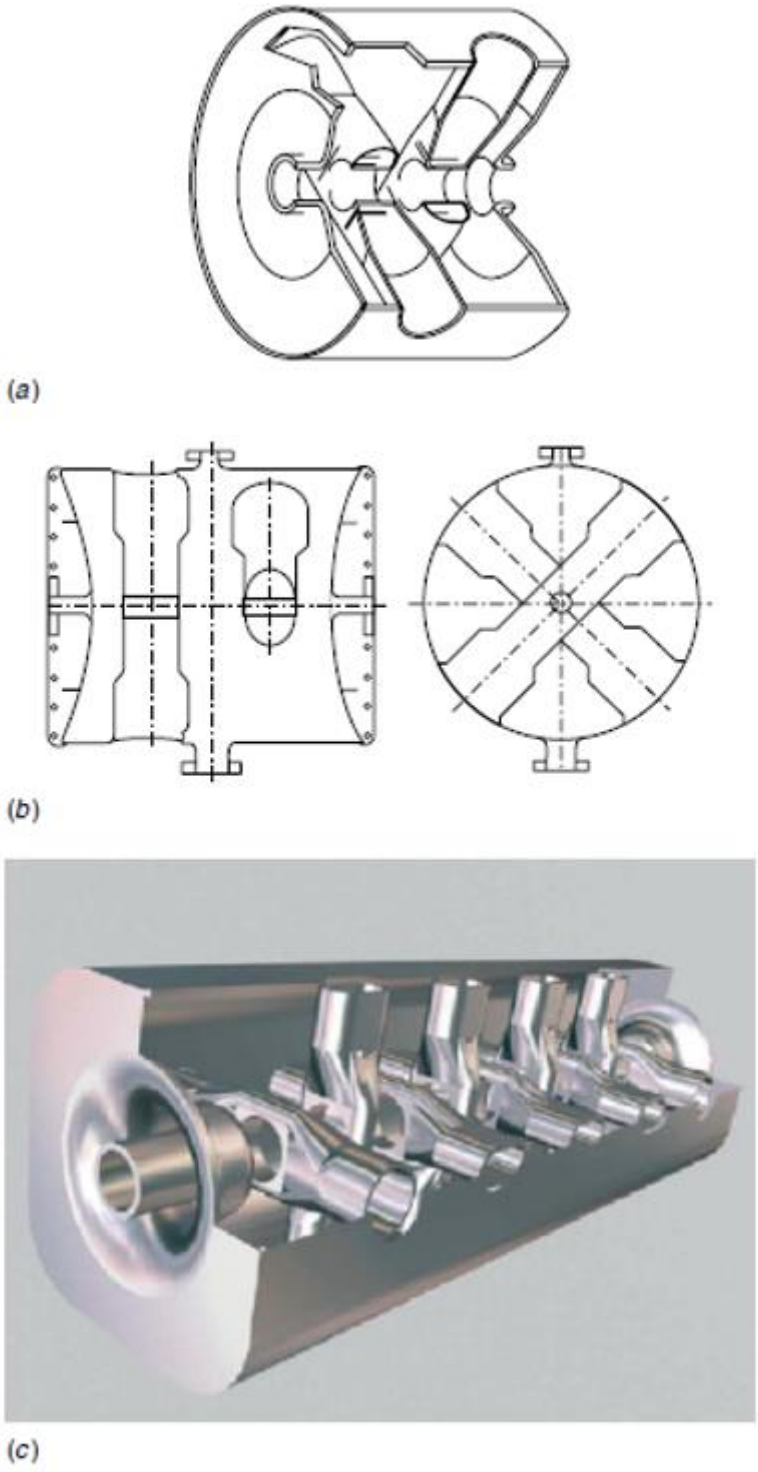


Figure 2. 2: Spoke cavities examples[7]

The SPK stage amplifies the beam's energy from the Drift Tube Linac, which delivers the beam with 90 MeV of energy, and accelerates it to 216 MeV, at which point it is injected into the Elliptical linac.

The spoke-cavities are followed by 36 Medium Beta Linac (MBL) cavities with β = 0.67 and 84 High Beta Linac (HBL) elliptical cavities, with β = 0.86. The geometrical beta in these contexts refers to the beta function, which characterizes the focusing strength of the

beam optics in the Medium Energy Beam Transport (MEBT) or High Energy Beam Transport (HEBT) sections. The beta function describes how the beam size changes along the beamline, providing crucial information for designing and optimizing the beam transport system. So, the elliptical linac takes the beam from the Spoke Linac at an energy of 216 MeV and accelerates it to 2.0 GeV, at which point it is injected into the HEBT and finally to the target.

The protons reach 96% of the speed of light before they hit the rotating target wheel. The wheel is 2.6 meters in diameter and consists of hundreds of heavy metal Tungsten bricks encased in a disk of stainless-steel shielding. The high-speed protons kick out the neutrons in a process known as spallation. It is these neutrons that are directed to the ESS instruments through a gauntlet of media, guides, optics and filters to be used for scientific research.

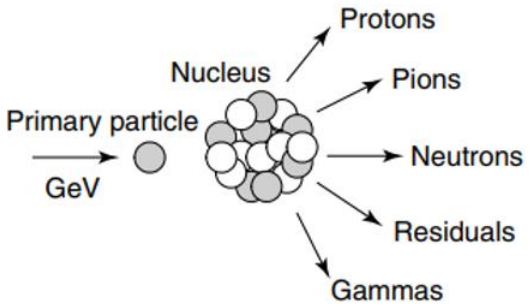


Figure 2. 3: Generalized possible particle of a particle-nucleus interaction in the GeV energy range [8]

Spallation is a high-energy nuclear reaction in which an energetic particle, typically a proton with energy above 50 MeV, strikes a heavy nucleus and causes it to eject numerous secondary particles. These include neutrons, protons, pions, gamma rays, and lighter nuclear fragments, leaving behind a residual nucleus of reduced mass. In the GeV energy range, such interactions lead to the production of tens of neutrons per incident proton, making spallation an efficient method for neutron generation. Unlike fission, which splits a heavy nucleus into two large fragments and releases only a few neutrons per event, spallation shatters the nucleus into many smaller fragments and secondary particles, producing tens of neutrons per incident proton, far higher than in fission reactions.

The practical realization of spallation for research purposes relies on large-scale proton accelerators capable of delivering high-energy beams onto heavy-metal targets to produce intense neutron fluxes. Over the past decades, several major facilities have been constructed worldwide, each advancing the limits of beam power, efficiency, and reliability. Table 2 summarizes the principal spallation neutron sources worldwide, emphasizing those equipped with cold neutron facilities and supporting fundamental physics programs. Cold neutrons are neutrons moderated to energies below approximately 5 meV and wavelengths longer than 4 Å, through scattering in cryogenic materials such as liquid hydrogen or deuterium. Their long wavelengths and low velocities make them ideal for precision studies in nuclear and particle physics, such as measurements of the neutron lifetime, parity violation, and the search for the

neutron electric dipole moment ,as well as for applications in materials science where high-resolution, non-destructive probing is required.

Facility	Location	Beam Power	Beam Energy	Status / Startup
LANCE	Los Alamos National Laboratory, USA	0.8 MW	800 MeV	1972
ISIS	Rutherford Appleton Laboratory, UK	160 kW	800 MeV	1985
SINQ	Paul Scherrer Institute, Switzerland	1 MW	590 MeV	1996
SNS	Oak Ridge National Laboratory	1.4 MW	1.3 GeV	2006
JSNS	Tokai, Japan	1 MW	3 GeV	2008
CSNS	Dongguan, China	0.5 MW	1.6 GeV	2018
ESS	Lund, Sweden	5 MW	2 GeV	2027 (expected)

Table 2: Operating parameters for existing and upcoming spallation neutron sources with fundamental physics programs ([9])

Among the facilities listed, several maintain dedicated beamlines for cold and fundamental neutron physics. The Los Alamos Neutron Science Center (LANSCE) in the United States combines fast and moderated neutron sources. The Spallation Neutron Source (SNS) at Oak Ridge operates at 1 GeV and 1.4 MW and hosts the Fundamental Neutron Physics Beamline (FnPB) for precision symmetry tests. Similarly, the Japan Spallation Neutron Source (JSNS) at J-PARC accelerates protons to 3 GeV for studies of neutron decay and time-reversal symmetry. In China, the China Spallation Neutron Source (CSNS) delivers a 1.6 GeV proton beam to a tungsten target, while the Swiss Spallation Neutron Source (SINQ) provides a continuous 590 MeV beam to a lead target, producing a steady flux of cold and ultra-cold neutrons. Finally, the European Spallation Source (ESS) in Sweden, designed for a 2 GeV, 5 MW long-pulse beam, will become the world's brightest cold-neutron facility, capable of supporting future beamlines dedicated to fundamental neutron physics.

Together, these sources illustrate the evolution of accelerator-driven neutron facilities toward higher intensity, greater efficiency, and increased versatility. Their ability to generate intense beams of cold neutrons has established spallation sources as indispensable tools for both applied research and the experimental investigation of fundamental symmetries in physics.

2.2 Microwave theory

Microwaves represent the portion of the electromagnetic spectrum with frequencies typically ranging from 300 MHz to 300 GHz, corresponding to wavelengths between one meter and one millimeter. The generation, transmission, and manipulation of microwave signals rely on specialized techniques that account for their distributed nature, since at these frequencies the physical dimensions of circuit elements become comparable to the wavelength. As a result, lumped-element circuit models are no longer sufficient, and transmission line theory must be employed to describe voltage and current variations along conductors The study of microwave theory forms the foundation for understanding high-frequency amplifier design, impedance matching, and overall system performance in modern RF systems.

2.2.1 S parameters

In high-frequency and microwave circuit analysis scattering parameters, or S-parameters, are used to describe the behavior of linear two-port networks in terms of incident and reflected waves. For a two-port network with a reference impedance Z_0, the normalized incident and reflected waves at each port are defined as:

$$\alpha_i = \frac{V_i^+}{\sqrt{Z_0}} \qquad b_i = \frac{V_i^-}{\sqrt{Z_0}} \tag{2.2}$$

where V_i^+ and V_i^- represent the incident and reflected voltage waves, respectively. The S-parameters relate these quantities as:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \qquad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2.3}$$

In matrix form:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.4}$$

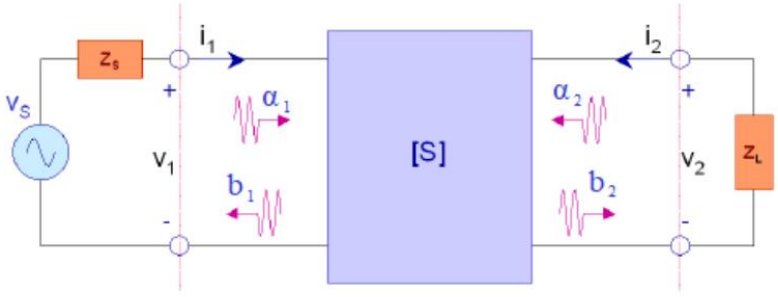


Figure 2. 4: 2-port network

Each of the four coefficients has a specific physical interpretation:

- S_{11}: Input reflection coefficient (input return loss).
- S_{21}: Forward transmission coefficient (gain).
- S_{12}: Reverse transmission coefficient (isolation).
- S_{22}: Output reflection coefficient (output return loss).

2.2.2 Transmission lines

Transmission line theory provides a bridge between circuit analysis and electromagnetic field theory, allowing accurate modeling of wave propagation, attenuation, and reflections in microwave networks. The key distinction between circuit theory and transmission line theory lies in the electrical size of the network. Conventional circuit analysis assumes that the physical dimensions of conductors and components are much smaller than the wavelength of the signals they carry. Under this assumption, voltage and current are considered uniform throughout the circuit, and the system can be accurately represented using lumped elements. As the operating frequency increases, the wavelength of the signal becomes comparable to the physical dimensions of the conductors and transmission line theory must be applied. A transmission line is a distributed-parameter network composed of two or more conductors that support transverse electromagnetic (TEM) wave propagation. To describe their behavior, an infinitesimal section of the line of length Δz is modeled as a lumped circuit characterized by four distributed parameters:

- R=series resistance per unit length (Ω/m)
- G=shunt conductance per unit length (S/m)
- L=series inductance per unit length (H/m)
- C=shunt capacitance per unit length (F/m)

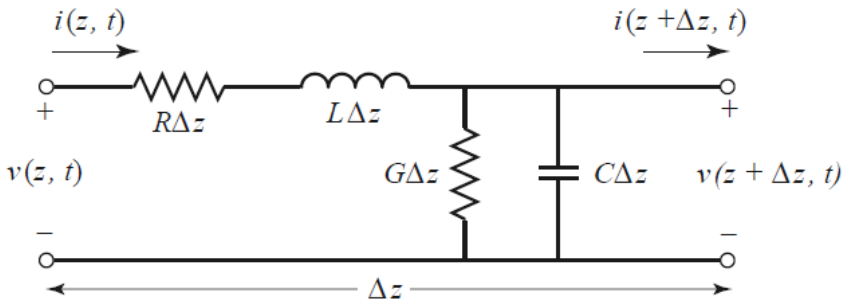


Figure 2. 5:Voltage and current definitions and equivalent circuit for an incremental length of transmission line, [10] page 49)

To describe voltage and current variations along the transmission line, Kirchhoff's laws are applied to the infinitesimal segment of length Δz.

Applying Kirchhoff's Voltage Law to the equivalent circuit yields:

$$v(z,t) - R\Delta z\, i(z,t) - L\Delta z\, \frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0 \tag{2.5}$$

Similarly, applying Kirchhoff's Current Law (KCL) gives:

$$i(z,t) - G\Delta z\, v(z+\Delta z,t) - C\Delta z\, \frac{\partial v(z+\Delta z,t)}{\partial t} - i(z+\Delta z,t) = 0 \tag{2.6}$$

Dividing both equations by Δz and taking the limit as $\Delta z \to 0$ yields the Telegrapher's equations:

$$-\frac{\partial v(z,t)}{\partial z} = R\, i(z,t) + L\, \frac{\partial i(z,t)}{\partial t} \tag{2.7}$$

$$-\frac{\partial i(z,t)}{\partial z} = G\, v(z,t) + C\, \frac{\partial v(z,t)}{\partial t} \tag{2.8}$$

Solving the Telegrapher's equations for voltage and current becomes more convenient under sinusoidal steady-state excitation. Assuming time-harmonic signals of angular frequency ω, the voltage and current along the line can be expressed as:

$$v(z,t) = \Re\{V(z)e^{j\omega t}\} \qquad i(z,t) = \Re\{I(z)e^{j\omega t}\} \tag{2.9}$$

Substituting these expressions into equations (2.2a) and (2.2b) gives the phasor form of the Telegrapher's equations:

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.10}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{2.11}$$

Differentiating each equation with respect to z and substituting appropriately eliminates either V or I, resulting in the wave equations:

$$\frac{d^2V(z)}{dz^2} = \gamma^2 V(z) \qquad \frac{d^2I(z)}{dz^2} = \gamma^2 I(z) \tag{2.12}$$

Where

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.13}$$

is the propagation constant.

The real part α represents the attenuation constant (Np/m), indicating power loss per unit length, while the imaginary part β represents the phase constant (rad/m), describing the phase variation along the line.

The general solution to the voltage and current wave equations is given by:

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{+\gamma z} \tag{2.14}$$

$$I(z) = \frac{1}{Z_0}(V_0^+ e^{-\gamma z} - V_0^- e^{+\gamma z}) \tag{2.15}$$

where $V_0^+$and $V_0^-$are the amplitudes of the forward and reflected waves, respectively, and

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.16}$$

is the characteristic impedance of the transmission line. At the load termination Z_L, the reflection coefficient is defined as:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.17}$$

For practical use, impedances are normalized to the characteristic impedance Z_0:

$$z_L = \frac{Z_L}{Z_0} = r + jx \tag{2.18}$$

Substituting the above equations yields:

$$\Gamma = \frac{z_L - 1}{z_L + 1} \tag{2.19}$$

Where $\Gamma = \Gamma_r + j\Gamma_i$ is the corresponding reflection coefficient. Every passive load with $|\Gamma| \leq 1$ maps to a unique point within the Smith chart. The chart consists of families of constant-resistance and constant-reactance circles, which intersect orthogonally to form a coordinate system useful for impedance matching and transmission-line analysis.

The magnitude $|\Gamma|$of the reflection coefficient indicates the degree of mismatch between the load and the characteristic impedance of the transmission line, while the angle of Γcorresponds to the phase of the reflected wave. For a matched load ($z_L = 1$), $\Gamma = 0$, and the point lies at the center of the chart, indicating no reflection. Conversely, a short circuit ($z_L = 0$)and an open circuit ($z_L \to \infty$)correspond to $\Gamma = -1$and $\Gamma = +1$, located at the left and right extremes of the horizontal axis, respectively.

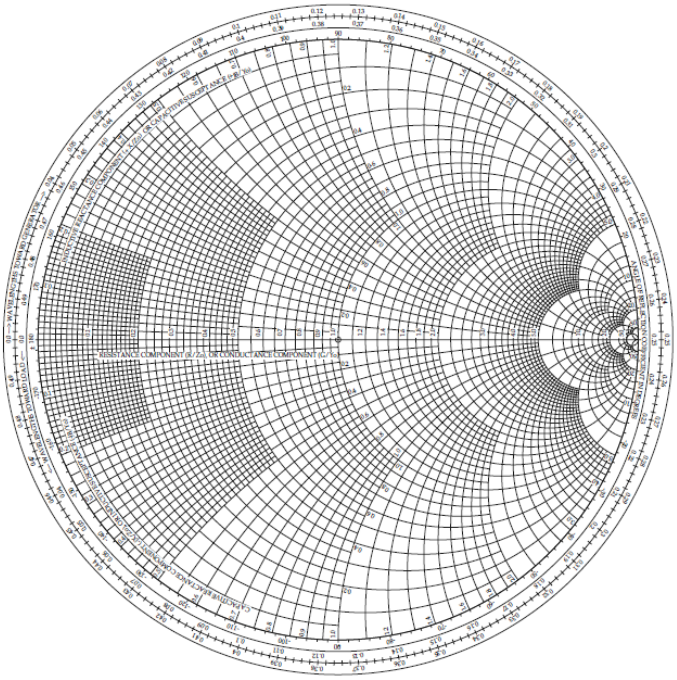


Figure 2.6: The Smith chart

2.2.3 Planar waveguides

Planar transmission lines are widely used in modern microwave integrated circuits due to their compact size, ease of fabrication, and compatibility with printed circuit board (PCB) and hybrid technologies. Unlike metallic waveguides, which confine electromagnetic fields within a closed conductive structure, planar transmission lines guide fields in an open configuration on a dielectric substrate using surface metallization patterns. The most common types are microstrip, stripline, and coplanar waveguide (CPW).

In practical RF and microwave design, planar transmission lines are typically designed for a characteristic impedance of 50 Ω, ensuring compatibility with coaxial connectors, test equipment, and standard components.

The 50 Ω Reference Impedance

A coaxial transmission line consists of a central conductor of radius a, surrounded by a concentric outer conductor of inner radius b, separated by a homogeneous dielectric of relative permittivity ε_r, as illustrated in Figure 2.7. The line supports a transverse electromagnetic (TEM) mode, in which the electric and magnetic fields are purely transverse to the direction of propagation. The characteristic impedance Z_0 of a lossless coaxial line and for air-filled lines (e_r =1) can be expressed as:

$$Z_0 = \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}}\ln\left(\frac{b}{a}\right) \quad or \quad Z_0 = 60\ln\left(\frac{b}{a}\right) \tag{2.20}$$

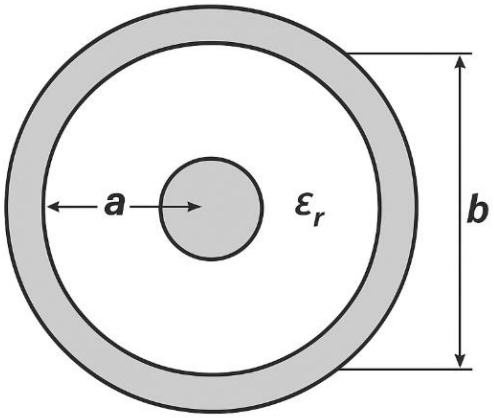


Figure 2.7: Cross section of a coaxial transmission line

To account for attenuation due to finite conductor conductivity, consider the following assumptions:

- Surface current exists due to the skin effect, characterized by the surface resistance:

$$R_s = \sqrt{\frac{\omega\mu}{2\sigma}} \ [\Omega/\square] \tag{2.21}$$

- Lossless dielectric: $\tan\,\delta \approx 0$.
- Low-loss TEM propagation: standard small-loss approximations apply.

The electric and magnetic fields for the TEM mode in a coaxial structure are given by:

$$E_r(r) = \frac{V}{r\ln\left(\frac{b}{a}\right)} \quad H_\phi(r) = \frac{I}{2\pi r} \tag{2.22}$$

The corresponding characteristic impedance and transmitted power are:

$$Z_0 = \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}}\ln\left(\frac{b}{a}\right) \qquad P_{\text{trans}} = \frac{1}{2}\Re\{VI^*\} = \frac{|\,I\,|^2\,Z_0}{2} = \frac{|\,V\,|^2}{2Z_0} \tag{2.23}$$

The average power dissipated on a good conductor surface per unit area is:

$$p_{\text{loss}} = \frac{1}{2}R_s\,|\,H_t\,|^2 \quad \left[\frac{\text{W}}{\text{m}^2}\right] \tag{2.24}$$

where H_t is the tangential magnetic field at the conductor surface.

For the inner conductor ($r = a$):

$$| H_t | = | H_\phi(a) | = \frac{| I |}{2\pi a}, \text{ surface per unit length: } 2\pi a \tag{2.25}$$

Thus:

$$P_{\text{loss, in}} = \frac{1}{2} R_s \left(\frac{| I |}{2\pi a}\right)^2 (2\pi a) = \frac{R_s | I |^2}{4\pi a} \tag{2.26}$$

For the outer conductor ($r = b$):

$$| H_t | = \frac{| I |}{2\pi b}, P_{\text{loss, out}} = \frac{R_s | I |^2}{4\pi b} \tag{2.27}$$

Hence, the total power loss per unit length is:

$$P_{\text{loss}} = \frac{R_s | I |^2}{4\pi}\left(\frac{1}{a} + \frac{1}{b}\right) \tag{2.28}$$

For a low-loss line, the attenuation constant due to conductor loss is defined as:

$$\alpha_c = \frac{P_{\text{loss}}}{2P_{\text{trans}}} \tag{2.29}$$

Substituting P_{loss} and P_{trans} gives

$$\alpha_c = \frac{R_s}{4\pi Z_0}\left(\frac{1}{a} + \frac{1}{b}\right) \text{ [Np/m]} \tag{2.30}$$

which is the exact small-loss expression for coaxial lines. For air-filled lines ($\varepsilon_r = 1$), set $x = b/\alpha$:

$$\alpha_c \propto \frac{\frac{1}{a} + \frac{1}{b}}{\ln\left(\frac{b}{a}\right)} = \frac{\frac{1}{b} + \frac{1}{b}}{\frac{x}{\ln x}} = \frac{1 + \frac{1}{x}}{\ln x} \equiv f(x) \tag{2.31}$$

To minimize attenuation, differentiate $f(x)$ with respect to x and set $df/dx = 0$:

$$f'(x) = \frac{-\ln x - 1 - \frac{1}{x}}{x(\ln\ x)^2} = 0 \Rightarrow \ln x = 1 + \frac{1}{x} \tag{2.32}$$

The positive root is $x = b/a \approx 3.59$. Hence

$$Z_{0,\min \alpha_c} = 60 \ln(3.59) \approx 77\ \Omega \tag{2.33}$$

which corresponds to the minimum-loss impedance of an air-filled coaxial line.

The peak electric field at the inner conductor is:

$$E(a) = \frac{V}{a\ \ln\left(\frac{b}{a}\right)} = \frac{V}{\left(\frac{b}{x}\right)\ln x} \tag{2.34}$$

For a given breakdown field E_{bd}, the maximum voltage scales as:

$$V_{\max} \propto a\ \ln\left(\frac{b}{a}\right) = \frac{b}{x}\ln x \tag{2.35}$$

The transmitted power is:

$$P = \frac{V^2}{2Z_0} \tag{2.36}$$

Using $Z_0 \propto \ln\ x$, the maximum power handling capability is proportional to:

$$P_{\max} \propto \frac{(b/x)^2(\ln\ x)^2}{\ln x} = b^2\ \frac{\ln x}{x^2} \equiv g(x) \tag{2.37}$$

To maximize $g(x)$, differentiate and set $dg/dx = 0$:

$$g'(x) = \frac{1 - 2\ln x}{x^3} = 0 \tag{2.38}$$

Thus for $\ln x = \frac{1}{2}$, $b/a = e^{\frac{1}{2}}$ the impedance value becomes:

$$Z_{0,\max P} = 60 \ln\left(e^{\frac{1}{2}}\right) = 30\ \ \Omega \tag{2.39}$$

This corresponds to the maximum-power impedance.

The maximum voltage breakdown condition occurs when the electric field intensity at the inner conductor reaches the dielectric breakdown strength E_{bd} of the insulating medium. The radial electric field distribution for a TEM wave is:

$$E_r(r) = \frac{V}{r \ln\left(\frac{b}{a}\right)} \tag{2.40}$$

At the inner surface ($r = a$), the field reaches its maximum value:

$$E(a) = \frac{V}{a \ln\left(\frac{b}{a}\right)} \tag{2.41}$$

Dielectric breakdown occurs when $E(a) = E_{bd}$. Hence, the maximum permissible voltage before breakdown is:

$$V_{bd} = E_{bd}\, a \ln\left(\frac{b}{a}\right) \tag{2.42}$$

Setting $x = b/a$ and holding b constant ($a = b/x$) gives:

$$V_{bd} \propto \frac{b}{x} \ln x \equiv h(x) = \frac{\ln x}{x} \tag{2.43}$$

To find the value of x that maximizes the breakdown voltage, differentiate h(x) with respect to x and set $\frac{dh}{dx} = 0$:

$$h'(x) = \frac{1 - \ln x}{x^2} = 0 \Rightarrow \ln x = 1 \tag{2.44}$$

Thus:

$$x = \frac{b}{a} = e \approx 2.718 \tag{2.45}$$

The corresponding impedance is then

$$Z_{0,\max V} = 60 \ln\left(\frac{b}{a}\right) = 60 \ln(e) = 60\ \Omega \tag{2.46}$$

This impedance yields the maximum voltage breakdown limit of the coaxial geometry. Hence, the analytical results derived above for the conditions of minimum attenuation, maximum power handling and maximum voltage breakdown are illustrated in Figure 2.8, which

depicts the normalized variation of attenuation and power capability with characteristic impedance, clearly showing the engineering compromise that established the universally adopted 50 Ω standard for coaxial transmission lines.

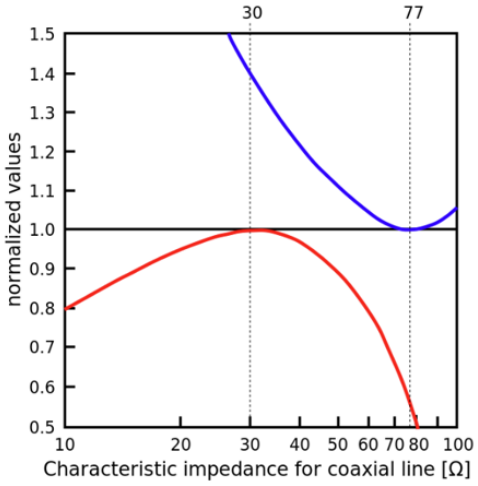


Figure 2.8: Normalized attenuation and power-handling characteristics of an air-filled coaxial line as a function of characteristic impedance

Consequently, considering the three fundamental constraints at 77 Ω, 30 Ω and 60 Ω, the 50 Ω characteristic impedance was adopted as a practical engineering compromise, representing an approximate average that optimally balances efficiency, power capability, and dielectric reliability in coaxial and planar transmission line systems.

Microstrip Line

The microstrip line is one of the most widely used types of planar transmission lines because it can be easily fabricated by photolithographic processes and directly integrated with both passive and active microwave components. Its simplicity, low cost, and compatibility with printed circuit technology make it ideal for modern amplifier and matching network design.

A microstrip line consists of a conducting strip of width Wprinted on a grounded dielectric substrate of thickness $h$and relative permittivity ε_r, as shown in Figure 2.9.

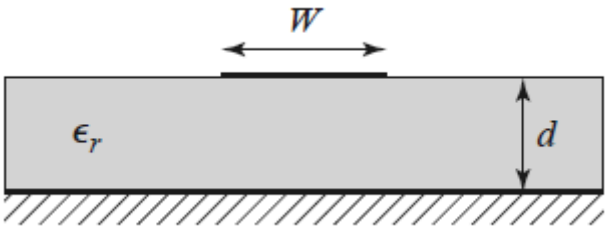


Figure 2. 9: Geometry of a microstrip transmission line
([10] page 148)

In the absence of the dielectric ($\varepsilon_r = 1$), the structure would behave as a simple flat two-wire line in air, supporting a TEM mode with phase velocity $v_p = c$and propagation con-

stant $\beta = k_0$. However, the presence of the dielectric substrate, which occupies only the region between the strip and the ground plane, alters the field distribution. Part of the electromagnetic field exists in the dielectric, while the rest extends into the air above it. As a result, the microstrip cannot support a pure TEM wave, since the phase velocity of fields in the dielectric region would be $c/\sqrt{\varepsilon_r}$while those in air propagate at c. The exact solution represents a hybrid TM-TE wave, but for most practical cases where the substrate is electrically thin ($h \ll \lambda$), the fields can be accurately described as quasi-TEM.

In this approximation, the line parameters can be obtained from quasi-static solutions. The effective dielectric constant ε_{eff}represents the dielectric constant of an equivalent homogeneous medium that replaces the two-layer (air–dielectric) structure. It satisfies:

$$1 < \varepsilon_{\text{eff}} < \varepsilon_r \tag{2.47}$$

and is expressed as [Pozar]:

$$\varepsilon_{\text{eff}} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(\frac{1}{\sqrt{1 + 12h/W}}\right) \tag{2.48}$$

The phase velocity and propagation constant are then:

$$v_p = \frac{c}{\sqrt{\varepsilon_{\text{eff}}}} \qquad \beta = k_0\sqrt{\varepsilon_{\text{eff}}} \tag{2.49}$$

where $k_0 = \omega/c$.

The characteristic impedance Z_0 of the microstrip line can be found from quasi-static field solutions. A widely used empirical expression is the Hammerstad–Jensen model:

$$Z_0 = \begin{cases} \dfrac{60}{\sqrt{\varepsilon_{\text{eff}}}} \ln\left(8\dfrac{h}{W} + 0.25\dfrac{W}{h}\right), & \text{for } \dfrac{W}{h} \le 1, \\ \dfrac{120\pi}{\sqrt{\varepsilon_{\text{eff}}}\left(\dfrac{W}{h} + 1.393 + 0.667\ln\left(\dfrac{W}{h} + 1.444\right)\right)} & \text{for } \dfrac{W}{h} \ge 1. \end{cases} \tag{2.50}$$

The effective dielectric constant and characteristic impedance depend primarily on the substrate permittivity and the geometry ratio W/h, allowing accurate impedance design for broadband microwave circuits.

Attenuation and Loss Mechanisms

Losses in a microstrip line arise from two main mechanisms: dielectric loss and conductor loss. The dielectric loss is associated with the substrate material and can be approximated by [Pozar]:

$$\alpha_d = k_0\varepsilon_r \frac{(\varepsilon_{\text{eff}} - 1)}{2\sqrt{\varepsilon_{\text{eff}}}(\varepsilon_r - 1)} \tan\ \delta[\text{Np/m}] \tag{2.51}$$

where $\tan\delta$ is the dielectric loss tangent. The conductor loss, due to finite conductivity and surface resistance, is given by [Pozar]:

$$\alpha_c = \frac{R_s}{Z_0 W} \text{[Np/m]} \tag{2.52}$$

where $R_s = \sqrt{\omega\mu_0/2\sigma}$ is the surface resistivity of the conductor.

Current Handling and Skin Effect

In high-power designs, such as amplifier driver stages, the current-handling capability of the microstrip is critical. The maximum DC current the trace can safely carry is governed by heating limits and can be approximated using IPC-2152 empirical data:

$$I_{\text{MAX}} = (k - T_{\text{RISE}}^{b}) A^{c} \tag{2.53}$$

where $A = T \cdot W \cdot 1.378$ [mils/oz/ft²] is the conductor area, T_{RISE} is the allowable temperature rise, and constants k, b, c depend on whether the trace is external or internal.

At microwave frequencies, this current distribution becomes nonuniform due to the skin effect, which confines current to a thin layer at the conductor surface. The skin depth δ, representing the depth at which current density decays to $1/e$of its surface value, is:

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{2.54}$$

and decreases with increasing frequency. As a result, the effective conductive area becomes approximately $W \cdot \delta$, increasing resistive losses and limiting current capacity. At 352 MHz, for copper ($\rho = 1.72 \times 10^{-8}$), the skin depth is approximately 3.5 μm, which is much smaller than typical copper thicknesses used in microwave PCBs.

Coplanar waveguide

The coplanar waveguide (CPW) is a planar transmission line consisting of a central conducting strip separated by narrow slots from two adjacent ground planes on the same surface of a dielectric substrate. This configuration supports a quasi-TEM mode of propagation, where both the electric and magnetic fields are primarily concentrated in the region between the center conductor and the adjacent ground planes. A typical geometry of a CPW is defined by the center conductor width a, the distance between the ground planes b, and the substrate height h.

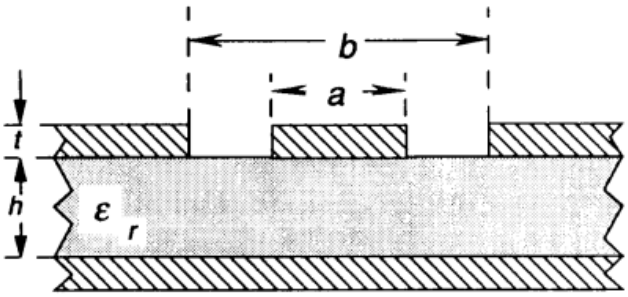


Figure 2. 10: Geometry of a coplanar waveguide[11]

Because all conductors lie on the same plane, CPWs offer easy integration of shunt and series components, direct access to ground, and compatibility with monolithic microwave integrated circuit (MMIC) processes. The analysis of the CPW structure is based on conformal mapping, which transforms the cross-section into an equivalent parallel-plate geometry. Using this method, the characteristic impedance $Z_0$and effective dielectric constant ε_{eff}can be expressed in terms of complete elliptic integrals of the first kind, $K(k)$and $K(k')$:

$$Z_0 = \frac{60\pi}{\sqrt{\varepsilon_{\text{eff}}}} \frac{1}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k_1')}} \tag{2.55}$$

Where

$$k = \frac{a}{b}, k' = \sqrt{1-k^2}, \qquad k_1 = \frac{\tanh\left(\frac{\pi a}{4h}\right)}{\tanh\left(\frac{\pi b}{4h}\right)}, \qquad k_1' = \sqrt{1-k_1^2} \tag{2.56}$$

The effective dielectric constant is given by:

$$\varepsilon_{\text{eff}} = \frac{1 + \varepsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}{1 + \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}} \tag{2.57}$$

Here, $K(k)$and $K(k')$denote the complete elliptic integrals of the first kind, defined as:

$$K(k) = \int_0^{\frac{\pi}{2}} \frac{d\theta}{\sqrt{1 - k^2 sin^2\theta}} \tag{2.58}$$

These relations accurately describe the field confinement and propagation characteristics of coplanar waveguides across a wide range of geometries and dielectric constants.

2.2.4 Microstrip discontinuities modelling

In practical microwave circuits, microstrip transmission lines often exhibit geometric discontinuities such as abrupt width changes, bends, or junctions. These discontinuities disturb the quasi-TEM field distribution, causing localized energy storage in the form of parasitic inductance and capacitance. As a result, they introduce impedance mismatches, signal reflections, and phase distortions that must be accurately modeled for high-frequency design. To predict their electrical behavior, such discontinuities are commonly represented by equivalent lumped-element circuits derived from empirical or semi-analytical formulations.

Abrupt Change in Width

An abrupt change in microstrip width introduces a step discontinuity, which disturbs the quasi-TEM field distribution, resulting in localized electric and magnetic energy storage. The transition can be either symmetric (equal substrate thickness on both sides) or asymmetric (step in conductor width without geometric symmetry), as shown in Figure 2.11. These discontinuities are typically modeled by an equivalent lumped-element network that captures their reactive behavior.

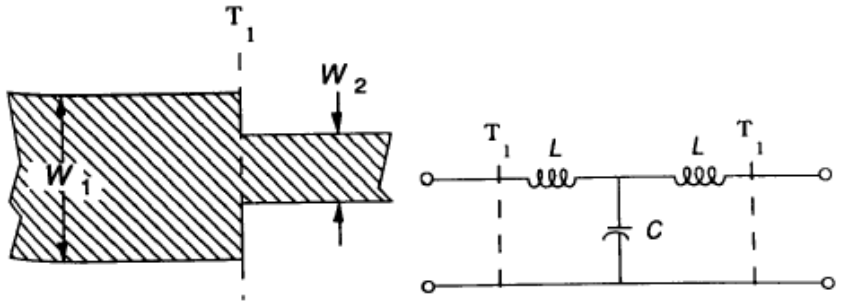


Figure 2.11: Microstrip line step (abrupt change in width) and equivalent circuit.

([11] page 315)

For a step transition from a line of width $W_1$to W_2, the junction can be represented by the equivalent π-network shown in Figure 2.11, consisting of a shunt capacitance C_s and series inductances L_s that account for the stored energy at the discontinuity.
For symmetric steps ($1.5 \leq W_1/W_2 \leq 3.5$) and $\varepsilon_r \leq 10$, Wadell [1] provides the following empirical design equations:

$$C_s = \sqrt{W_1 W_2}\left[(10.1\log\varepsilon_r + 2.33)\frac{W_1}{W_2} - 12.6\log\varepsilon_r - 3.17\right]\text{[pF/m]} \qquad (2.59)$$

For $3.5 \leq W_1/W_2 \leq 10.0$and $\varepsilon_r = 9.6$:

$$C_s = \sqrt{W_1 W_2}\left[130.0\log\left(\frac{W_1}{W_2}\right) - 44.0\right]\text{[pF/m]} \qquad (2.60)$$

The equivalent inductance per unit length is:

$$L_s = h\left[40.5\left(\frac{W_1}{W_2} - 1.0\right) - 75.0\log\left(\frac{W_1}{W_2}\right) + 0.2\left(\frac{W_1}{W_2} - 1.0\right)\right] \text{[nH/m]} \tag{2.61}$$

These expressions are accurate within approximately 5% for $W_1/W_2 \leq 5.0$. The total effect of the step can thus be described by:

$$Z_{\text{eq}} = j\omega L_s + \frac{1}{j\omega C_s} \tag{2.62}$$

indicating a reactive impedance that depends on both the width ratio and dielectric constant.

Microstrip Line Bends

Another common discontinuity in planar transmission lines is the right-angle bend in a microstrip trace. The bend introduces a localized disturbance in the electromagnetic field distribution, resulting in stored reactive energy that can be modeled using a lumped-element equivalent circuit consisting of a series inductance $L$and a shunt capacitance C, as shown in Figure 2.X.

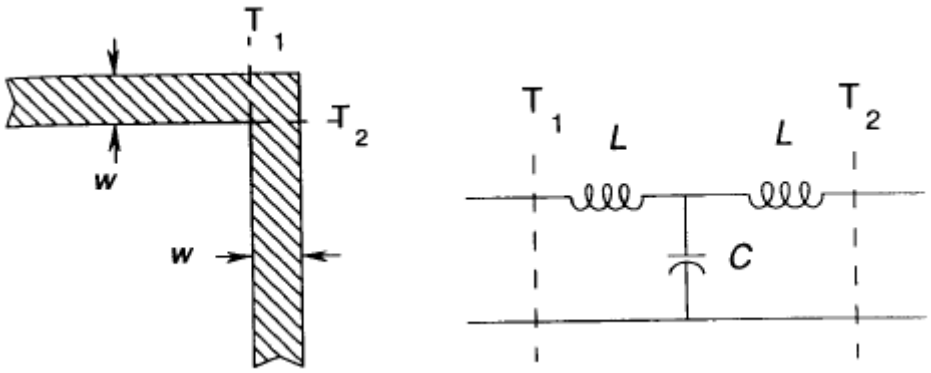


Figure 2.12: Microstrip line right-angle bend and equivalent circuit

([11] page 287)

The equivalent parameters describing the discontinuity are given empirically by Wadell [1] as follows:

For $w/h < 1$:

$$\frac{L}{h} = 100.0\left(4.0\sqrt{\frac{w}{h}} - 4.21\right) \text{[nH/m]} \tag{2.63}$$

$$\frac{C}{w} = \frac{(14.0\,\varepsilon_r + 12.5)\left(\frac{w}{h}\right) - (1.83\,\varepsilon_r - 2.25)}{\sqrt{\frac{w}{h}}} + 0.02\,\varepsilon_r\,\frac{w}{h} \text{[pF/m]} \tag{2.64}$$

and for $w/h \geq 1$:

$$\frac{C}{w} = (9.5\,\varepsilon_r + 1.25)\left(\frac{w}{h}\right) + 5.2\,\varepsilon_r + 7.0[\text{pF/m}] \tag{2.65}$$

These equations are accurate to within 5 % for $2.5 \leq \varepsilon_r \leq 15.0$ and $0.1 \leq w/h \leq 5.0$. Later, there were proposed refined closed-form approximations valid for $2.0 \leq \varepsilon_r \leq 13.0$ and $0.2 \leq w/h \leq 6.0$, which achieve an agreement with measured data within 0.3 %:

$$C = 0.001\,h\,[(10.35\,\varepsilon_r + 2.5)\left(\frac{w}{h)^2} + (2.6\,\varepsilon_r + 5.44)\left(\frac{w}{h}\right)\right][\text{pF}] \tag{2.66}$$

$$L = 0.22\left[1.0 - 1.35\,e^{-0.18\,(w/h)^{1.39}}\right][\text{nH}] \tag{2.67}$$

The right-angle bend, therefore, introduces both capacitive and inductive parasitic effects, leading to small impedance mismatches and phase errors at high frequencies. These effects become more pronounced as the electrical length of the bend approaches a significant fraction of the wavelength. In practical designs, mitigation techniques such as mitered bends or curved corners are used to minimize these discontinuity effects and maintain good impedance matching.

2.2.5 Stability

The stability of a transistor amplifier is governed by the behavior of its input and output reflection coefficients, $\Gamma_{in}$and Γ_{out}, which depend on the device's scattering parameters and the source and load terminations. If either $|\,\Gamma_{in}\,| > 1$or $|\,\Gamma_{out}\,| > 1$, the circuit exhibits a negative resistance and can oscillate, rendering it unstable. To ensure reliable amplifier operation, the stability condition must be evaluated across all frequencies of interest and under various terminations.

A convenient analytical approach to assess stability is through Rollet's stability factor (K) and the determinant (Δ), derived directly from the two-port scattering matrix. These parameters provide necessary and sufficient conditions for unconditional stability, defined as stability for all passive source and load impedances ($|\,\Gamma_S\,| < 1$ and $|\,\Gamma_L\,| < 1$). They are expressed as:

$$K = \frac{1 - |\,S_{11}\,|^2 - |\,S_{22}\,|^2 + |\,\Delta\,|^2}{2\,|\,S_{12}S_{21}\,|} \qquad \Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.68}$$

For a transistor to be unconditionally stable, the following two inequalities must hold simultaneously:

$$K > 1, |\,\Delta\,| < 1 \tag{2.69}$$

These conditions guarantee that both the input and output ports present positive resistances for all passive terminations. If either condition is violated, the device becomes conditionally stable, and graphical techniques such as stability circles must be employed to identify the safe operating regions for $\Gamma_S$and Γ_L.

In addition to K and Δ, alternative stability factors μ_s and μ_l are also used to assess stability more precisely, especially near the boundary between stable and unstable operation. They are defined as:

$$\mu_S = \frac{1-|S_{11}|^2}{|S_{22}-\Delta S_{11}^*|+|S_{12}S_{21}|} \quad \mu_L = \frac{1-|S_{22}|^2}{|S_{11}-\Delta S_{22}^*|+|S_{12}S_{21}|} \tag{2.70}$$

For unconditional stability, the following conditions must be satisfied:

$$\mu_S > 1, \mu_L > 1 \tag{2.71}$$

These parameters provide a more intuitive numerical measure of stability margin — values significantly greater than 1 indicate a well-stabilized design, while values near or below 1 suggest potential oscillation risk.

2.3 Power Amplifiers

Power amplifiers are essential components in RF systems, as they provide the high output power levels needed to drive accelerator cavities, antennas, or other loads. In accelerator applications, RF power amplifiers are typically designed to operate either in continuous wave (CW) mode or in pulsed mode. CW operation delivers constant RF power to the cavities and requires extremely efficient cooling systems to manage the continuous thermal load. Pulsed operation, as implemented at ESS, delivers high peak power during short time intervals, significantly reducing the average power consumption and easing cooling requirements. However, pulsed systems must maintain excellent stability during the pulse rise and fall times, avoid transient distortions, and ensure that the duty cycle does not compromise component lifetime or reliability.

2.3.1 MOS and LDMOS Transistors

Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) are widely used in RF amplification due to their high input impedance, ease of integration, and good linearity. A specialized version, the Laterally Diffused MOSFET (LDMOS), is the dominant device technology in high-power RF applications below a few gigahertz.

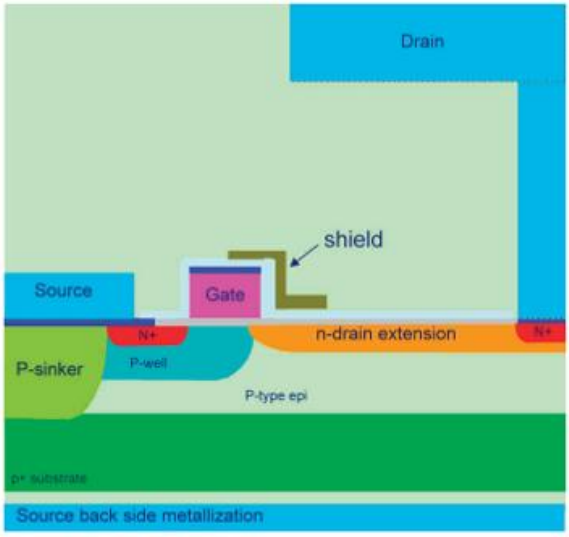


Figure 2. 13:LDMOS diagram[12]

The Laterally Diffused Metal–Oxide–Semiconductor (LDMOS) field-effect transistor constitutes one of the most mature and widely adopted device technologies for high-efficiency RF power amplification. Its ability to simultaneously achieve high gain, high breakdown voltage, and robust thermal performance has established it as the device of choice for base-station transmitters, industrial and medical RF systems, and radar applications. Figure 2.5 illustrates a schematic cross-section of a representative LDMOS device, highlighting the critical regions that define its electrical and thermal behavior.

The LDMOS transistor is a lateral device, in which current conduction occurs horizontally along the surface of a silicon wafer from the source to the drain. The structure is typically fabricated on a heavily doped p^+ silicon substrate, upon which a lightly doped p-type epitaxial layer is grown to accommodate the lateral expansion of the depletion region under high-voltage operation. The source region is formed by a heavily doped n^+ diffusion, while the gate electrode, controls the carrier density in the underlying p-well. The drain region is located laterally across the device and is connected to the channel through a lightly doped n-type drift or drain extension region. This drain extension is a defining feature of the LDMOS architecture: it enables the device to sustain large drain–source voltages by distributing the electric field horizontally rather than vertically, thereby enhancing the breakdown voltage.

The p-well underneath the gate defines the transistor's channel. When a positive gate-to-source voltage is applied, an inversion layer is formed at the silicon–oxide interface, creating an n-type conductive path that connects the source and the drain extension. Electrons injected from the source are accelerated by the electric field along this channel and traverse the drift region before being collected at the drain. The gate voltage thus modulates the electron concentration in the channel, controlling the drain current according to the square-law or velocity-saturation models, depending on the biasing regime, as shown in the following equation. The device therefore acts as a voltage-controlled current source, where small variations in gate potential induce proportionally large variations in drain current.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{2.72}$$

A feature of the LDMOS structure is the inclusion of a metallic shield between the gate and the drain extension, and electrically connected to the source. This shield performs two essential functions: it suppresses the parasitic gate–drain feedback capacitance, thereby improving gain and stability at microwave frequencies, and it redistributes the electric field in the drain extension region to mitigate hot-carrier degradation and premature avalanche breakdown.

The p-sinker region provides a low-resistance vertical connection between the source and the heavily doped p^+ substrate, which in turn is metallized on the backside to form the global ground terminal. This configuration ensures minimal source inductance and efficient heat removal from the active region to the package or heat sink. The drain metallization is designed to support high current densities and large RF voltage swings; it typically consists of multiple thick metal layers to minimize on-resistance and electromigration, while simultaneously enhancing thermal conduction.

The operation of the LDMOS transistor in amplification mode is governed by the electrostatic control of the inversion channel by the gate and the lateral transport of electrons across the surface. Under quiescent bias, the gate is maintained at a DC potential slightly above the threshold voltage, such that the device operates in class AB mode, conducting for slightly more than half of the RF cycle. The superposition of the RF input signal on the gate bias modulates the channel charge density, producing a time-varying drain current that mirrors the input waveform. This modulated drain current, when flowing through the output

matching network and load impedance, gives rise to a large RF voltage swing at the drain, thus generating amplified power at the output.

The device's drain efficiency, defined as the ratio of RF output power to total DC power consumption, depends on both conduction losses and capacitive charging losses in the drain extension. The attainable efficiency is fundamentally constrained by the trade-off between the drift region length, which determines breakdown voltage, and the series resistance and parasitic capacitances, which govern conduction and switching losses.

The geometrical proportions of the device are therefore central to its performance. The gate length dictates the transit time of carriers and thus the upper frequency limit, while the drain extension length governs the voltage-handling capability. The incorporation of field plates and shield structures enables further optimization of this trade-off by shaping the electric field to reduce peak intensity without compromising lateral conduction. The overall design ensures that the LDMOS transistor can sustain large voltage swings, achieve high current densities, and maintain linearity under RF excitation.

In essence, the LDMOS transistor realizes power amplification through the precise electrostatic modulation of a laterally conducted electron flow. The combination of a short gate for high transconductance, an extended drift region for voltage robustness, and a shielded architecture for field control allows the device to attain exceptional performance in terms of efficiency, gain, and reliability. Electrons move laterally from the source to the drain under the influence of both gate and drain electric fields, while the structural innovations in the device geometry ensure that this process occurs with minimal parasitic losses and excellent thermal stability. As a result, LDMOS technology provides the optimal balance between high power capability, cost-effectiveness, and scalability, securing its position as the leading solution for RF and microwave power amplification

2.3.2 RF Power Definitions

The performance of an RF power amplifier is evaluated through a set of key parameters that quantify how effectively it converts DC power into RF output power. These parameters are essential for understanding the amplifier's behavior and for making design trade-offs between efficiency, linearity, cost, and complexity.

Input Power

The RF power applied to the input of the amplifier, defined as P_{in}. It serves as the reference for calculating gain and efficiency metrics.

Output Power

The RF power delivered to the load. It can be measured either in watts (W) or decibel-milliwatts (dBm). Their relation is given by:

$$P_{dBm} = 10\log_{10}\left(\frac{P_W}{1\ mW}\right) = 10\log_{10}(P_W) + 30 \tag{2.73}$$

Gain

The ratio of output power to input power, indicating how much the amplifier increases the signal strength. It is commonly expressed in decibels (dB) as:

$$G = 10 \log_{10} \frac{P_{out}}{P_{in}} \tag{2.74}$$

Efficiency

It is defined as RF output power over DC input power; commonly, the Drain Efficiency and Power-Added Efficiency (PAE) are used. The Drain Efficiency is given by:

$$n_D = \frac{P_{out}}{P_{DC}} \, x \, 100\% \tag{2.75}$$

A more comprehensive efficiency metric that accounts for the input RF power is Power Added Efficiency (PAE). PAE is particularly useful for comparing amplifiers with different gains, as it reflects how much additional RF power is generated beyond what is supplied at the input.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \times 100\% \tag{2.76}$$

Linearity

The ability of the amplifier to preserve the spectral purity of the input signal, avoiding distortion and unwanted harmonics. These definitions are central for analyzing the trade-offs between performance, cost, and complexity in amplifier design.

When the goal is to achieve maximum output power, the amplifier is typically driven into the saturation region, where the active device delivers its maximum possible output. As the input power increases, amplifiers eventually reach saturation, where further input power does not result in proportional output increase but introduces significant nonlinearities. These nonlinearities result in harmonic distortion, the creation of frequency components at integer multiples of the input frequency and intermodulation distortion when multiple tones are present. Both effects degrade the spectral purity of the transmitted signal and can cause spectral regrowth, violating emission masks and interfering with neighboring channels. The transition from the linear to the nonlinear region is often characterized by the 1 dB compression point (P_1dB), the input level at which the amplifier's gain decreases by 1 dB from its small-signal value.

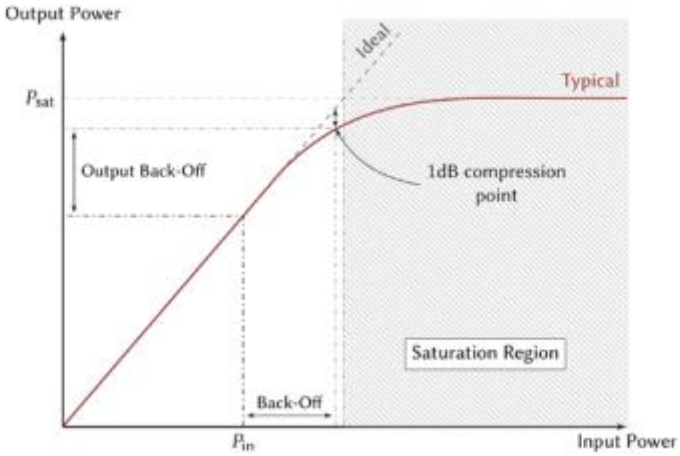


Figure 2.14: Amplifier operating regions[13]

2.3.3 Classes of Operation (A, B, AB)

Power amplifiers are classified by the conduction angle of the active device during one RF cycle:

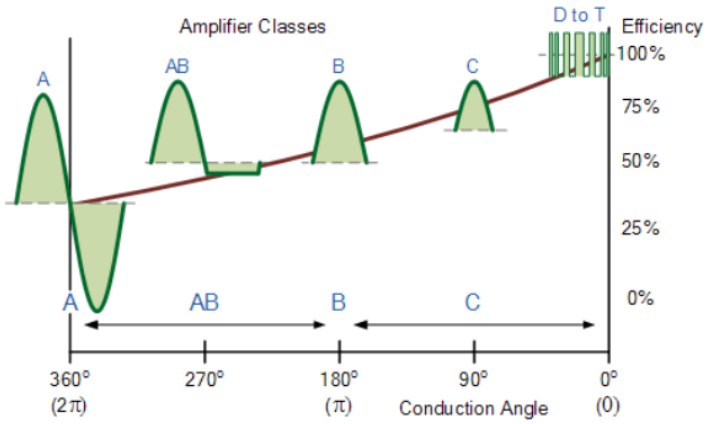


Figure 2. 15: Amplifier classes of operation[14]

- **Class A**: The device conducts for the entire cycle (360°). Offers maximum linearity but poor efficiency. The operating point of the transistor is set high enough so that it is never driven into its cut-off region.
- **Class B**: The device conducts for half the cycle (180°) as the device is biased at the cutoff point and does not conduct for the full waveform. Efficiency is improved (~78.5%) but with increased distortion.
- **Class AB**: A compromise between A and B, where conduction is slightly more than 180°. Provides good efficiency and acceptable linearity, making it the most common choice for RF power amplifiers in accelerator applications.

2.3.4 Power Amplifiers Applications in Accelerators

In particle accelerators, RF power amplifiers generate the electromagnetic fields that accelerate charged particles inside the cavities. The required RF power per cavity can range from tens of kilowatts to several megawatts, depending on the accelerator's architecture and beam dynamics. Historically, high-power RF generation has relied on vacuum tube technologies such as klystrons and tetrodes, which are capable of delivering very high power but are constrained by efficiency, lifetime, and maintenance complexity[15], [16].

Recent advances in semiconductor technology have led to the widespread adoption of Solid-State Power Amplifiers based on LDMOS transistors, which offer enhanced efficiency, modularity, and reliability[17], [18]. As detailed by [19], [20], SSPAs have evolved from early prototypes into mature systems capable of delivering continuous-wave power levels of several hundred kilowatts at frequencies from 88 MHz to over 1 GHz. High-power Solid-State Power Amplifiers have gained significant attention in accelerator RF systems over the past two decades, gradually replacing vacuum tube technologies. Compared to traditional tube-based transmitters, SSPAs offer high modularity, redundancy, maintainability, and do not require high-voltage operation. Leveraging advancements in semiconductor processes, especially with laterally diffused metal oxide semiconductor (LDMOS) devices, modern SSPAs can deliver high RF power with improved efficiency and reduced noise levels.[21]

The first large-scale application of SSPAs in particle accelerators was pioneered at the Synchrotron SOLEIL in France, where 35 kW and 190 kW amplifiers based on 330 W MOSFET modules have been successfully operating since 2004[21]. Following this success, several major facilities adopted solid-state transmitters for their RF systems: 150 kW SSPAs at 352.2 MHz for the European Synchrotron Radiation Facility [22] 65 kW at 500 MHz for the Swiss Light Source [23] and 50 kW at 476 MHz for the Brazilian Synchrotron Light Laboratory [24]. Further deployments include 80 kW systems at 500 MHz for SESAME and NSRRC, and a 2 MW solid-state system at 200 MHz for CERN's SPS.

Recent projects have continued to push the boundaries of solid-state RF technology. The High Energy Photon Source (HEPS) in Beijing, a 6 GeV diffraction-limited storage ring, has adopted solid-state technology across all its RF stations, including the development of a modular 166.6 MHz 50 kW and a 499.8 MHz 260kW prototype under the HEPS Test Facility program [25], [26]. The IHEP-ADS project similarly integrates 10–150 kW SSPAs at 325 and 650 MHz to drive superconducting spoke cavities in its injector linac, forming one of the first large-scale solid-state implementations in Asia [18].

Parallel research at the FREIA Laboratory, Uppsala University, has focused on developing high-efficiency LDMOS-based amplifiers and advanced power-combining structures for ESS-related applications[27]. The European Spallation Source (ESS) in Lund employs 400 kW, 352.21 MHz SSPAs to feed 26 superconducting spoke cavities. Similarly, CERN's Linac4 uses 80–160 kW 352.2 MHz solid-state transmitters composed of fifty 1.6 kW modules combined through coaxial combiners, marking a complete transition from klystrons to solid-state RF amplification [16]. Integration of such amplifiers with advanced low-level RF (LLRF) systems, as implemented at facilities like the European XFEL, demonstrates how solid-state transmitters support the high reliability, maintainability, and digital control required for modern accelerator operations [28].

Through these efforts, solid-state amplification has proven to be a reliable, scalable, and energy-efficient solution for modern accelerator RF systems, supporting long-term sustainability and operational robustness in next-generation synchrotron and linear accelerator facilities.

Facility	Location	Frequency	Power level	Amplifier Type
ESS	Lund, Sweden	352.21 MHz	400 kW per cavity	SSPA (LDMOS-based)
Linac4 (CERN)	Geneva, Switzerland	352.2 MHz	80–160 kW	SSPA (50 × 1.6 kW modules)
SNS	Oak Ridge , USA	402.5 / 805 MHz	550 kW (klystron), 10 kW (SSPA drivers)	Hybrid / SSPA upgrade
IHEP / ADS Project	Beijing, China	325 / 650 MHz	10–150 kW	SSPA (LDMOS, modular)
HEPS (High Energy Photon Source)	Beijing, China	166.6 / 499.8 MHz	50–260 kW	SSPA (BLF188XR LDMOS)
DESY (PETRA IV / XFEL / FLASH)	Hamburg, Germany	1.3 GHz	10–120 kW	SSPA
SOLEIL Synchrotron	Gif-sur-Yvette, France	352.2 MHz	35 kW, 190 kW	SSPA

Table 3: Solid-State Power Amplifiers in Accelerator RF Systems

Chapter 3: System description of 400kW SSPA

3 Introduction

In this chapter, the 400 kW SSPA system is explained. The architecture choice is analyzed, and the function and component selection of each block are examined. I also worked on the Bill of Materials for the system, and the results of this work will be presented. All prices mentioned in this chapter are accurate as of April 2024.

3.1 Overview

The ESS LINAC is comprised of 26 spoke cavities, each requiring 400 kW of RF power at 352.21MHz[1]. To meet the energy needs of this part of the LINAC, we will use 26 SSPA systems, each with an output of 400 kW. As discussed in the previous chapter, power amplifiers have physical limitations on how much they can amplify the input power we provide. Therefore, a decision needs to be made on how to amplify the input power of 1 mW to 400 kW. After considering the power needs, the physical limitations of the amplifiers, and the options supported by the market, we concluded that this architecture is the best solution:

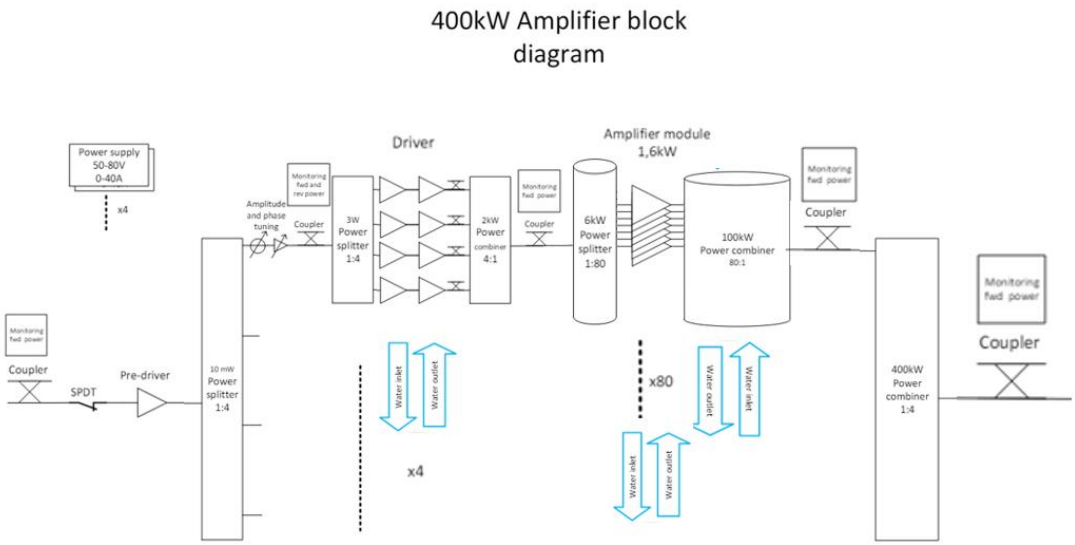


Figure 3.1: Block diagram of the 400kW SSPA system

As we can see, the system is composed of five different amplifying stages: the predriver, the amplitude tuner, the driver's first stage, the driver's second stage, and the main power ampli-

fier. All of these work in multiple parallel stages to ensure reliability and optimize output power. Throughout the system, couplers provide sufficient information about the operational conditions, allowing us to monitor the process.

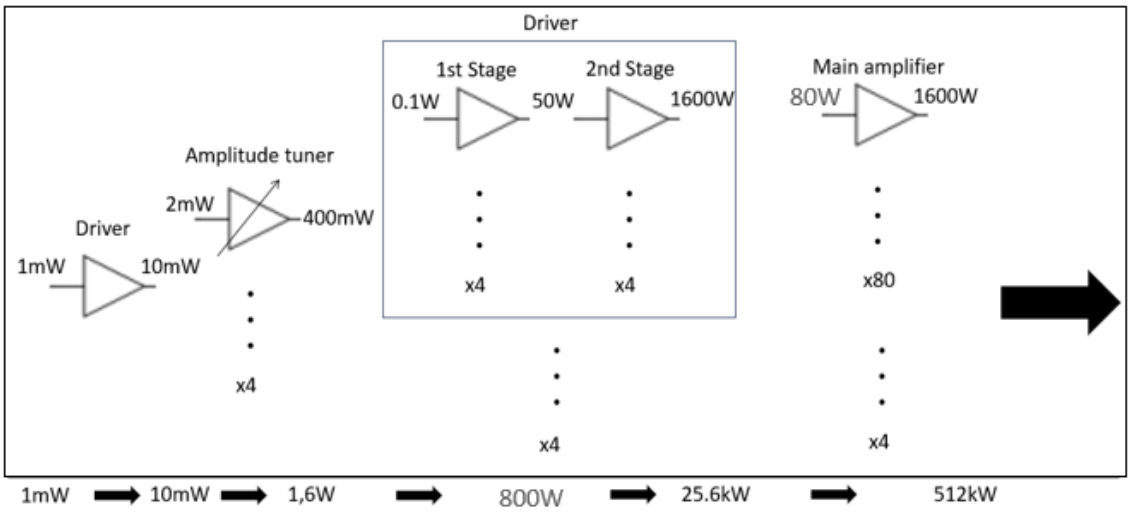


Figure 3.2: Power per stage estimation of the 400kW SSPA system

Above we can see a power budget estimation of the entire system with the input and output of each amplifier and below the sum of power at each stage. Based on this architecture and power estimations we will try to find the components that can satisfy the specifications of the system.

3.2 Input block

The input block is the first part of the system and is comprised of: a coupler to monitor the input power, a Single-Pole Double Throw switch to protect the system from possible overload, a predriver to start the amplifying process of the system and finally a 1:4 power splitter to split the power at the end of this stage to 4 in parallel operating driver blocks.

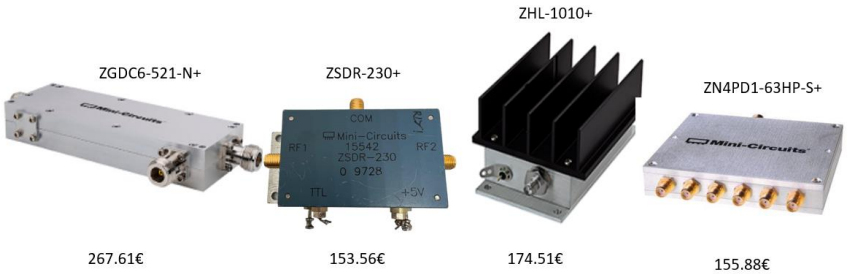


Figure 3.3: List of components with manufacturer reference and price for Input block

Above we can see pictures of the chosen components with the manufacturer reference and the price in euros. The components listed in this report are a courtesy of: Minicircuits. This block has a total cost of 751.55€. To choose these components, and every component in this

thesis, we looked at the datasheet of every component, it provides enough information to understand if the product fulfills our needs.

This block has an input of 1mW and amplifies it to 10mW. All of these components, as they are operating on low power already exist on the market so there is no need to design anything new. As we start searching the market for available solutions, we need to know what the important characteristics of a coupler are so as to be able to fulfill our needs.

The first important parameter that we consider is the frequency of operation. It is vital to choose a component that can operate in our frequency, as there are many different types of couplers based on wavelength. Next, we consider insertion loss. This parameter shows us how much power is dissipated when using this component. We need it to be as low as possible. A closely connected parameter with this is directivity. Directivity of coupler shows us its ability to differentiate between forward or reverse power which is important as there are always reflections in RF systems. Another important parameter is power handling. Since our application has very high-power demands, we need couplers that can operate at that power level without degradation or failure.

3.3 Driver stage

The driver stage is the block that this thesis focuses on. In particle accelerators the driver is a vital part of an RF system that provides enough power to the cavities to accelerate the beam. The system is comprised of an amplitude tuner, a phase tuner, a 1:4 power divider, the driver's 1st stage, the driver's 2nd stage, a 4:1 power combiner and three directional couplers. There are four systems of this type working in parallel.

Figure 3. 4: List of components with manufacturer reference and price for Driver's block

The reason behind using tuners is to ensure that the electromagnetic power that we will feed the modules covers our specifications to avoid any failure or sparks while we are in operation. The amplitude tuner is comprised of an amplifier, the same amplifier used for driver's 1st stage for reasons explained in the next chapters and a variable attenuator to control the output power. Then, a power divider provides power to 4 amplifiers working in parallel, the driver's 1st stage who then feeds the driver's 2nd stage and finally the power is combined before being forwarded to next stage. A directional coupler is placed after the amplitude tuner, the driver's 2nd stage and the power combiner. This is done to provide monitoring ability of the amplifying process in case of failures and to measure insertion losses.

Below we can see the driver's 1st stage:

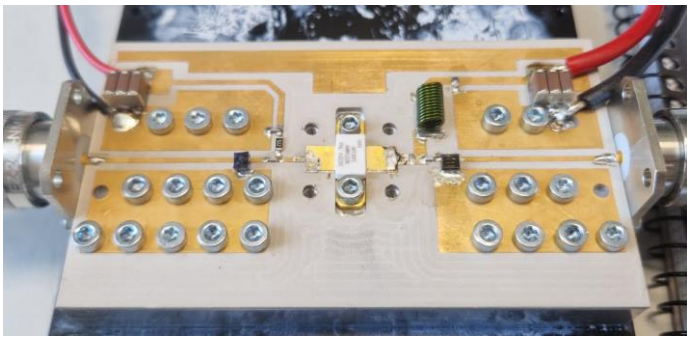


Figure 3.5: Driver's 1st stage

3.4 Main amplifier

This block is the last part of the amplifying chain and the biggest contributor to the overall produced power. Below we can see a picture of a module manufactured in the ESS RF lab:

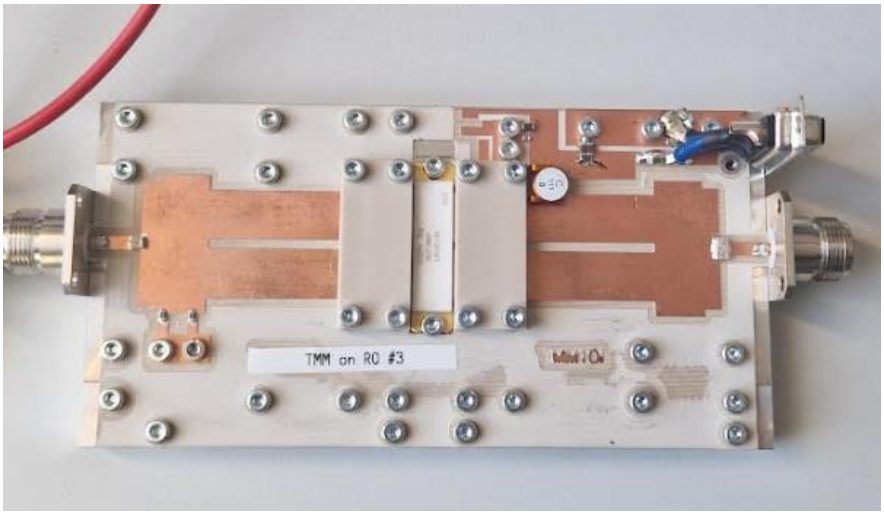


Figure 3.6: Driver's 2nd stage

The power splitter and combiner needed for this block are both designed by Uppsala university. There are no available options in the market able to serve at this power level. This amplifier receives power from the driver and delivers up to 2.5kW of pulsed RF power.

3.5 Output block

The last block of the SSPA system is comprised of four couplers, one for each of the 4 different main amplifier blocks, to monitor the power forwarded to the power combiner. For

these components a special order will be placed at MEGA, an RF hardware manufacturer. The last power combiner has to be able to combine 4 input ports of 100kW power and deliver it to the spoke cavity. Because the handling power needed is very high, a new combiner will be designed specifically for this purpose by the ESS RF power sources group. Lastly, before providing the power to the spoke cavities we connect in series a high-power coupler in order to monitor the process and protect against arcs.

3.6 Monitoring systems, cooling systems and Supporting hardware

There are some more issues that need to be assessed:

1. The information provided by the couplers is processed by the monitoring systems that will be designed by the ESS RF sources group.
2. The amplifiers are put under a lot of stress during the soak tests, and produce a lot of heat. Thus, we need to take into consideration the cooling systems that are going to dissipate the heat produced. The ESS RF lab is equipped with water cooling systems.
3. The Bill of Materials also includes essential components required for system functionality, such as N-type connectors, protective capacitors for the main amplifier, equipment racks, and necessary cabling.

3.7 Summary

The Bill of Materials (BoM) was created to: have a proper estimation of the total cost, to organize all the information gathered so far for the architecture of the project and for the author to gain experience and understanding of the RF components and their datasheet. The total cost was valued at 534.024,79 €. The BoM includes:

1. Manufacturer
2. Manufacturer reference
3. Provider
4. Price per unit
5. Price of sum of units
6. Datasheet
7. Link to URL adress of supplier

Chapter 4: Designing Driver's 1st stage schematic

4 Introduction

In this chapter, we analyze the process of designing the Driver's first-stage. We discuss the transistor selection and choose the amplifier topology at the schematic level using Advanced Design System (ADS) from Keysight.

4.1 Transistor choice

In this sub-chapter, a brief overview of available transistor technologies is provided, along with the reasons for selecting LDMOS technology for the transistor material.

4.1.1 Material Choice

Below is a survey of ETH university [29] a frequency-power diagram comparing various existing technologies based on these two parameters, indicating for which set of frequency and power each technology is applicable:

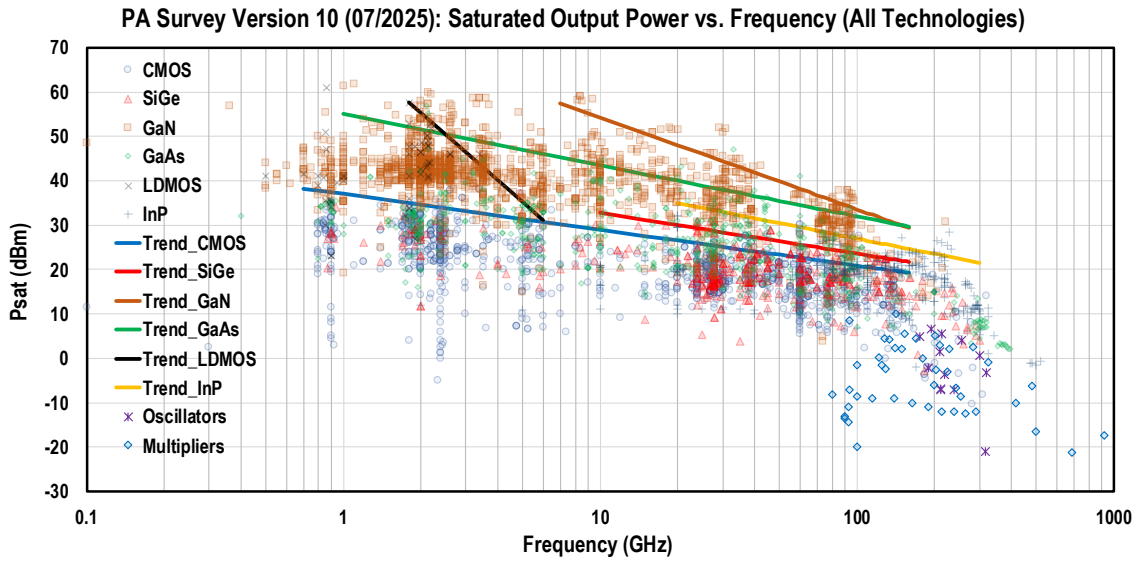


Figure 4.1: Comparison of Semiconductor Technologies for Different Materials [[29]]

To choose which of these materials and which transistor is best suited for our system, we need to take a look on the design specifications. They are listed on the table below:

Design Parameters	Design Specification
Frequency	352.21 MHz
Input Power	20 dBm
Output Power (max)	47dBm
Gain	27 dB
Typical Drain efficiency	60%

Table 4: Design Specifications

4.1.2 Device choice

The transistor that was chosen is ART35FE by Ampleon. Ampleon is a company that specializes in manufacturing hardware solutions for RF applications like transistors, amplifiers and radars. They recently designed a new series of transistors based on Advanced Rugged Technology (ART). The ruggedness of a transistor is a way of characterizing its ability to withstand harsh operating conditions, such as high temperatures, voltage spikes, mismatch of the impedances and high current handling without degradation or failure. Our transistor boasts excellent ruggedness, high efficiency and the provider has committed to manufacturing it for at least 15 more years[30]. The longevity of supply for a product is crucial because it ensures viability for the accelerator industry, where systems are designed for use of at least five years. This commitment means that in case of failure, we do not have to worry about running out of transistors. The specifications that led to the selection of this transistor are shown in the table below[31]:

Parameters	Transistor Specifications
Frequency range	1-650 MHz
Typical Efficiency at 108 MHz	70%
Typical Gain at 108 MHz	30 dB
Typical Output power	35W
Maximum Qualified Drain Voltage	65V
Maximum Qualified Gate Voltage	2.5V

Table 5: Specifications of chosen transistor

Here we can see two graphs provided by the datasheet of the transistor for operation at frequency of 108MHz and Drain voltage of 65 V for different values of Drain-Source current. The left graph is a function of Gain, G_P in dB with output power, P_L in W and the right graph is a function of efficiency, n_D with output power, P_L in W:

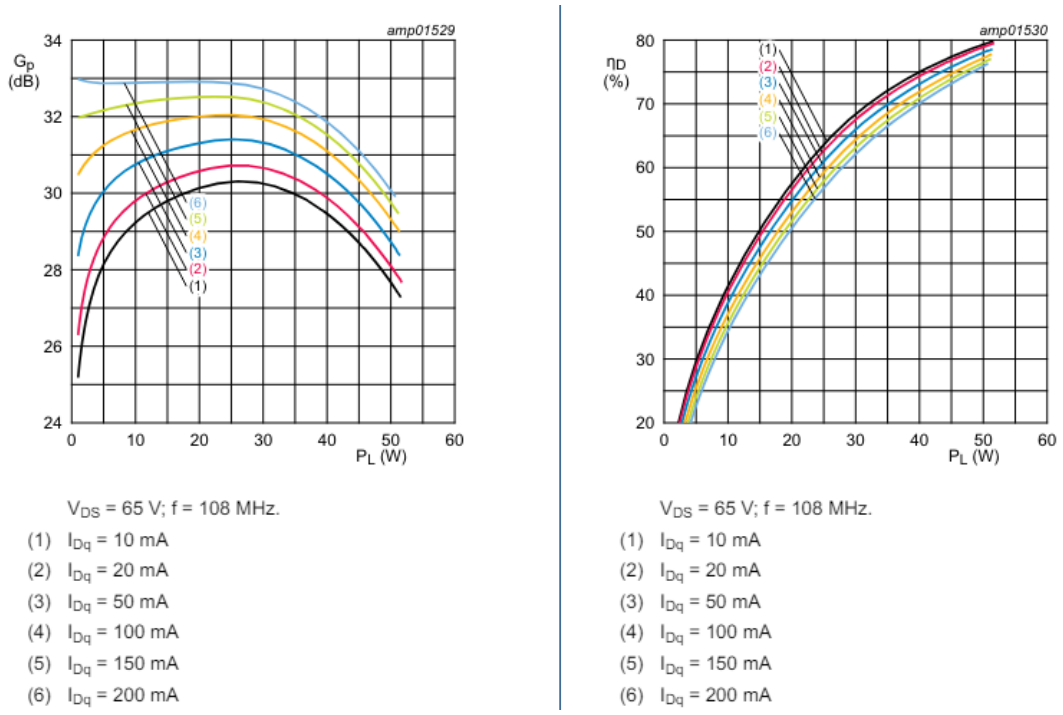


Figure 4.2: Gain and Drain Efficiency as a function of output power[31]

As we can see, the more we increase Drain current, the more gain we have but the less efficiency we can achieve[32].

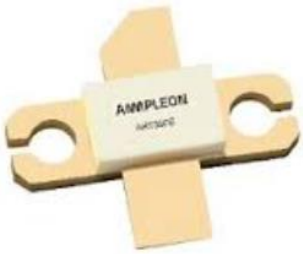


Figure 4.3: ART35FE picture

On figure 2.9 we can see a picture of the transistor. Parallel to the axis labeled with the transistor's name is a metal surface, which is the Source. On either side of the Source, there are two metal surfaces: the square one is the Gate, and the one with an engraving is the Drain. Ampleon provides a model of the transistor in ADS, allowing us to simulate our design.

In addition to all these reasons, the company's recommendation for systems with high power requirements played a role in the decision. The recommended line-up to achieve that is to use the ART2K0FEG transistor as the main amplifier and ours as the driver. So overall, these two transistors were chosen for the last three stages of amplification since, as analyzed in chapter 3, the fourth and fifth stages have the same requirement for output power of 1.6 kW, a value that the main amplifier can deliver as its maximum value is 2kW.

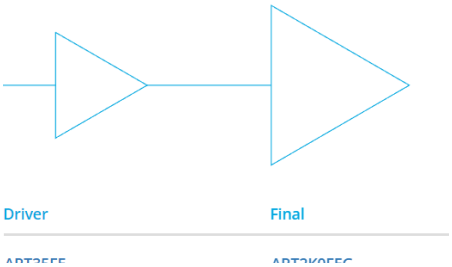


Figure 4.4: Recommended amplification line-up by Ampleon

4.2 DC Simulations and Bias optimization

Now that we have chosen the transistor, we can proceed to designing the amplifier. We will use Advanced Design System (ADS), a comprehensive software suite that includes system, circuit, and electromagnetic (EM) simulators, as well as layout tools and powerful optimizers. This software helps ensure accuracy and validate high-yield designs before manufacturing. The first step in the design process is to select the bias voltages for the transistor. The gate voltage determines the length of the valence band, which controls the amount of current that can pass through the transistor and the drain voltage dictates the amount of current supplied to flow through the transistor[33]. This step is crucial because the selected biasing impacts the input and output impedance, necessitating the design of different matching networks.

4.2.1 Gate Bias

In order to choose the biasing, we run a Direct Current (DC) sweep for the two voltages. Below we can see the schematic of the circuit that was simulated. It is composed of our transistor, two DC sources and two ammeters to measure the current flowing from gate and drain to the source. To present our results we use a template that was created by ADS[34]:

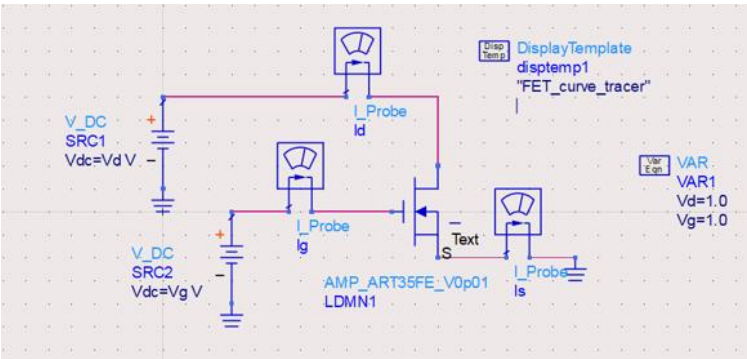


Figure 4.5: Circuit topology simulated on ADS for DC curves

Firstly, we plot the graph of drain current with gate voltage so as to find when the transistor starts to conduct. As we can see the conduction starts at Gate voltage of 2 Volts:

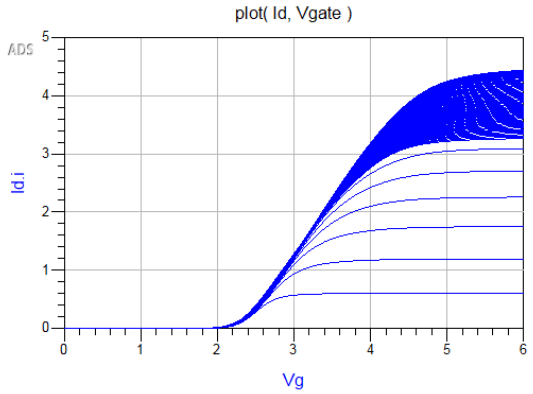


Figure 4.6: Drain current as a function of Gate voltage

The reason why we care about VGS is because the transconductance of the MOSFET in saturation is dependent on this voltage by these equations*[32], [35], [36]*:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \qquad g_{m\ (sat)} = \frac{\partial I_{D(sat)}}{\partial V_{GS}} = \frac{W\ \mu_x\ C_{ox}}{L}\ (V_{GS} - V_{th}) \tag{4.1}$$

To understand the qualitative behavior of transconductance we define it as shown below and we run a simulation to analyze the behavior based on gate and drain voltage:

$$g_m = \frac{I_{DS}}{V_{GS}} \tag{4.2}$$

IDS = current of drain-source
VGS= voltage of gate-source

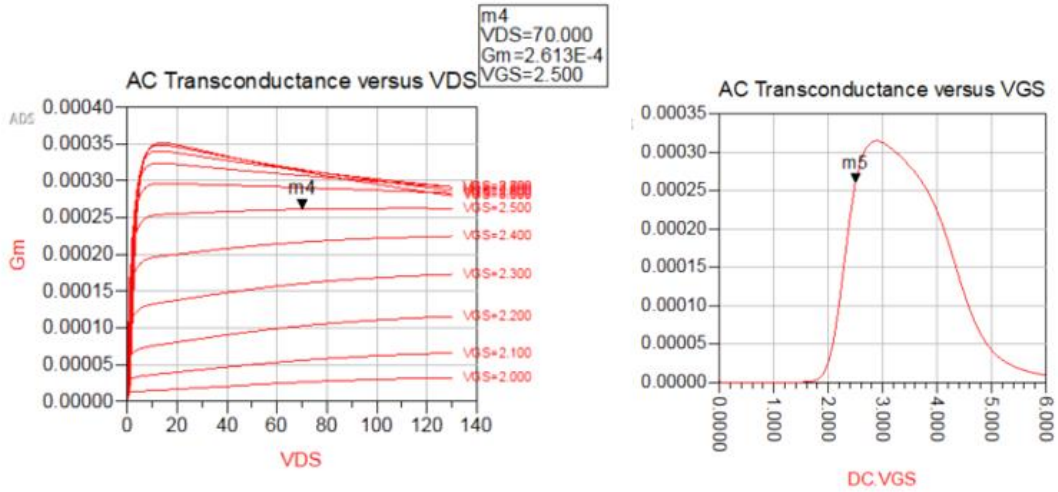


Figure 4.7: AC Transconductance a function of Drain-Source and Gate-Source Voltage

As we can see Gm is not dependent of the drain-source voltage in saturation but is greatly dependent on gate-source voltage. It increases similarly to the drain current but at a value close to 2.9 Volts it hits a maximum and then decreases, as expected since the current is stable but the voltage increases. The reason we do a qualitative analysis of Gm is that this model is not accurately describing what is happening in the real circuit, since it does not take into consideration the Volterra-Series and the non-linearities that occur in high power operation, but it is enough to help us choose the biasing and class of operation of the amplifier.

So, it was decided to use a gate bias of 2.5 Volts.

4.2.2 Drain Bias

Next step is to determine the drain voltage that we will use. The drain current is also dependent on the effect of channel-length modulation as shown below[32], [35], [36]:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{2.72}$$

In order to choose the correct bias point, we need to understand the load line plot of the transistor, which is given on the next page:

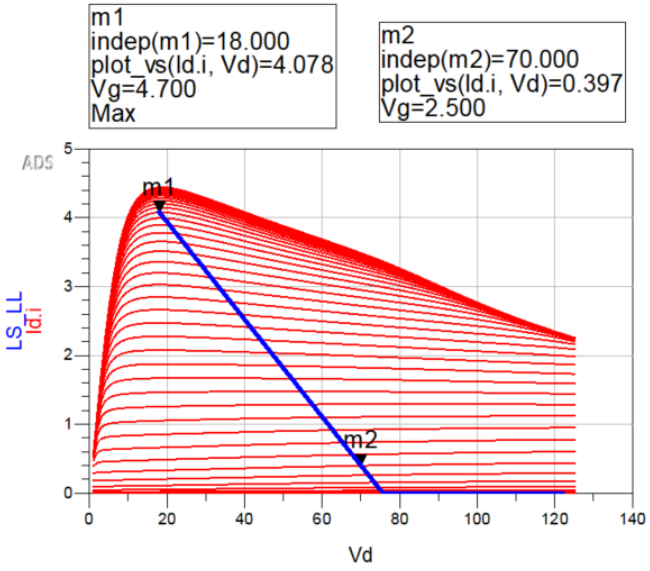


Figure 4.8: Drain current as a function of Drain-Source voltage and the load-line selected

The load line plot of a transistor is a superposition of two graphs, the drain current-voltage plot and the plot of current-voltage for standard load[36]. The first one is seen above with red. The load-line plot is showing how current and voltage change for standard value of load, exactly as we intend to design the amplifier. Below we can see using a simple DC sweep the load line of a load of 20 Ohms:

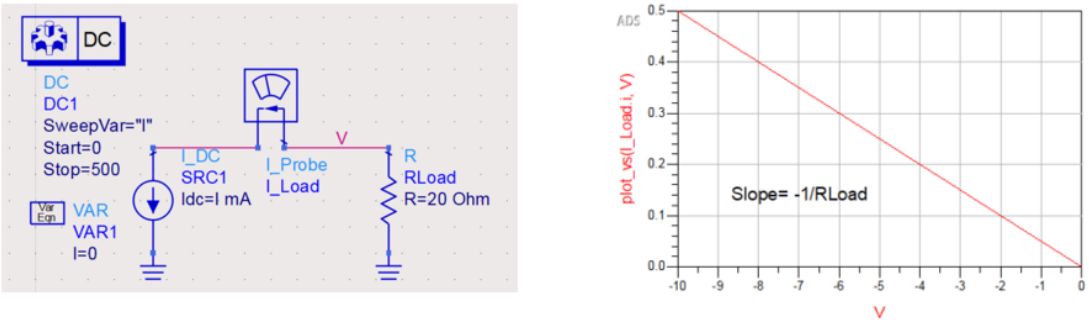


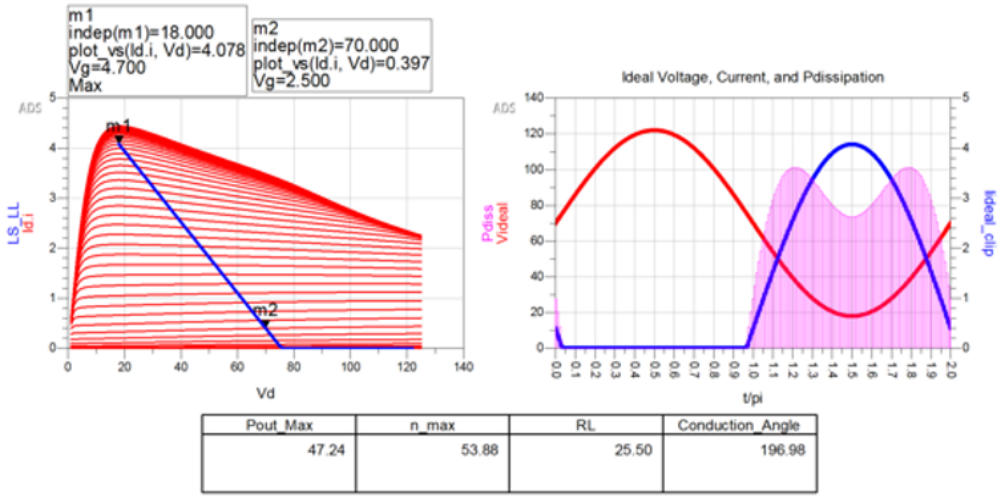
Figure 4.9: Circuit simulated for steady load and current-voltage plot

To better understand Figure 4.9, we need to have in mind the parameters given on the table below:

Parameter	Value
Gate voltage	2.5 Volt
Desired Input Power	1 mWatt
Impedance of transmission line	50 Ohm
Desired Input Voltage	2.23 Volt
Drain Voltage	70 Volt
Maximum Gate voltage	4.73 Volt

Table 6: Voltage values calculation

The first design choice was the GS voltage, as we analyzed previously. Now to choose the drain voltage we need to understand how current and voltage will behave with the input power we want to feed to the amplifier. From chapter 3, the input power is 1 mWatt delivered from a 50 Ohm transmission line which translates to 2.23 Volts value of voltage[10]. Subsequently, the maximum voltage that the gate will operate on is 4.73 volts, the value we chose on figure 2.14. We place the marker on the voltage knee/ maximum current position to limit the oscillation of the current. Since we know the desired output power, 50 Watts, we can calculate again the voltage for this power, 50 Volts on 50 Ohm transmission line. So, we must limit the x-axis to value big enough to with handle the maximum output voltage, 120 Volts. We limit it to a value of 125 Volts. Now the load line can be plotted on the ID-VD graph. Knowing that drain current increases with drain voltage, the bigger the voltage the more power the amplifier can deliver. The maximum drain voltage based on the datasheet is 65V. We will also try to push this limit and utilize the ruggedness of the transistor by testing the amplifier at 70 Volts. For these drain voltages, we have different load line graphs as shown below:



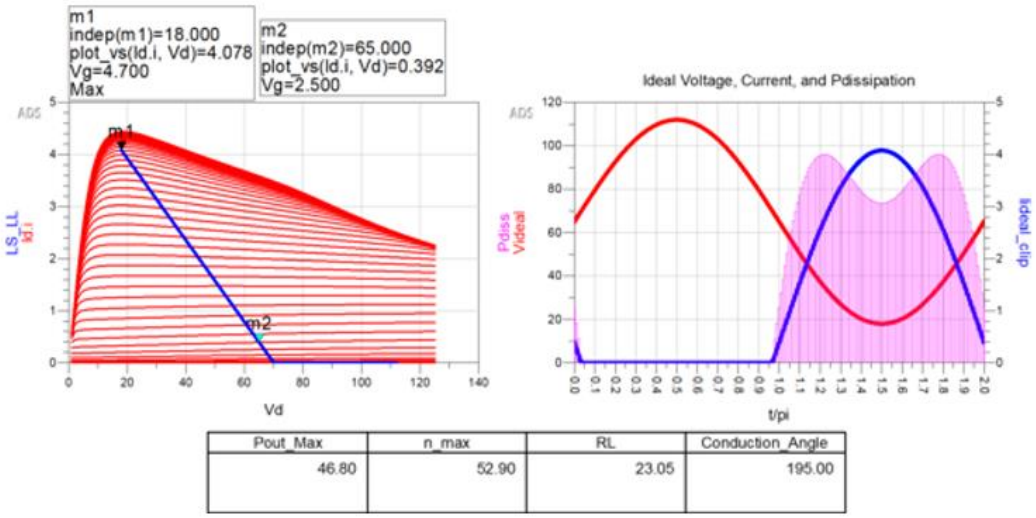


Figure 4.10: I-V curves, load-lines and voltage, current and power waveforms for different load values with tables of output power, efficiency, load and conduction angle

We notice on the top graph, where the quiescent point is at 70 volts, we have higher output power, better efficiency but larger conduction angle and thus more thermal dissipation. We also notice how the load line changes value as the slope of the 65 volts is steeper, as explained in load line graph. With this analysis, we can decide to use 70 Volts as the drain bias. With this bias, the amplifier works as class AB, combining high output power with high efficiency. We know that the transistor is class AB because of the conduction angle and of how the waveform behaves.

For the positive part of the input waveform and for a very small part of the negative part, we can see that the amplifier conducts and thus, delivers power. For the remaining waveform the gate voltage is smaller than the threshold, so the transistor stops conducting. We can see the conduction angle over one period on the graph below:

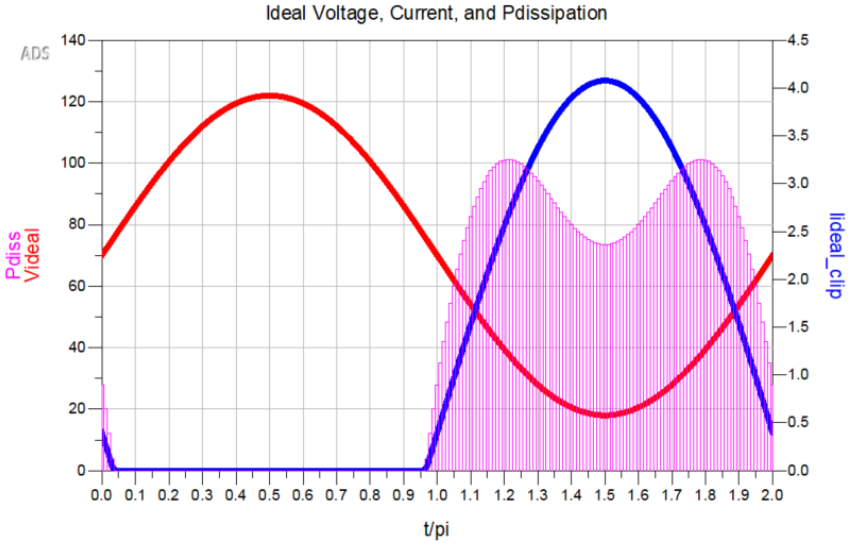


Figure 4.11: Voltage, current and power waveforms for optimal load

The red line is ideal drain voltage, the blue is ideal drain current and the pink one is power dissipated. As we can see, we only lose power when current flows through the device.

So, to summarize this chapter we have:

Parameter	Value
Gate voltage	2.5 Volt
Drain Voltage	70 Volt
Conduction angle	196.98°
Class of operation	AB
Efficiency	53.88%
Output power in dBm	47.24 dBm
Output power in Watts	52.97 Watts

Table 7: Summary of DC simulations

With these parameters in mind, we utilize an online tool given by Ampleon that provides information for mean time of failure of the transistor and junction temperature based on the operational conditions[37]. The results are:

Parameter	Value
Inputs of tool	
Drain Voltage	70 Volt
Drain current	1 A
Input power	0.1
Output power (limited by the tool)	49
Outputs of tool	
Mean Time of Failure	18.100 years
Maximum Junction Temperature	99.41 °C
Thermal resistance	0.92

Table 8: Operational conditions for transistor failure

It is clear that the transistor can withstand the stress we put it through because it has a very long mean time of failure provided that we dissipate the heat with a cooling system so that it does not reach the limit.

4.3 Bias networks and Behavior of real components

Now that we have chosen the bias voltages of the transistor, we need to determine how we are going to provides this power to the transistor. We are going to discuss the importance of decoupling and coupling capacitors, of RF choke inductors or resistors and how to choose real components to fulfill these needs. As expected, the behavior of real components is not ideal. Therefore, we need to search the market and specifically the datasheet of every component in order to gather all the information needed to make the right choice.

4.3.1 Bias networks topology

In the previous chapter it was analyzed how the DC voltages were chosen that will power the transistor. The next step to complete the design is to decide the circuit topology that will enable this[38]. The general idea is shown below from a schematic we designed on ADS:

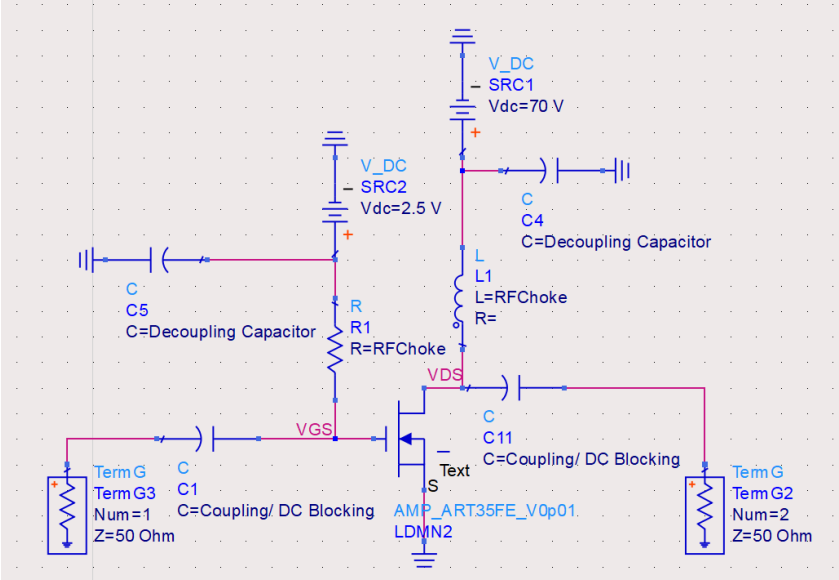


Figure 4.12: Circuit topology of Bias networks on ADS

We can see the DC sources that are going to bias our amplifier. The first components we notice close to the sources are the decoupling or bypass capacitors. Their purpose is to behave like a block for DC currents and as a zero capacitor for AC currents and directly guide them towards ground, in order to protect the circuit from ripple, sparks or any interference coming from an AC source[39]. The capacitor stabilizes voltage fluctuations, preventing biasing instability. The term zero capacitor indicates that at the specified operating frequency the impedance of said capacitor approaches zero[39]. It can also be used to protect the power supply from receiving RF power that flows through the amplifier. This can create several problems like: overheating of power supply components, power being reflected back to the transistor producing current spikes that may stress components beyond qualified limits of operation and power being radiated to the other ports of the device.

As we notice on the picture above, there is another use for zero capacitors, to couple the amplifier input and output with the rest of the system. Their purpose is to allow all the RF

power to flow freely by presenting zero impedance at the given frequency and to block all the DC power from flowing to any path but to the transistor.

The last component to be discussed in the biasing topology is the RF choke inductor. As indicated by its name, the purpose of this inductor is to "choke" or block the RF power from flowing to the power supply but to allow all the DC power to flow with no resistance. This component is crucial, especially on the output stage, since it is directing the power to the output and it changes the total impedance the transistor sees. We also notice that on the input RF choke we have used a resistor. This can be done since the current flowing from gate to source is ideally zero since there is no path to the ground. For that reason, we can use a resistor with high impedance, which is easier to find than a high impedance inductor, to block the RF power from flowing to the power supply. Another benefit of using a resistor is that it can be used in a wide-band design since its response is not dependent on the frequency of operation.

4.3.2 Behavior of real components

Now that we've analyzed the bias topology, it's time to select the actual components that will meet our requirements. In this chapter, we will explore the behavior of both ideal and real capacitors and inductors.

The impedance of the ideal capacitor and its dependence on frequency are:

$$Z = \frac{1}{j\omega C} \quad (4.3)$$

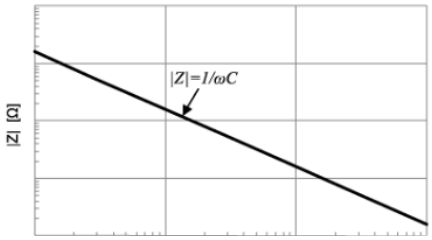


Figure 4. 13: Ideal capacitor Frequency-Impedance dependency

In real capacitors, however, due to the geometry of the capacitor, which is comprised of dielectric plates and electrodes, there is some equivalent series resistance (ESR) and some equivalent series inductance (ESL) [40]. Also, there is some field leakage between the plates that can be modelled as a parallel resistance to the coupling. Its frequency response and circuit model are given below:

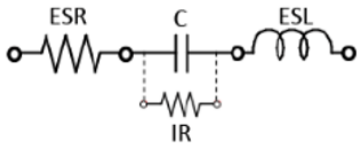


Figure 4.15: Real capacitor circuit equivalent model

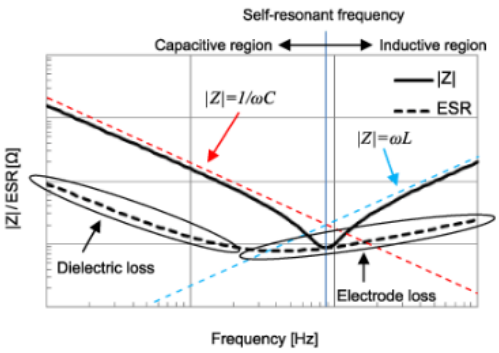


Figure 4.14:Real capacitor Frequency-Impedance dependency

We notice that for smaller frequencies the model behaves like a capacitor until it reaches a self-resonant frequency and then it behaves like an inductor because the ESL becomes domi-

nant in the model. This happens because in higher frequencies the length of the dielectric plates becomes significant and thus it starts to behave like an inductor. It is important to choose a component that can deliver the impedance we need while behaving as a capacitor.
It is known that the impedance of the ideal capacitor and its dependence on frequency is:

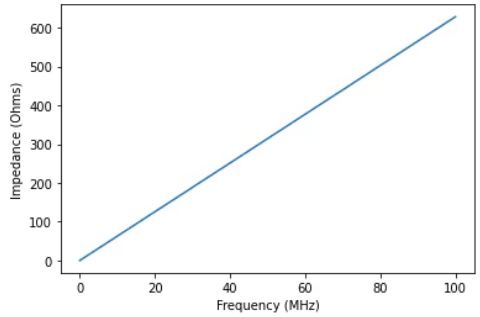
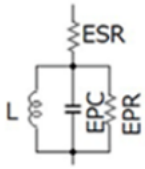


Figure 4.16: Ideal Inductor Frequency-Impedance dependency

$$Z = j\omega L \ (4.4)$$

In real inductors, however, there is some equivalent series and parallel resistance (ESR), (EPR) and equivalent parallel capacitance (EPC)[40]. Capacitance occurs because the edges of the inductor can act as dielectric plates and the coil's conductive part creates the distance between the plates and thus a self-resonant frequency occurs:



model

Figure 4. 18: Ideal Inductor circuit equivalent

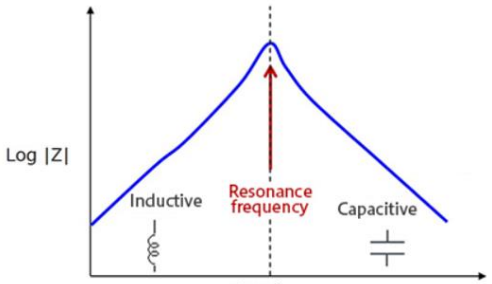


Figure 4. 17:Real capacitor Frequency-Impedance dependency

We notice that for smaller frequencies the model behaves like an inductor until it reaches a self-resonant frequency and then it behaves like a capacitor because the EPC becomes dominant in the model.

A very important parameter we take into consideration when choosing a component is the quality factor Q. The Q factor is a parameter that shows us how efficiently the component uses the power we supply to it. It is given by the following equations[40]:

$$Q_C = \frac{X_C}{R_c} = \frac{1}{\omega_0 C R_C} \qquad Q_L = \frac{X_L}{R_L} = \frac{2\pi f L}{R_L} \quad (4.5)$$

It is defined as the quotient of the imaginary impedance of the component divided by the resistive impedance it presents. By this definition we understand how much is the imaginary impedance that the component can deliver at a certain consumption of power because of imperfections in the real model. Now, with all these parameters in mind we proceed to choose the real components.

4.3.3 Decoupling

The first component we need to choose is the capacitor that is going to protect against ripple or sparks coming from the power supply. In order to do that we need to choose a capacitor with big capacitance to cover our needs. For that reason, we chose this capacitor:

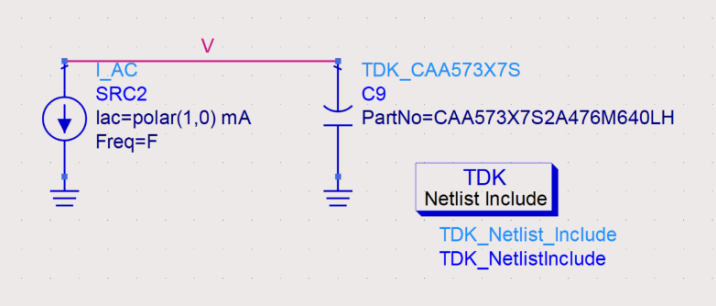
Figure 4.19: Picture of Bias capacitor CAA573X7S2A476M640LH

Parameter	Value
Nominal capacitance	47 µF
Rated voltage	100 Volt DC
Tolerance	20%
Dielectric material	Ceramic
Mounting technology	Surface-Mount
Size	5750
Self-resonant frequency	2 MHz
Manufacturer	TDK Corporation
Unit price	9.47 €

Table 9: Specifications of CAA573X7S2A476M640LH

Data from component datasheet

This is a ceramic capacitor rated to operate under 100 Volt DC power manufactured by TDK. The technology used for mounting is Surface-Mount, a selection that will be analyzed in the layout chapter. Tolerance in electronic components is a variation that indicates how much the actual value of a component can differ from its nominal value due to manufacturing imperfections. So, in our case this capacitor has a range of values between 37.6-56.4 µF. In order to specify the self-resonant frequency of this capacitor we simulated it on ADS. We run a frequency sweep with the model that the manufacturer provided us with the following results:



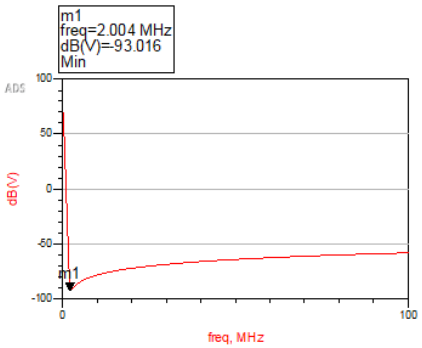


Figure 4.20: Circuit simulated and frequency response of CAA573X7S2A476M640LH

As we can see, the capacitor in our frequency behaves like an inductor since it is past its self-resonant frequency. In order to counterbalance this, we need to use many zero-capacitors to

change the frequency response of the decoupling block and make a zero-impedance path to the ground for our frequency. In order to do that we chose this capacitor:

Figure 4.21: Picture of bias capacitor GRM1885C2A121JA01

Parameter	Value
Nominal capacitance	120 pF
Rated voltage	100 Volt DC
Tolerance	5%
Dielectric material	Ceramic
Mounting technology	Surface-Mount
Size	0603
Self-resonant frequency	581 MHz
Manufacturer	Murata
Unit price	0.15 €

Table 10: Specifications of GRM1885C2A121JA01

This is a ceramic capacitor rated to operate under 100 Volt DC power manufactured by Murata. Tolerance in electronic components is a variation that indicates how much the actual value of a component can differ from its nominal value due to manufacturing imperfections. So, in our case this capacitor has a range of values between 114-126 pF. In order to specify the self-resonant frequency of this capacitor we simulated it on ADS. Similarly:

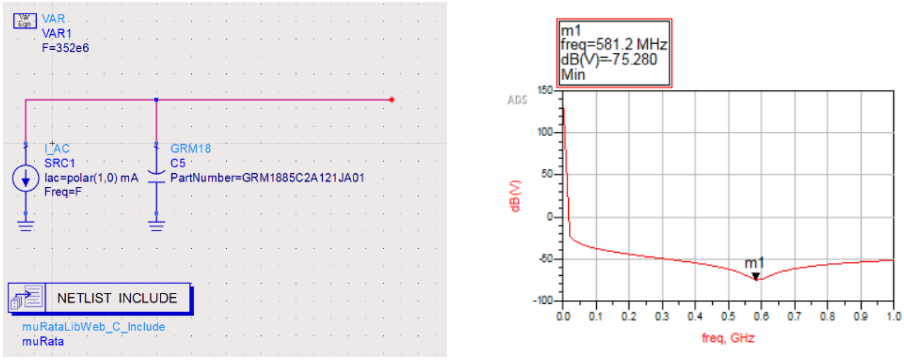


Figure 4.22: Circuit simulated and frequency response of GRM1885C2A121JA01

We notice that in our frequency the capacitor behaves like a zero capacitor. So, in total:

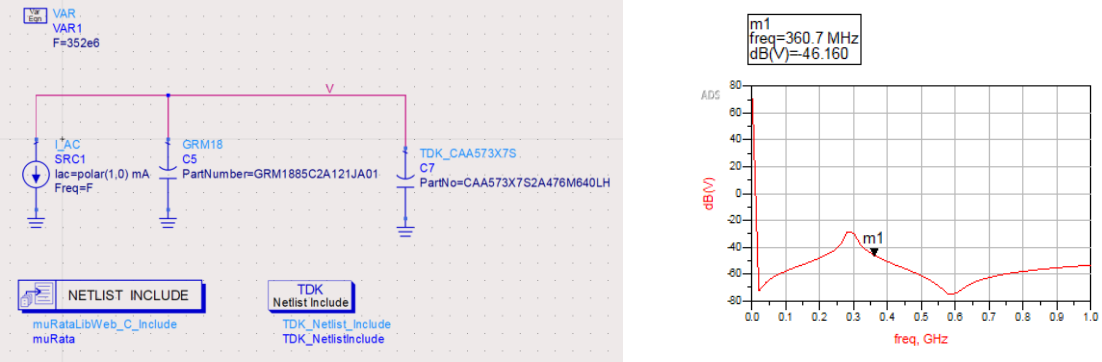


Figure 4.23: Circuit simulated and frequency response of 2 Bias capacitors

We notice from this diagram how the two self-resonant frequencies combine and form areas of capacitive and inductive behavior. At the operational frequency we notice a very good capacitive performance. To further improve this behavior, we add another capacitor with these specifications:

Figure 4.24: Picture of Bias capacitor GRM1885C2A331JA01

Parameter	Value
Nominal capacitance	330 pF
Rated voltage	100 Volt DC
Tolerance	5%
Dielectric material	Ceramic
Mounting technology	Surface-Mount
Size	0603
Self-resonant frequency	360 MHz
Manufacturer	Murata
Unit price	0.15 €

Table 11: Specifications of GRM1885C2A331JA01

The frequency response of this capacitor on ADS:

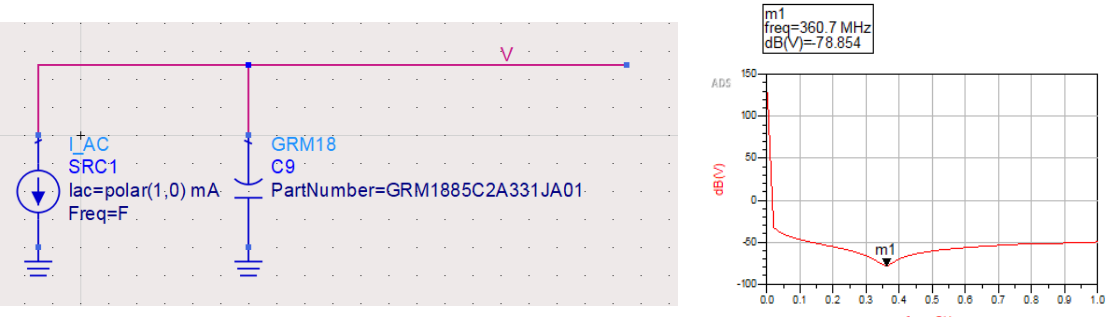


Figure 4.25: Circuit simulated and frequency response of GRM1885C2A331JA01

We notice that the self-resonant frequency is very close to the operational frequency. This capacitor presents almost zero impedance to the system. So, in total:

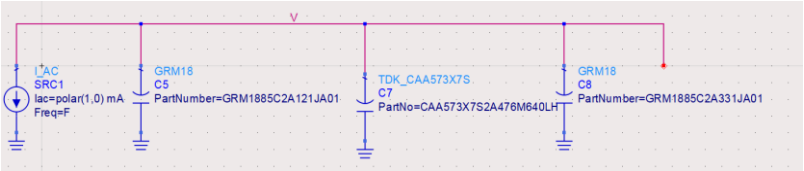


Figure 4.26: Circuit simulated of Bias capacitors

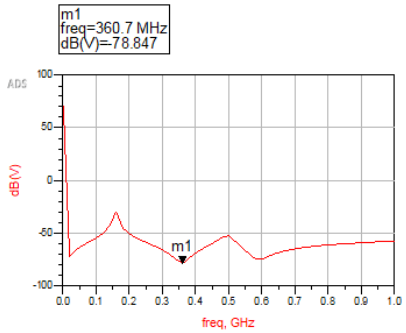


Figure 4.27: Frequency response of Bias network

We clearly see the three resonant frequencies in superposition, marking regions of capacitive and inductive behavior. In our frequency the decoupling block behaves like a zero capacitor whilst providing the benefits of having a charged capacitor that can equilibrate the power provided to the transistor[39]. As we previously mentioned, the mounting technology and the positioning of the components will be analyzed in the layout chapter.

4.3.4 RF Choke

The first component we need to choose is the RF choke that is going to drive all the input power towards the transistor. The component we chose for this use is this resistor:

Figure 4.28: Picture of resistor RMCF1206JT5K10

Parameter	Value
Nominal resistance	5.100 Ω
Maximum voltage	200 Volt DC
Tolerance	5%
Dielectric material	Ceramic
Mounting technology	Surface-Mount
Size	1206
Power handling	0.25 W
Manufacturer	Stackpole Electronics
Unit price	0.1 €

Table 12: Specifications of RMCF1206JT5K10 Data from component datasheet

This is a thick film resistor rated to operate under 200 Volt DC power manufactured by Stackpole Electronics. It can with handle power up to 0.25 W. Since our goal is to feed the amplifier with 0.1 W, we leave margin to operate safely. This resistor's due to tolerance has a range of values between 4.845-5,355 Ω. The size coding of this resistor is 1206 which denotes dimensions of 3x1,5 mm. Size in RF parts is critical because there is a trade-off between power handling and signal integrity. In this case, power is the deciding factor.

The next component we need to choose is the RF choke on the output block. This inductor is very critical since it needs to allow all the DC power to flow with no consumption while in parallel blocking all the RF power directed to the bias network, in order to direct it to the output. The deciding factor in this decision are the current handling of the inductor, because as we analyzed on chapter 2 the RF current the transistor needs to handle is several Amperes, the impedance it can present at the operational frequency and the Q factor. Based on these variables we decided to choose this component:

Figure 4.29: Picture of RF choke coil 2222SQ-221_E

Parameter	Value
Nominal inductance	220 nH
Maximum I_{RMS}	5.5 A
Tolerance	2.5%
Typical Q factor	140
Mounting technology	Surface-Mount
Power handling	0.25 W
Manufacturer	Stackpole Electronics
Unit price	1.23 €

Table 13: Specifications of 2222SQ-221_E

This is an air core inductor, its core has no magnetic material, that is using the self-inductance of a wire coil to store energy in a magnetic field. Due to this geometry the coil has a very good quality factor. The nominal impedance it presents is 220 nH or 486.6 Ω at our frequency, making it a good block for RF power since typical impedance values at that point of the circuit is 20-50 Ω. The Root Mean Square (RMS) current it can handle is 5.5 A, providing us enough margin to operate. To better understand how this coil behaves we run an S-parameter simulation on ADS to analyze Z11 parameter behavior of the inductor. Below is given the simulated circuit and a graph that shows the dependence of the imaginary part of Z11 divided by ω and frequency, which is nothing more than the inductance:

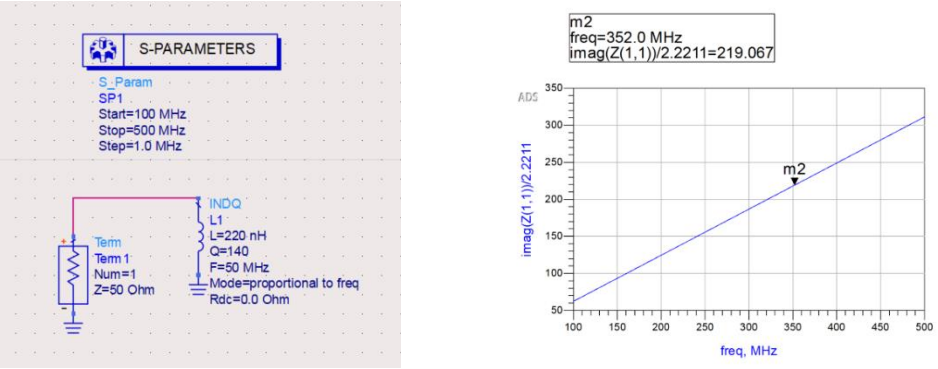


Figure 4.30: Circuit model simulated and Z11-frequency graph

We set up the simulation based on the data from the component's datasheet and we analyzed the behavior. As we can see, the inductance we get based on this model is 219 nH. The qualitative behavior of this component can also be understood from the graphs of the datasheet given below:

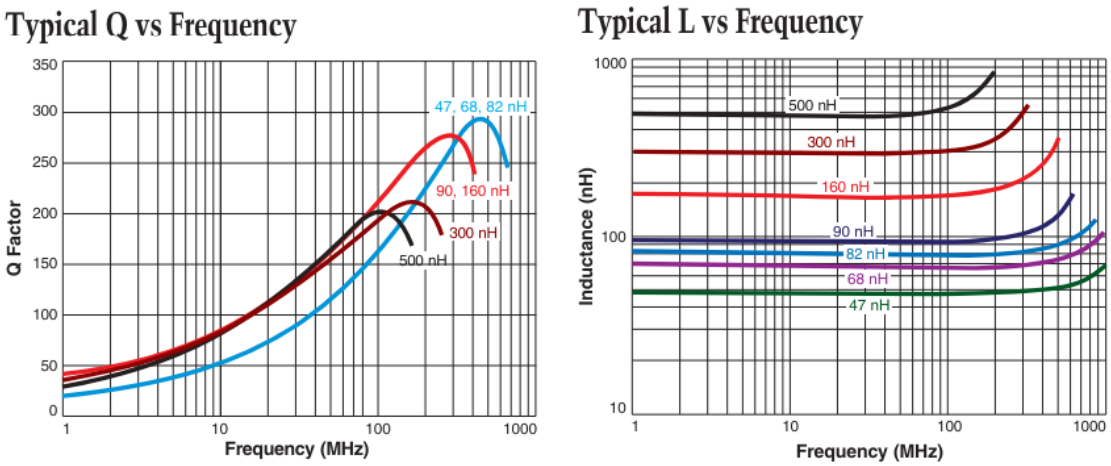


Figure 4. 31: Quality factor and Inductance as a function of frequency for the RF choke coil 2222SQ-221_E[41]

In these graphs we can see the dependence of Q factor and inductance based on frequency on a logarithmic scale for a series of inductors. Manufacturing companies produce many similar components with small differences, usually only the impedance, to offer a variety of solutions. Our components behavior would be an average between 160nH series and 300 nH. Both series have a self-resonant frequency higher than the operational frequency. But, the more we move closer to the SRF, the more the impedance increases. So, to control that deviation, we order 3 different components with inductance values of 160, 180, 220 nH. Later, in the RF lab we will choose the optimal.

4.3.5 Coupling

The last component to discuss in this topology is the coupling capacitor. As we previously discussed, coupling and decoupling capacitors serve the same purpose of behaving like a zero capacitor. But there is one important difference, the coupling capacitor can alter the impedance that the RF power feels while traversing the transmission line and thus present the non-optimal impedance to the transistor. For that reason, the coupling capacitors will be chosen and analyzed as a part of the matching networks in the layout chapter.

4.4 Load pull simulations

As analyzed in chapter two, power amplifier behavior is dependent on input power. When the transistor enters saturation region, S-parameters can-not accurately describe the phenomenon due to the generation of non-linearities[42]. To overcome this obstacle, we will do load-pull simulations. Load-pull simulations is a tool used by RF engineers to test the best set of input and output impedances to optimize the behavior of output power or gain. Load-pull simulations help us determine the best impedance values for maximizing efficiency and output power. By varying input and output impedances, we can visualize optimal points on a Smith chart. To run a load-pull simulation, the device under testing is connected to the load-pull tool of ADS and sweeps the values of input/output impedance and measures the performance of the variables mentioned.

This way, we are able to design the power and gain contours on the smith chart and finally choose the impedances we want to present to the transistor. Below we can see the simulation set up and the results:

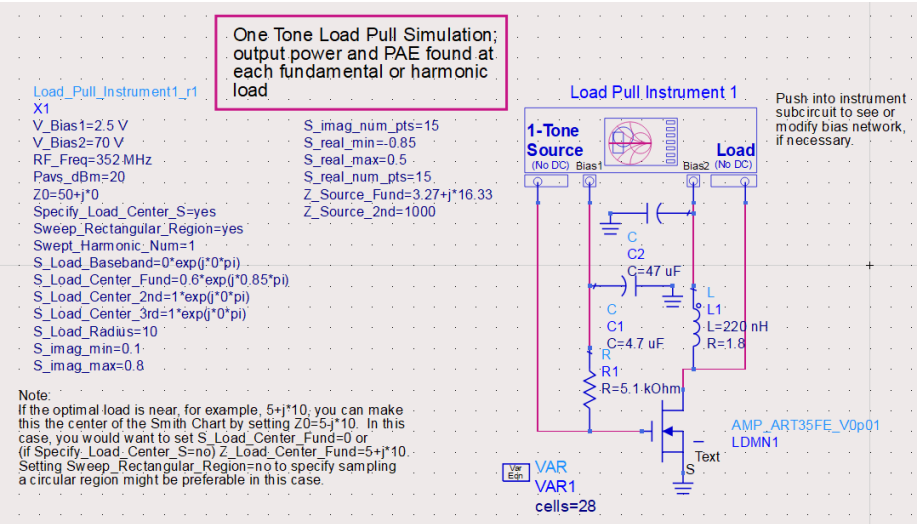


Figure 4.32: Circuit topology simulated for load-pull simulations

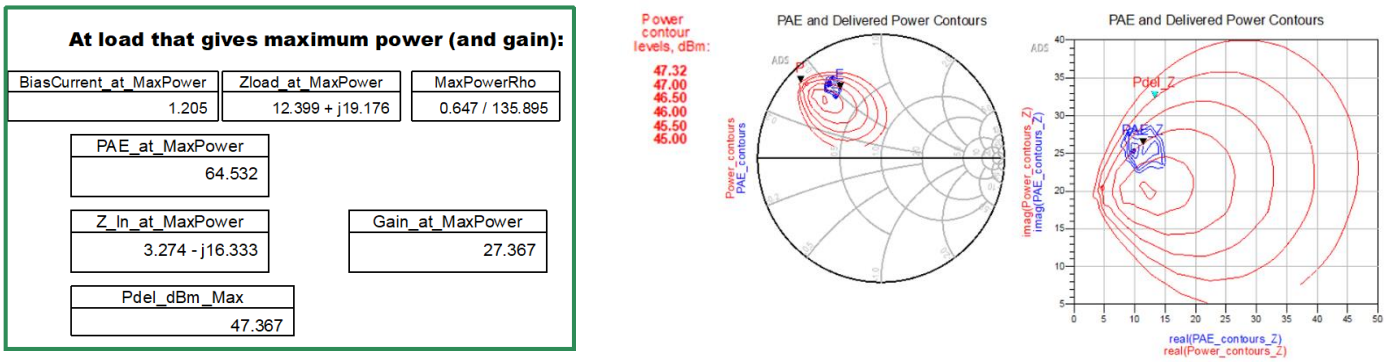


Figure 4.33: Smith and cartesian chart of the power and power added efficiency contours

As we can see, we gather information regarding the gain, the output power, the power added efficiency and the impedances that we are looking for. On the right, we see in cartesian form the output power and power added efficiency. The real part of the complex impedance is on the horizontal axis and the imaginary part on the vertical axis. We can also see the input and output impedance we need to present to maximize output power.

4.5 Stability

A very important parameter when designing an RF amplifier is its stability, as analyzed in Chapter 2. Now that we designed the amplifier's schematic, we can test the behavior of the S parameters. Below we can see the topology designed[34]:

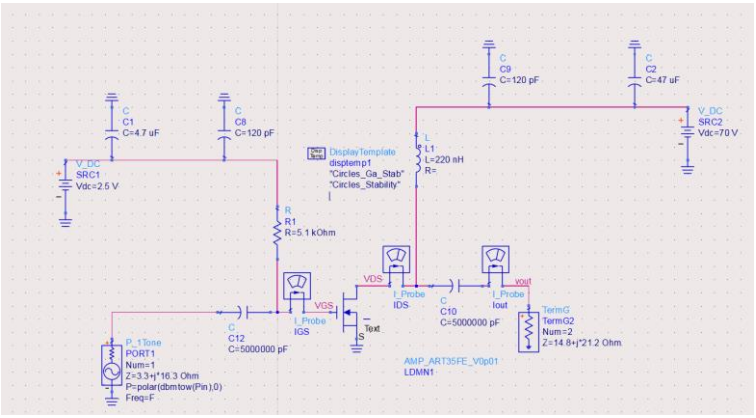


Figure 4.34: Circuit topology simulated for small signal stability testing

To test the stability of the amplifier for this topology, we need to run two different simulations, one for small signal analysis and one for large signal analysis. Small signal stability

ensures the amplifier doesn't oscillate at low power, while large signal stability prevents instability at high power when nonlinearities dominate. As explained earlier, when the amplifier reaches saturation the S-parameters can no longer describe the stability behavior of the device. For small signal analysis we simply run an s-parameter simulation for our frequency and use a display template by ADS to plot the smith chart contours:

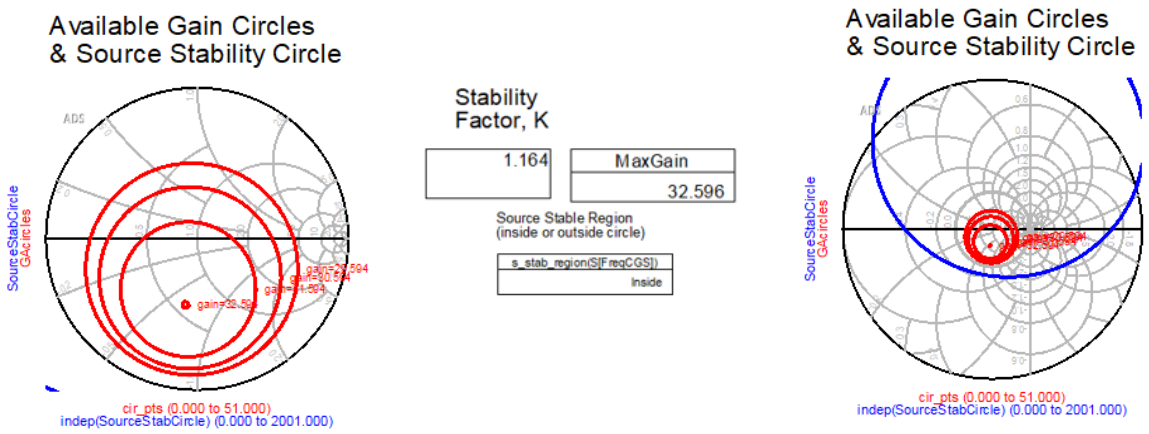


Figure 4.35: Smith chart with available gain and source stability circles

The results demonstrate unconditional stability, as indicated by the entire Smith chart being encompassed by the stable region. Additionally, the calculated K-factor exceeds 1, confirming stability mathematically[10], [43].

Next, we run a large signal S-parameter simulation. This simulation controller runs a harmonic balance simulation so that the amplifier operates in saturation and produces harmonics. Then, the controller measures live S-parameters by the superposition of each harmonic. Below we can see the simulated schematic and the results showing S-parameters behavior dependent on frequency:

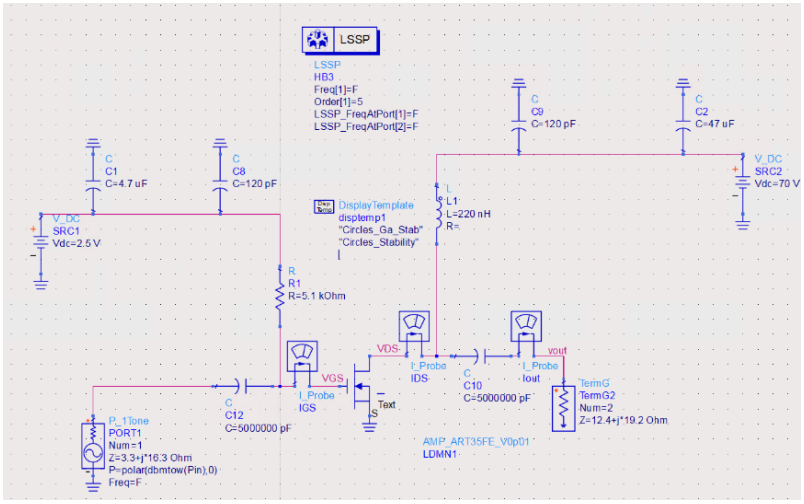


Figure 4.36:Circuit topology simulated for large signal stability testing

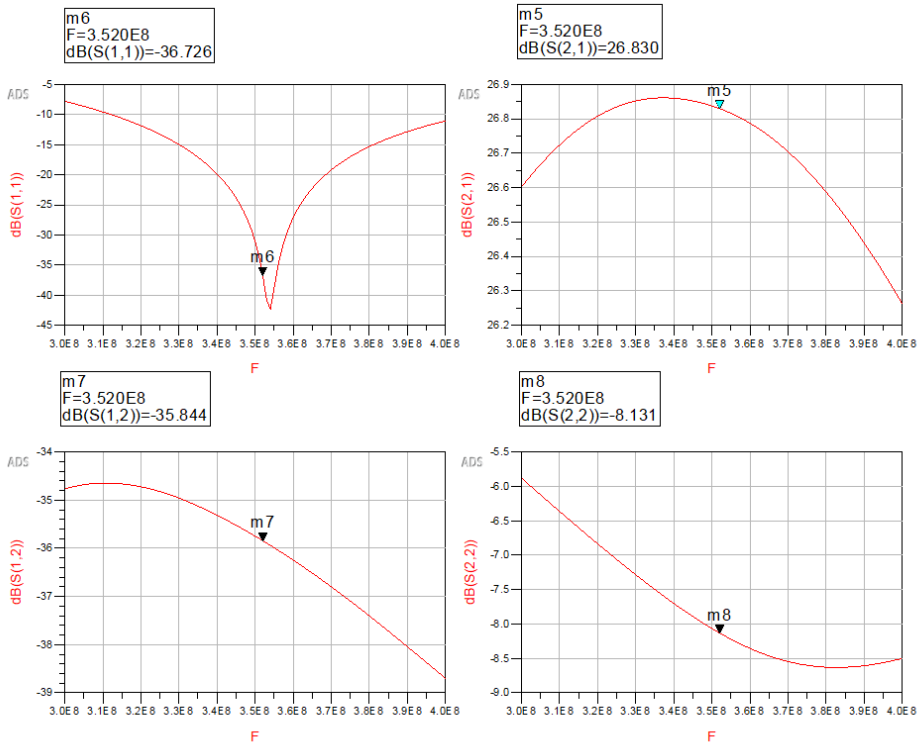


Figure 4.37: S parameters magnitude in dBs of large signal simulation

For these set of values we calculate the Rollet's stability factor, K-factor, after converting S-parameters values to linear and we have [10]:

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|} = 1.38 \qquad |\Delta| = 0.3484 \tag{4.6}$$

Thus, satisfying K-Δ test, where K>1 and |Δ|<1, for unconditional stability. For further insight, we also compute the source and load stability factors:

$$\mu_S = 1.33 \quad \mu_L = 1.67 \tag{4.7}$$

Since both are greater than 1, the amplifier is unconditionally stable from both ports, reinforcing the results obtained from the K-factor. In conclusion, the amplifier demonstrates stability across the full range of input power levels.

4.6 Summary

The development of the SSPA driver's 1st stage schematic involves selecting an optimal transistor based on material and device characteristics, and conducting DC simulations to fine-tune gate and drain biasing for maximum efficiency. The design also includes configuring bias networks and analyzing the behavior of real components, such as capacitors and inductors, to ensure high-quality performance. Decoupling, RF choke, and coupling strategies are incorporated to maintain signal integrity. Additionally, load-pull simulations and stability analyses are performed to achieve robust and reliable operation of the amplifier. The summary of this chapter can be presented by the table below:

Parameter	Value
Transistor	ART35FEU
Gate Bias	2.5 V
Drain BIas	70 V
Decoupling capacitor	CAA573X7S2A476M640LH
Decoupling capacitor	GRM1885C2A121JA01
Decoupling capacitor	GRM1885C2A331JA01
RF choke resistor	RMCF1206JT5K10
RF choke coil	2222SQ-221_E_
Impedance to present to input	3.3-j*16.3
Impedance to present to output	12.4+j*19.2
Stability	Unconditional

Table 14: Summary of Bias networks

Chapter 5: SSPA Driver's 1st stage Layout Development

5 Introduction

In this chapter, we examine the amplifier layout design process in detail. The steps followed to complete the design are: material choice, transmission line technology, matching networks, heatsink design and simulation of layout on ADS.

5.1 Material choice

In this chapter, we delve into the crucial role of material selection in amplifier design. The choice of materials impacts everything from thermal management and signal integrity to overall efficiency and reliability of the amplifier. The material chosen for our application was RO3210, a high frequency ceramic-filled laminate material manufactured by Rogers Corporation. We already have this material available at the ESS RF lab, where we are also utilizing it for the production of the main amplifier. Below we can see the key properties that make this material a viable choice:

Parameter	Value
Dielectric constant, Process	10.2 ± 0.5
Dielectric constant, Design	10.8
Dissipation factor	0.0027
Thermal conductivity	0.81 W/m/K
Thermal coefficient of er	-459 ppm/°C

Table 15: Specifications of RO3210 material

A high dielectric constant of 10.8 enables the design of compact circuits, which is essential when designing systems for the gallery, where space is limited. We need to optimize the spatial footprint of our application, as there are many systems that have to operate simultaneously. We will manufacture a total of 16 amplifiers for the driver's first stage, making it crucial to design them as compactly as possible. When selecting the Printed Circuit Board (PCB) material based on the dielectric constant, it is essential to consider the thermal coefficient of er. Our chosen material has a thermal coefficient of er of -459 ppm/°C, indicating that the dielectric constant decreases by approximately 0.459% for each degree Celsius increase in temperature. This variation can lead to challenges in the matching networks as temperature rises. However, since our amplifier will operate in pulsed mode and we will incorporate cooling systems to dissipate heat, we can ensure thermal stability in our design.
Thermal conductivity is another key factor in maintaining thermal stability. A conductivity of 0.91 W/m/K means the material can transfer 0.91 watts of heat per meter of thickness for each degree Celsius of temperature difference. For the estimated 25 W of power that needs to

be dissipated, this level of conductivity will help spread heat across the material, while the cooling systems will manage overall heat dissipation. Lastly, this material stands out from the norm due to its very low dissipation factor, which results in minimal energy loss. As previously mentioned, system efficiency is crucial, as one of the primary goals of designing the SSPA system is to replace the tetrode amplifiers and improve efficiency.

5.2 Transmission lines

In this section, the way that the components will be connected is examined, in order to create a functional circuit at the layout level. Specifically, we will analyze the PCB transmission line design and dimensions, transistor placement on the PCB and connector integration.

5.2.1 Trasmissioin line technology

Now that we have chosen the PCB material we need to find the optimal transmission line technology for our application. There are three options when designing a PCB: microstrip, stripline and coplanar waveguide. The respective geometries are shown below:

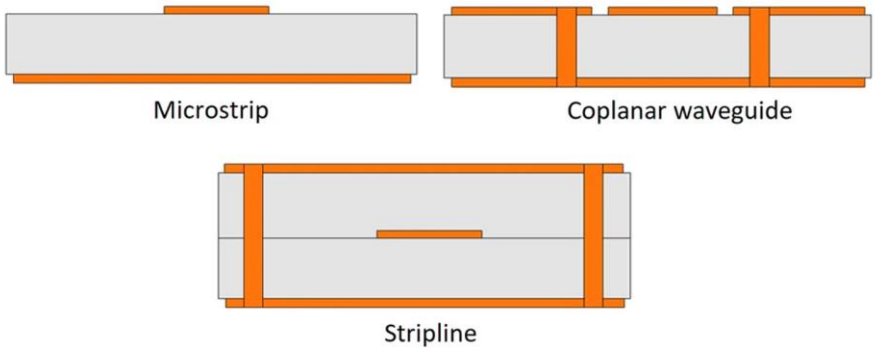


Figure 5.1: Transmission line technologies of PCBs

A microstrip is a type of transmission line in which a conductive trace runs on one side of a dielectric substrate, with a ground plane on the opposite side. The signal travels along the conductive trace, and the ground plane acts as the return path[11]. A coplanar waveguide consists of a central conductive trace on a dielectric substrate, flanked by two parallel ground planes on the same side as the signal trace, a ground plane on the opposite side of the substrate, directly beneath the signal trace and vias connecting the ground planes[11]. A stripline is a transmission line where the conductive trace is sandwiched between two parallel ground planes, fully embedded within the dielectric substrate. This structure fully encloses the electromagnetic fields in the dielectric, resulting in a true transverse electromagnetic mode of propagation[11].

For our amplifier we chose a combination of microstrip and coplanar waveguide. The key features behind this choice are: structure, impedance control, thermal management, ease of fabrication. The open structure of the microstrip line simplifies the process of connecting

components, adjusting their positions, and manufacturing the circuit. With only two layers on our PCB, we can utilize the drilling machine available in the RF lab to efficiently produce our boards. This approach contrasts with the more complex process required to create a stripline board.

While stripline technology provides certain advantages, many of these can be achieved with microstrip technology through careful design choices. To enhance our impedance matching options, we will use coplanar waveguide technology, which allows for greater flexibility in component placement, optimizing matching and overall circuit performance. Finally, stripline's dual ground planes offer superior heat dissipation with an additional return path for current. To boost our amplifier's thermal performance, we will implement dedicated cooling systems, as discussed earlier.

5.2.2 Dimensions of Microstrip and Current Handling

Based on the dimensions of the microstrip transmission line and coplanar waveguide the characteristic impedance and the current handling capacity differ[44]. To understand how they behave, we need to understand the equations describing the geometry:

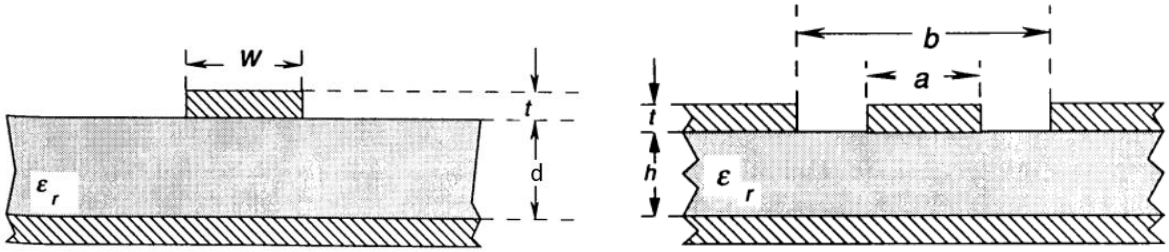


Figure 5.2: Dimensioning of microstrip and coplanar waveguide

The characteristic impedance of the transmission lines is determined using the equations provided in chapter 2. For the coplanar waveguide that guides RF power to the amplifier's input and from the amplifier's output to the output connector, it is essential to maintain a characteristic impedance of 50 ohms to ensure minimal signal loss. The required dimensions to achieve this are as follows:

Parameter	Value
Trace width, a	1.084 mm
Trace thickness, t	0.035 mm
Dielectric thickness, h	1.27 mm
Trace width with gaps, b	3.184 mm
Gap	1.55 mm

Table 16: Dimensions of the microstrip traces and coplanar waveguides

For the current handling of these lines, we will use the microstrip's formula. A coplanar waveguide has a better current-handling capacity than a microstrip with the same dimensions. This is mainly due to its geometry and current distribution.

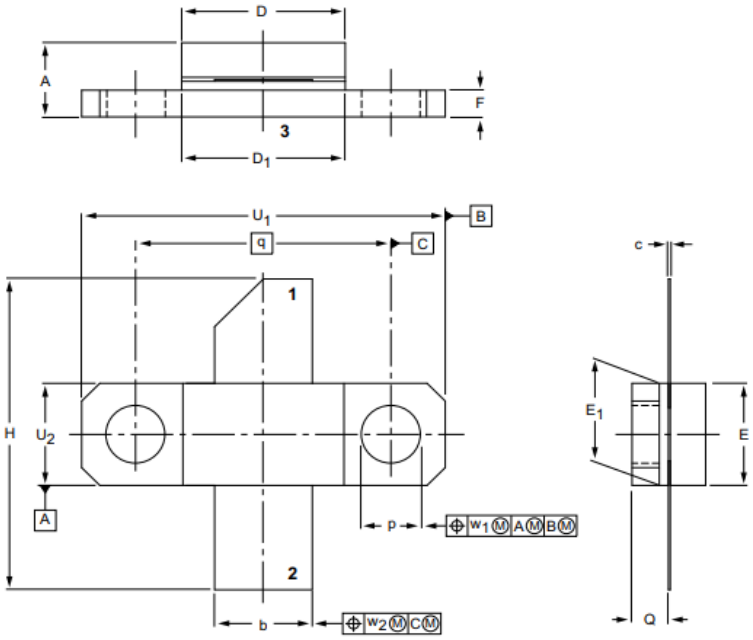
In a coplanar waveguide, the signal trace is surrounded by ground planes on the same layer, offering several advantages regarding our issue. Heat dissipation improves because the adjacent ground planes provide an additional return path for current, which reduces current density and minimizes heat buildup. Additionally, the larger surface area reduces the impact of the skin effect, thereby minimizing resistive losses. By calculating the maximum current of a microstrip with the same dimensions to the coplanar waveguide, it is certain our design will be able to handle that power. For these dimensions the maximum current is 2.5 A.
Our design on the output, where power is at its peak, needs to deliver 50 W of power at 50 Ohms impedance, which translates to 1 A. These dimensions can safely deliver the power to the output connector.

Another critical point in our circuit requiring careful attention regarding current-handling capacity is the connection between the transistor output and the RF choke coil. Based on our estimations made while selecting the amplifier's quiescent point, the maximum current at this juncture reaches approximately 4.1 A. To safely manage this current, the microstrip line must be at least 2.2 mm wide.

5.2.3 Transistor placement

A key consideration in designing the microstrip transmission lines is how to connect the transistor on the layout. The transistor, as well as the components, is surface mount. we need to accurately measure the pad dimensions for the gate and drain leads, as well as the body of the transistor. The mechanical design from the component datasheet, shown on the right, provides these critical dimensions. The trace width and length should be at least 6x6 mm to ensure optimal contact with the transistor and maximize power transfer. In the following chapters, we will explore how using larger dimensions can also aid in achieving impedance matching.

The transistor body is indicated by units U1 and U2. To properly fit the transistor onto the PCB, we will create a 6.1x25 mm cutout, centered precisely on the transistor's midpoint.
The transistor's connection on the layout faces an issue: the pads experience mechanical stress at the edge adjoining the body, causing upward stress and torque that lifts them away from the transmission line. To address this, we have two options. The first is to directly solder the transistor to the layout, ensuring optimal contact. The second is to utilize the RF lab's 3D printer to create Polylactic Acid (PLA) blocks that apply consistent pressure to stabilize the pads against the microstrip trace. Below, the amplifier geometry, including microstrip traces for connection, the cutout for the transistor, screw holes for securing the PLA blocks, and additional microstrip traces for block alignment are shown:



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

Figure 5.3: Mechanical design of the transistor

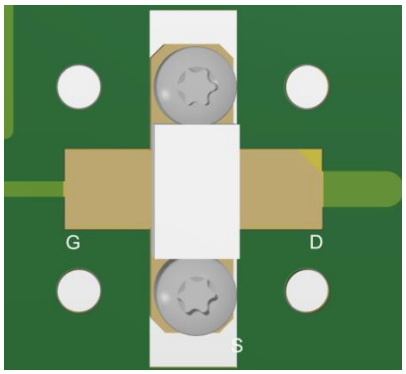


Figure 5. 5: Transistor placement on Altium Designer

Figure 5. 4: PLA blocks picture

The added traces on the input and output are 1.084mm and 2.5mm respectively. By using the PLA blocks, we can test the same transistor on a different PCBs, making it simpler to compare their performance. The transistor is the most expensive component and should be specially handled to avoid overspending in the manufacturing, testing and redesigning process.

5.2.4 Connectors

In RF systems the devices are connected using coaxial cables. In order to be able to transfer the RF power from the microstrip transmission line we need an N-type connector. These connectors on the one side are soldered on the trace and on the other side have a female socket of 50Ohms characteristic impedance. Below we can see the mechanical designs of the component:

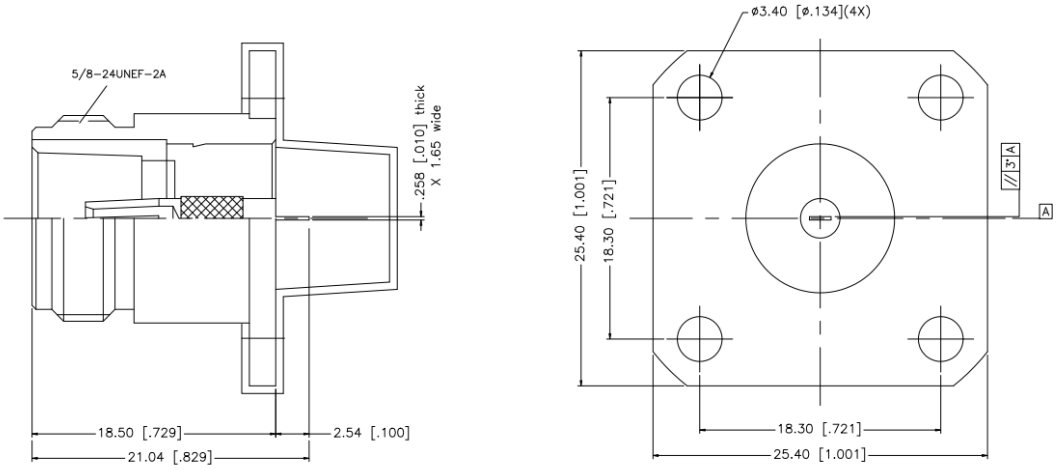


Figure 5.6: N-type connectors mechanical design

The key dimensions are the width and length of the pad to be soldered, which measure 1.65x2.54 mm, as illustrated in the left image. Equally important is the precise position of the holes used to secure the connector directly to the heatsink, ensuring mechanical stability, as shown in the image on the right.

5.3 Matching networks

The only step left to complete the layout of our amplifier is to design the matching networks. Based on the maximum power transfer theorem, we need to present to the input and output of the transistor the conjugate impedance of each port that was calculated with the load-pull simulations[42] . The optimal input and output impedance are respectively 3.3-j*16.3 and 14.8-j*21.2. We chose these sets of values based on the delivered power contours presented on the previous chapter. For every matching network, firstly we design the pads that will connect the transistor to the PCB, compute the impedance transformation caused by the microstrip traces and design network to match the impedance computed to 50 Ohms. In this chapter we will present the process of designing the matching networks and all the iterations that were designed.

5.3.1 1st iteration

As previously mentioned, the initial step involves designing the transistor pads and calculating the impedance transformation. For the first iteration, we created two 6x6 mm pads for the gate and drain terminals, matching the transistor's dimensions. Following this, we added a microstrip trace to accommodate the PLA blocks, a T-junction, the transmission line connecting the transistor to the RF choke components and the DC bias, and the matching networks. In this iteration, we assumed that the transistor simulation model started at the edges of the component. However, in reality, the model begins 0.7 mm from the component edges, as shown below. This was confirmed after contacting the Manufacturer regarding this issue.

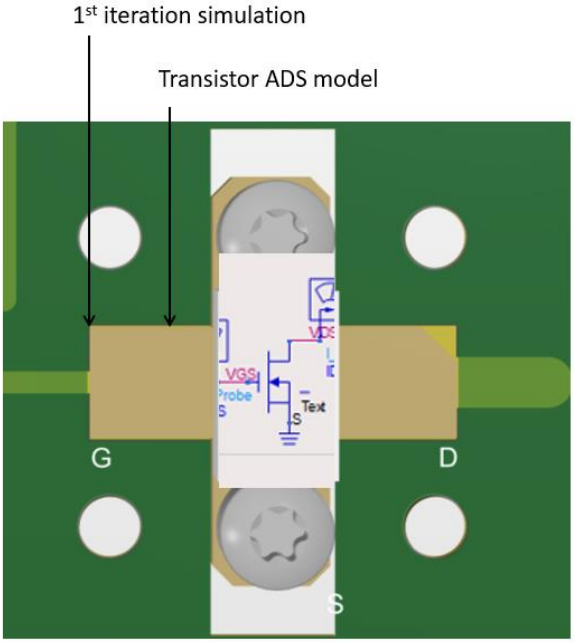


Figure 5. 7: Included distance in the transistor model

This resulted to an amplifier operating at the correct frequency, providing the power we need, but only for the simulation model. Below we can see the topology simulated and the layout designed on ADS on Gerber format for the copper layer:

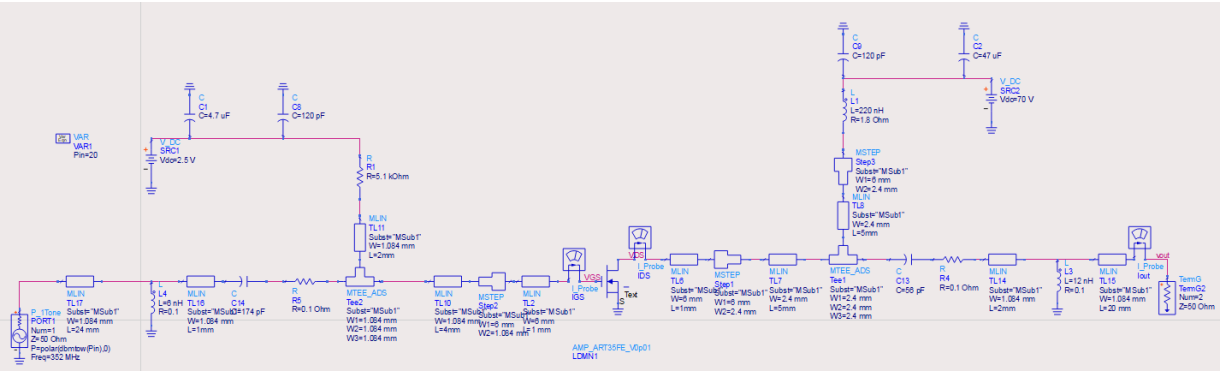


Figure 5.8: Total amplifier circuit simulated

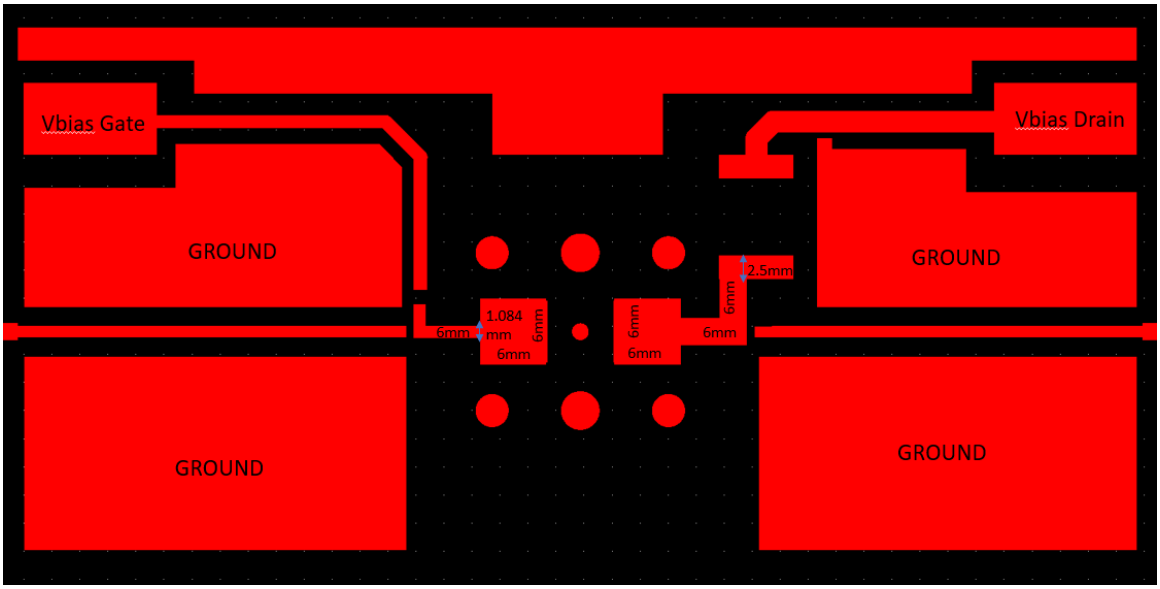


Figure 5.9: Coppel layer design on Altium Designer

Here we can see the ground planes added so that the transmission line is coplanar waveguide. We can also see where the cable to provide the DC voltage will be soldered (top left and right corner) and how this power is provided to the transistor. The components used for the matching networks are two in series capacitors to decouple the amplifier from the input and output and block DC power and two parallel coils to complete the topology[39]. The components used are displayed on the side:

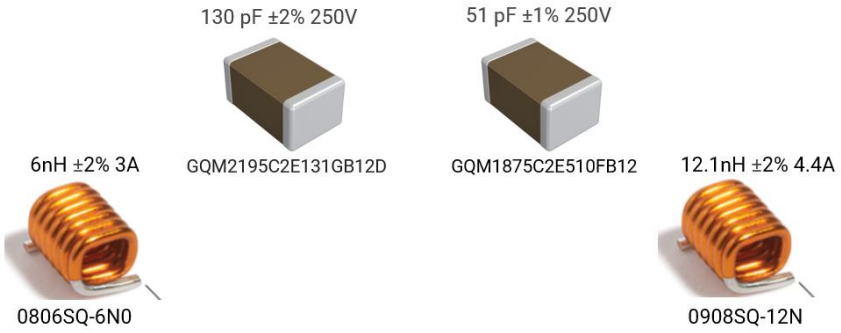


Figure 5.10: List of components of matching networks of iteration #1 with manufacturer reference and impedance

5.3.2 2nd iteration

On the second iteration the behavior of the transistor was well understood. Consequently, the topology was redesigned with dimensions as seen below:

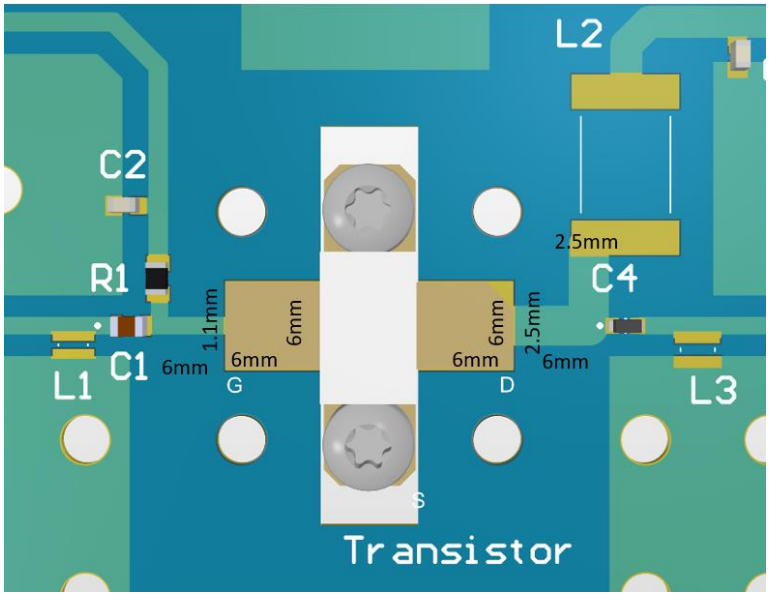


Figure 5.11: Dimensions of microstrip traces connecting the transistor to the copper layer and the rest of the circuit

This new layout was then simulated on ADS to compute the impedance that we needed to present at the edge of the microstrip trace. To perform this simulation, we used the microstrip trace models from ADS and defined all their dimensions and the parameter values of the PCB material, a discontinuity model for sudden width changes, a T-junction to connect the bias network and run a S-parameter simulation[34], [39].

Input 3.3-j*16.3 → 2.5-j*6.6

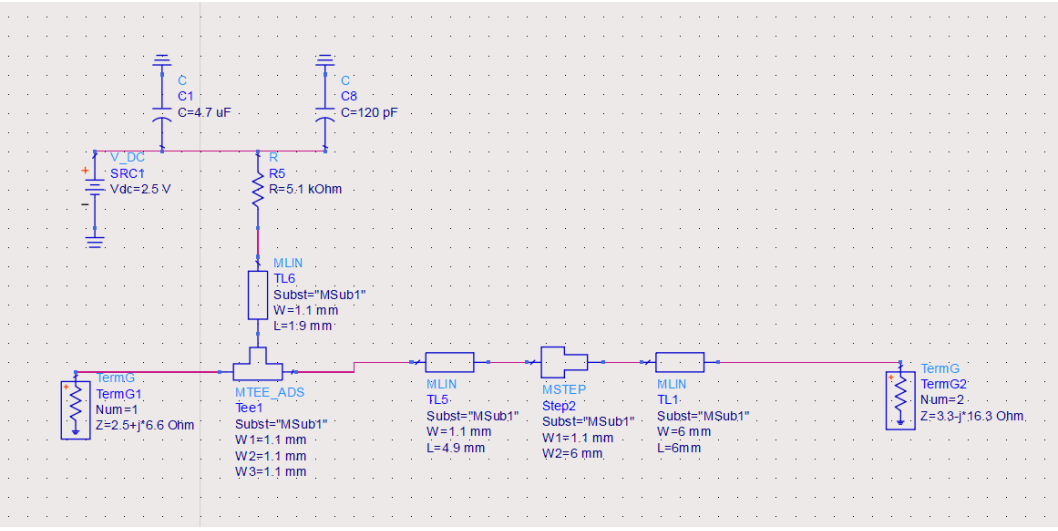


Figure 5. 12: Circuit simulated on ADS to calculate input impedance transformation from transistor pad

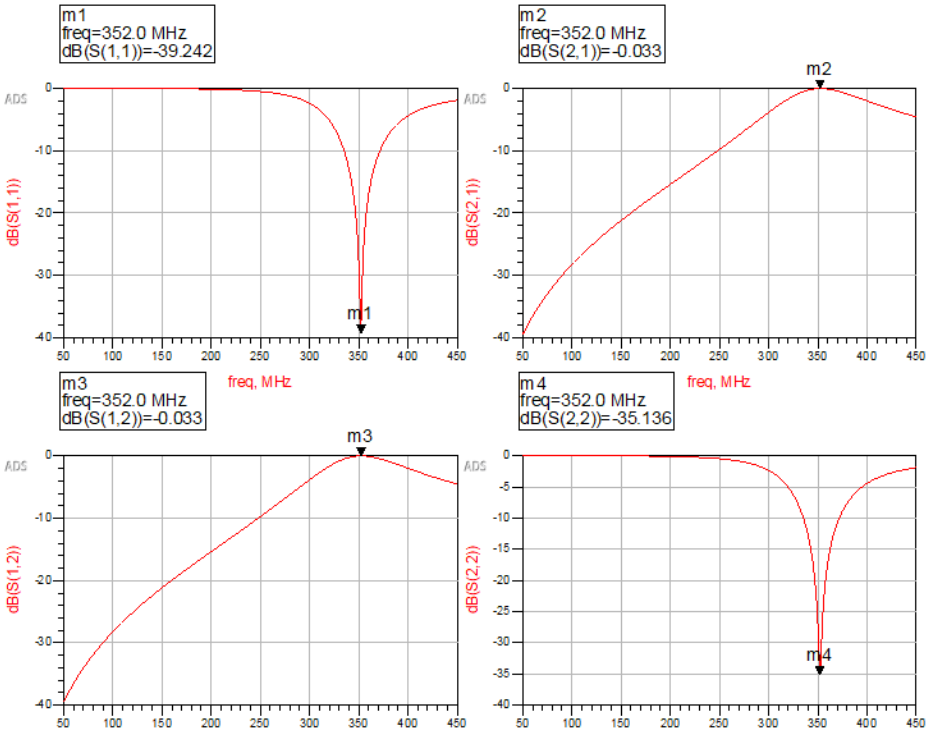


Figure 5.13: S-parameters of input transistor pad magnitude

Output 14.8-j*21.2 → 8.6+j*13

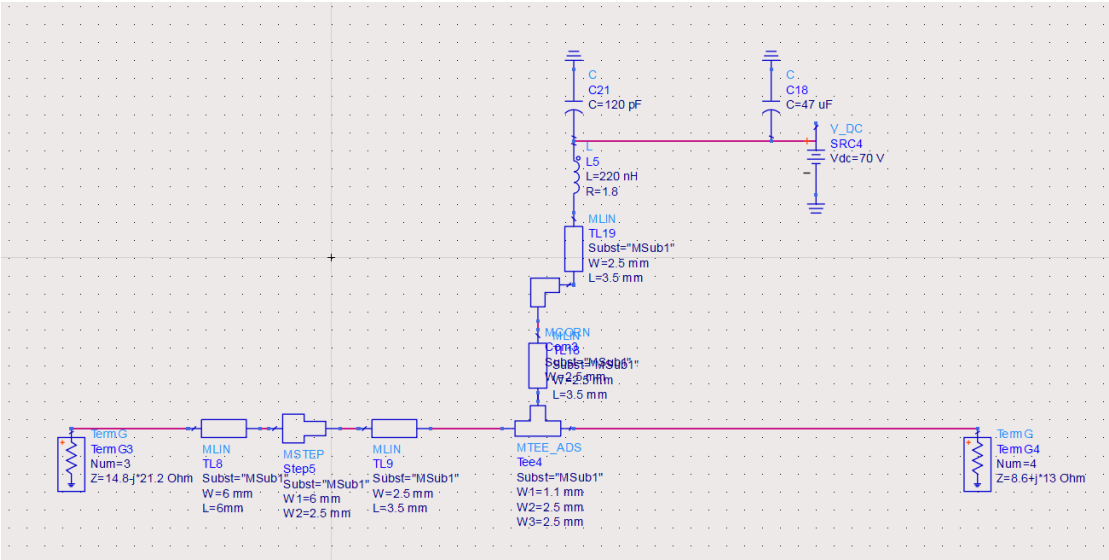


Figure 5.14: Circuit simulated on ADS to calculate output impedance

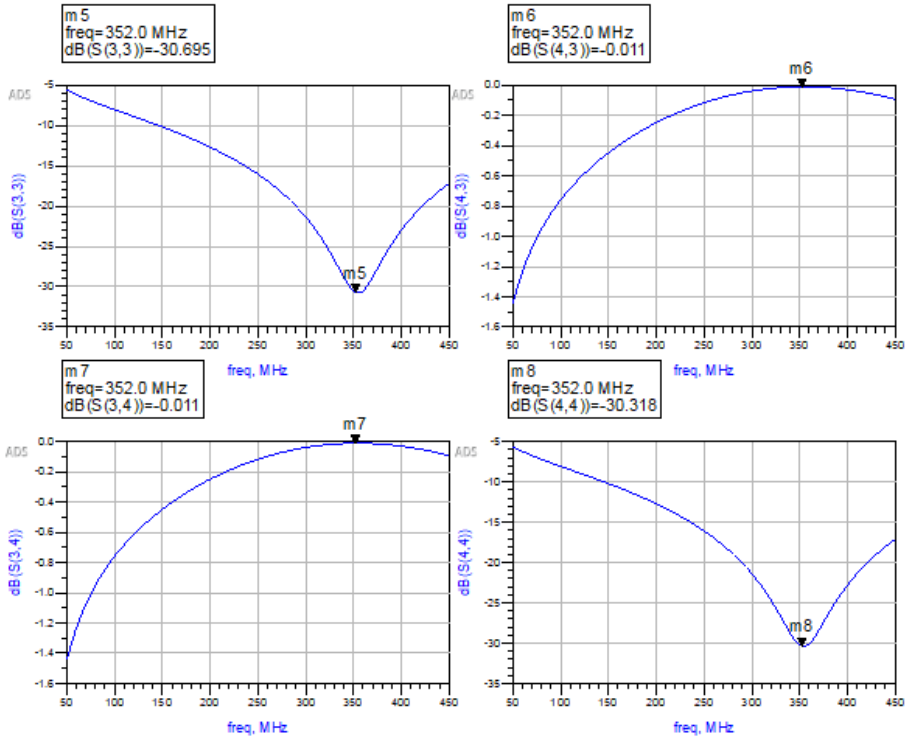


Figure 5.15: S-parameters of output transistor pad magnitude in dB as a function of frequency

Through these simulations, we calculated the required impedance at the endpoints of the microstrip trace. We did not simulate the transmission line following the RF choke components, as it has no impact on the amplifier's behavior. We qualify the performance of these microstrip transmission lines by running an S-parameter simulation. The forward transmission parameter is almost perfect, which is logical since RF choke components are also present in the circuit.

To complete the matching networks, we will use again a decoupling capacitor and a coil in parallel. A critical parameter to take into consideration is the position that the coil will be soldered, as the transmission line shifts the impedance as we move around the Smith chart. Below we can see how we move on the Smith chart with point #1 being the impedance we calculated and each point we proceed to is consequently the point after the capacitor, the point after the microstrip trace and finally the matching point after the inductor.

Input

Output

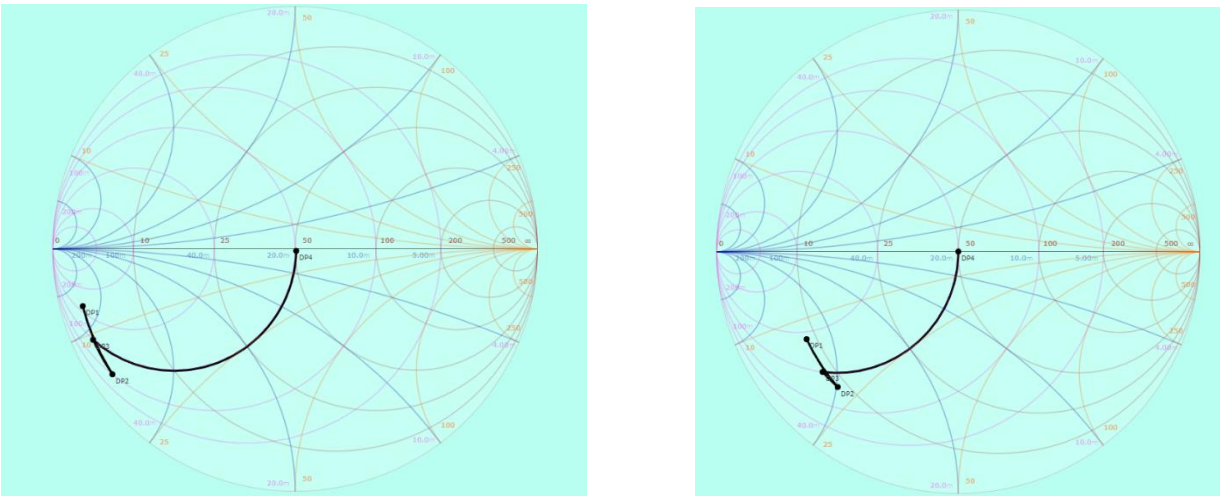


Figure 5.16: Impedance transformations due to matching components on Smith chart

The circuit simulated on ADS to test the S-parameter behavior with the results for input and output:

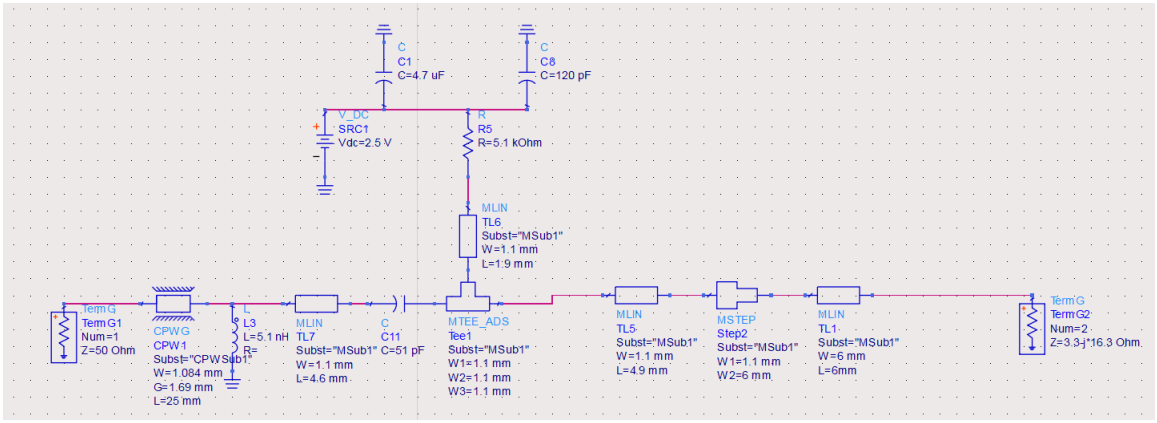


Figure 5.17: Circuit simulation of input matching network

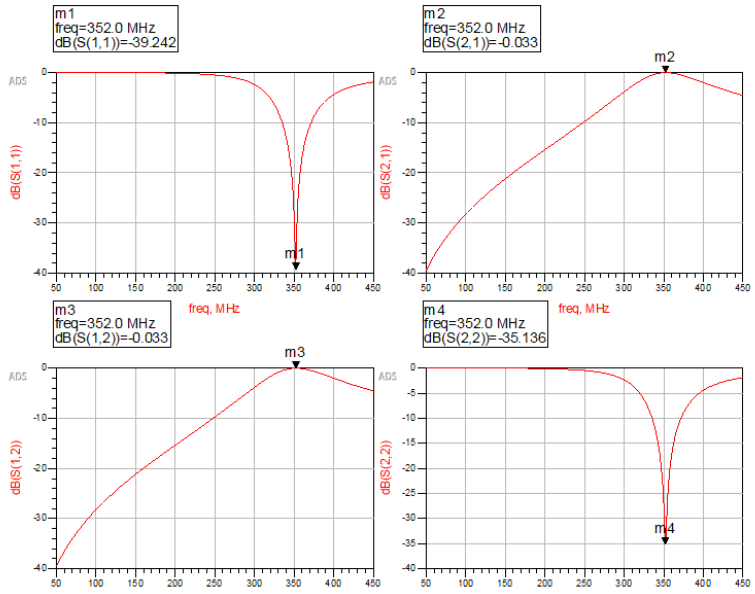


Figure 5.18: Magnitude in dB of S-parameters of input matching network as a function of frequency

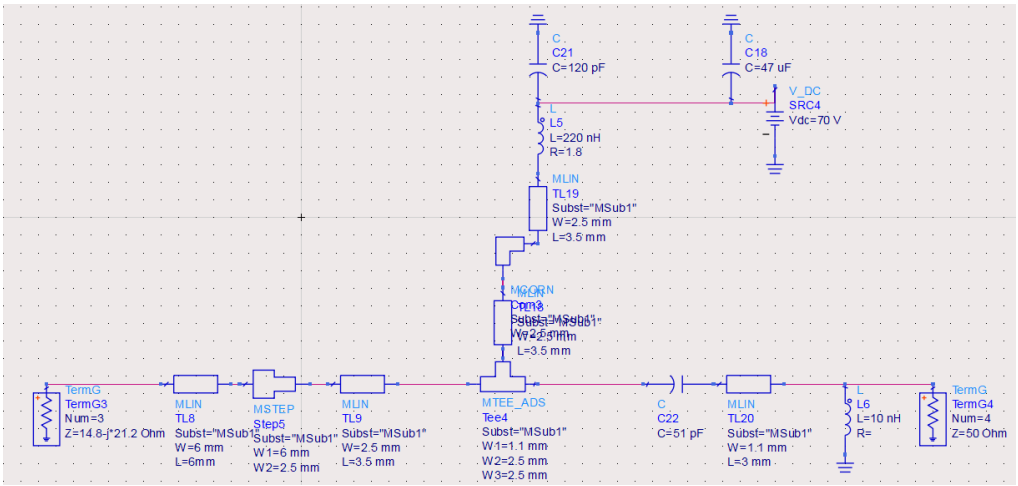


Figure 5.19: Circuit simulation of output matching network

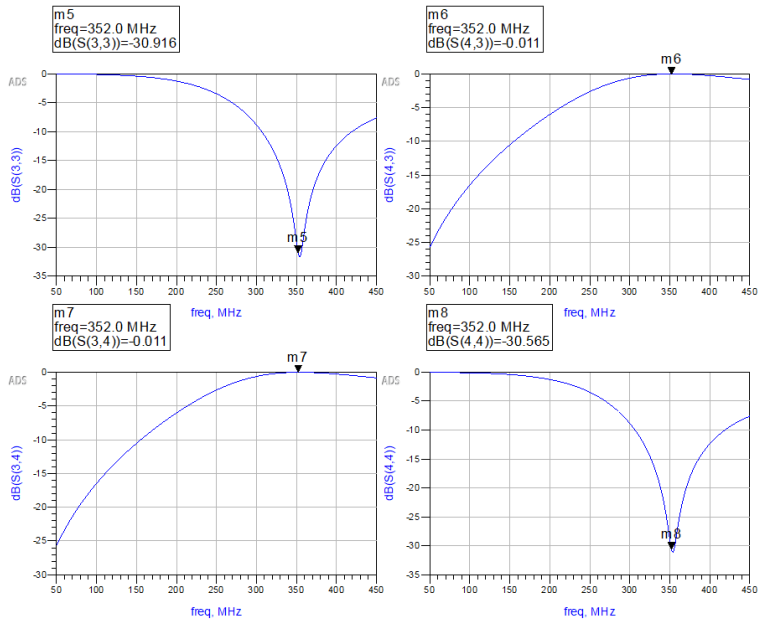


Figure 5.20: Magnitude in dB of S-parameters of output matching network as a function of frequency

We notice that the forward transmission coefficient is close to zero dB. The components used and the designed layout are shown on the next page:

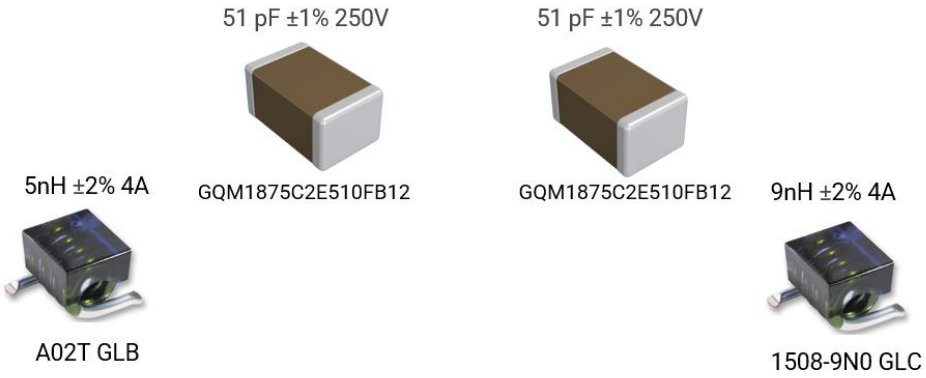


Figure 5.21: List of components of matching networks of iteration #2 with manufacturer reference and impedance

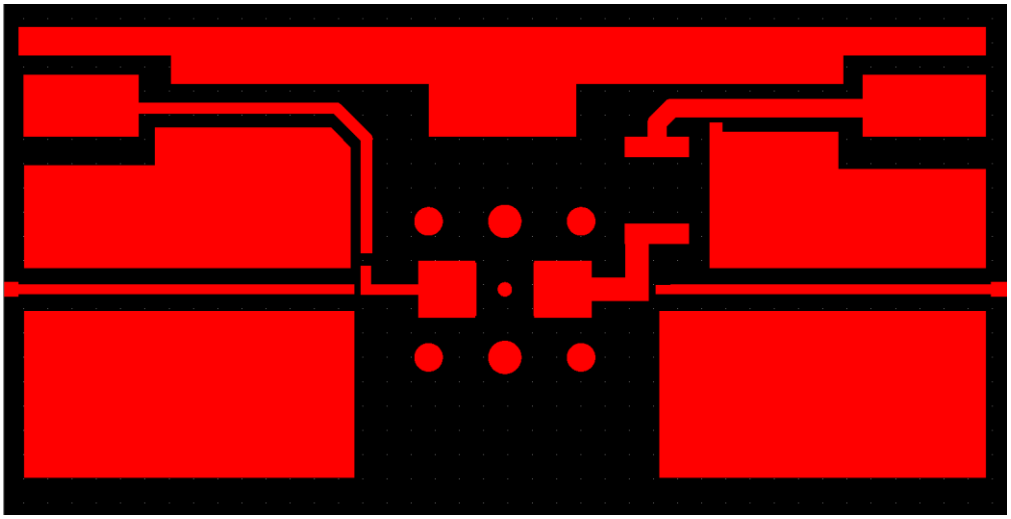


Figure 5. 22: Layout designed for iteration #2

5.3.3 3rd iteration

In the third iteration, while the simulation model of the matching network remained unchanged, modifications were made to enhance the amplifier's performance. The microstrip trace's edges and corners were smoothed to reduce losses, and the two ground planes beneath the transmission lines were connected. When microstrip lines have 90-degree bends, current density increases at these points, leading to localized heating and RF power loss. Additionally, connecting the ground planes resolved issues observed in the RF lab, where the S22 parameter showed instability. This problem was traced to ground loops caused by separate reference planes on the PCB's top layer. The updated design is shown in the next below:

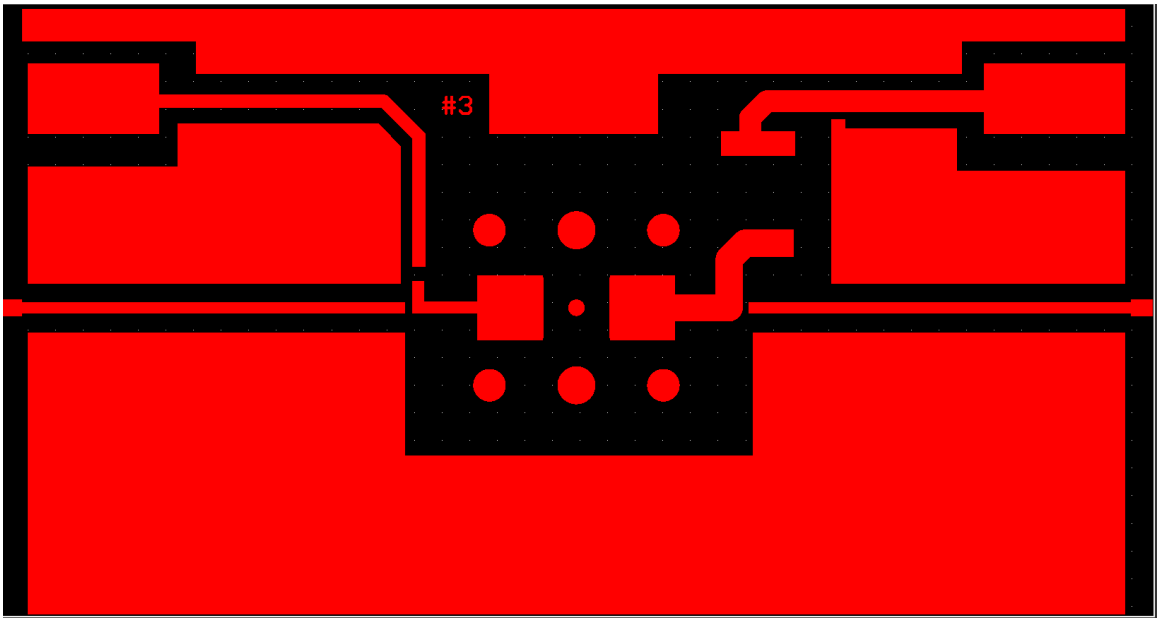


Figure 5.23: Layout designed for iteration #3

5.3.4 4th iteration

In the fourth iteration the matching network of the output was redesigned. The reason behind this change is that the temperature of the decoupling capacitor was still very high, even though the bends were softened. The problem was that the capacitor operating at that point was small in size and could not handle that much power without its temperature to increase. In order to handle this occurrence, we used a capacitor of 0.1 uF that was larger and distributed the power evenly across its body. Then, we used the transmission line as a matching component and almost at the edge of the amplifier connected two capacitors in parallel to complete the matching. Below we can see how we move on the Smith chart:

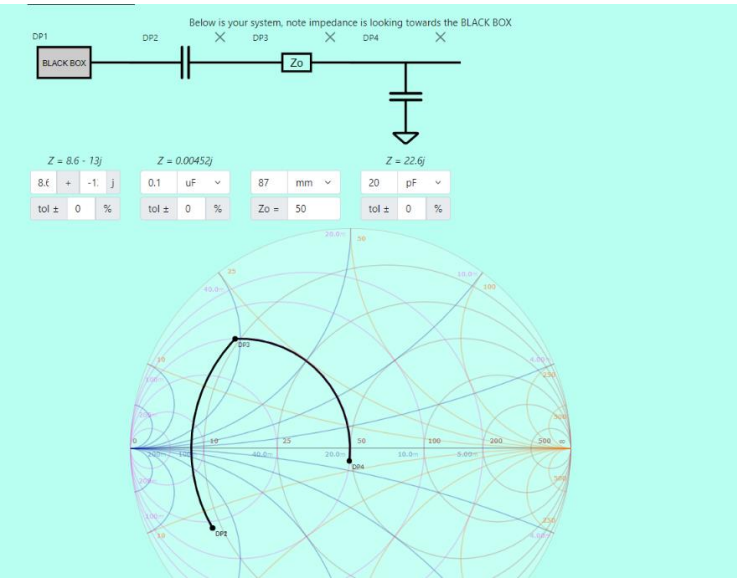


Figure 5. 24: Impedance transformation on Smith chart for iteration #4

The components that were used:

Figure 5.25: List of components for output matching network of iteration #4 with capacitance and manufacturer reference

5.3.5 5th iteration

On the last iteration we did, we changed completely the output matching. We replaced the previous one with one large pad that connects directly with the RF choke coil. The new pad has a width of 8.75mm and length of 10.02mm. We add a small trace so that we can solder the coil and use the same decoupling capacitor we iteration #4. Then, we use again the microstrip for matching and place the same capacitors in parallel, but the distance of the components this time is 35.5mm. With these changes we minimize the effects of the output bias network. Below we can see how we move on the Smith Chart:

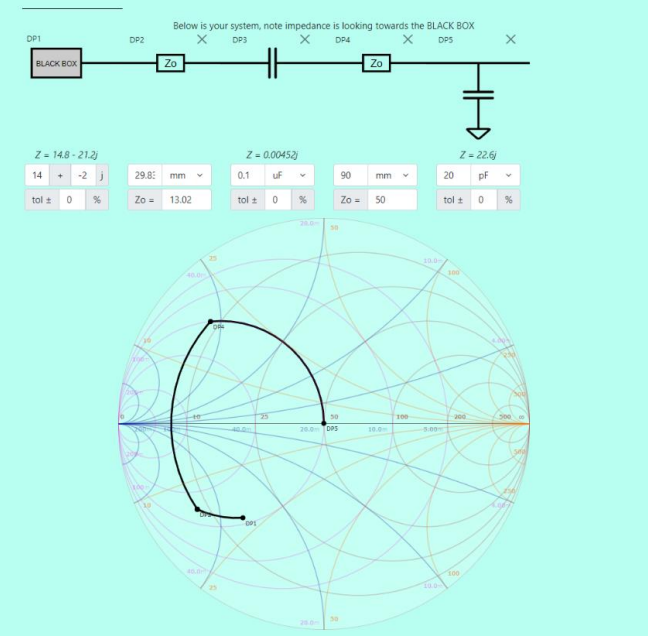


Figure 5.26: Impedance transformation on Smith chart for iteration #5

The layout designed:

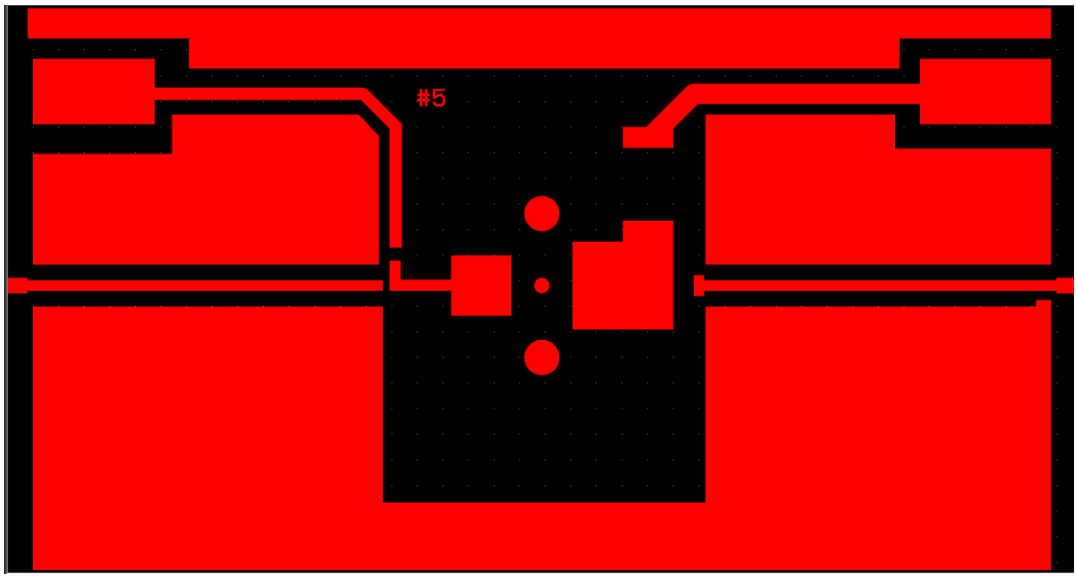


Figure 5.27: Layout designed for iteration #5

5.4 Heatsink design

In this chapter we will analyze all the factors that played a role while designing the heatsink. As mentioned earlier, it is critical to develop a system to help dissipate the heat and spread it evenly throughout the board. We designed a heatsink with many holes for M3 screws and dimensions of 60x106mm, as shown by the mechanical design below:

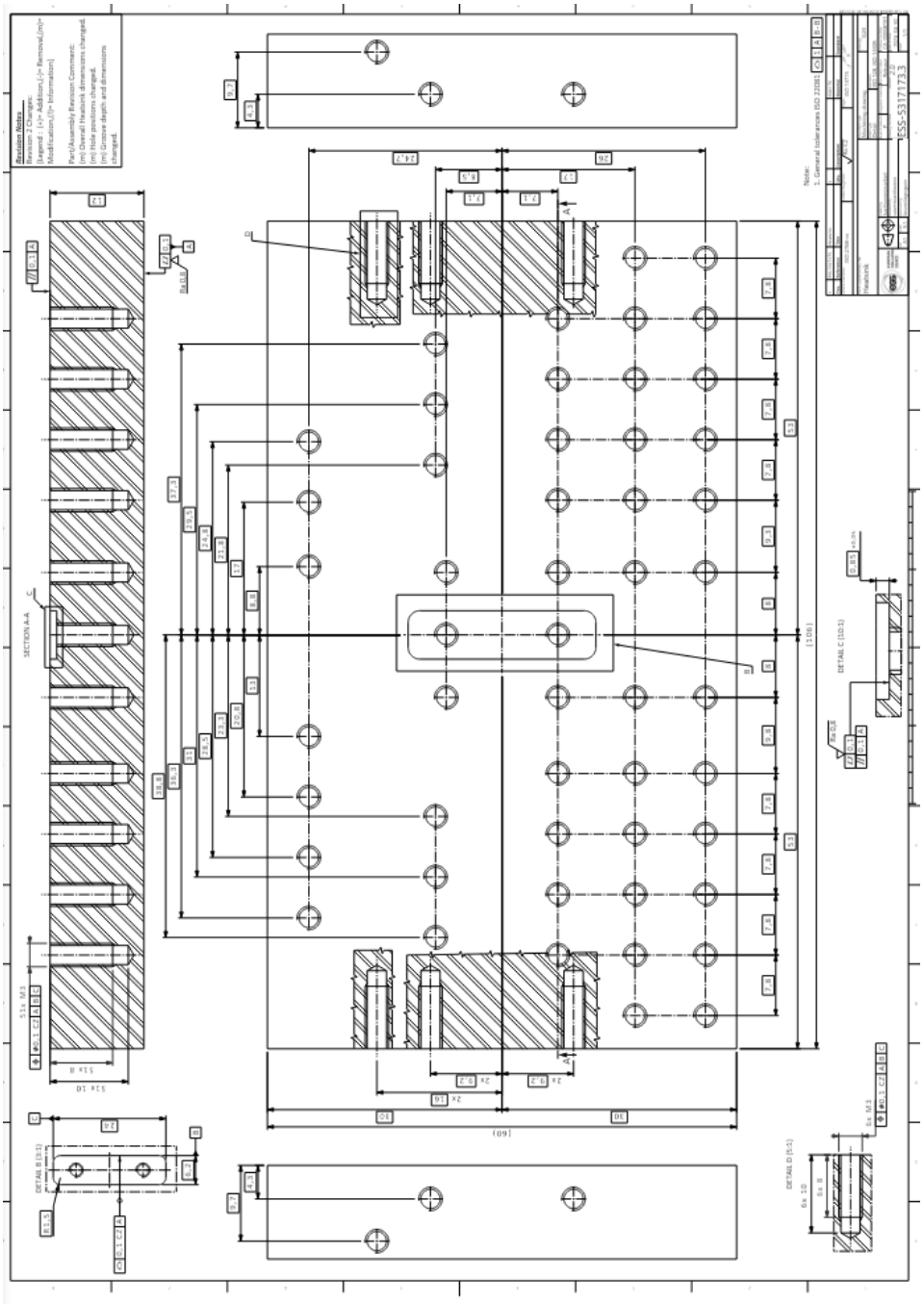


Figure 5.28: Mechanical design of heatsink

In this model, various screws are used for specific purposes, including securing the transistor and PLA blocks, ensuring firm contact between the PCB and the heatsink, and attach-

ing N-type connectors along the side. Here, the layout displays precisely drilled holes to accommodate these components for iteration #3:

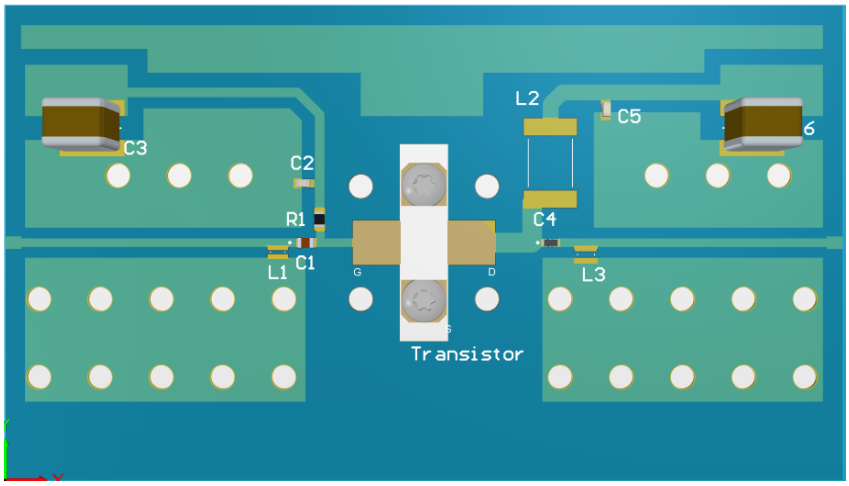


Figure 5.29: Layout designed on Altium with holes for heatsink connection

At the center of the heatsink, where the transistor is placed, a hole is carved so that the transistor can be placed to have perfect contact with the aluminum surface. It is important because the heatsink is also used as ground reference. Below is a picture of the designed product, as manufactured by the ESS mechanical lab:

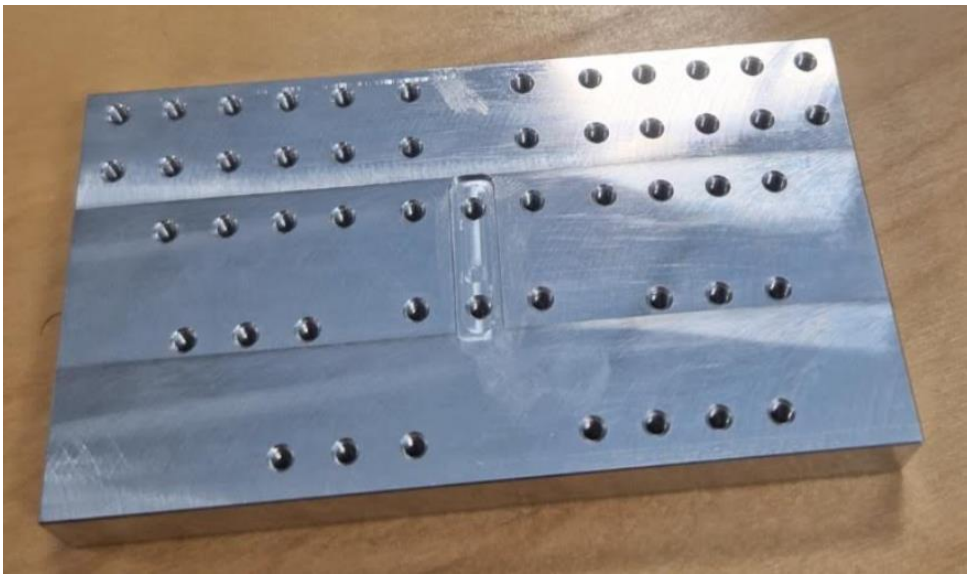


Figure 5.30: Picture of heatsink

5.5 Simulation of layout

To finalize the design process, a comprehensive model of the amplifier is built in ADS, incorporating every component and transmission line to accurately simulate its performance. Realistic models, rather than idealized ones, are used for each component. These models were sourced from manufacturer-provided libraries or created from spice models when necessary. The resulting schematic for simulation is shown below fore iteration #2 and #5:

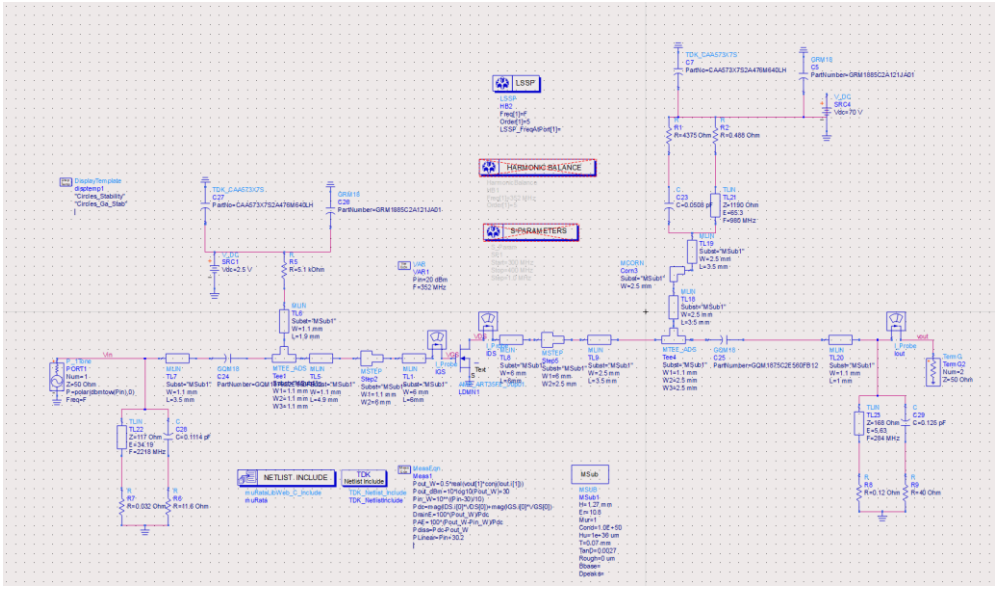


Figure 5.31: Circuit equivalent of layout #2 simulated on ADS

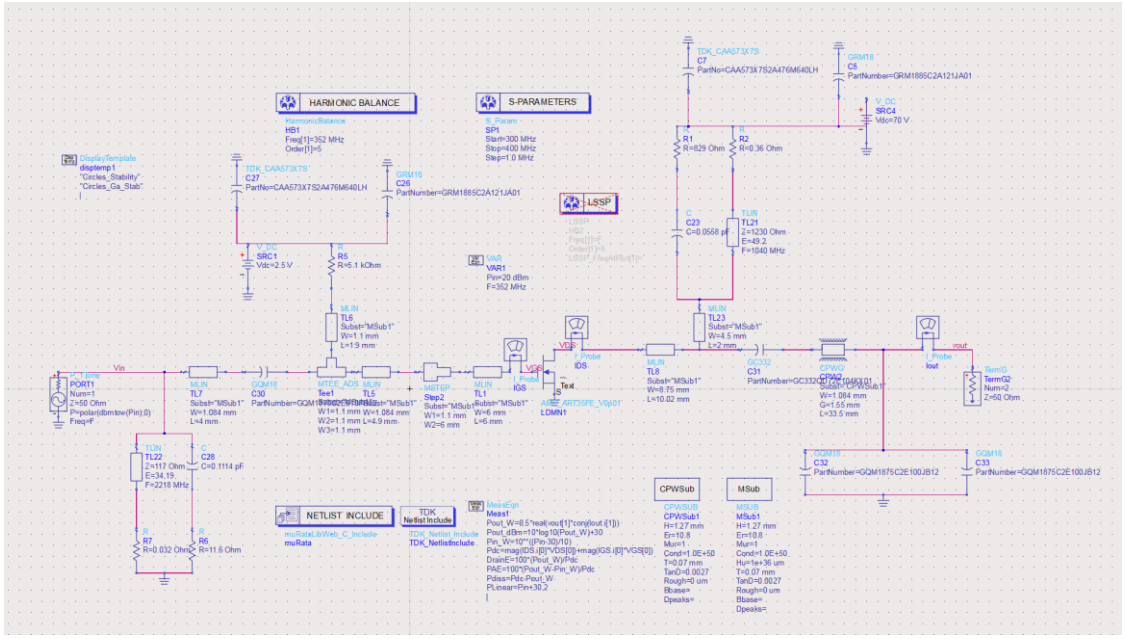


Figure 5.32: Circuit equivalent of layout #2 and #5 simulated on ADS

The layouts that were designed in total:

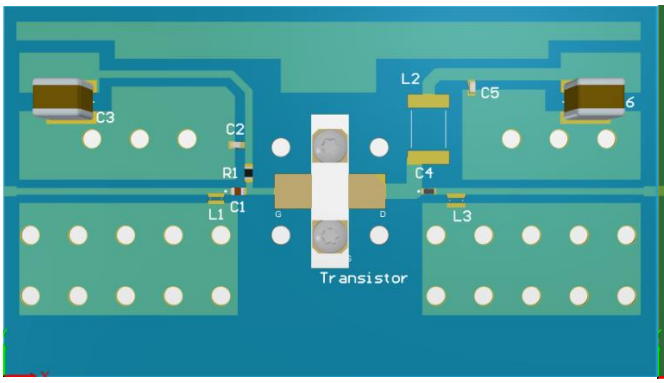


Figure 5.33: Layout 1 in Altium

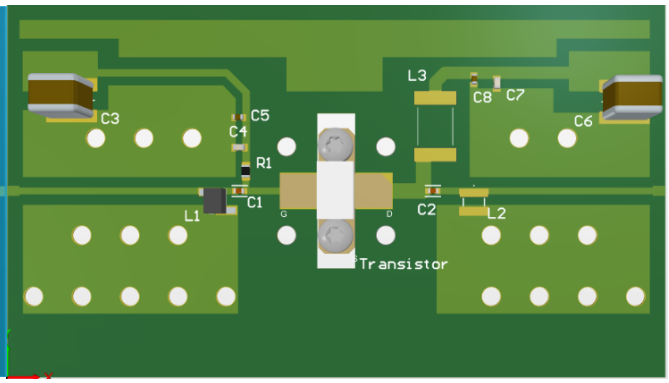


Figure 5.34: Layout 2 in Altium

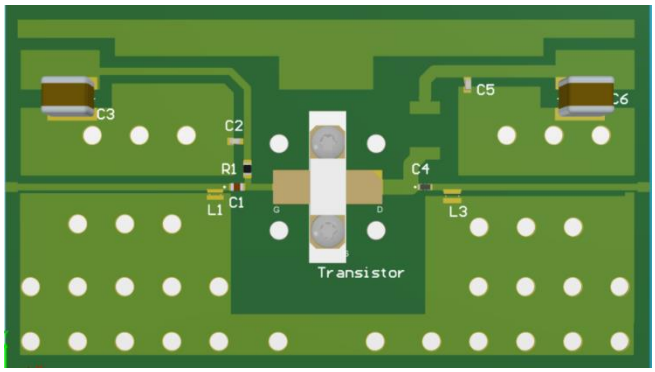


Figure 5.35:Layout 3 and 4 in Altium

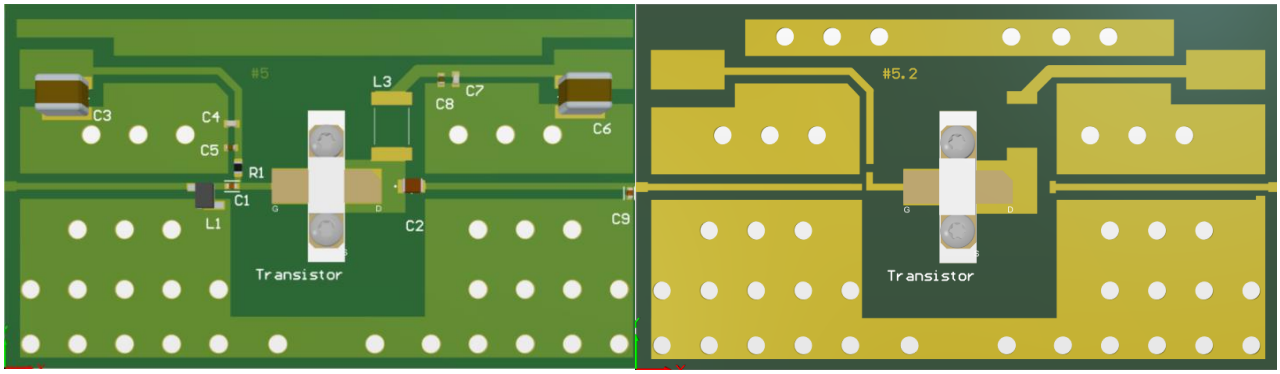


Figure 5.36:Layout 5 and 5.2 in Altium

In iterations 3 and 4, the layout remains the same, but the design uses a different decoupling capacitor, and capacitors replace the inductor for matching. Similarly, iterations 5 and 5.2 share the same layout; however, in version 5.2, the top copper plane is grounded to enhance the coplanar waveguide performance of that section.

Iteration 2 received the most in-depth study, as it was the first design created and had to be tested against numerous specifications. The primary parameter of interest was the amplifier's output power, for which we obtained the following results:

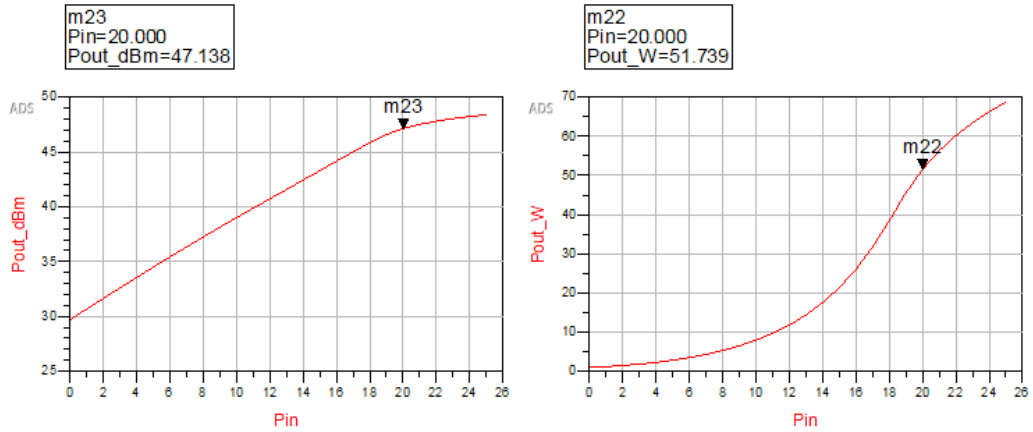


Figure 5.37: Simulation results of output power in dBm and W as a function of input power

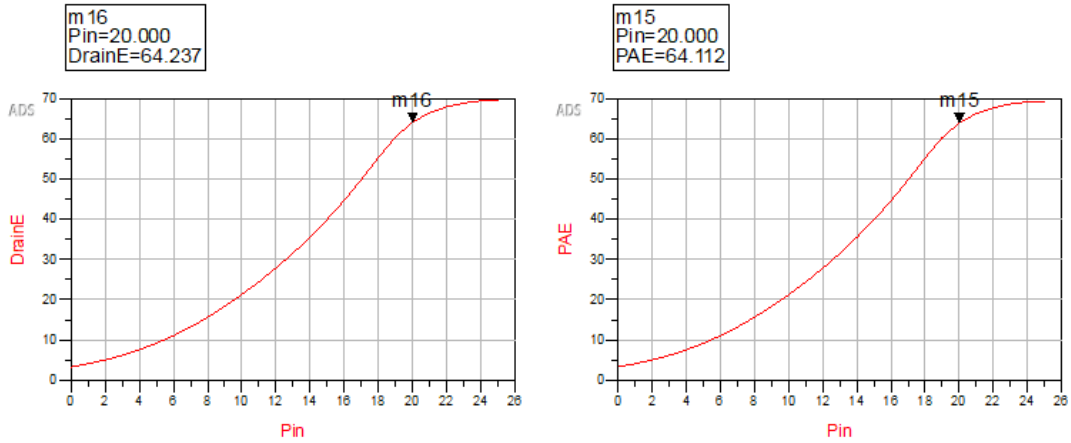


Figure 5.38: Simulation results of drain efficiency and power added efficiency as a function of input power

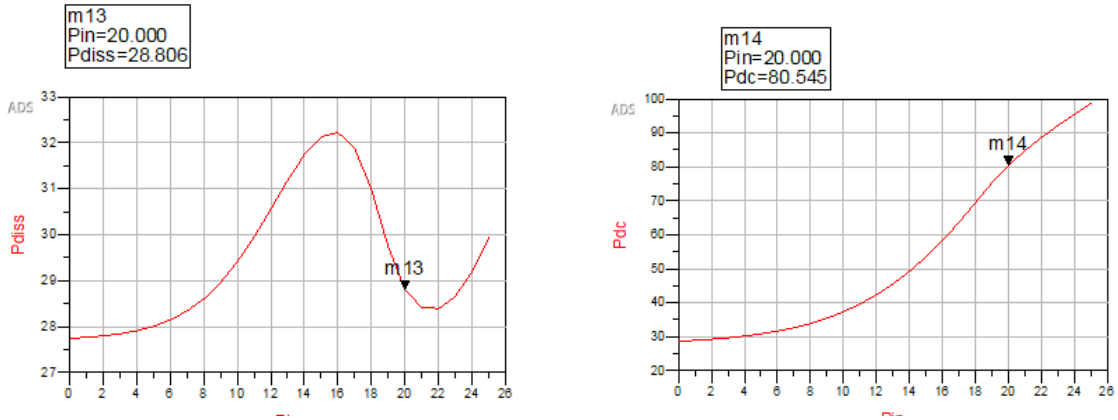


Figure 5.39: Simulation results of power dissipated and DC power offered as a function of input power

On figure 5.37 we notice that for 20dBm input power, we achieve the 50W of power that we need, with an efficiency of 64%.

Next, we measure the gain behavior:

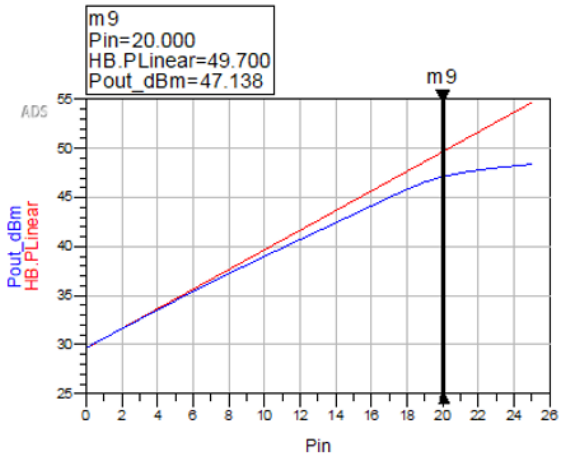


Figure 5.40: Simulation results of output power for and without standard gain

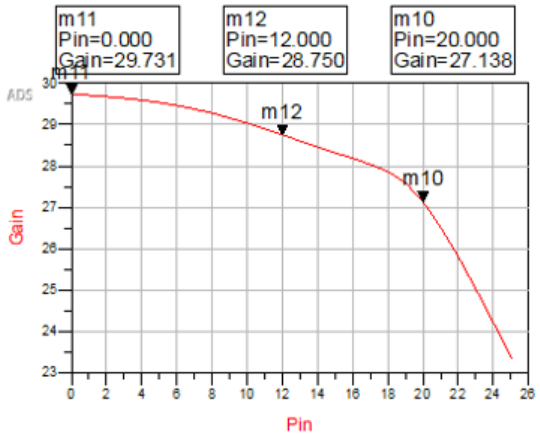


Figure 5.41: Simulation results of gain and output power as a function of input power

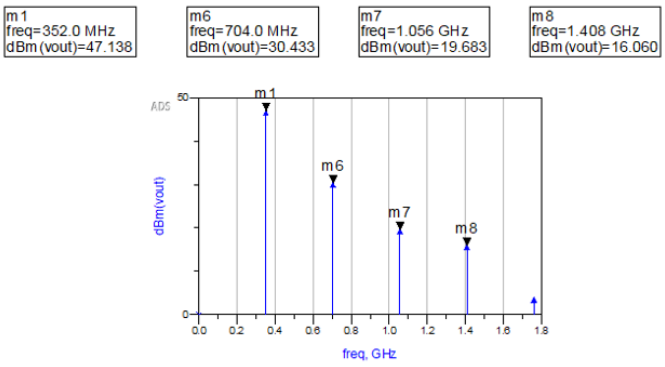


Figure 5.42: Simulation results of Harmonics

We observed significant saturation, indicated by a gain compression of nearly 3 dB from the unsaturated linear value. Additionally, we examined harmonic performance at an input power of 20 dBm.

Finally, we analyzed the behavior of the S-parameters:

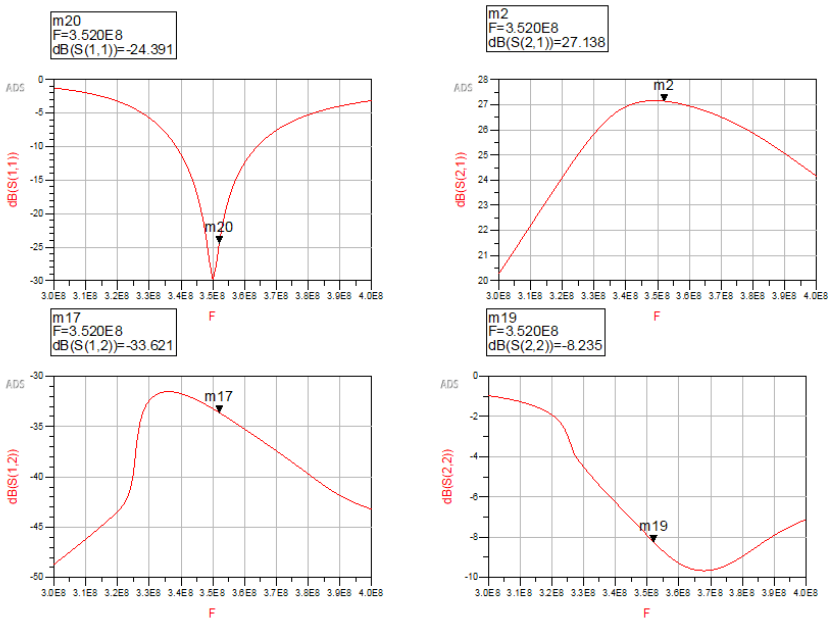


Figure 5.43: Simulation results of S-parameters as a function of frequency

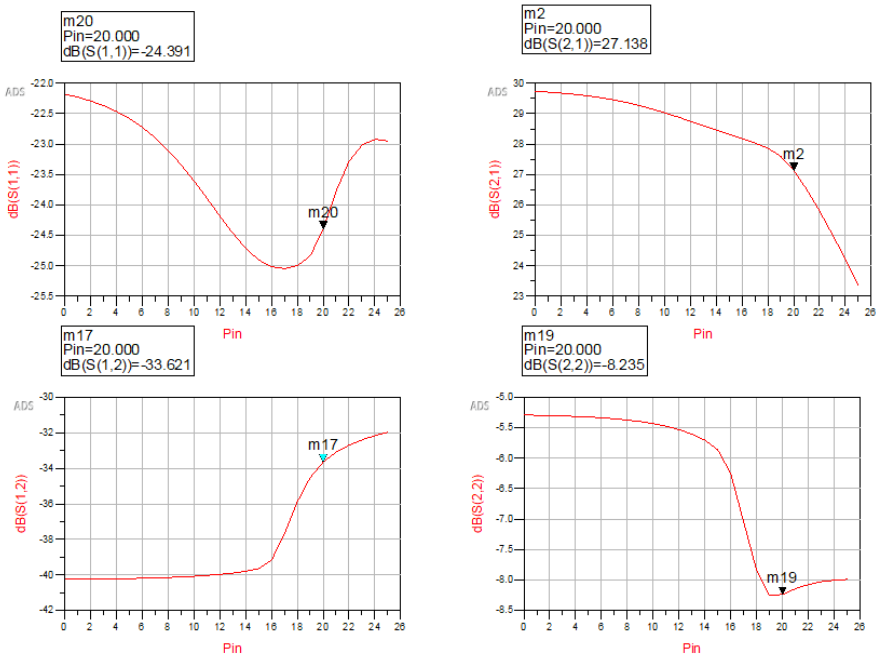


Figure 5.44: Simulation results of S-parameters as a function of input power

In the first set of S-parameter values, we observe how they vary with frequency, while the second set shows their dependency on input power. As expected, the S-parameters fluctuate with frequency and also shift based on input power, reflecting the amplifier's power-sensitive behavior. At 20dBm input power, we calculate the K stability factor to be 1.136, which is greater than 1, thus meeting the criteria for unconditional stability.

On figure 5.45 we also attach the simulation estimation of output power for PCB iterations 4 and 5 respectively:

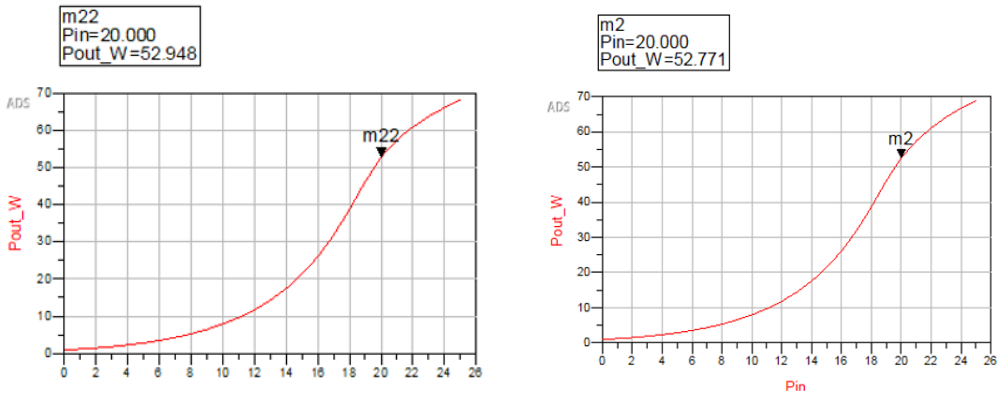


Figure 5.45: Simulation results of iterations #4 and #5 for output power as a function of input power

5.6 Summary

The layout development of the SSPA driver's first stage includes selecting the suitable PCB material and comparing transmission line types—microstrip, stripline, and coplanar—to choose the optimal one for each specific application. Key layout decisions involve the precise placement of the transistor and connectors to ensure performance and reliability. Matching networks are refined through several iterations to maximize efficiency. Thermal management is achieved through a carefully designed heatsink, considering factors such as transistor geometry, PCB dimensions, drilled holes, and quality checks. The finalized layout undergoes simulation to validate its robustness, and a summary outlines the key design choices and improvements. The summary of this chapter can be presented by the tables below:

Parameter	Value
Material	RO3210
Dielectric constant, Design	10.8
Dissipation factor	0.0027
Thermal conductivity	0.81 W/m/K
Thermal coefficient of er	-459 ppm/°C
Height	1.27mm
Trace Thickness	0.035mm

Table 17: Summary of PCB material

Parameter	Value
Trace width, a	1.084 mm
Trace width with gaps, b	3.184 mm
Gap	1.55 mm

Table 18: Dimensions of transmission line for 50 Ohms characteristic impedance

Parameter	Value
Trace width, a	2.2mm
Current to handle	4.1 A

Table 19: Transmission line dimensions for RF choke – transistor connection

Parameter	Value
Input coupling capacitor	GQM2195C2E131GB12D
Output coupling capacitor	GQM1875C2E510FB12
Input inductor	A02T GLB
Input inductor distance from capacitor	3.5mm
Output inductor	1508-9N0 GLC
Output inductor distance from capacitor	1mm

Table 20: Summary of matching network 2 and 3

Parameter	Value
Input coupling capacitor	GQM2195C2E131GB12D
Output coupling capacitor	GC332QD72E104KX01L
Input inductor	A02T GLB
Input inductor distance from capacitor	3.5mm
Output capacitor	2x (GQM1875G2E100JB12D)
Output capacitor distance from coupling at 4	34mm
Output capacitor distance from coupling at 5	35.5mm

Table 21: Summary of matching network 4 and 5

Parameter	Value
Design 2	51.75W
Design 3	51.75W (expect improvement)
Design 4	52.95W
Design 5	52.8W

Table 22: Summary of power estimations per iteration

Chapter 6: SSPA Manufacturing and Testing

6 Introduction

In this chapter, the manufacturing processes involved in assembling the amplifier are outlined, the required specifications are presented, the lab setups used for essential measurements are described, and obtained results are analyzed.

6.1 Gerber file and PCB Production

In order to start the manufacturing process, the first step is to produce the Gerber files, which are already shown in the previous chapter. Gerber files are the standard file format used in the electronics industry to describe the physical layout of a printed circuit board. These files contain all the information necessary for manufacturing the PCB, including the details about copper layers, solder masks, silkscreen, and drill holes. Below we can see how we can produce them on Altium:

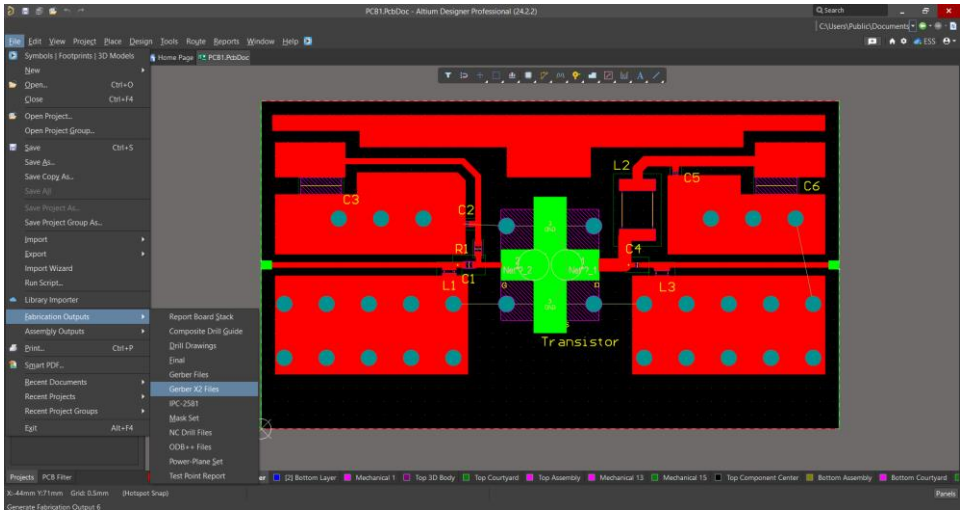


Figure 6.1: Altium workspace

In the Gerber options menu given below, we need to choose layers we want to generate in this format. We need the board outline, to define the size of the board, the top copper layer, to contain all the traces and ground planes without the bottom layer since it is pure copper and the drills to contain all the information needed for screw holes and the cut made for the transistor placement.

The generated Gerber file:

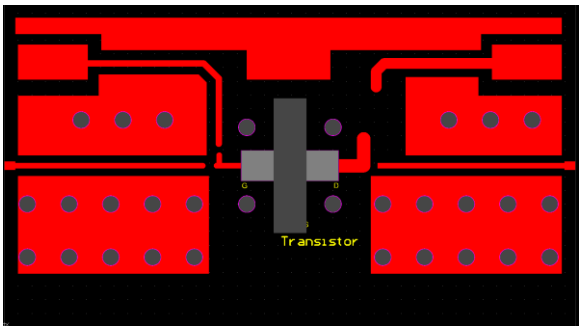


Figure 6.2: Generated Gerber file

Next, we load the Gerber files produced on a USB and connect with the LPKFS63 drilling machine. We place a copper board of the RO3210 material and attach tape to keep it mechanically stable:

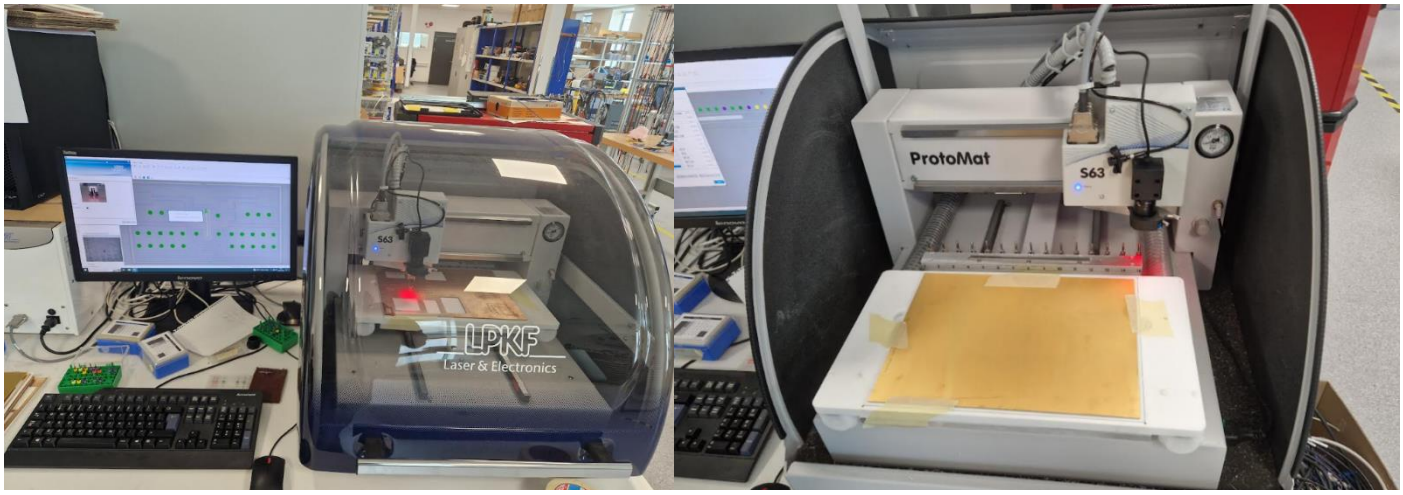


Figure 6.3: Drilling machine and copper plate

The final product of this operation is shown below:

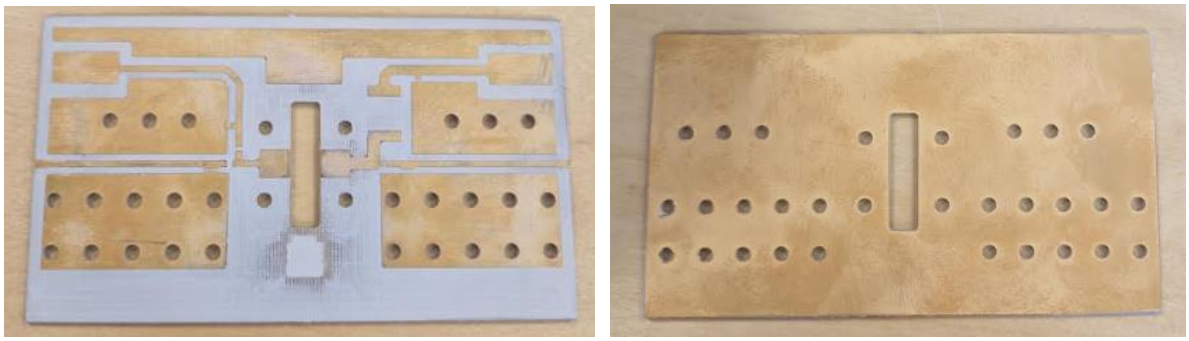
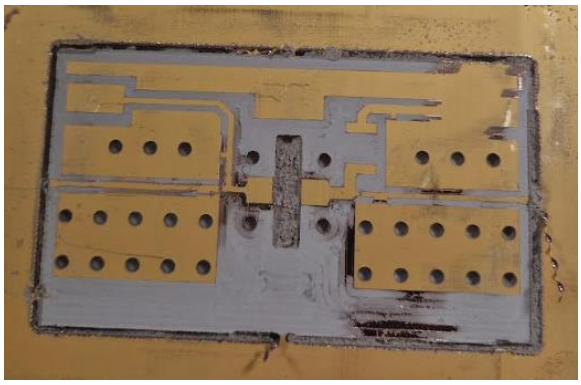


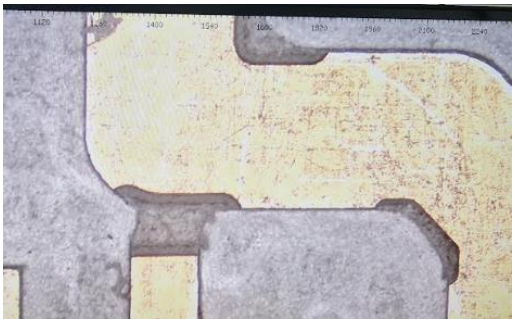
Figure 6.4: Top and Bottom layer after the drilling

There are many iterations that faced problems, sometimes catastrophic for the copper board. This happened due to the limited capabilities of our drilling machine. The drilling tools needed to be refreshed in order to be sharper, as they “overdrilled” on 270 degrees bends and at discontinuities of the microstrip trace width or they did not drill at all as shown below:

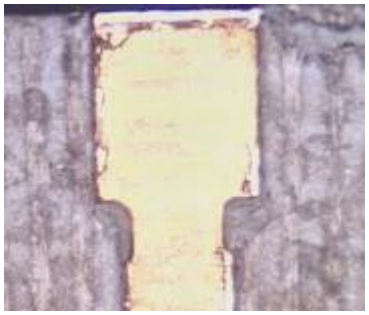


Destroyed PCB

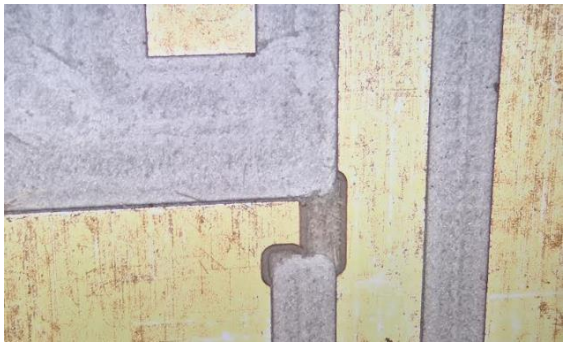
Transistor pad



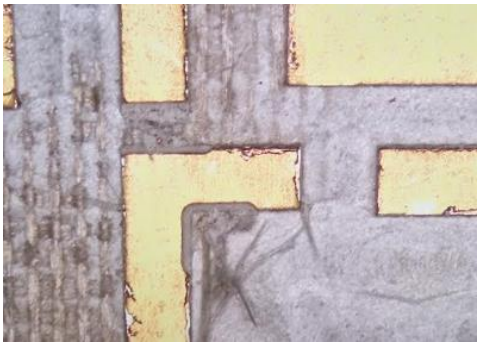
Output coupling capacitor and RF choke coil



N-connector pad



Decoupling capacitor



Input coupling capacitor and choke resistor

Figure 6.5: Pictures of PCB impairments

6.2 Soldering and Assembly

The next step involves soldering the components and assembling the PCB. This includes attaching components and N-connectors to the PCB, carefully positioning and securing the transistor for mechanical stability, attaching the heatsink, and mounting a heat dissipator.

Proper soldering is critical to the overall performance of the amplifier. Issues such as solder voids, excessive solder, or solder bridges creating unwanted connections can lead to significant problems. To ensure reliable connections, we begin by applying flux to the designated area to improve solder flow. The surface is then pre-heated, followed by melting the solder to create clean, even pads for the surface-mount components. Each component is carefully soldered, ensuring enough heat is applied for the solder to spread evenly while avoiding excessive heat that could damage components. For example, the coupling capacitor (GQM1875C2E510FB12) was previously overheated, leading to its destruction and preventing RF power from flowing. This highlights the importance of temperature control and precision during soldering.Below are examples of soldering completed during this process:

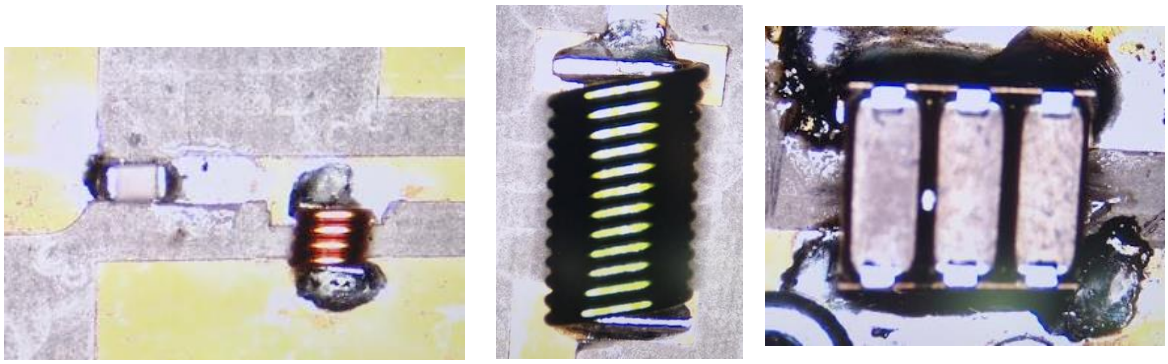


Figure 6.6: Pictures of examples of good soldering

On the top three pictures, there is enough solder material to keep good contact between the microstrip trace and the components. On the bottom picture there is excess solder and some solder voids, adding noise in the system and increasing losses.

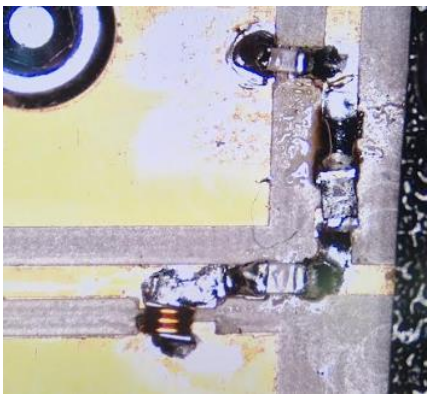


Figure 6.7: Picture example of bad soldering

Next, the heatsink is attached to the PCB. To ensure optimal performance, we first assess the planarity and surface quality of the heatsink, as illustrated below. This assessment, conducted by the ESS mechanical lab, ensures the surface is as smooth as possible to achieve excellent contact. A smooth surface is critical not only for efficient heat dissipation but also for effective grounding.

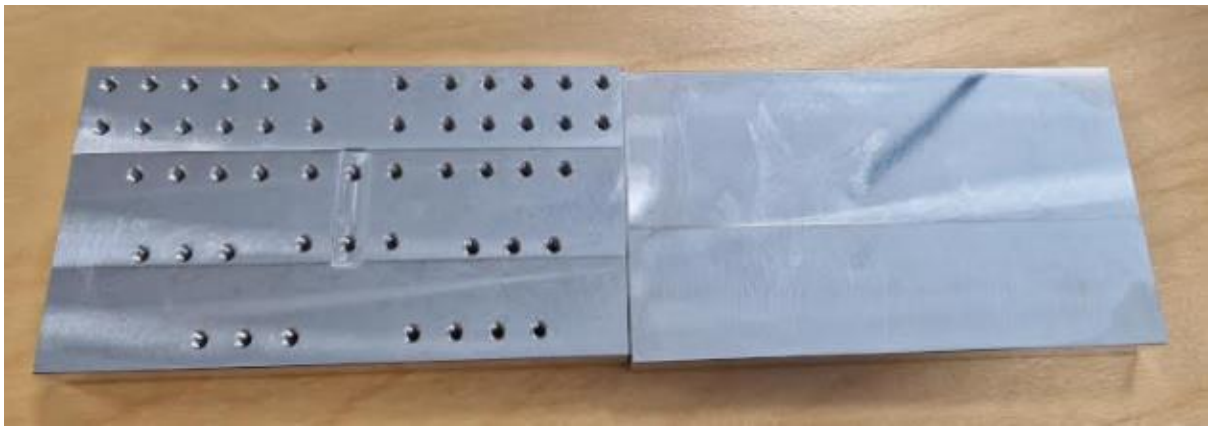


Figure 6.8: Heatsink top and bottom view

The PCB is mounted onto the heatsink using M3 screws to ensure stability. The N-connectors are screwed on the side for mechanical stability and are soldered afterward. The transistor is then put into place, requiring modifications to its screw head for proper fitment. To achieve that, we had to trim the diameter of the head of the screw as the distance between the transistor white body and the center of screw hole was 3.5 mm, while the screw diameter was 5.5 mm. This process altered the flatness of the screw and deteriorated the transistor copper body, when connected. Furthermore, one screw was insufficiently trimmed, exerting excessive stress on the transistor's white body and ultimately causing it to crack. These issues collectively degraded the amplifier's performance.

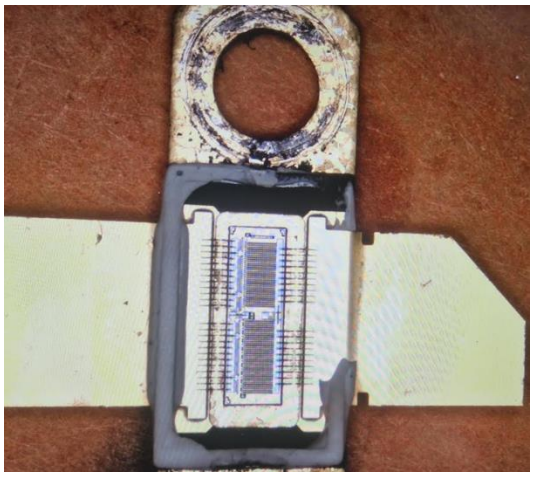


Figure 6.9: Picture of broken transistor

Another key factor affecting the amplifier's performance is the method used to connect the transistor pads—specifically the gate and drain terminals—to the microstrip trace. Two approaches were employed: direct soldering and mechanical pressure applied using PLA blocks. These blocks were custom-designed and manufactured in the ESS RF lab using a 3D printer. The same PLA blocks also played a role in ensuring firm contact between the heatsink and the heat dissipator. PLA (Polylactic Acid) is a biodegradable thermoplastic derived from renewable resources commonly used in 3D printing due to its ease of use, low melting point, and environmentally friendly properties.

Figure 6.10: Picture of the 3D printer

To enhance the system's thermal performance, a heat dissipator was integrated. The heatsink ensures even heat distribution across the PCB, while the dissipator facilitates efficient heat transfer from the system to the surrounding environment, improving overall thermal management. More pressuring blocks were designed and manufactured with the 3D printer to keep good contact between all the integrated parts. Lastly, we solder the bias cables to the microstrip trace to provide the DC power. The amplifier with PLA blocks, with soldered transistor and the assembled amplifier with PCB, heatsink and heat dissipator are shown below:

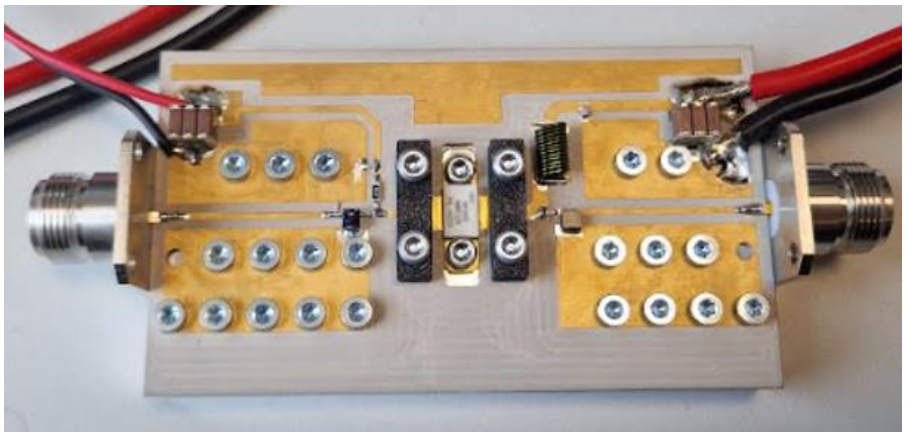


Figure 6.11: Picture of amplifier with PLA blocks

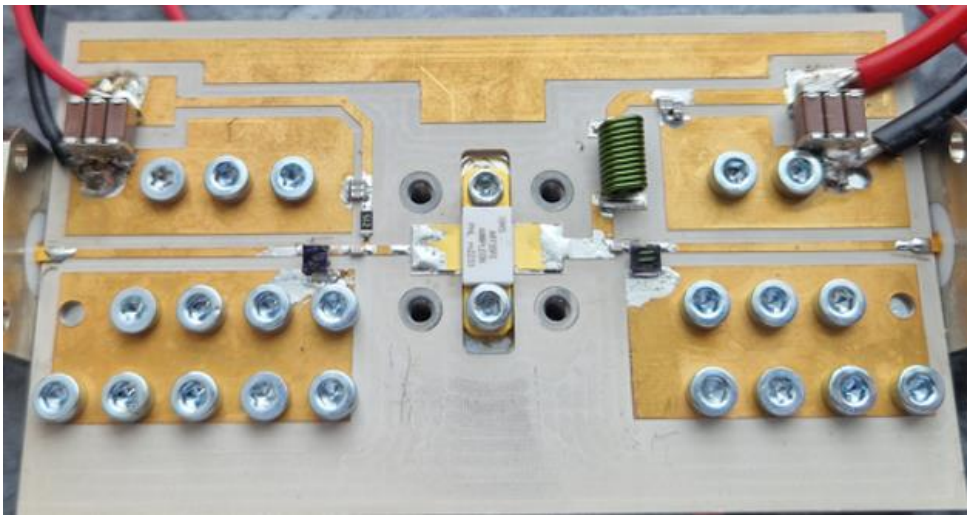


Figure 6.12: Picture of amplifier with soldered transistor

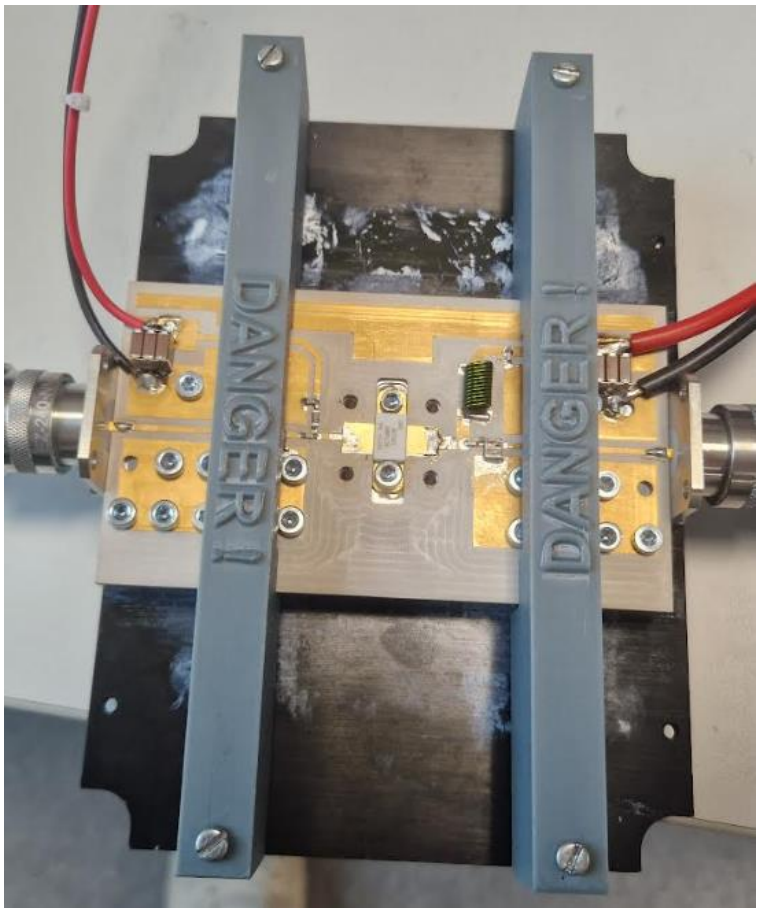


Figure 6.13: Picture of assembled amplifier with PCB, heatsink and heat dissipator

6.3 Manufacturing non-idealities

Figure 6.14 highlights several factors that influenced the amplifier's performance. These issues stem from non-ideal conditions during PCB assembly and amplifier operation. The two orange levels are the copper layers with a gray layer in the middle for the dielectric. The pads of the transistor and the N-type connector are depicted with gold, while the transistor is the white body and the connector is shown on the left. Number 12 are the PLA pads and with number 13 the the PLA blocks that were manufactured in house in order to put pressure on the PCB and force to keep good contact with the heatsink and the dissipater shown in gray and black below. Each factor is numbered in the image and explained in detail as follows:

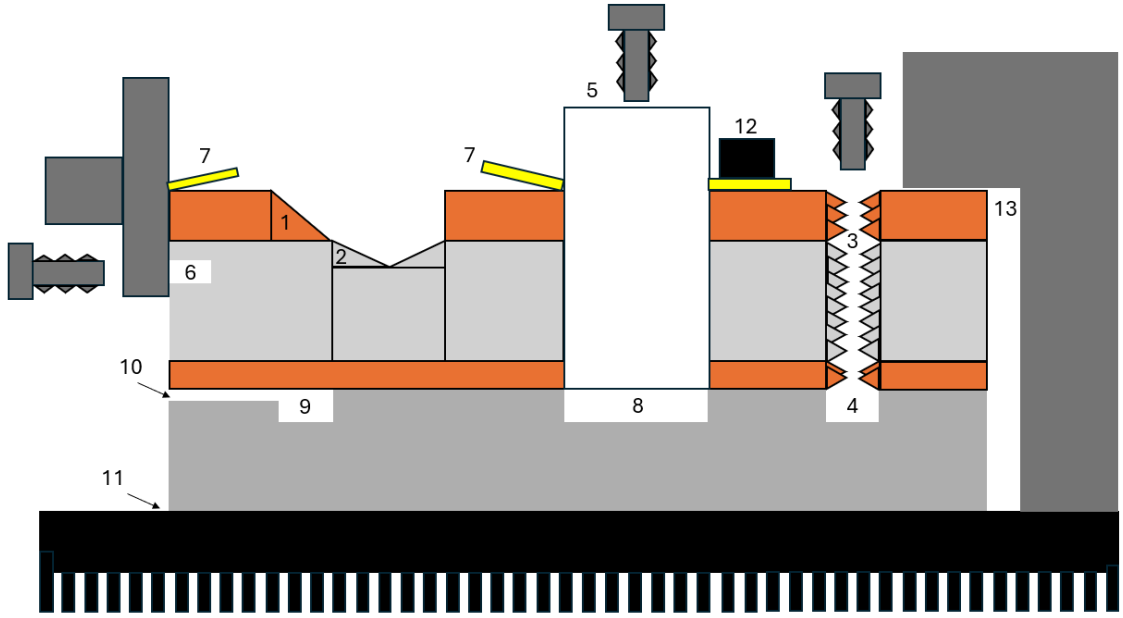


Figure 6.14: Manufacturing non idealities

1 & 2: Due to the drill's movement tolerance and tool wear, the copper at point 1 is unevenly cut, altering the trace dimensions. Similarly, at point 2, the dielectric is modified under the same conditions. These deviations change the characteristic impedance, as the electric field is forced to follow longer paths before reaching ground.
3: The drilling machine cuts through the RO3210 layers to create space for the screws. However, due to tool imperfections, small residuals often remain around the holes. These irregularities disturb the local electric field distribution, introducing parasitic effects that can degrade circuit performance.
4 & 6: The heatsink includes designated holes for screw placement. If screws shorter than the hole depth are used, small cavities may form, trapping electric fields and altering the local ground potential. Similarly, precise screw placement is essential when mounting the N-type connector, as misalignment can compromise both mechanical stability and electrical grounding.
5 & 8: The transistor is fixed to the heatsink using two screw holes to ensure both mechanical stability and proper thermal contact. However, excessive screw force may damage the transistor body, while insufficient tightening can leave a gap between the transistor and the heatsink (issue 8). Such imperfections degrade the common ground reference, since the heatsink also serves as a grounding plane. In addition, poor contact reduces thermal conductivity, increasing device temperature. To improve heat transfer and minimize ground discontinuities, thermal paste is applied between the surfaces.
7 & 12: N-type connectors are used to deliver RF power to and from the amplifier. Their attachment requires precise alignment, as even small angular deviations or excess solder can alter the geometry of the joint. Such imperfections introduce capacitive parasitics, created by the conductive layers separated by the dielectric medium. A similar issue arises with the transistor pads during soldering. When PLA blocks are used to secure the pads (issue 12), their

non-ideal dielectric properties (εr ≈ 3.2) allow partial coupling of RF energy to ground, further degrading circuit performance.
9: Not all the screw holes provided on the heatsink are utilized in the amplifier design. The unused holes act as small cavities that can trap electromagnetic fields, disturbing current distribution and adversely affecting the grounding integrity of the system.
10 & 11 & 13: Reliable contact between the PCB, heatsink, and heat dissipator is essential for both electrical and thermal performance. Misalignment during assembly may create small gaps—between the PCB and the heatsink (issue 10) or between the heatsink and the dissipator (issue 11). Such gaps reduce thermal conduction and compromise the continuity of the ground reference. To mitigate this, thermal paste is applied to both interfaces. Furthermore, a PLA block is used to apply pressure on the PCB ground planes (issue 13), ensuring good mechanical contact. However, the presence of PLA introduces an additional dielectric path, which can disturb the ground level and create unintended RF current leakage.

6.4 Specifications

With the manufacturing complete, the amplifier is now ready for testing. The testing phase is essential to verify the amplifier's compliance with the outlined specifications, ensure optimal performance under operating conditions, and identify potential improvements or adjustments needed before integration into the full system. The delivered equipment must meet the specifications outlined below. These requirements were established to align with the 400 kW SSPA system design, ensuring it delivers the required power with the correct characteristics. Additionally, the specifications account for compatibility with the Low-Level RF systems to guarantee system stability and effective monitoring. The specifications table is shown below, as per the official report approved by the RF group and Uppsala University at 2024-02-14:

Parameter	Specification per 2024-02-12	Specification per 2024-08-12
Operating frequency	352.21 MHz	352.21 MHz
-1 dB bandwidth	≥ ±1 MHz	≥ ±1 MHz
Peak output power	30 W (or higher)	50 W
RF pulse width	Up to 3.5 ms	Up to 3.5 ms
Repetition rate	Up to 14 Hz	Up to 14 Hz
Gain	23 dB min	27 dB at 20dBm input
Efficiency	> 50 %	> 50 %
Maximum no-damage RF drive input	26 dBm	26 dBm

Harmonic content at output power	< -30 dBc	< -30 dBc
Spurious and sideband levels in ± 20 MHz	< -60 dBc	< -60 dBc
RF Input Connector	N type, 50 Ω, Female	N type, 50 Ω, Female
RF Output Connector	N type, 50 Ω, Female	N type, 50 Ω, Female
Input/output impedance	50 Ω	50 Ω
Input VSWR	≤ 1.2:1 (target requirements)	≤ 1.12:1 or -25dB (target requirements)
output VSWR	≤ 1.2:1 (target requirements)	≤ 1.12:1 or -25dB (target requirements)
Load VSWR	Infinity	Infinity
Gain flatness	ΔG ≤ ±0.5 dB (over 10dB dynamic)	ΔG ≤ ±0.5 dB (over 10dB dynamic)
Phase flatness	≤ 2°(over 10dB dynamic)	≤ 2° (over 10dB dynamic)
RF Power Drop across the pulse	≤ 5% p-p (or Max 0,21dB) (power) (Within 3.5ms RF pulse excluding first 100µs of the pulse)	≤ 10% p-p (or Max 0,21dB) (power) (Within 3.5ms RF pulse excluding first 100µs of the pulse)
Power ripple across pulse	≤ 0.25% rms (Within 3.5ms RF pulse excluding first 100µs of the pulse)	≤ 0.25% rms (Within 3.5ms RF pulse excluding first 100µs of the pulse)
Phase shift across the pulse	≤ 5° (Within 3.5ms RF pulse excluding first 100µs of the pulse)	≤ 10° (Within 3.5ms RF pulse excluding first 100µs of the pulse)
Phase ripple across pulse	≤ 0.25° rms (Within 3.5ms RF pulse excluding first 100µs of the pulse)	≤ 0.25° rms (Within 3.5ms RF pulse excluding first 100µs of the pulse)
Pulse-to-pulse power stability	≤ 2%	≤ 2%
Pulse-to-pulse phase stability (repeatability)	≤ 2°	≤ 2°
RF Pulse Rise/ Fall Time	≤ 1 µs	≤ 1 µs
compression point @ 0,1dB	54 W	54 W
Total Group Delay (not sure we need this parameter)	≤ 50 ns	≤ 50 ns

Size	Max size of the PCB 20x10 cm	Max size of the PCB 20x10 cm

Table 23: Specifications of the Driver's 1st stage

Meeting these specifications is critical to the overall functionality of the 400 kW SSPA system, ensuring efficient power delivery, precise control of RF signals, and long-term reliability in operational environments. Once the amplifier passes all tests, it will be integrated into the SSPA system and subjected to additional system-level evaluations to confirm its performance in conjunction with other components.

6.5 Lab preparation

In this chapter, we will explore the process of testing whether the manufactured amplifier meets the required specifications. We begin by introducing the equipment and components used, detailing their functionality and the rationale behind their selection. Following this, we delve into how these elements are interconnected to perform specific measurements, forming a cohesive test system.

6.5.1 Equipment

In order to test an RF amplifier there are several more parts needed in order to complete a setup. To complete the characterization of the amplifier, the following equipment was used:

- For signal generation

Figure 6. 15: Picturers of Rohde & Swartz SMC100A and Keysight Technologies N5182B-503 signal generators

The SMC100A generator is used for low-power testing, as it can deliver up to 14 dBm. The N5182B-503 generator, capable of producing up to 30 dBm, and push the amplifier to produce maximum power. Additionally, the N5182B-503 supports the generation of pulsed signals, similar to the signals used by the accelerators and, consequently, our amplifier. Every time we want to use these to provide power we need to calibrate the output power indicated by the device and the real power received by the amplifier. This misalignment occurs because

the generator is not ideal and may have decayed. There is power loss in the connection points and in the RF cables that should also be taken into consideration.

- For DC power generation

Figure 6.16: Pictures of Aim-TTi EL 302 R and Rohde & Schwarz HMC8043 power supplies

We use the Aim-TTi EL 302 R power supply for the gate bias and the HMC8043 for the drain bias. The second device can monitor the current consumption and limit it, which is critical since the amplifier needs almost 80W of power to operate.

- For power measurements

Figure 6.17: Pictures of Rohde & Schwarz NRP2 Rohde & Schwarz NRX Power meters

- For signal analysis

Figure 6.18: Picture of Keysight Technologies N9020B MXA signal analyzer

- For amplitude and phase measurements of electromagnetic waves

Figure 6.19: Picture of Rohde & Schwarz ZNB4 Vector Network Analyzer

- For signal attenuation

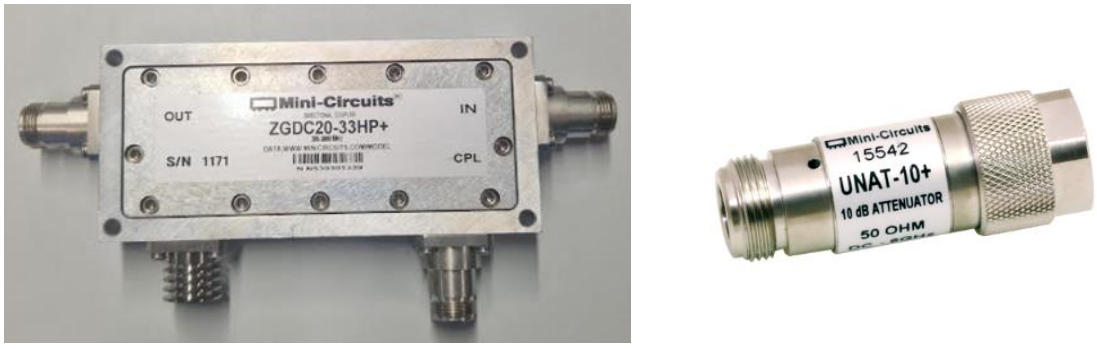


Figure 6.20: Picture of a High-Power Directional Coupler and an Attenuator

The measuring devices have a limit for the input power they can handle without deterioration. For this reason, before measuring sometimes we need to attenuate the signal.

- For termination and circulation

Figure 6.21: Pictures of Weinschel Associates WA1453 and Valvo Circulator VAD1447A

- For thermal monitoring

Figure 6.22: Picture of RFS FLIR E63900 thermal camera

6.5.2 Bench Setup

In this subchapter, we detail the measurement setup and outline the procedures used to conduct the tests. Every bias circuit, unless mentioned, has gate voltage and drain voltage set at 2.5 and 70 Volts.

- **Power measurements**

In this setup, we will measure the output power of the amplifier. The signal generator provides the input signal, which is transmitted to the amplifier via RF cables. The amplifier, powered by connected power supplies, amplifies the RF signal. We use the second signal generator because it is the only one capable of delivering a 25 dBm signal.
A directional coupler is connected at the amplifier's output. The coupler's output port is terminated with a 50-ohm load, which completes the circuit and dissipates the generated power safely. The coupler's coupling port, with a coupling factor of -24.5 dB at our operating fre-

quency, is connected to a 10 dB attenuator to protect the measurement equipment. The attenuated signal is then sent to the power meter for precise measurement. The way to connect these is shown below:

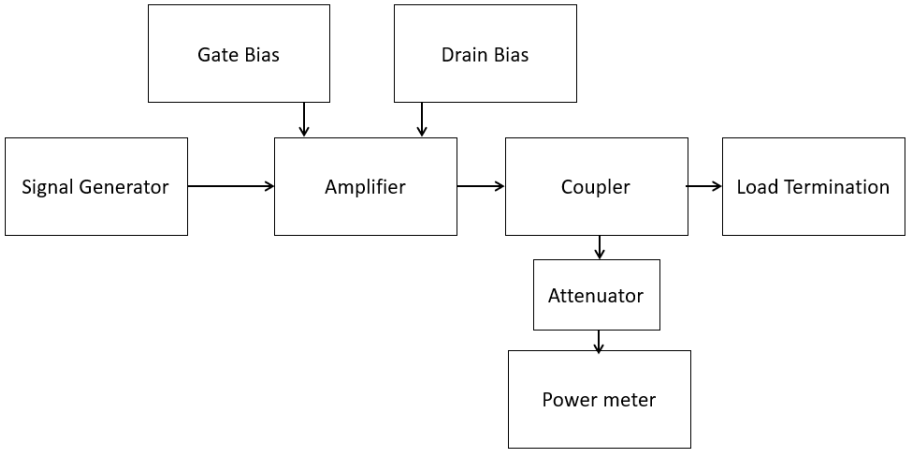


Figure 6.23: Topology for power measurements

We need to calibrate the signal generator to ensure that the power delivered to the RF cable matches the power indicated on its display. Additionally, we must measure the total attenuation introduced by the coupler, attenuator, and RF cables.

With this setup, we can evaluate the amplifier's performance across various specifications. By comparing the input power from the generator to the output power measured by the power meter, we can determine the amplifier's output power and gain. This allows us to identify key parameters such as the 1 dB and 3 dB compression points, gain flatness, and performance variations across different PCB iterations.

By adjusting the generator's operating frequency, we can also measure the amplifier's -1 dB bandwidth and 10 MHz bandwidth. Using the drain power supply's display, we can monitor current consumption to calculate the DC power supplied, enabling us to determine the system's efficiency. Finally, a thermal camera can be employed to assess the PCB's thermal behavior, providing valuable insights into heat dissipation and potential thermal challenges.

- **Signal analysis measurements**

In this setup, we will analyze the signal and its spectral content. The equipment configuration remains the same, except that the power meter is replaced by a signal analyzer. The detailed configuration is illustrated on the next page:

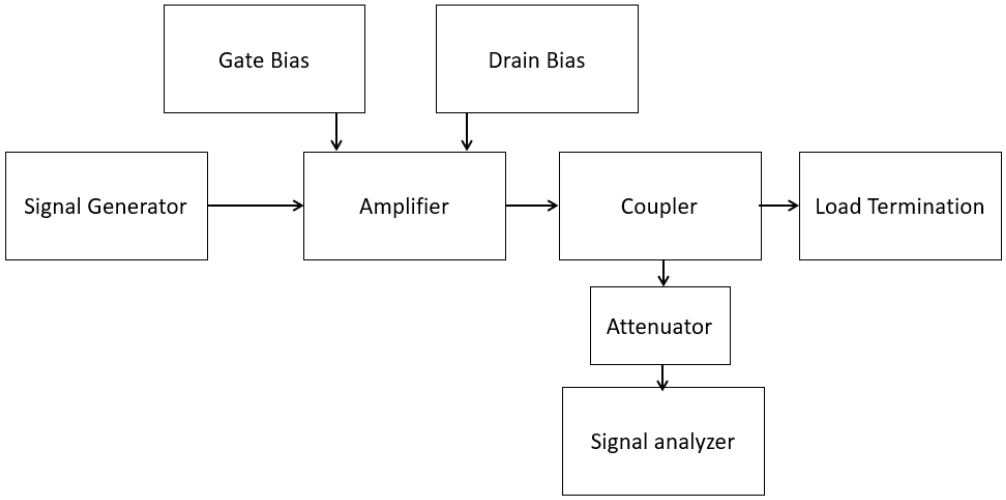


Figure 6.24: Topology for signal analysis

This way, we can monitor the harmonics, the spurious and the sideband levels. Moreover, since the accelerator is operating in pulsed mode, we can use the second generator to produce pulsed signals and monitor phase and power drop, phase flatness, power ripple across the pulse, pulse-to-pulse repeatability.

- **Vector Network Analyzer configuration**

In this setup, we will measure the amplitude and phase of the wave quantities. The configuration is shown below:

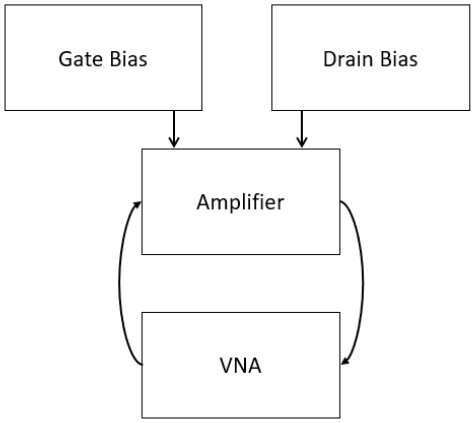


Figure 6.25: Topology for Vector Network Analyzer measurements

The VNA can generate up to 13dBm output power. So, with this setup we can measure low-power S-parameters and total group delay. For full S-parameter characterization we need different setup.

- **S11 measurements**

As previously mentioned, a different configuration from the VNA is required to measure the S11 performance of the amplifier. Using the available equipment, this is achieved by directly measuring the amplitude of the reflected wave. In this setup, a signal generator provides RF power to the biased amplifier through a directional coupler, while the amplifier's output is connected to a load termination. The coupler's coupling port is connected to a signal analyzer, which measures the reflected wave. The high directivity of the coupler, approximately 28 dB at the operating frequency, ensures that the incident wave traversing the coupler does not interfere with the measurement. The detailed configuration is shown below:

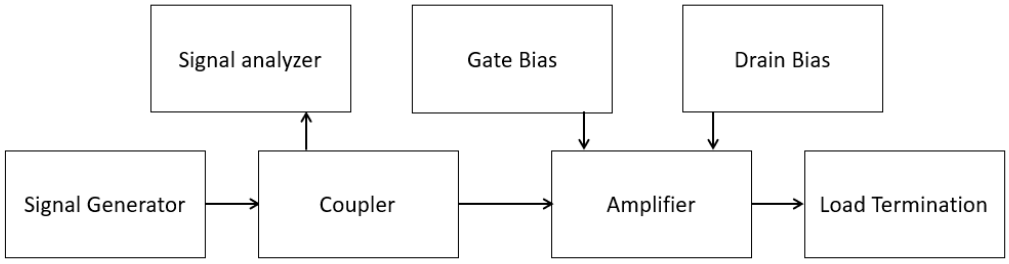


Figure 6.26: Topology for S11 measurements

- **S22 measurements**

To measure the S22 performance, we require a different setup. This is achieved by directly measuring the amplitude of the reflected wave from the amplifier's output, commonly referred to as a "hot S22" measurement. Since the amplifier operates in saturation, its S-parameter behavior depends on the input power. For accurate high-power measurements, it is essential to replicate the output match characteristics of the amplifier.

In this setup, the amplifier is biased and supplied with RF power. The output of the amplifier is connected to two directional couplers in series, with a load termination at the end. The coupling port of the second coupler is connected to a signal generator via a circulator. The circulator ensures that power flows from the generator to the system while blocking any power in the reverse direction, redirecting it to a load termination. The signal generator produces a signal at a slightly different frequency than 352.21 MHz. The frequency offset is small enough to emulate the amplifier's behavior at the operating frequency but large enough to be distinguishable. This signal is directed to the amplifier’s output, and the reflected wave is captured through the coupling port of the first coupler. The reflected wave is then routed through an attenuator, to protect the equipment, before being measured by the signal analyzer.

This configuration, which is shown below, ensures accurate S22 measurements while safeguarding the equipment involved:

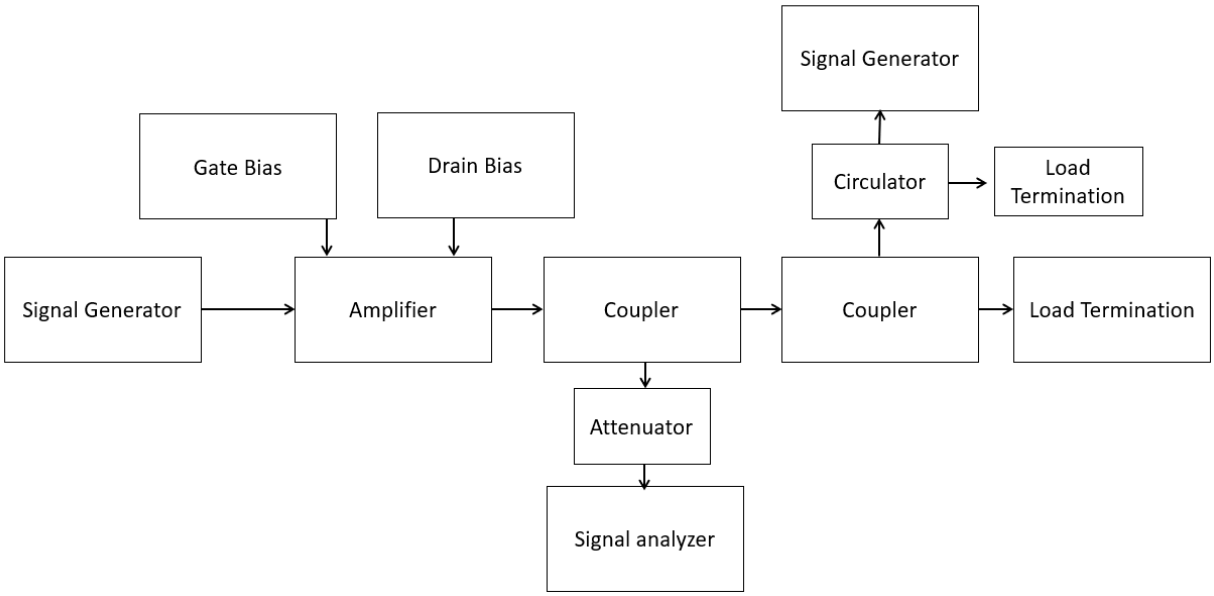


Figure 6.27: Topology for S22 measurements

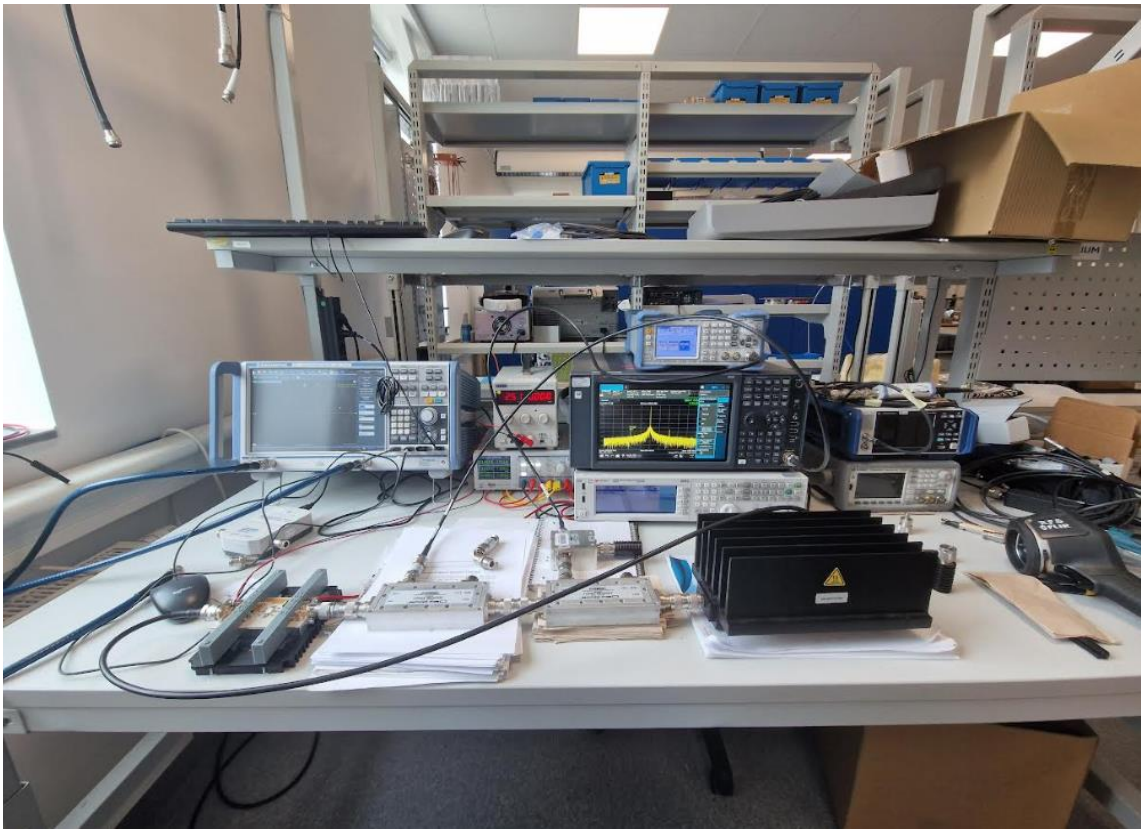


Figure 6.28: Bench overview of S22 measurements

- **Cascaded amplifiers**

After verifying that the amplifier met all the required specifications, the performance of the driver was tested. As previously described, the driver consists of a 1st and 2nd stage. To evaluate its behavior, the two amplifiers were cascaded and interconnected through a coupler to monitor the amplification process, and a circulator to prevent reflected waves from reaching and potentially damaging the 1st stage. A signal generator was used to produce the pulsed signals required for testing. Additional couplers were placed at the input and output of the system to monitor the RF power levels. At the output, a signal analyzer was connected to examine the spectral content of the amplified signal. The biasing of the second stage was configured with 2 volts for the gate and 70 volts for the drain. The complete topology of this setup is illustrated on the next page:

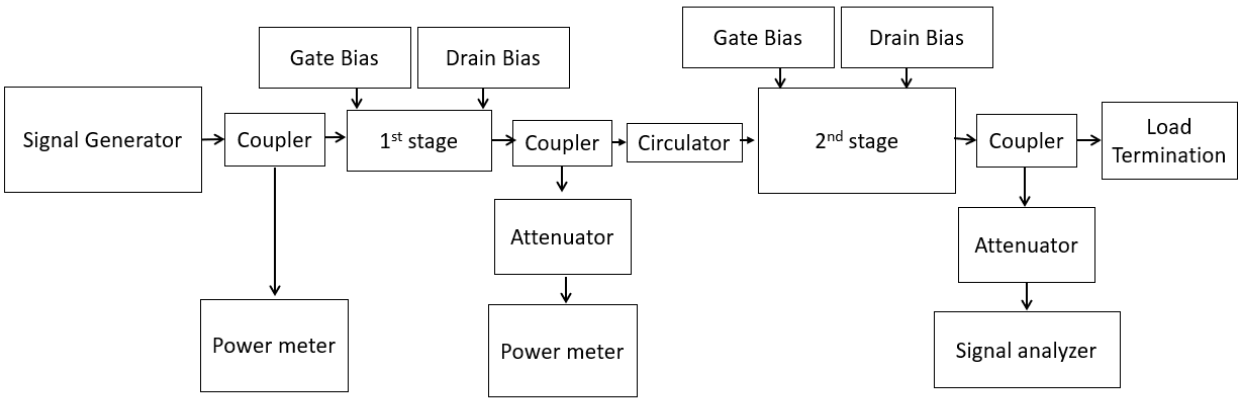


Figure 6.29: Topology for cascaded amplifiers measurements

6.6 Measurements

In this chapter, we present the detailed measurements conducted to evaluate the amplifier's performance and verify its compliance with the specified requirements. Through this comprehensive evaluation, we aim to demonstrate that the amplifier is fully optimized and adheres to the intended design specifications. The complete set of measurements was done for the 2nd PCB iteration, which are presented below:

Firstly, we present the results obtained by the power measurements under continuous wave operation for PCB iteration number 2.

Input power (dBm)	Output power (dBm)	Output power (Watts)	Gain (dB)
0	30.2	1	30.2
1	31.1	1.3	30.1
2	32	1.59	30
3	33	2	30
4	34	2.5	30
5	35.1	3.2	30.1
6	36.1	4.1	30.1
7	37.05	5.1	30.05
8	38	6.3	30
9	38.9	7.8	29.9
10	39.8	9.5	29.8
11	40.7	11.7	29.7
12	41.6	14.5	29.6
13	42.3	17	29.3
14	43.1	20.4	29.1
15	44.1	25.7	29.1
16	44.9	30.9	28.9
17	45.6	36.3	28.6
18	46.16	41.3	28.16
19	46.53	45	27.53
20	46.85	48.4	26.85
21	47.1	51.29	26.1
22	47.3	53.7	25.3
23	47.4	54.9	24.4
24	47.5	56.2	23.5
25	47.63	58	22.63

Table 24: Power measurements of iteration #2

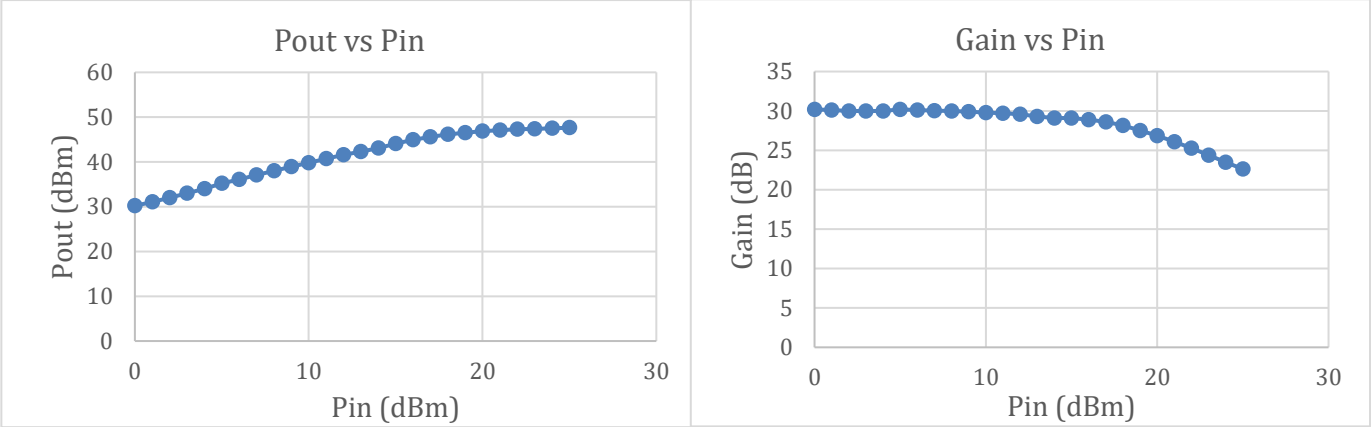


Figure 6.30: Measurements of output power and gain as a function of input power

At an input power of 20 dBm, the amplifier delivers 48.4 W, and at 21 dBm, 51.3 W, exceeding the requirements of the system. These measurements indicate that the amplifier is operating deep in saturation. At low input power levels, the gain exceeds 30 dB, while at the operational input power of 20 dBm, the gain decreases to 26.85 dB. Over a 10 dB dynamic range, the gain drops by 3 dB, demonstrating the amplifier's saturation characteristics. The 0.1 dB and 1 dB compression points occur at input powers of 3 dBm and 15 dBm, respectively.

These measurements are done on the PCB with the soldered transistor, which can provide more power than the PCB with the PLA blocks. The results can be seen below:

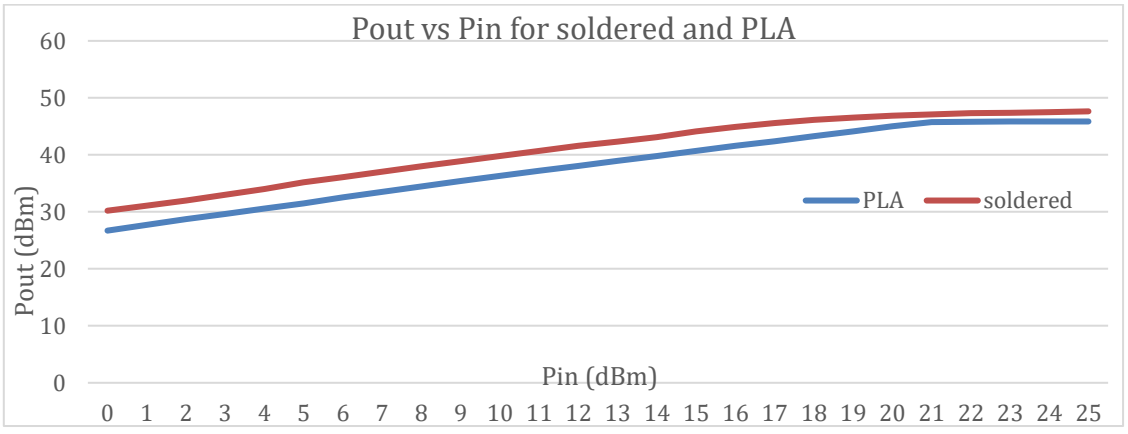


Figure 6.31: Measurements of output power as a function of input power for soldered transistor and PLA blocks connection

Input power (dBm)	Output power (dBm) for PLA	Output power (dBm) for soldered
0	26.7	30.2
1	27.7	31.1
2	287	32
3	29.65	33
4	30.6	34
5	31.5	35.1
6	32.55	36.1
7	33.5	37.05
8	34.45	38
9	35.4	38.9
10	36.3	39.8
11	37.2	40.7
12	38.05	41.6
13	38.95	42.3
14	39.8	43.1
15	40.7	44.1
16	41.6	44.9
17	42.4	45.6
18	43.3	46.16
19	44.1	46.53
20	45	46.85
21	45.75	47.1
22	45.76	47.3
23	45.83	47.4
24	45.85	47.5
25	45.85	47.63

Table 25: Power measurements comparison of soldered transistor and PLA blocks

As indicated by figure 2.112, the PLA blocks consume power and decrease output power. The optimal solution is to solder the transistor. We also monitored the thermal behavior of the different PCBs with the following results:

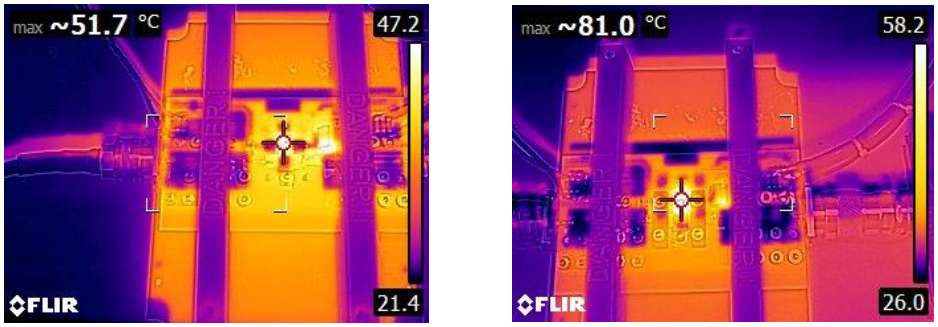


Figure 6.32: Pictures from the thermal camera for soldered transistor and PLA blocks connection monitoring transistor's temperature

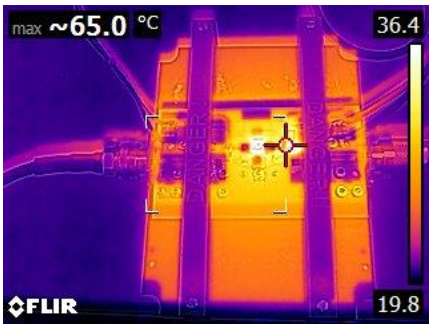


Figure 6.33: Picture from the thermal camera monitoring output capacitor

The performance of the soldered PCB is much better, as it stabilizes at 50-55 °C. We also notice on the output coupling capacitor the temperature is higher than the transistors. This happened because it was a sharp 90 degrees bend and current density increased at that point.

Similarly, during pulsed operation, the amplifier stabilizes at a temperature of approximately 45 °C. This occurs because the reduced current consumption leads to lower heat generation, ensuring more stable thermal performance.

Figure 6.34: Picture from thermal camera monitoring transistor temperature of soldered transistor in pulsed mode

While measuring the output power performance of the amplifier, we also monitored the current consumption through the power supply and calculated several parameters:

Output power (Watts)	Current Consumption (mA)	Input DC Power (W)	Efficiency (%)	Power Added Efficiency (%)	Power dissipated (W)
1	393	27.51	3.6	3.63	26.51
1.3	395	27.65	4.7	4.7	26.35
1.59	398	27.86	5.7	5.7	26.27
2	403	28.21	7.1	7.09	26.21
2.5	408	28.56	8.75	8.74	26.06
3.2	415	29.05	11	11	25.85
4.1	424	29.68	13.8	13.8	25.58
5.1	436	30.52	16.7	16.7	25.42
6.3	450	31.5	20	20	25.2
7.8	470	32.9	23.7	23.68	25.1
9.5	496	34.72	27.4	27.33	25.22
11.7	520	36.4	32.14	32.1	24.7
14.5	554	38.78	37.4	37.35	24.28
17	596	41.72	40.75	40.7	24.72
20.4	644	45.08	45.3	45.2	24.68
25.7	700	49	52.45	52.38	23.3
30.9	765	53.55	57.7	57.63	22.65
36.3	836	58.52	62	61.94	22.22
41.3	906	63.42	65.12	65	22.12
45	966	67.62	66.55	66.43	22.62
48.4	1015	71.05	68.12	68	22.65
51.29	1060	74.2	69.12	68.95	22.91
53.7	1100	77	69.74	69.48	23.3

Table 26: Calculations of current consumption, DC power, efficiency, power added efficiency and dissipated power

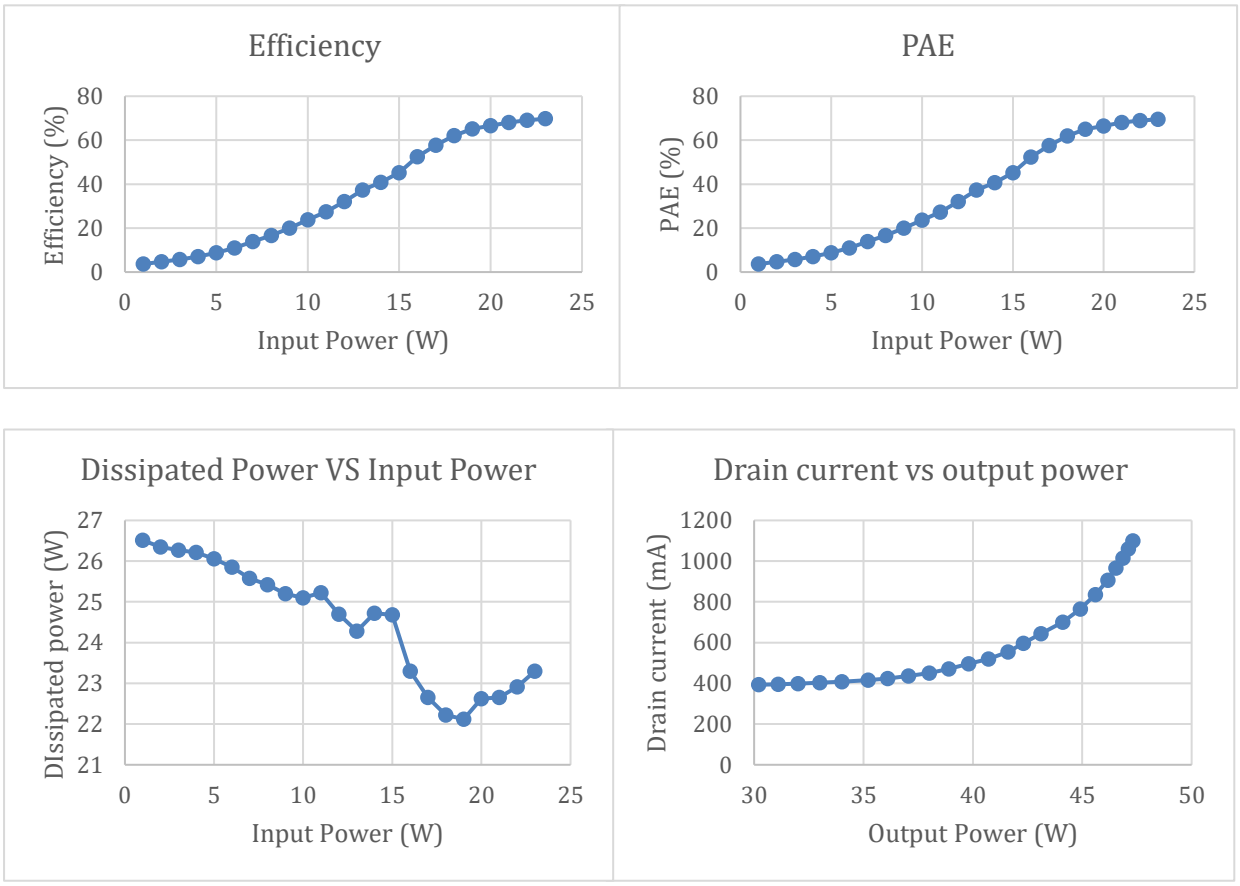


Figure 6.35: Measurements of Efficiency, Power Added Efficiency, Dissipated power and Drain current as a function of input power

As we increase the input power to the amplifier, both efficiency and power-added efficiency (PAE) show significant improvements, while the dissipated power decreases. Additionally, current consumption exhibits an exponential relationship with the output power. This behavior underscores the need for caution when driving the amplifier beyond its specified operational limits, as exceeding these thresholds could result in equipment damage.

Next, we tried to measure the 1dB bandwidth. To do that, we monitored the output power while changing the frequency of the input signal. The results can be seen below:

Operating Frequency (MHz)	Output Power (dBm)	Gain (dB)
312	45.87	25.87
314	46	26
316	46.1	26.1
318	46.2	26.2
320	46.36	26.36
322	46.46	26.46
324	46.59	26.59
326	46.68	26.68
328	46.74	26.74
330	46.78	26.78
332	46.81	26.81
334	46.82	26.82
336	46.83	26.83
338	46.83	26.83
340	46.8	26.8
342	46.81	26.81
344	46.78	26.78
346	46.75	26.75
348	46.72	26.72
350	46.7	26.7
352	46.7	26.7
354	46.6	26.6
356	46.55	26.55
358	46.5	26.5
360	46.43	26.43
362	46.36	26.36
364	46.3	26.3
366	46.2	26.2
368	46.1	26.1
370	45.98	25.98
372	45.83	25.83
374	45.67	25.67

Table 27: 1dB Bandwidth power measurements

The reduced performance at the operational frequency was attributed to overheating of the amplifier, caused by extended operation under continuous wave conditions and frequent frequency adjustments. The measured -1 dB bandwidth is 50 MHz. Additionally, the circuit exhibits resonance at a slightly shifted frequency. This deviation is likely due to minor imperfections in soldering and component placement, as the assembly was performed manually.

Next, we present the results obtained by the signal analyzer under continuous wave operation and pulsed. For the Harmonics generated under operational conditions at continuous wave we measured:

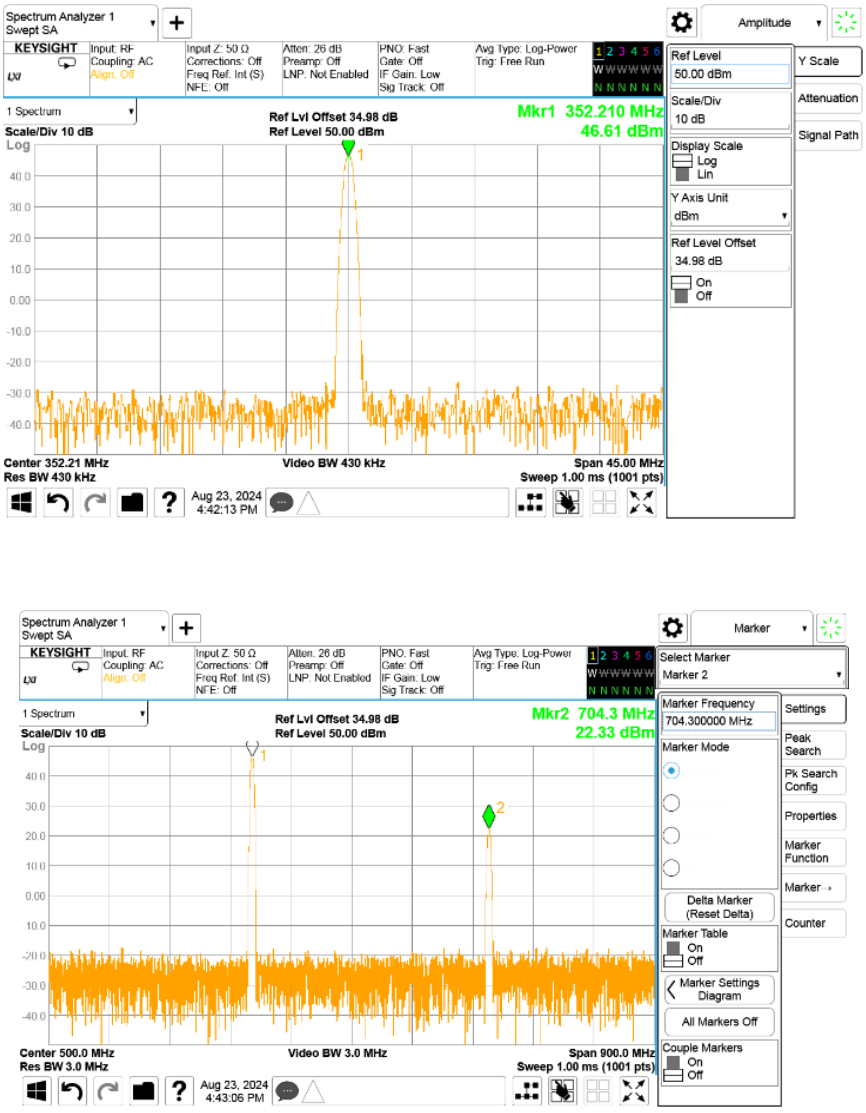


Figure 6.36: Signal Analyzer screenshot measurements for amplitude of 1st and 2nd Harmonic

Figure 6.37: Signal Analyzer screenshot measurements for amplitude of 3rd, 4th and 5th Harmonic

At the operational frequency, the amplifier delivers an output power of 46.6 dBm. The second and third harmonics are measured at 22.33 dBm and 24.76 dBm, corresponding to harmonic suppression levels of -24.27 dBc and -21.84 dBc, respectively. No sidebands or spurious signals are present, ensuring clean operation without interference in the system. The fourth and fifth harmonics are measured at 23.24 dBm and 6.72 dBm, respectively, highlighting the saturated operating state of the amplifier.

The phase flatness over a 10 dB dynamic range was targeted to be within 2° to ensure that when the electromagnetic wave interacts with the protons in the accelerator, the amplitude of the sinusoidal wave is maximized, providing the protons with sufficient power. This is crucial because the amplifier's gain may fluctuate based on the power levels required for the cavity. To monitor this, we set the signal generator to perform power sweeps from 10 dBm to 20 dBm and observed the phase shifts during the process.

First, we detect the moments the sweep starts and stops and then set the markers in the phase domain to monitor its value:

Figure 6. 38: Signal Analyzer measurements for phase stability over 10dB dynamic (a)

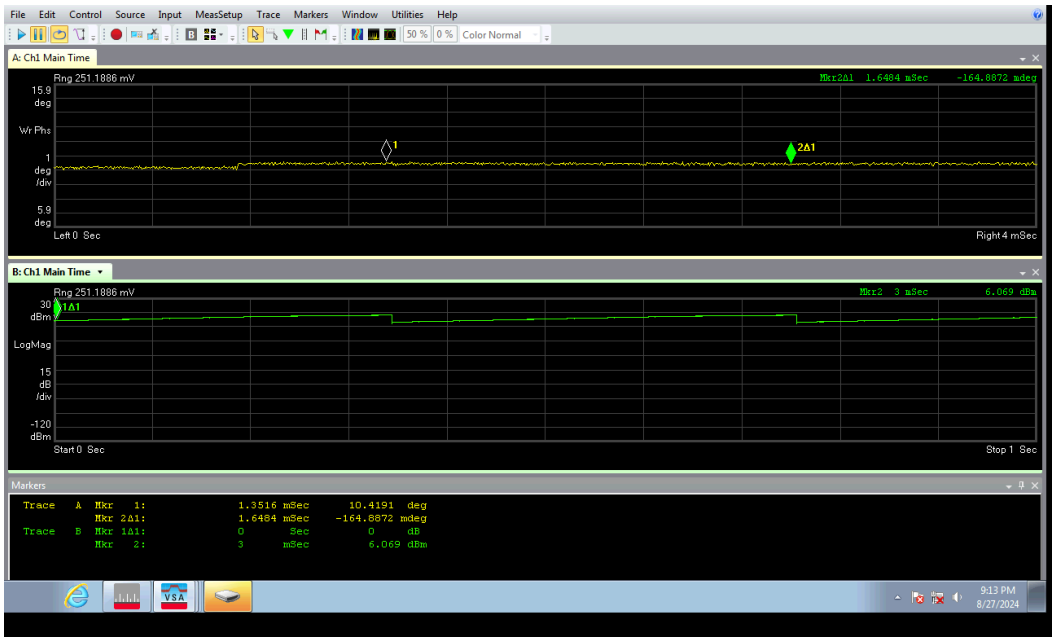


Figure 6.39: Signal Analyzer measurements for phase stability over 10dB dynamic (b)

Next, we set both the signal generator and the signal analyzer to operate in pulsed. We analyze each pulse for power and phase behavior and pulse to pulse repeatability, RF power drop and phase shifts across the pulse and test if power and phase ripple exists.

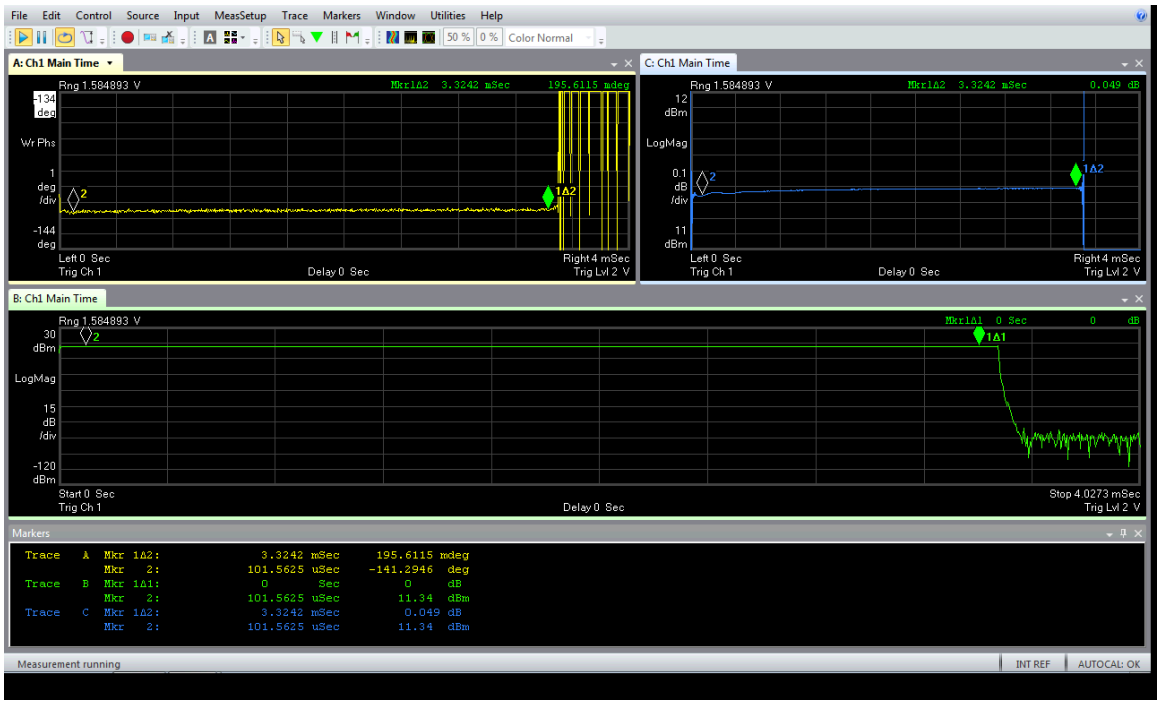


Figure 6.40: Signal Analyzer screenshot for pulse measurements

In the green graph, we identify the first 100 µs of the pulse and set the markers for power and phase to start after this point, as per the specifications that require excluding the initial 100

μs. The blue and yellow graphs, representing power and phase respectively, show no significant ripple. The power drop is minimal at 0.05 dB, and the phase shift is only 0.2°. Additionally, pulse-to-pulse power and phase stability were monitored, and both were consistent, with no noticeable deviations.

Another important measurement we did was to monitor pulse repeatability with voltage drops. Because the two amplifying stages will have a lot of stages working parallel, it is possible the power supplies may not provide the 70Volts bias steadily, but with some voltages drops below we can see how power and phase shifts with these changes:

Drain Voltage (V)	Output Power (dBm)	Phase (°)
68	46.52	1.4
68.1	46.52	1.4
68.2	46.52	1.4
68.3	46.525	1.4
68.4	46.53	1.4
68.5	46.535	1.4
68.6	46.54	1.35
68.7	46.545	1.35
68.8	46.55	1.35
68.9	46.555	1.4
69	46.557	1.4
69.1	46.56	1.3
69.2	46.565	1.35
69.3	46.57	1.3
69.4	46.58	1.3
69.5	46.585	1.35
69.6	46.59	1.4
69.7	46.6	1.35
69.8	46.6	1.32
69.9	46.61	1.4
70	46.62	1.4

Table 28: Pulse repeatability under voltage drops

Power drop is 0.1dB and phase shift is 0.1 °.

Now we proceed to Vector Network Analyzer measurements. We measured total group delay by sending an wave from input and measured how much time it needed to traverse the amplifier:

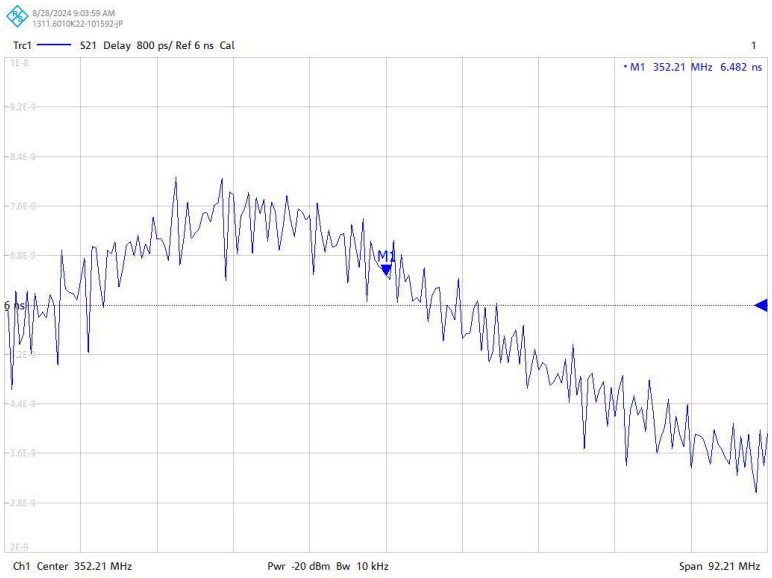


Figure 6.41: Screenshot from the VNA for group delay measurements

Group delay was measured at 6.482ns

For low power values we tested the amplifier for stability:

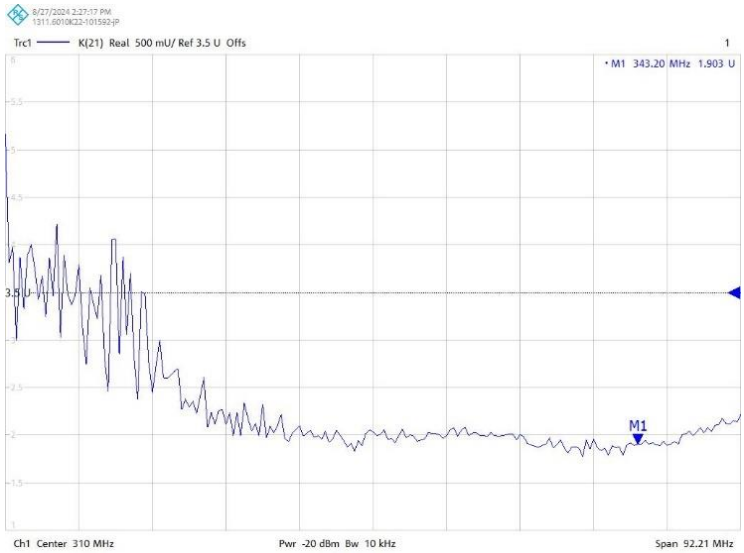


Figure 6.42: Screenshot from the VNA for K-factor measurements

K-factor greater than 1.

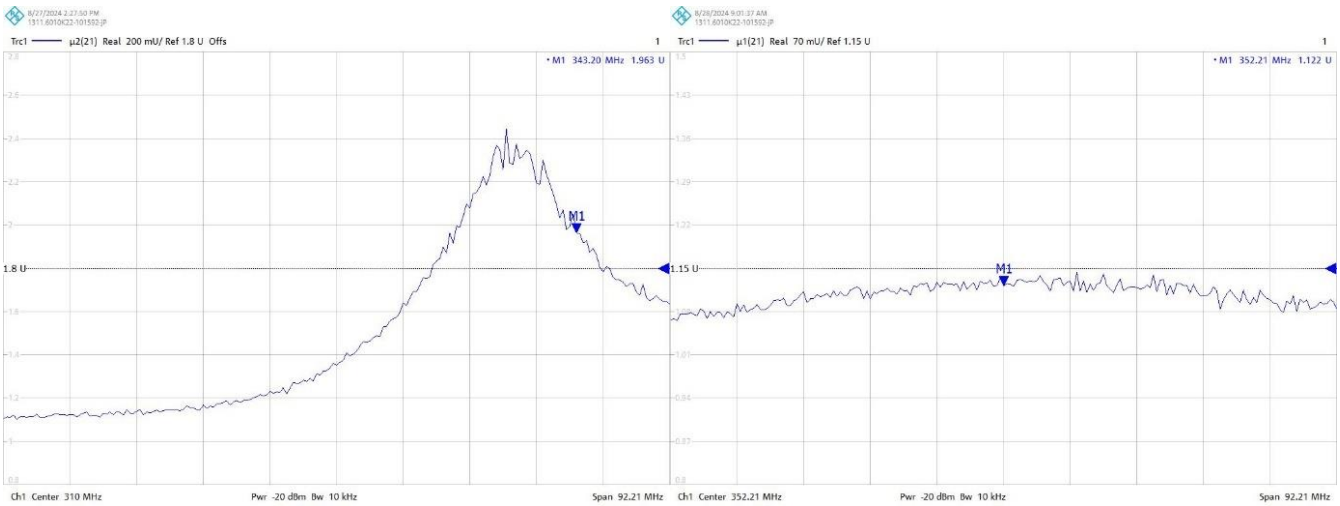


Figure 6.43: Screenshot from the VNA for μ 2 and 1 factor measurements

μ2 and μ1 greater than 1.

For S11 measurements we used the setup previously mentioned and we have:

Input power(dBm)	S11(dB)
0	-13.3
1	-13.3
2	-13.3
3	-13.3
4	-13.3
5	-13.3
6	-13.3
7	-13.3
8	-13.4
9	-13.4
10	-13.4
11	-14
12	-14
13	-13.6
14	-13.6
15	-13.65
16	-13.65
17	-13.65
18	-13.5
19	-13.3
20	-13.1

21	-13
22	-13
23	-13.1
24	-13.1
25	-13

Table 29: S11 measurements

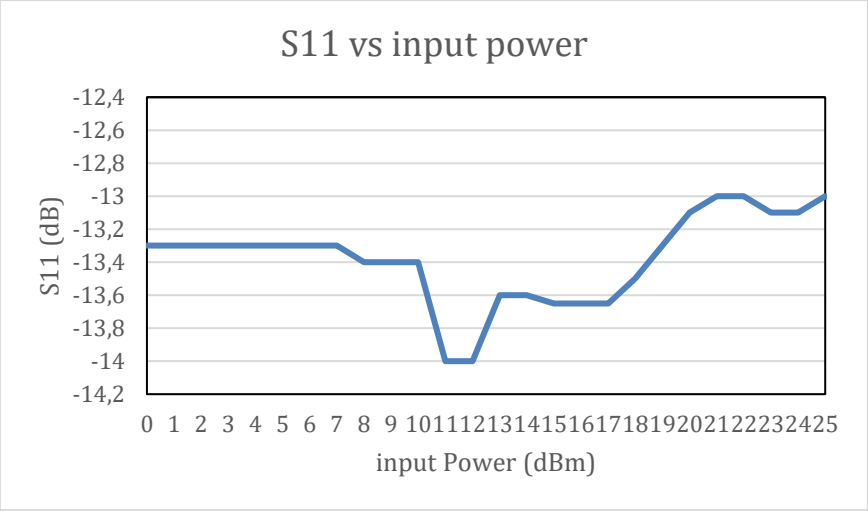


Figure 6.44: Measurements of S11 parameter as a function input power

For S22 measurements we used the setup previously mentioned and we have:

Input power(dBm)	S22 (dB)
0	-2
1	-2.1
2	-2
3	-2.1
4	-2
5	-2
6	-2
7	-2
8	-2
9	-2
10	-2.1
11	-2
12	-2.1
13	-2.1
14	-2
15	-2.1

16	-2.3
17	-2.8
18	-4
19	-6
20	-7.5
21	-8.3
22	-8.5
23	-8.5
24	-8.5
25	-8.5

Table 30: S22 measurements

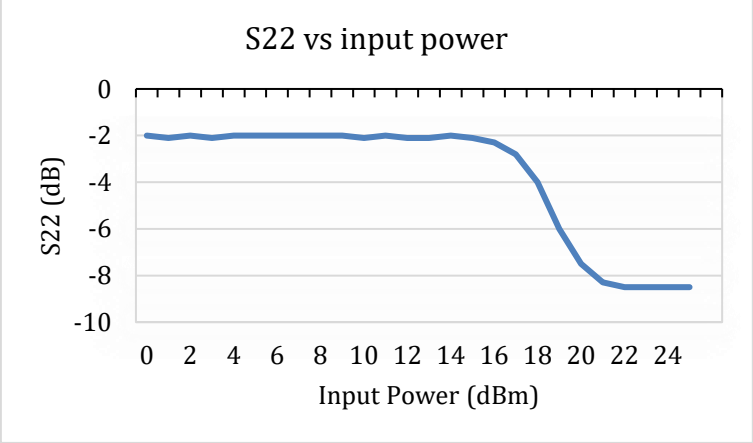
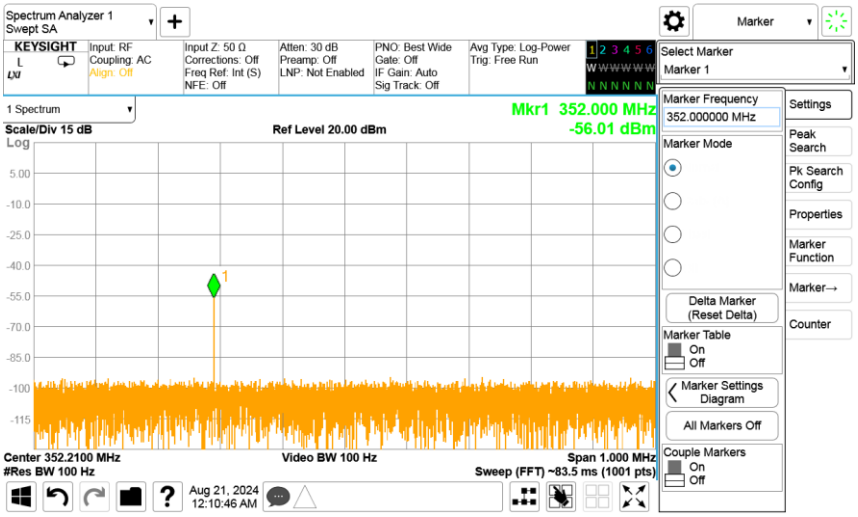


Figure 6.45: Measurements of S22 parameter as a function input power

First, we set the output generator to produce the signal that is going to be reflected and measured. And set that point as the zero reference:



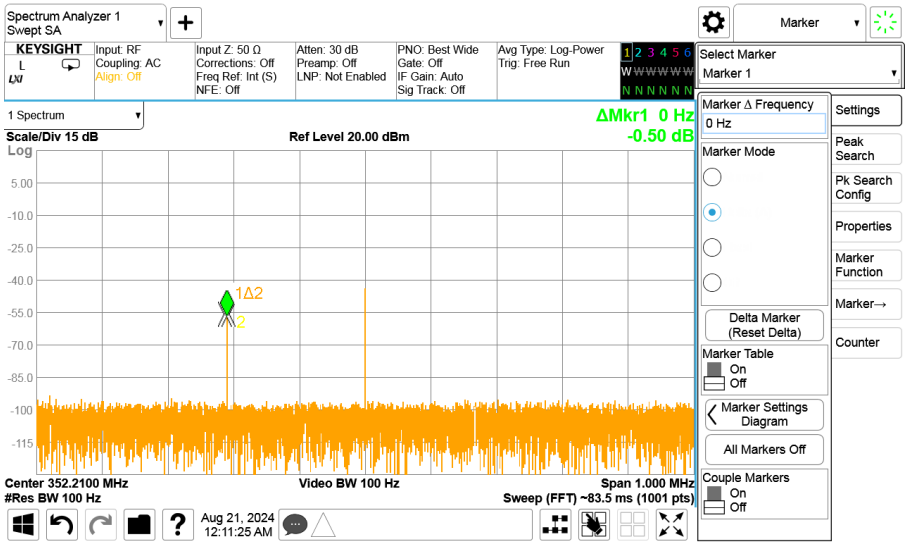


Figure 6.46: Signal Analyzer screenshots of preparing S22 measurements

Next, we start the system operation and operate the amplifier in the saturation region:

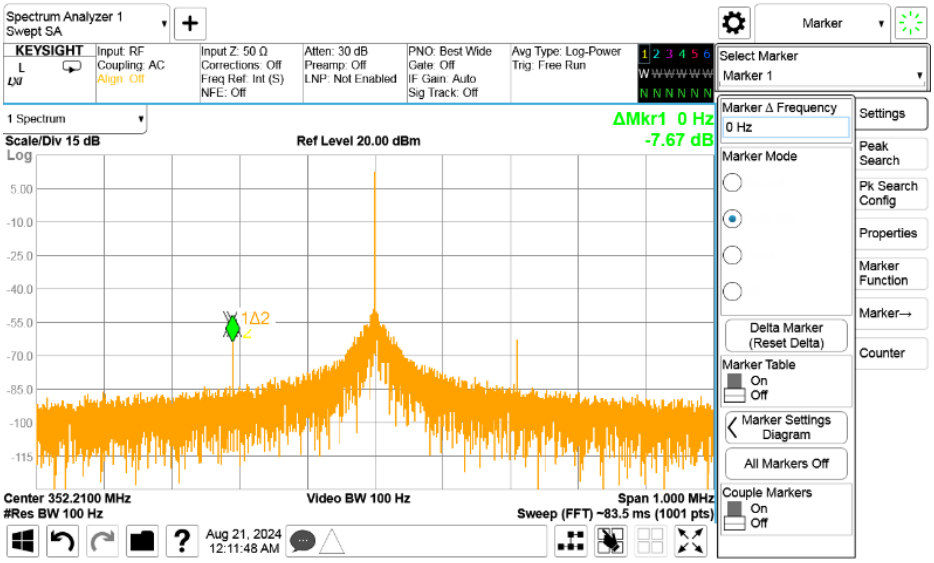


Figure 6.47: Signal Analyzer screenshot measuring the S22 parameter

The value of the marker is the S22 value.

The last measurement we did for that PCB is the cascaded topology discussed in the lab preparation chapter. The results obtained are show below:

Input power(dBm)	1st stage Output (dBm)	2nd stage Output (dBm)	Pulse drop (dBm)	1st Harmonic (dBm)	2nd Harmonic (dBm)	3rd Harmonic (dBm)
0	29.35	32.8	2.3	35.1	18.5	30.6
1	30.3	36.4	2	38	21.3	33.4
2	31.3	39.8	1.8	40.8	24.1	35.9
3	32.26	42.5	1.5	43.3	26.5	38
4	33.24	44.8	1.3	45.5	28.7	39.7
5	34.2	46.9	1.1	47.5	30.6	41.2
6	35.16	48.8	1	49.3	32.3	42.3
7	36.35	51	0.8	51.4	34.2	43.3
8	37.3	52.55	0.7	52.9	35.5	43.8
9	38.2	53.9	0.6	55.3	36.7	43.9
10	39.1	55.3	0.6	55.6	37.8	43.7
11	40	56.6	0.55	56.8	38.8	42.9
12	40.9	57.8	0.5	58	39.7	41.2
13	41.8	58.8	0.45	59	39.9	37.2
14	42.65	59.95	0.45	60.1	40.7	34
15	43.5	61.1	0.4	61.2	41.6	37
16	44.35	62	0.3	62.1	42	43.5
17	45.15	62.7	0.25	62.8	41.9	47.8
18	45.8	63.13	0.2	63.2	41.6	50.4
19	46.23	63.33	0.1	63.4	41.4	51.7
20	46.54	63.47	0.1	63.55	41.2	52.3
21	46.8	63.55	0.08	63.63	41	52.75
22	46.98	63.6	0.05	63.7	41	53.1
23	47.15	63.66	0.05			

Table 31: Cascaded amplifiers measurements

We notice we have pulse drops. This happens because for low power values the gain is increasing in the second amplifier. So, during the pulse as input of the amplifier increases so is the gain, resulting in uneven amplifying of the pulse.

The system can deliver the 1600 Watts of power needed to operate at 16dBm input. This leaves enough margin to push the amplifiers and generate more power, or operate at that level and minimize the stress to the equipment.

Notice that the driver has serious intermodulation problems at 13 dBm and 14 dBm input. This needs to be studied. The problem can be noticed in the next picture:

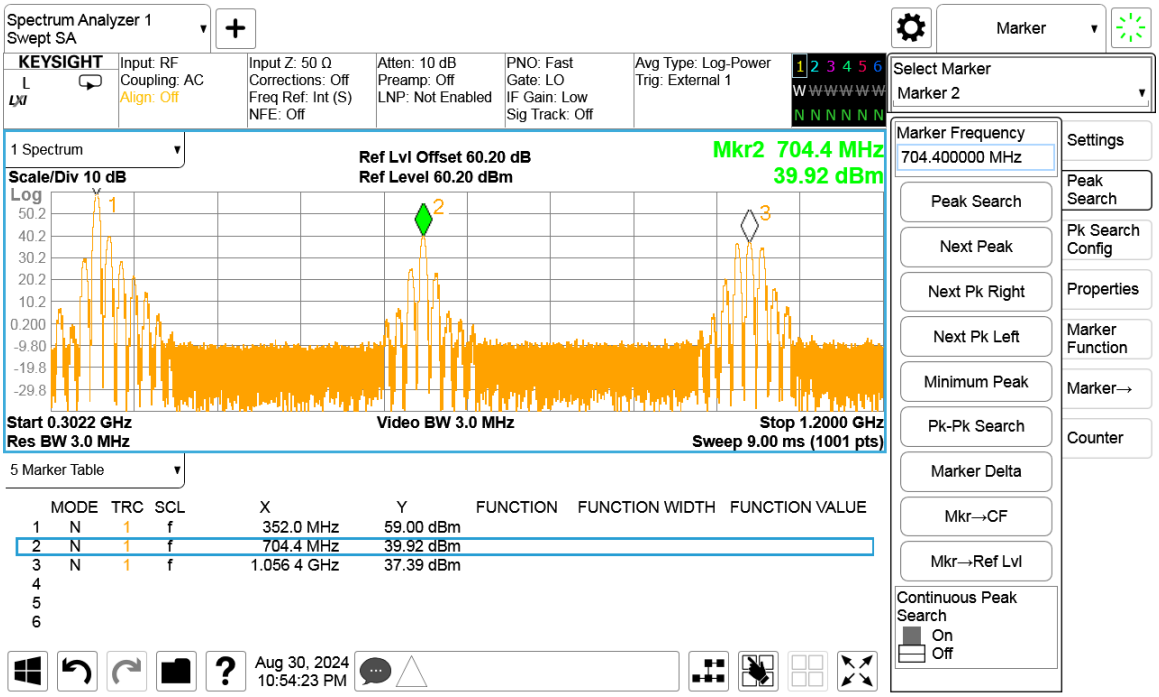


Figure 6.48: Signal Analyzer screenshot for harmonics distortions

The next measurements presented are about the 1st iteration. As mentioned before, the 1st iteration was resonant at a different frequency than the operational of the accelerator.

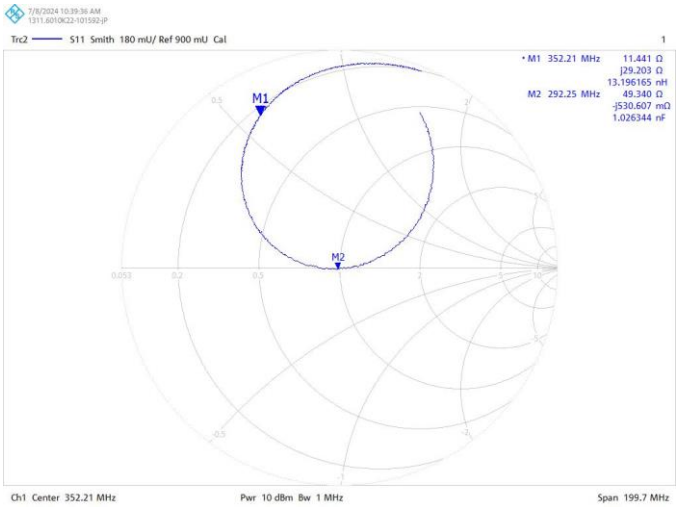


Figure 6.49: Screenshot from VNA Smith chart measurements of

The amplifier resonates at 295 MHz for the S11 parameter.

The first step in understanding what caused this misalignment was to test if the transmission line is 50 Ohms. For that, I soldered two 100Ohm resistors in parallel and measure S11 behavior:

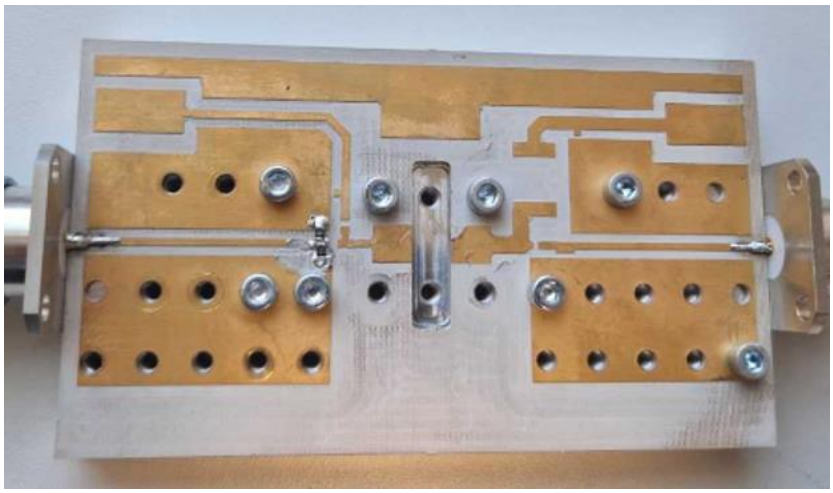


Figure 6.50: Picture of the circuit created to measure the characteristic

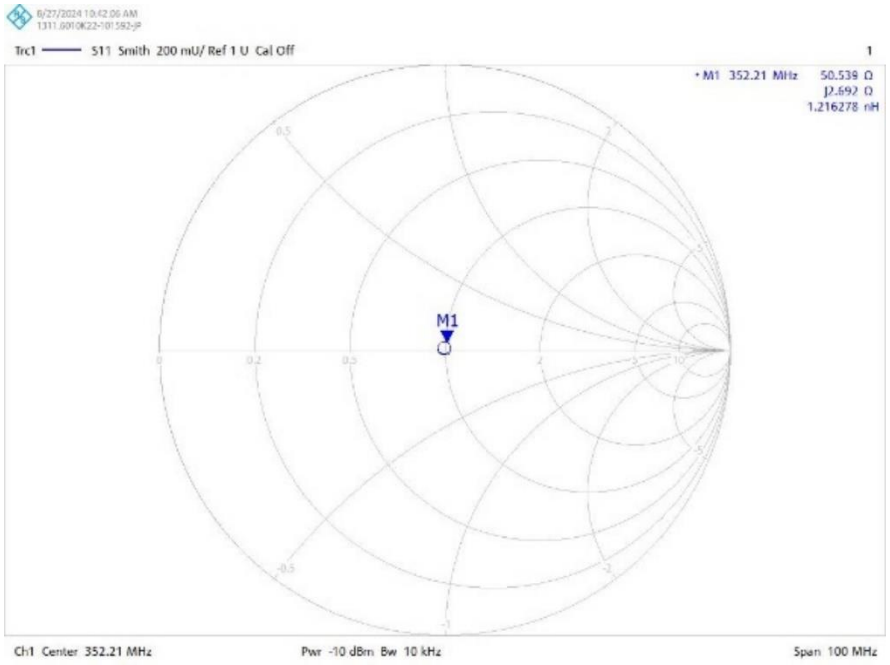


Figure 6.51: Screenshot from VNA Smith chart measurements of impedance

The smith chart indicates that the matching is almost perfect at the operational frequency. Following this measurement, the researcher returned to the simulation model and verified the issue that had been corrected during the second design iteration.

For iteration 3 and 4 we did not manage to complete the measurements. For iteration number 5 we have:

Input Power (dBm)	Output Power (dBm)	Output Power (W)	Gain (dB)	Current Consumption (mA)
0	28.9	0.776247	28.9	400
1	29.71	0.935406	28.71	402
2	30.75	1.188502	28.75	407
3	31.7	1.479108	28.7	411
4	32.7	1.862087	28.7	415
5	33.7	2.344229	28.7	421
6	34.65	2.917427	28.65	428
7	36.1	4.073803	29.1	430
8	37	5.011872	29	450
9	38	6.309573	29	464
10	38.9	7.762471	28.9	483
11	39.8	9.549926	28.8	505
12	40.7	11.74898	28.7	535
13	41.6	14.4544	28.6	567
14	42.45	17.57924	28.45	610
15	43.3	21.37962	28.3	660
16	44.15	26.0016	28.15	715
17	44.95	31.26079	27.95	777
18	45.6	36.30781	27.6	838
19	46.1	40.73803	27.1	886
20	46.5	44.66836	26.5	927
21	46.8	47.86301	25.8	960
22	47.1	51.28614	25.1	992
23	47.4	54.95409	24.4	1024
24	47.64	58.07644	23.64	1054
25	47.9	61.6595	22.9	1.083
26	48.16	65.46362	22.16	1.1
27	48.35	68.39116	21.35	1.13

Table 32: Power and current consumption measurements for iteration #5

The PCB iteration 5 can deliver almost 70W of power at lower current consumption. Also, at operational conditions it behaves better thermally:

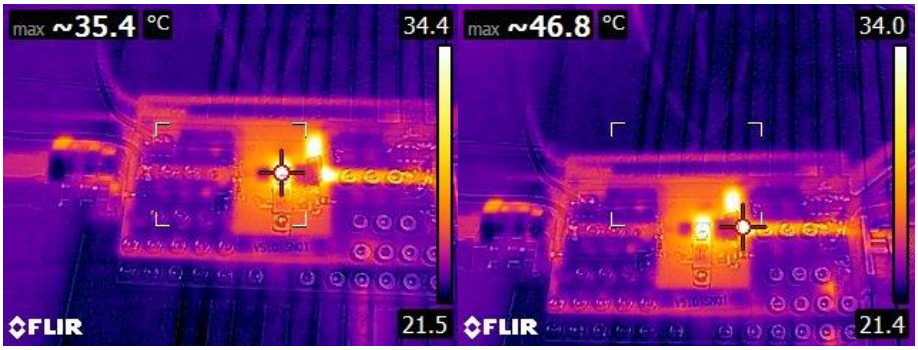


Figure 6.52: Pictures from the thermal camera monitoring the temperature of the transistor and the output coupling capacitor of iteration #5

6.7 Summary

This section outlines the process of designing, manufacturing, and testing the first stage of the SSPA driver, emphasizing the steps taken to ensure its compliance with specifications and functionality in the overall system.

Parameter	Specification per 2024-02-12	Specification per 2024-08-12	Measurement For PCB#2
Operating frequency	352.21 MHz	352.21 MHz	352.21 MHz
-1 dB bandwidth	≥ ±1 MHz	≥ ±1 MHz	50MHz
Peak output power	30 W (or higher)	50 W	58W
RF pulse width	Up to 3.5 ms	Up to 3.5 ms	3.5 ms
Repetition rate	Up to 14 Hz	Up to 14 Hz	14 Hz
Gain	23 dB min	27 dB at 20dBm input	26.85 dB
Efficiency	> 50 %	> 50 %	68%
Maximum no-damage RF drive input	26 dBm	26 dBm	26 dBm
Harmonic content at output power	< -30 dBc	< -30 dBc	-20 dBc, -27dBc
Spurious and sideband levels in ± 20 MHz	< -60 dBc	< -60 dBc	No spurious
RF Input Connector	N type, 50 Ω, Female	N type, 50 Ω, Female	N type, 50 Ω, Female
RF Output Connector	N type, 50 Ω, Female	N type, 50 Ω, Female	N type, 50 Ω, Female
Input/output impedance	50 Ω	50 Ω	50 Ω
Input VSWR	≤ 1.2:1 (if possible)	≤ 1.12:1 or -25dB (if possible)	1.5:1
output VSWR	≤ 1.2:1 (if possible)	≤ 1.12:1 or -25dB (if possible)	2.3:1
Load VSWR	Infinity	Infinity	
Gain flatness	ΔG ≤ ±0.5 dB (over 10dB dynamic)	ΔG ≤ ±0.5 dB (over 10dB dynamic)	2.95 dB
Phase flatness	≤ 2°(over 10dB	≤ 2° (over 10dB dynamic)	0.2°

	dynamic)		
RF Power Drop across the pulse	≤ 5% p-p (or Max 0,21dB) (power) (Within 3.5ms RF pulse excluding first 100µs of the pulse)	≤ 10% p-p (or Max 0,21dB) (power) (Within 3.5ms RF pulse excluding first 100µs of the pulse)	0.05 dB drop
Power ripple across pulse	≤ 0.25% rms (Within 3.5ms RF pulse excluding first 100µs of the pulse)	≤ 0.25% rms (Within 3.5ms RF pulse excluding first 100µs of the pulse)	No
Phase shift across the pulse	≤ 5° (Within 3.5ms RF pulse excluding first 100µs of the pulse)	≤ 10° (Within 3.5ms RF pulse excluding first 100µs of the pulse)	0.2°
Phase ripple across pulse	≤ 0.25° rms (Within 3.5ms RF pulse excluding first 100µs of the pulse)	≤ 0.25° rms (Within 3.5ms RF pulse excluding first 100µs of the pulse)	No
Pulse-to-pulse power stability	≤ 2%	≤ 2%	0%
Pulse-to-pulse phase stability (repeatability)	≤ 2°	≤ 2°	0°
RF Pulse Rise/ Fall Time	≤ 1 µs	≤ 1 µs	
compression point @ 0,1dB	54 W	54 W	2 W
Total Group Delay (not sure we need this parameter)	≤ 50 ns	≤ 50 ns	6ns
Size	Max size of the PCB 20x10 cm	Max size of the PCB 20x10 cm	10.6x6 cm

Table 33: Summary of specifications and measurements

Pulse rise/fall time and load VSWR were not measured.

The chapter begins by detailing the creation of the Gerber files and the subsequent PCB production process. This includes the layout considerations and optimizations necessary for high-frequency operation. The next section discusses the assembly process, focusing on the careful soldering and placement of components to ensure proper functionality and minimal signal degradation. The key performance specifications for the amplifier are presented, establishing the benchmarks for the subsequent testing phases. The next session covers the preparation steps taken in the lab, including the equipment used and the setup of the testing bench. The equipment is selected and configured to measure critical parameters like gain, efficiency, and power output accurately. The measurements section provides the results of the testing process, including a detailed analysis of the amplifier's performance. Parameters such as output power, gain, bandwidth, and stability are evaluated, along with comparisons to the expected specifications.

The amplifier manufactured complies with all the critical specs for power, gain and efficiency. The measurements results are very similar to the simulation results as indicated by the following graphs:

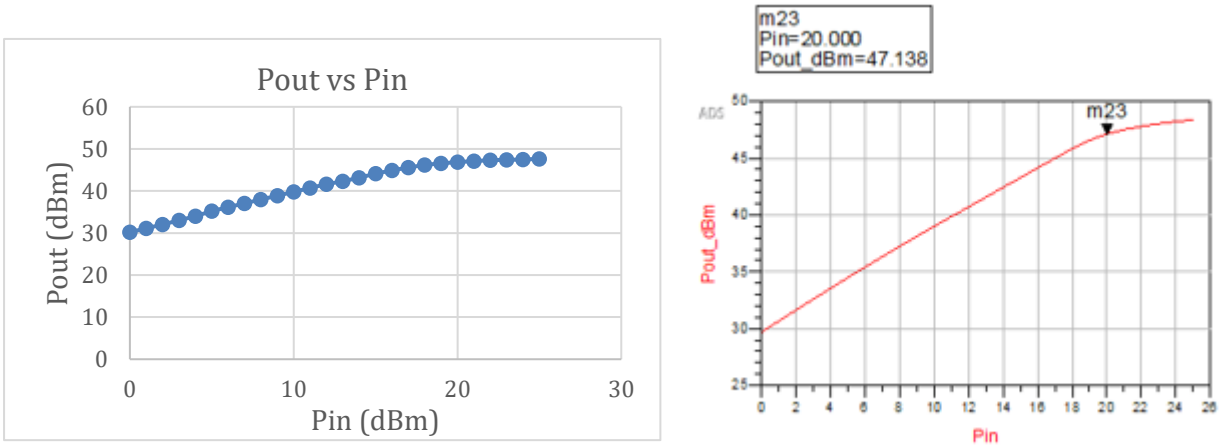


Figure 6.53: Comparison of measurements and simulated results of output power as a function of input power

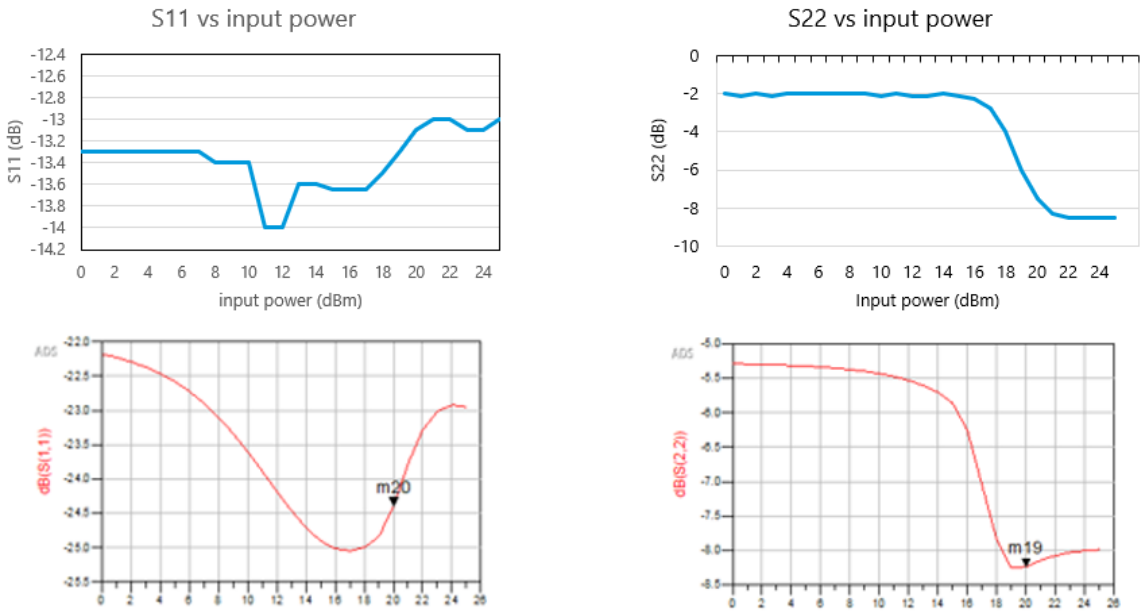


Figure 6.54: Comparison of measurements and simulated results of S-parameters as a function of input power

Blue graphs: Measurement
Red graphs: Simulation

Chapter 7: Conclusion

7.1 Summary

During this six-month internship, the author was engaged as an RF Engineer within the RF Sources Group at the European Spallation Source (ESS) in Lund, Sweden. In the first weeks, all the necessary safety and hazard training sessions were completed, ensuring compliance with ESS laboratory standards and procedures. The trainings attended are listed below:

- Basic Access to G01
- ESS Internal Safety Training
- Training for Electrical Authorisation at ESS
- Cryogenic Safety Awareness
- Radiation Protection Awareness

During this period, the RF Sources Group initiated a collaboration with Uppsala University to design an alternative system for powering the spoke cavities. To meet the energy demands of the system, it was decided to utilize Solid-State Power Amplifiers (SSPAs) as a replacement for traditional tetrode-based amplifiers. The complete system consists of 26 spoke cavities, each requiring 400 kW of power, and therefore 26 SSPA systems will be manufactured, each delivering 400 kW.

In the first month, the author contributed to the project by developing the Bill of Materials (BOM) based on the designed system architecture. Through this process, valuable experience was gained in identifying and selecting essential RF components and in understanding the critical parameters affecting their performance and reliability.

In the following months, the author embarked on a personal project, taking on the responsibility of designing and manufacturing an RF amplifier to serve as the first stage (Driver) of the SSPA system. The amplifier was designed to operate at 352.21 MHz and deliver 50 W of output power, while meeting stringent specifications to ensure proper operation without introducing issues to the low-level RF systems or the traversing beam.

The amplifier was designed and simulated using Advanced Design System (ADS) by Keysight, while the layout was developed in Altium Designer, providing substantial experience in RF circuit and PCB design. The prototype was subsequently manufactured and tested in the RF laboratory, offering hands-on experience in PCB assembly, SMD soldering, and the use of RF measurement equipment. A complete characterization of the amplifier was performed, including work with high-power applications up to 2.5 kW. The project concluded successfully with the fabrication of an amplifier capable of delivering nearly 70 W of power. The work was later presented to the ESS community.

In summary, this internship provided the opportunity to work within a high-caliber scientific environment, marking both the beginning of the author's professional career and his first experience living abroad. The placement not only offered invaluable hands-on knowledge in RF engineering but also allowed a meaningful contribution to a major international scientific project. It was a rewarding experience that combined technical growth,

teamwork, and personal development — a small yet significant contribution to the broader pursuit of scientific progress.

7.2 Next steps

In this chapter, the next steps after completing the 6-month internship. The tasks left to complete the driver are mentioned and possible extensions in the future are analyzed.

Bias topology switch

Since the amplifier is working under pulsed conditions, there is no need for it to operate for 360°. A switch that is triggered synchronously with the input pulse needs to be designed. This way, the power consumed, the heat generated and the deterioration of the equipment will be reduced.

Improve Rise/Fall time

For accelerator applications, it is important to have sharp rise/fall time. Both can be improved, especially fall time, because all the components in the circuit can charge and save energy capacitively or inductively. Parallel L-C circuits to the matching networks can help minimize this effect. If applied, there is need for careful redesign of the matching networks.

Microcontroller

A microcontroller can be designed and assembled to closely monitor the amplifying process and protect against arcs or system failure. This way we can monitor the entire system block by block for parameters like input/output power, current consumption and temperature. This system could also be programmed to cut the power supply or disconnect the amplifier from the system with switch to protect against damaging other equipment in case of failure.

Shielding Box

Every PCB has power dissipated both thermally and by radiation losses. Since the PCB has contact with the environment, some RF power is being radiated, causing possible problems interfering with the other systems and becoming dangerous for human exposure. A shielding box that would block all incoming and outcoming RF power would both improve the performance and increase safety.

Amplitude Tuner

As discussed in the system overview, there is a need for an amplitude tuner capable of providing 25 dB gain at 0dBm to 5dBm input power values. As showcased by the lab measurements, the driver's 1st stage manufactured in this report is capable of offering almost 30dB of gain at that power level, making it a viable option for this system architecture.

More PCBs to evaluate in order to have 16 for the spoke cavities

After all these steps are evaluated and completed, we need to manufacture at least 16 operating amplifiers to test the entire system and however more we need in order to have spare ones in case of failure or for amplitude tuner use.

7.3 The Road Ahead

The continuous advancement of Solid-State Power Amplifier (SSPA) technology is redefining the future of high-power RF systems in scientific research and accelerator facilities. As semiconductor devices evolve toward higher power densities, improved efficiency, and operation at increasingly higher frequencies, SSPAs are rapidly emerging as the next-generation alternative to traditional vacuum-tube technologies. Their modularity, scalability, and reliability make them ideally suited for large-scale infrastructures such as particle accelerators, fusion reactors, and radar systems, where long-term stability and precise control are paramount.

In the context of accelerator science, the transition toward solid-state RF sources promises not only enhanced operational robustness but also greater flexibility in power distribution, redundancy, and fault tolerance. Looking ahead, advances in wide-bandgap materials (such as GaN and SiC), intelligent power combining architectures, and digital control systems will continue to push the limits of efficiency and power density. These developments will enable accelerators to operate with higher repetition rates, improved beam stability, and reduced maintenance demands—ultimately contributing to more reliable and energy-efficient research infrastructures. The convergence of solid-state RF engineering, advanced materials science, and accelerator physics thus represents a pivotal direction for the next generation of scientific discovery.

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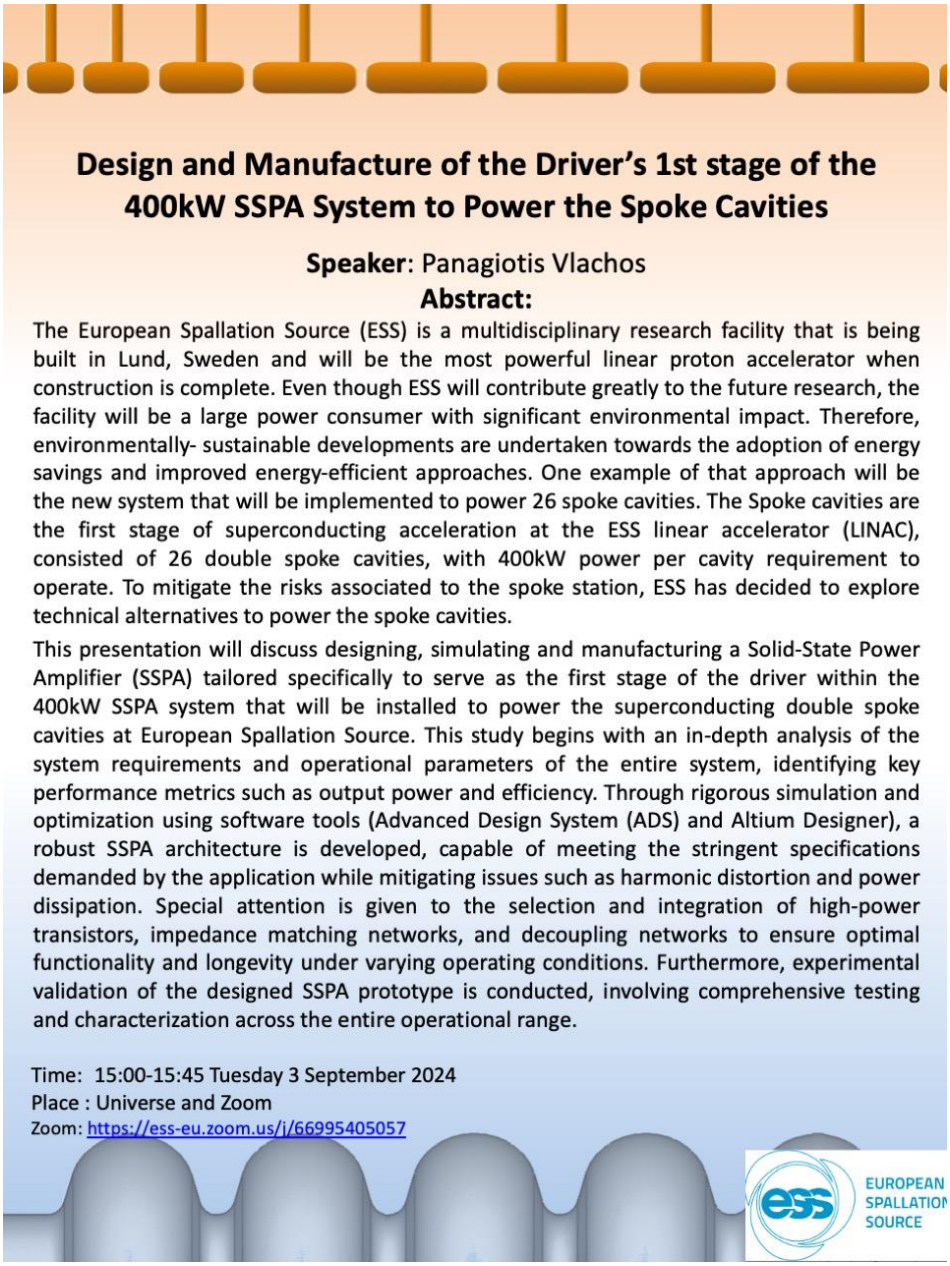
Appendices

The following poster presents the abstract and announcement for my presentation titled *"Design and Manufacture of the Driver's 1st Stage of the 400 kW SSPA System to Power the Spoke Cavities"*, delivered at the European Spallation Source (ESS) in Lund, Sweden, on Tuesday, 3 September 2024.

This presentation summarized the design process, simulation, and experimental validation of the developed Solid-State Power Amplifier (SSPA) prototype, and was part of the internal ESS research dissemination series. It was a great honor and a defining moment for me, marking my transition from being a science enthusiast to actively contributing a small part to the greater project called science.



Design and Manufacture of the Driver's 1st stage of the 400kW SSPA System to Power the Spoke Cavities

Speaker: Panagiotis Vlachos

Abstract:

The European Spallation Source (ESS) is a multidisciplinary research facility that is being built in Lund, Sweden and will be the most powerful linear proton accelerator when construction is complete. Even though ESS will contribute greatly to the future research, the facility will be a large power consumer with significant environmental impact. Therefore, environmentally- sustainable developments are undertaken towards the adoption of energy savings and improved energy-efficient approaches. One example of that approach will be the new system that will be implemented to power 26 spoke cavities. The Spoke cavities are the first stage of superconducting acceleration at the ESS linear accelerator (LINAC), consisted of 26 double spoke cavities, with 400kW power per cavity requirement to operate. To mitigate the risks associated to the spoke station, ESS has decided to explore technical alternatives to power the spoke cavities.

This presentation will discuss designing, simulating and manufacturing a Solid-State Power Amplifier (SSPA) tailored specifically to serve as the first stage of the driver within the 400kW SSPA system that will be installed to power the superconducting double spoke cavities at European Spallation Source. This study begins with an in-depth analysis of the system requirements and operational parameters of the entire system, identifying key performance metrics such as output power and efficiency. Through rigorous simulation and optimization using software tools (Advanced Design System (ADS) and Altium Designer), a robust SSPA architecture is developed, capable of meeting the stringent specifications demanded by the application while mitigating issues such as harmonic distortion and power dissipation. Special attention is given to the selection and integration of high-power transistors, impedance matching networks, and decoupling networks to ensure optimal functionality and longevity under varying operating conditions. Furthermore, experimental validation of the designed SSPA prototype is conducted, involving comprehensive testing and characterization across the entire operational range.

Time: 15:00-15:45 Tuesday 3 September 2024
Place : Universe and Zoom
Zoom: https://ess-eu.zoom.us/j/66995405057

ess EUROPEAN SPALLATION SOURCE